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iMOTION™ IMC300A Data Sheet

High performance motor control IC series with an additional microcontroller

Features

Dual core computation – Motion Control Engine (MCE) and ARM® Cortex®-M0 based user application controller (MCU)

Motion Control Engine (MCE)

- MCE offers a ready-to-use solution with easy configuration for variable speed motor control
  - Space Vector PWM with sinusoidal commutation and integrated protection features
  - Current sensing via single or leg shunt configuration
  - Sensorless and / or Hall sensor (analog / digital) based operation
  - Integrated and / or external temperature sensor
  - Optional boost or totem pole PFC control
  - Integrated Script language for additional MCE and I/O control.
  - High speed communication interface (JCOM) between MCE and ARM® core processor
  - Parameter programming and debug support with MCEWizard and MCEDesigner

User Application Controller (MCU)

- CPU Subsystem
  - 32-bit Arm® Cortex®-M0 core for user application control
  - 48/96 MHz core/peripherals clock
  - Nested Vectored Interrupt Controller (NVIC)
  - Event Request Unit (ERU) for event interconnections
  - MATH Co-processor: 24-bit trigonometric calculation (CORDIC), 32-bit division unit
- On-Chip Memories
  - 8 Kbyte ROM
  - 16 Kbyte SRAM (with parity)
  - 128 Kbyte FLASH memory (with ECC)
- Supply, Reset and Clock
  - 3.3 V to 5.5 V supply with power on reset and brownout detector
  - On-chip clock monitor
  - Internal slow and fast oscillators
  - External crystal oscillator support (32 kHz and 4 to 20 MHz)
- System Control
  - Window watchdog
  - Real Time Clock (RTC) modue
  - Pseudo random number generator

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Block Diagram Reference

- Communication Peripherals
  - Universal Serial Interface Channels (USIC), usable as UART, double-SPI, IIC, IIS and LIN interfaces
  - MultiCAN+, Full-CAN/Basic-CAN with 2 nodes, 32 message objects (up to 1 MBaud)
- Analog Frontend Peripherals
  - 12-bit ADC converter with adjustable gain, up to 1 MS/s and up to 7 analog inputs
  - 0 V to 5.5 V input voltage range
  - 2 fast analog comparators
  - DAC with one-bit sigma-delta generator, external low-pass filter and up to 7 outputs
  - Temperature sensor
- High Speed Timers
  - 2x Capture Compare Unit with 4 timer channels each (CCU4)
  - Clock up to 96 MHz
  - Up to 8 capture inputs
  - Up to 8 PWM outputs (center/edge aligned)
- Input/Output Lines With Individual Bit Controllability
  - Tri-stated in input mode
  - Push/pull or open drain output mode
  - Configurable pad hysteresis
- Debug System
  - 4 breakpoints, 2 watchpoints
  - ARM serial wire debug (SWD), single-pin debug (SPD) interfaces
  - Independent operation of the MCE

Potential Applications

- Air-conditioners
- Refrigerators

Product Validation

Industrial

Ordering Information

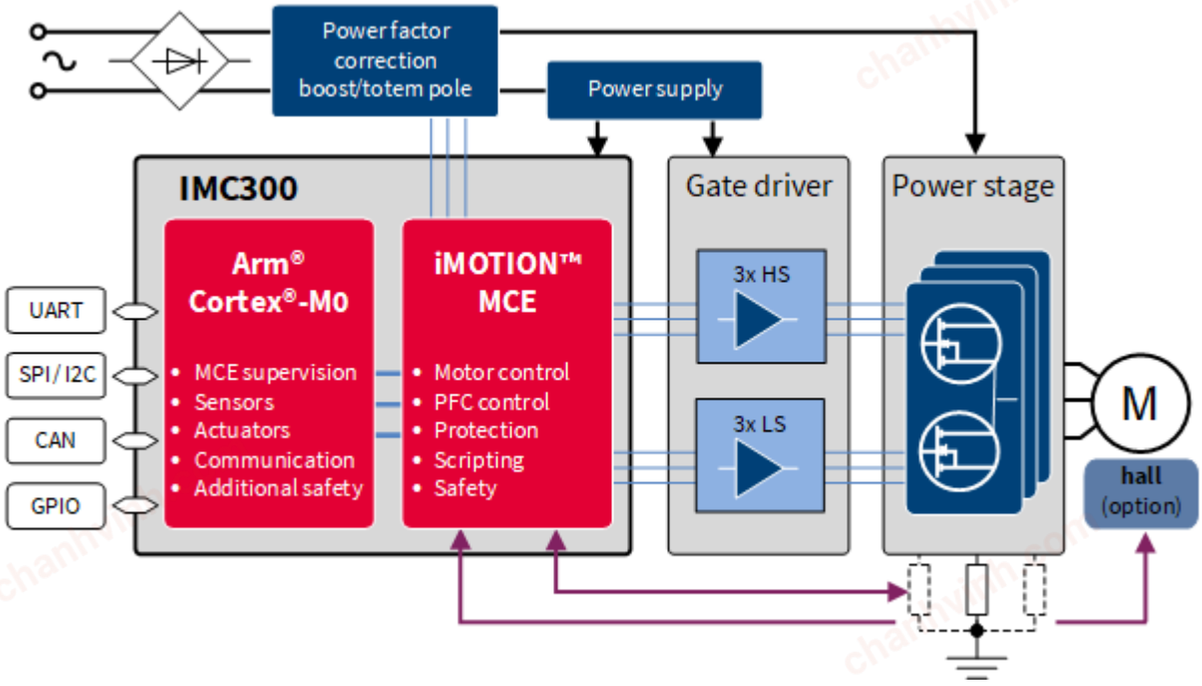
Product Type	Application	Package
IMC301A-F048	Single motor	LQFP-48
IMC301A-F064		LQFP-64
IMC302A-F048	Single motor + PFC (boost, totem pole)	LQFP-48
IMC302A-F064		LQFP-64

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Block Diagram Reference

Description

iMOTION™ IMC300 is a family of highly integrated ICs for the control of variable speed motor control system with an additional user programmable microcontroller. By integrating the required hardware, software and user program to perform control of a permanent magnet synchronous motor (PMSM) it offers a high flexibility of motor control system at the lowest system and development cost.



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Table of Contents

Features **1**
Potential Applications **2**
Product Validation **2**
Ordering Information **2**
Description **3**
Table of Contents **4**
About this document **5**
1 Block Diagram Reference **6**
2 Pin Configuration **7**
2.1 Pin Configuration IMC301A / IMC302A 7
2.2 Pin Configuration Drawing IMC301A 10
2.3 Pin Configuration Drawing IMC302A 12
3 Functional Description **14**
3.1 Application Schematics for IMC301A with Single Shunt Current Sensing 14
3.2 Application Schematics for IMC302A with Single Shunt Current Sensing 15
3.3 Application Schematics for IMC302A with Leg Shunt Current Sensing 16
4 Electrical characteristics and parameters **17**
4.1 General Parameters 17
4.1.1 Parameter Interpretation 17
4.1.2 Absolute Maximum Ratings 17
4.1.3 Pin Reliability in Overload 18
4.1.4 Operating Conditions 20
4.1.5 Input / Output Characteristics 21
4.1.6 Analog to Digital Converter (ADC) 23
4.1.7 Power Supply Current 24
4.1.8 Flash Memory Parameters 24
4.2 AC Parameters 25
4.2.1 Testing Waveforms 25
4.2.2 Power-Up and Supply Threshold Characteristics 26
4.2.3 On-Chip Oscillator Characteristics 28
4.3 Motor Control Parameters 29
4.3.1 PWM Characteristics 29
4.3.2 Current Sensing Characteristics 29
4.3.3 Fault Timing 30
4.3.4 Analog Hall Sensing Characteristics 30
4.4 Power Factor Correction (PFC) parameters 31
4.4.1 Boost PFC characteristics 31
4.4.2 Totem Pole PFC characteristics 31
4.4.3 PFC current sensing characteristics 31
4.4.4 PFC Fault timing 31
4.5 Control Interface Parameters (MCE) 32
4.5.1 UART Interface 32
4.5.2 Over Temperature Input 32
4.5.3 Pulse Output 33

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Block Diagram Reference
4.5.4 LED Output 33
5 Quality Declaration 34
6 Device and Package Specification 35
6.1 SBSL and Chip-IDs 35
6.2 Package Drawings 36
6.2.1 PG-LQFP-48-11 36
6.2.2 PG-LQFP-64-29 37
6.3 Thermal Characteristics 38
6.4 Part Marking 39
Revision history 40

About this document

Scope and purpose

This Datasheet describes the mechanical, electrical and functional characteristics of the iMOTION™ IMC300 series of motor control ICs. If no specific device is given the characteristics are valid for all devices within the iMOTION™ IMC300 series. For a detailed description of the functionality and configuration options please refer to the device hardware reference manual and the relevant MCE software reference manual.

Intended audience

The Datasheet is targeting developers implementing a variable speed drive system.

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1 Block Diagram Reference

The block diagram below gives an overview on the available functional units in the iMOTION™ IMC300 family. Not all units are required in all applications and some modules might share pins in smaller packages. Please refer to the pin configuration for individual packages and the application schematics examples given in the following sections.

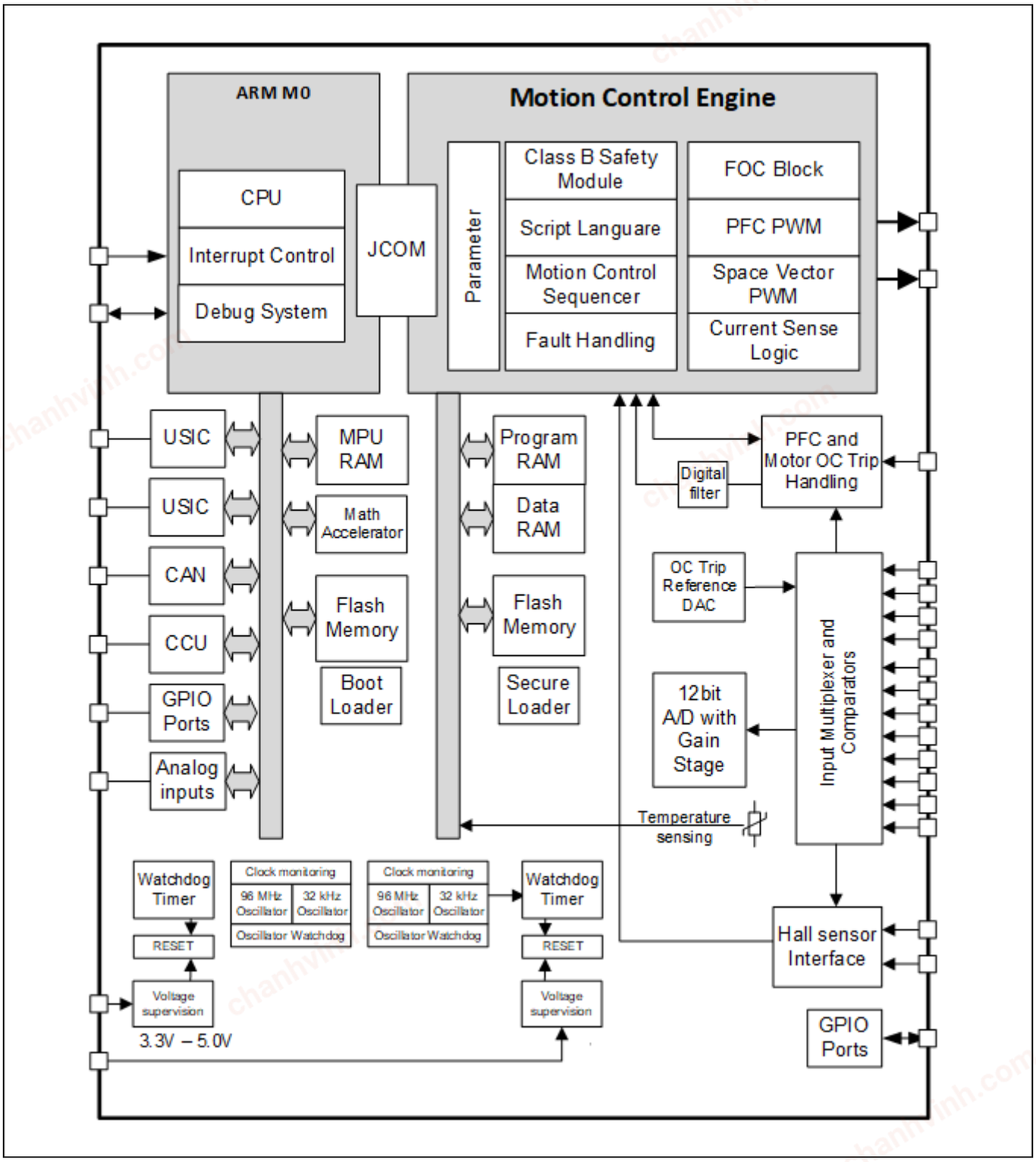


Figure 1 Block Diagram

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2 Pin Configuration

The following tables show the pin configurations for each individual device from the IMC300 series in the available packages.

The pin type is specified as follows:

- P – power and ground pins
- I - digital input
- O - digital output
- IO – digital input or output
- AIN - analog input
- AO – analog output

Each of the IMC300 cores has control over a different set of pins. The MCE core pins are labeled by system function which can be a single fixed function or multiple function options that are selected according to the MCE software configuration. The MCE functions and configuration options are described in the MCE software reference manual.

The user application core (MCU) pins are labeled by port number (Pn.m) and have peripheral I/O functions selected according to the user software. The peripheral I/O function selection and configuration options are described in the IMC30xA hardware reference manual.

Pins that do not have any signal assigned are reserved for future use. These pins should be left unconnected and neither be connected to ground nor to the positive supply.

Note: The reference voltage for motor current trip protection is generated by an internal DAC, therefore pins like REFU, REFV, and REFW only require a blocking capacitor.

2.1 Pin Configuration IMC301A / IMC302A

Table 1 Pin List

Signal	Type	IMC301A-F064	IMC301A-F048	IMC302A-F064	IMC302A-F048	Description
Supply Pins						
VDD	P	24, 25, 35, 50	21, 28, 38	24, 25, 35, 50	21, 28, 38	Supply Voltage
VSS	P	23, 49	20, 37	23, 49	20, 37	Ground
Motor control (MCE)						
PWMUL	O	29	22	29	22	PWM output phase U low side
PWMUH	O	30	23	30	23	PWM output phase U high side
PWMVL	O	31	24	31	24	PWM output phase V low side
PWMVH	O	32	25	32	25	PWM output phase V high side
PWMWL	O	33	26	33	26	PWM output phase W low side
PWMWH	O	34	27	34	27	PWM output phase W high side
GK	I	36	29	36	29	Motor gate kill input
VDC	AIN	14	11	14	11	DC bus voltage sensing input

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Pin Configuration

ISS/IU	AIN	18	15	18	15	Current sense input single shunt / phase U
IV	AIN	15	12	15	12	Current sense input phase V
IW	AIN	11	8	11	8	Current sense input phase W
REFU	AO	17	14	17	14	Itrip phase U reference output
REFV	AIN	16	13	16	13	Itrip phase V reference output
REFW	AIN	10	7	10	7	Itrip phase W reference output
Hall sensor inputs (MCE)						
AHALL1+	AIN	10	7	10	7	Analog Hall sensor input 1+
AHALL1-	AIN	11	8	11	8	Analog Hall sensor input 1-
AHALL2+	AIN	16	13	16	13	Analog Hall sensor input 2+
AHALL2-	AIN	15	12	15	12	Analog Hall sensor input 2-
HALL1	IO	26	-	26	-	Digital Hall sensor input 1
HALL2	IO	27	-	27	-	Digital Hall sensor input 2
HALL3	IO	28	-	28	-	Digital Hall sensor input 3
Power Factor Correction (MCE)						
PFCG0	O	-	-	44	33	PFC gate drive 0 output
PFCG1	O	-	-	43	32	PFC gate drive 1 (totem pole PFC) output
IPFC	AIN	-	-	12	9	PFC current sensing input
IPFCREF	AIN	-	-	21	18	PFC Itrip reference input
IPFCTRIP	AIN	-	-	22	19	PFC Itrip current sensing input
VAC1	AIN	-	-	20	17	AC voltage sensing input 1
VAC2	AIN	-	-	19	16	AC voltage sensing input 2
Interface (MCE)						
PGOUT	O	42	31	42	31	Pulse output
NTC	AIN	13	10	13	10	External thermistor input
LED	O	41	30	41	30	Status LED
Communication (MCE)						
RXD0	I	45	35	45	35	MCE UART0 receive input
TXD0	O	46	36	46	36	MCE UART0 transmit output
Scripting (MCE)						
AIN1	AIN	10	7	10	7	Analog input
AIN2	AIN	11	8	11	8	Analog input
AIN3	AIN	12	9	-	-	Analog input
AIN4	AIN	13	10	13	10	Analog input
AIN7	AIN	16	13	16	13	Analog input
AIN8	AIN	17	14	17	14	
AIN10	AIN	19	16	-	-	Analog input
AIN11	AIN	20	17	-	-	Analog input
GPIO2	IO	-	32	-	-	User configurable I/O, digital
GPIO3	IO	-	33	-	-	User configurable I/O, digital

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Pin Configuration

GPIO4	IO	-	34	-	34	User configurable I/O, digital
GPIO5	IO	-	18	-	-	User configurable I/O, digital
GPIO6	IO	-	19	-	-	User configurable I/O, digital
GPIO7	IO	21	-	-	-	User configurable I/O, digital
GPIO8	IO	22	-	-	-	User configurable I/O, digital
GPIO9	IO	26	-	26	-	User configurable I/O, digital
GPIO10	IO	27	-	27	-	User configurable I/O, digital
GPIO11	IO	28	-	28	-	User configurable I/O, digital
GPIO12	IO	37	-	37	-	User configurable I/O, digital
GPIO13	IO	38	-	38	-	User configurable I/O, digital
GPIO14	IO	39	-	39	-	User configurable I/O, digital
GPIO15	IO	40	-	40	-	User configurable I/O, digital
GPIO16	IO	43	-	-	-	User configurable I/O, digital
GPIO17	IO	44	-	-	-	User configurable I/O, digital
MCU						
P0.8	IO	51	39	51	39	Programmable I/O
P0.9	IO	52	40	52	40	Programmable I/O
P0.10	IO	53	41	53	41	Programmable I/O
P0.11	IO	54	42	54	42	Programmable I/O
P0.12	IO	55	43	55	43	Programmable I/O
P0.13	IO	56	44	56	44	Programmable I/O
P0.14/SWDIO	IO	57	45	57	45	Programmable I/O, or MCU SWD debug interface data input / output
P0.15/SWDCLK	I	58	46	58	46	Programmable I/O, or MCU SWD debug interface clock input
P1.0	IO	48	-	48	-	Programmable I/O
P1.1	IO	47	-	47	-	Programmable I/O
P2.0	IO/AIN	3	2	3	2	Programmable I/O, or MCU UART0 receive input, or analog input
P2.1	IO/AIN	4	3	4	3	Programmable I/O, or MCU UART0 transmit output, or analog input
P2.2	I/AIN	5	4	5	4	Digital input, or analog input
P2.6	I/AIN	6	5	6	5	Digital input , or analog input
P2.8	I/AIN	7	-	7	-	Digital input, or analog input
P2.10	IO/AIN	8	-	8	-	Programmable I/O, or analog input
P2.11	IO/AIN	9	6	9	6	Programmable I/O, or analog input
P4.0	IO	59	-	59	-	Programmable I/O
P4.1	IO	60	47	60	47	Programmable I/O
P4.2	IO	61	48	61	48	Programmable I/O
P4.3	IO	62	1	62	1	Programmable I/O
P4.4	IO	63	-	63	-	Programmable I/O, or MCU UART1 receive input

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Pin Configuration

P4.5	IO	64	-	64	-	Programmable I/O, or MCU UART1 transmit output
P4.6	IO	1	-	1	-	Programmable I/O
P4.7	IO	2	-	2	-	Programmable I/O

2.2 Pin Configuration Drawing IMC301A

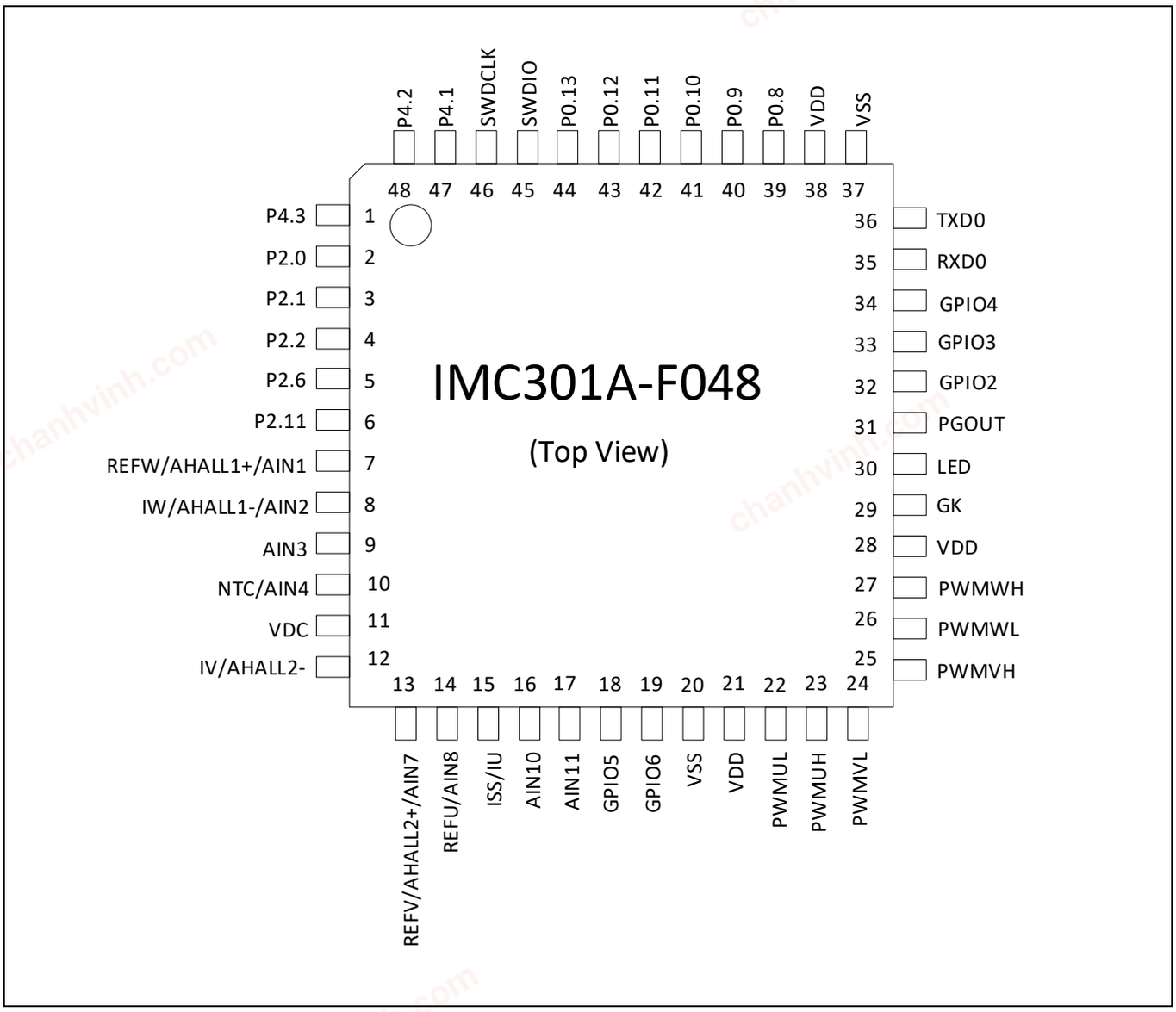


Figure 2 IMC301-F048

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Pin Configuration

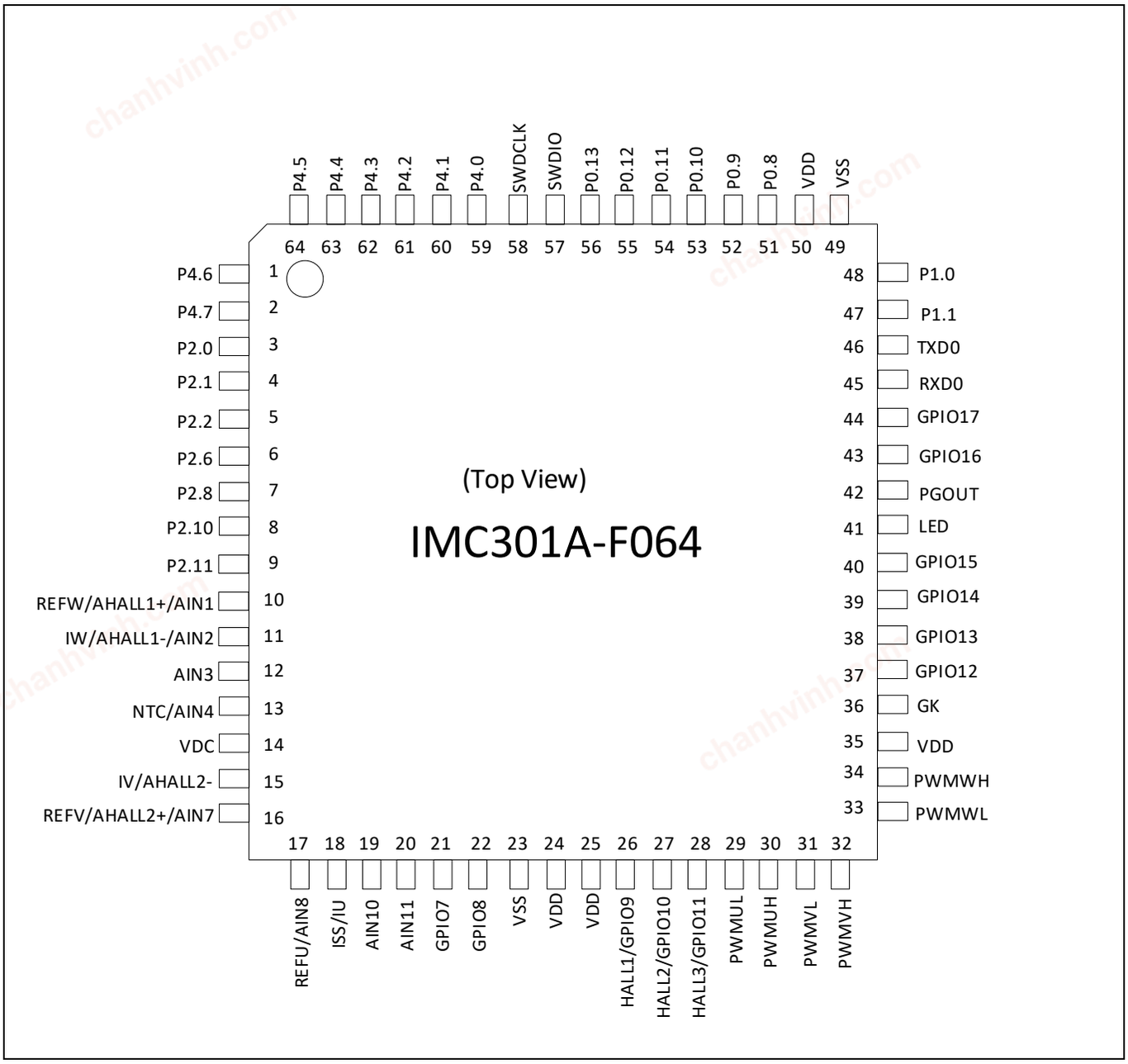


Figure 3 IMC301A-F064

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2.3 Pin Configuration Drawing IMC302A

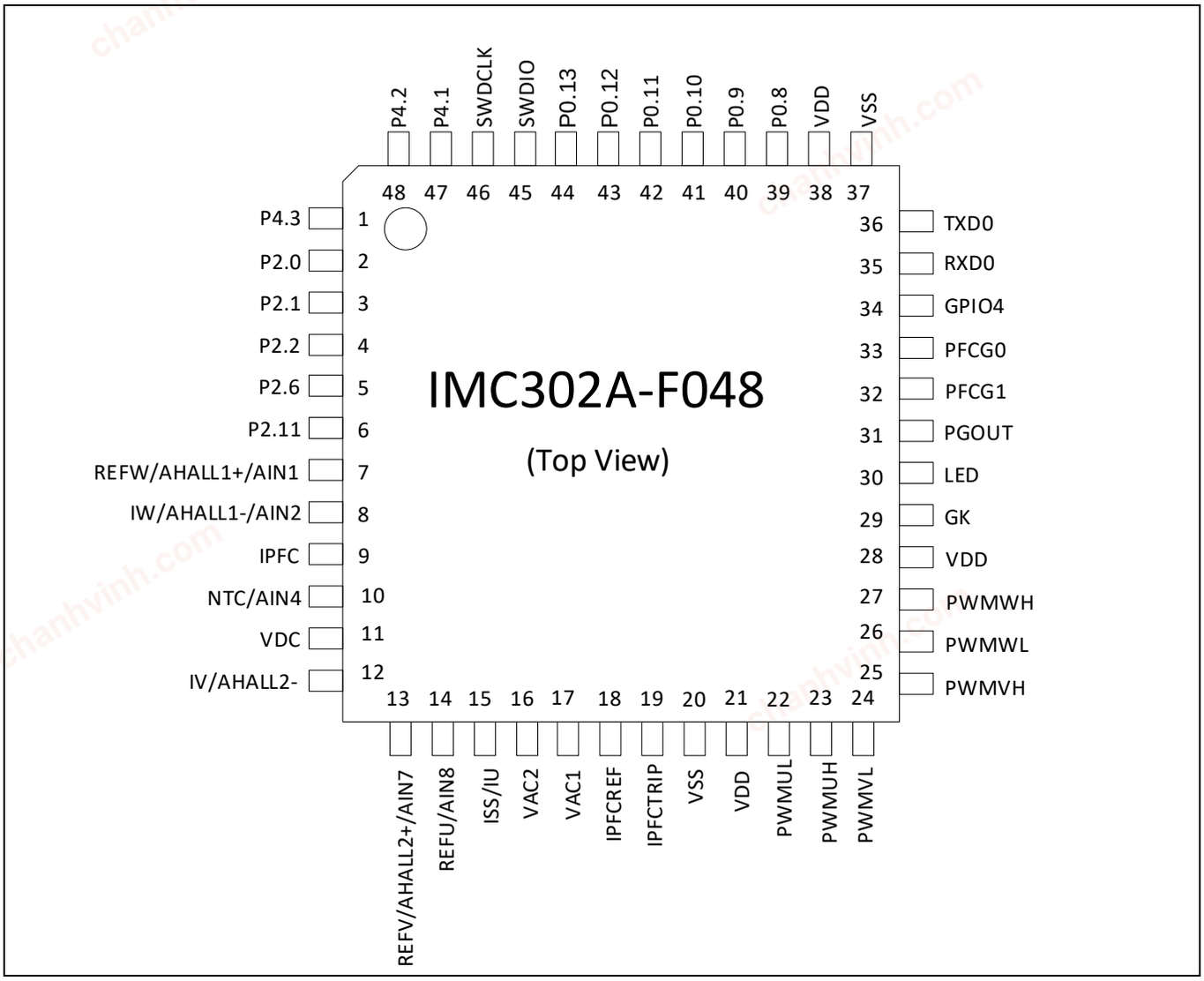


Figure 4 IMC302A-F048

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Pin Configuration

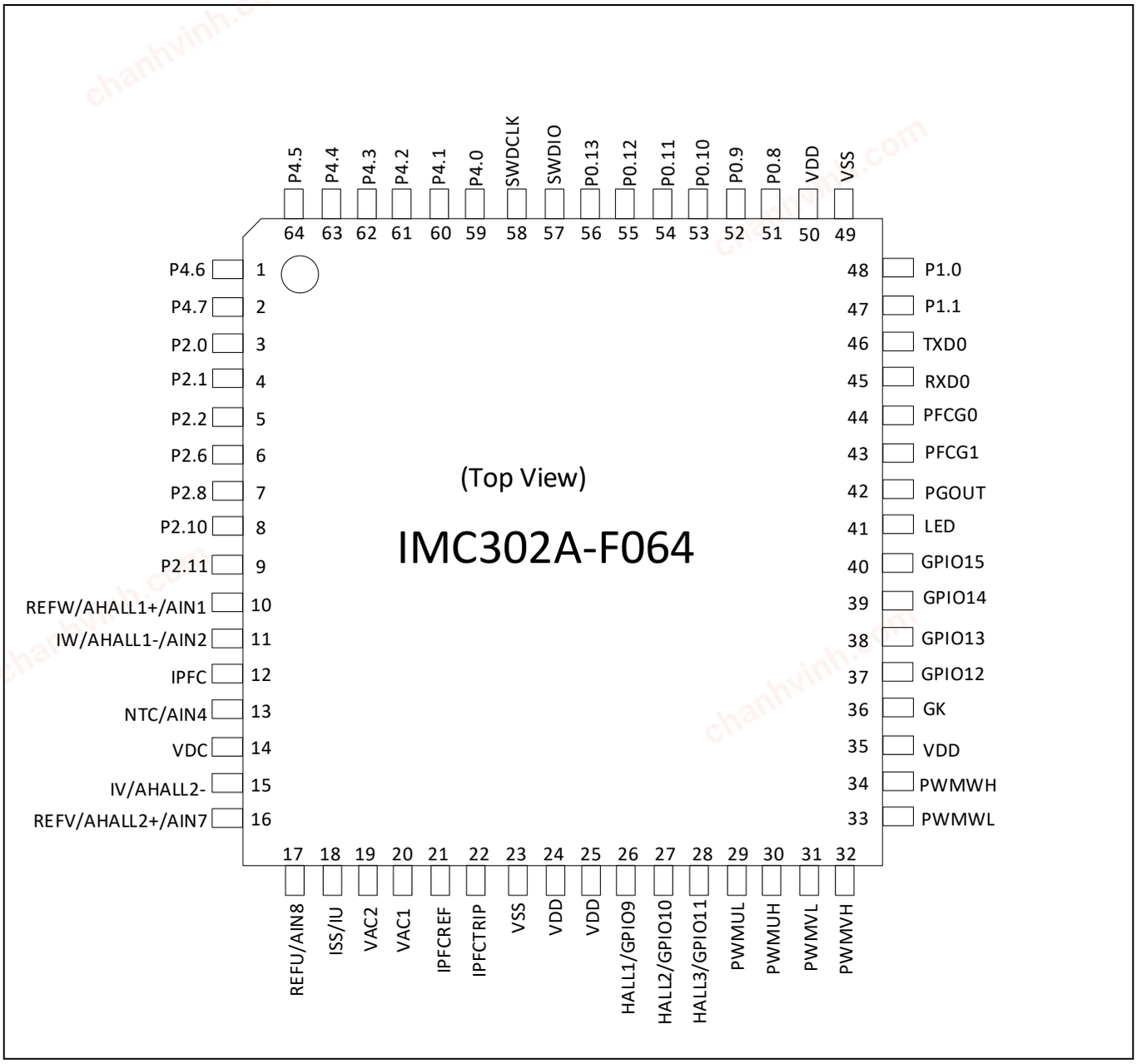


Figure 5 IMC302A-F064

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3 Functional Description

The IMC300 architecture is based on the combination of the Motion Control Engine (MCE) for Hall sensor based or sensorless motor control and PFC regulation and an additional microcontroller (MCU) based on an Arm® Cortex®-M0 core.

The MCE contains an embedded motor control algorithm with fast angle sensing at startup and enables low and ultra-high speed operation, and offers either single shunt current sensing or leg shunt current sensing. PFC control supports two topologies, namely a single stage boost mode PFC and a totem-pole PFC with 50 kHz fast switching application to minimize the inductor size. Users can configure the motor and PFC parameters for each specific motors and store into the onboard Flash memory. The MCE also contains the UL 607310-1 software safety certified library and modules.

The MCU is based on an Arm® Cortex®-M0 core and provides 128 Kbyte of flash and 16 Kbyte of RAM memory. The peripheral set is targeting communicaton and system application tasks.

Both units – MCE and MCU – run largely independantly up to the fact that the MCU can be debuged while the motor is still running. Communication between the two units is using a fast serial interface called JCOM.

3.1 Application Schematics for IMC301A with Single Shunt Current Sensing

Figure 6 shows the application schematics diagram for a single motor control system with single shunt current sensing configuration.

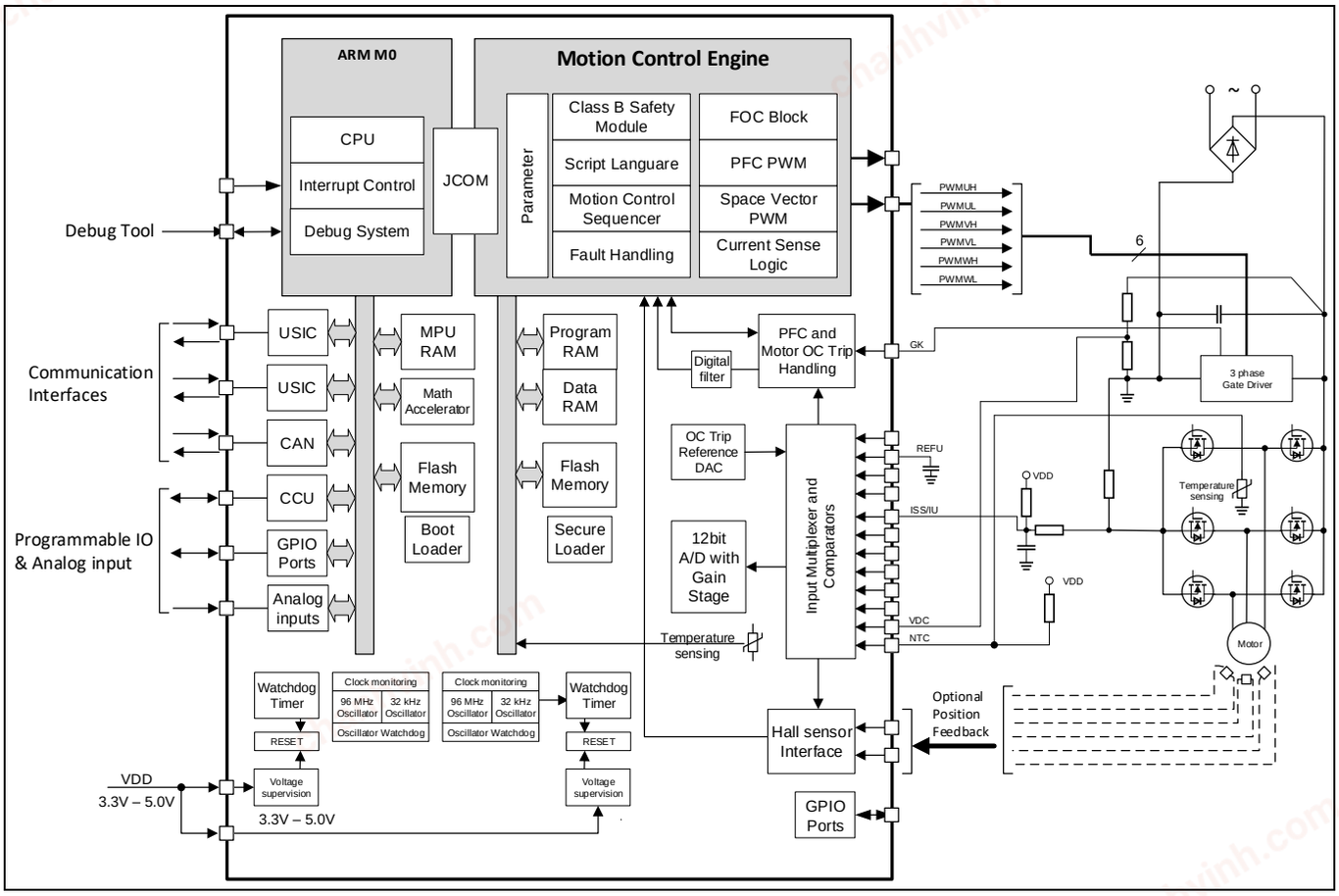


Figure 6 IMC301A Application Schematics Diagram (Single Shunt Current Sensing)

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3.2 Application Schematics for IMC302A with Single Shunt Current Sensing

Figure 7 shows the application schematics diagram for an air-conditioner outdoor unit system with single shunt current sensing and a boost mode PFC configuration. Hall sensor feedback options support applications requiring high torque during start-up.

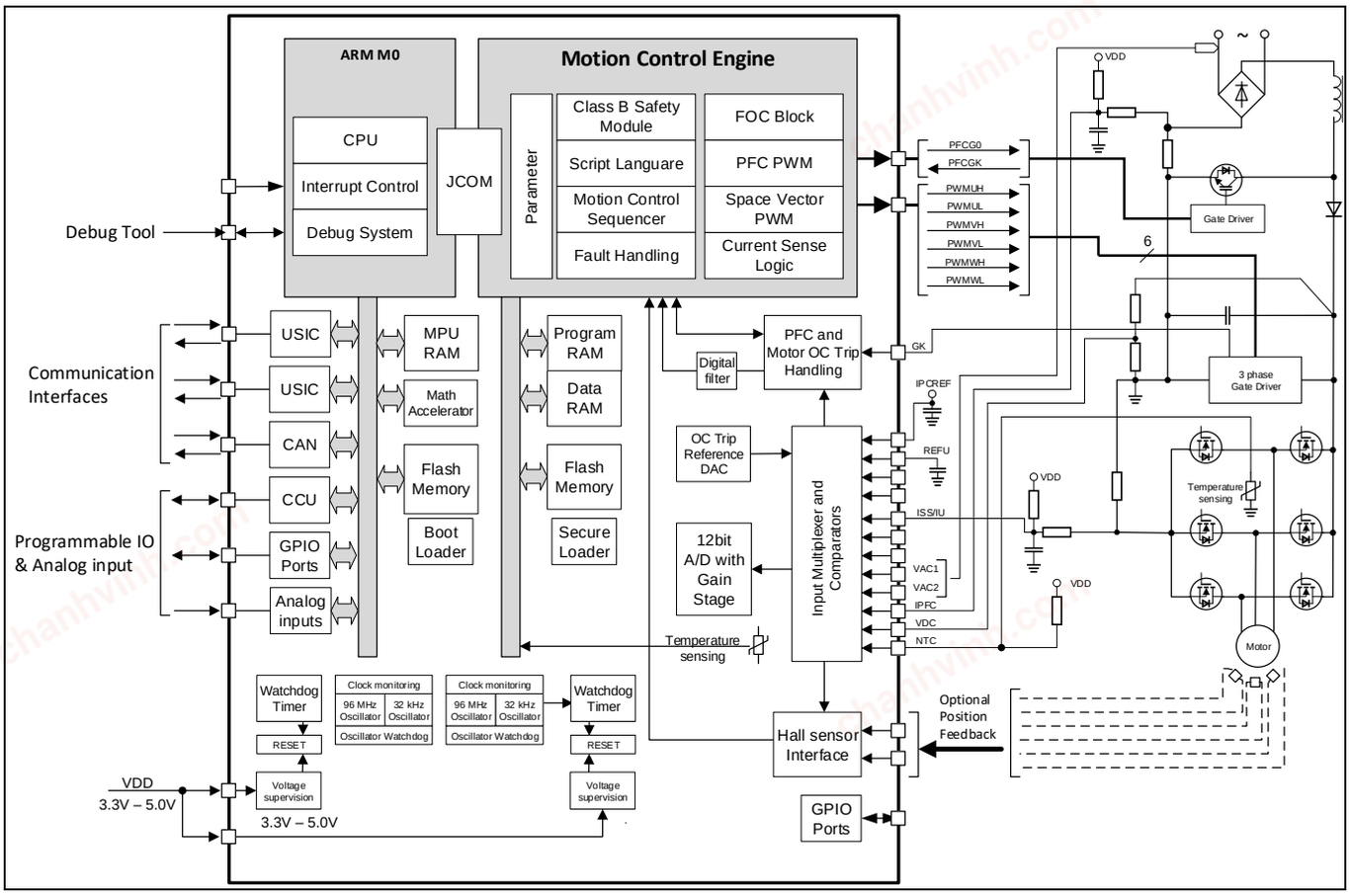


Figure 7 IMC302A Application Schematics Diagram (Single Shunt Current Sensing)

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3.3 Application Schematics for IMC302A with Leg Shunt Current Sensing

Figure 8 shows the application schematics diagram for an air-conditioner outdoor unit system with leg shunt current sensing and a boost mode PFC configuration.

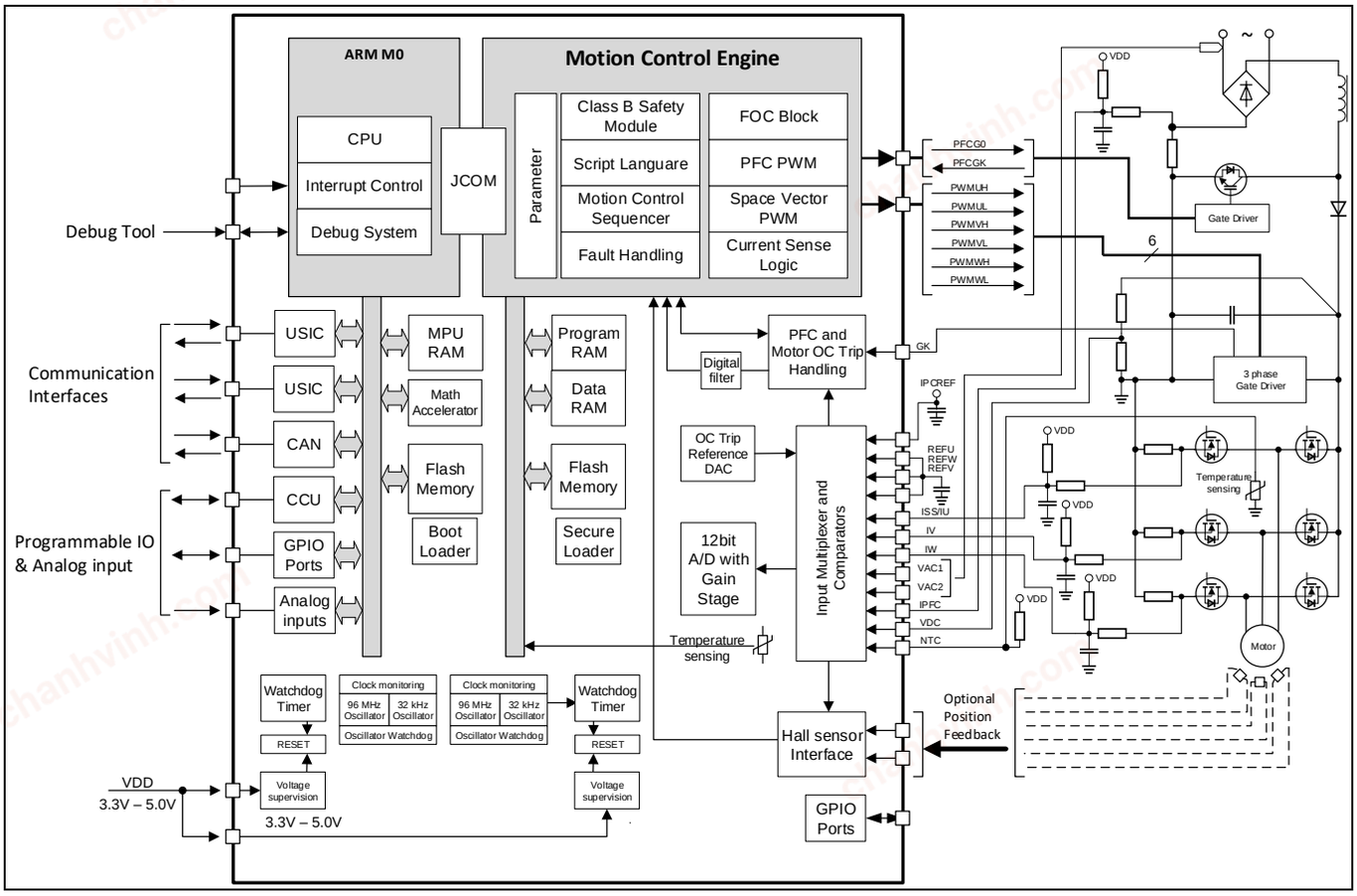


Figure 8 IMC302A Application Schematics Diagram (Leg Shunt Current Sensing)

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4 Electrical characteristics and parameters

4.1 General Parameters

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the IMC300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the IMC300 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the IMC300 is designed in.

4.1.2 Absolute Maximum Ratings

Stresses above the values listed under ***Absolute Maximum Ratings*** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Ambient temperature	T_A SR	-40	–	105	°C	–
Junction temperature	T_J SR	-40	–	115	°C	–
Storage temperature	T_{ST} SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SS}	V_{DD} *SR*	-0.3	–	6	V	–
Voltage on pins with respect to V_{SS}	V_{IN} SR	-0.3	–	V_{DDP} + 0.3	V	
Input current on any pin during overload condition	I_{IN} *SR*	-5	–	5	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN} *SR*		–	25	mA	–

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4.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.
Table 3 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- ***Operating Conditions*** are met for
  - pad supply levels (V_{DDP})
  - temperature

If a pin current is outside of the ***Operating Conditions*** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: *An overload condition on one or more pins does not require a reset.*

Note: *A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

Table 3 Overload Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input current on analog port pins during overload condition	I_{OVA} SR	-3	–	3	mA	
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

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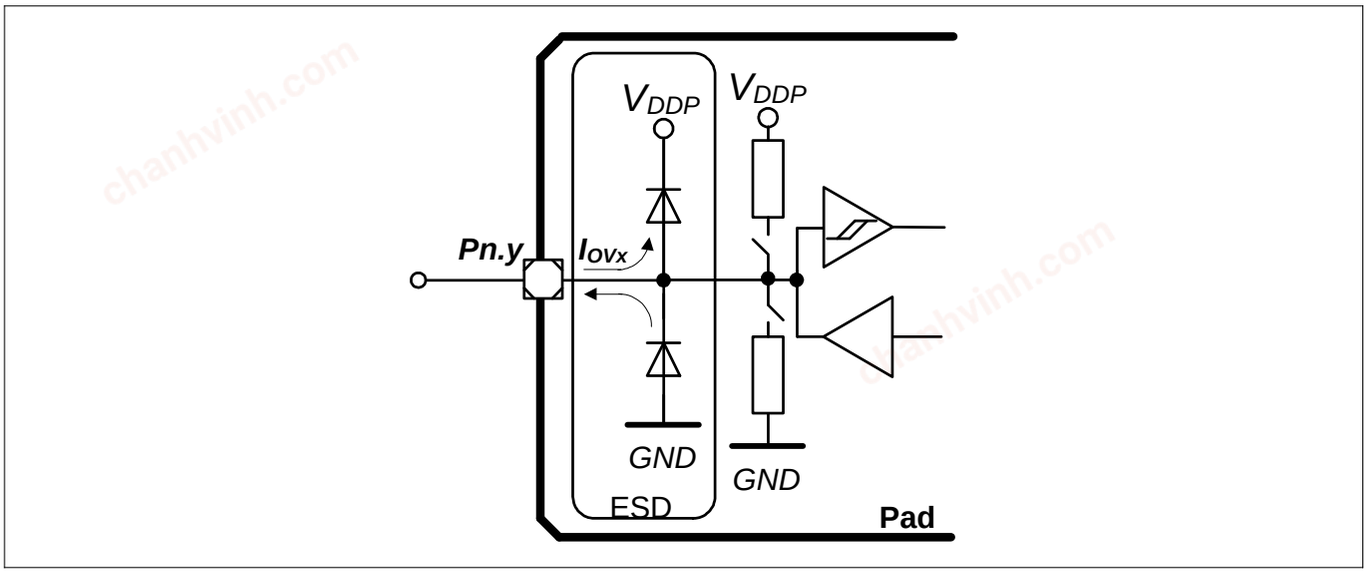


Figure 9 Input Overload Current via ESD structures

Table 4 and *Table 5* list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the *Absolute Maximum Ratings* must not be exceeded during overload.

Table 4 PN-Junction Characterisitics for Positive Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DD}$ +(0.3 ... 0.5) V $V_{AIN} = V_{DD}$ + 0.5 V $V_{AREF} = V_{DD}$ + 0.5 V

Table 5 PN-Junction Characterisitics for Negative Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS}$ - (0.3 ... 0.5) V $V_{AIN} = V_{SS}$ - 0.5 V $V_{AREF} = V_{SS}$ - 0.5 V

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4.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the IMC30xA. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 6 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	105	°C	
Junction temperature	T_J SR	-40	–	115	°C	
Digital supply voltage[1)]	V_{DDP} SR	3.0	3.3	5.5	V	All V_{DD} pins need to be connected on the circuit board.
Short circuit current of digital outputs[2)]	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device[2)]	ΣI_{SC_D} SR	–	–	25	mA	For MCE peripheral pins
Absolute sum of short circuit currents of the device[3)]	ΣI_{SC_D} SR	–	–	25	mA	For MCU peripheral pins

[1] See also the Supply Monitoring thresholds ***Power-Up and Supply Threshold Characteristics***.

[2] Applicable for digital outputs.

[3] See also section "Pin Reliability in Overload" for overload current definitions.

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4.1.5 Input / Output Characteristics

The table below provides the characteristics of the input/output pins of the IMC300.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Note: *Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.*

Table 7 Input / Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on PWM outputs	V_{OLP1}	CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
			–	0.32	V	I_{OL} = 10 mA (5 V)
			–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on PWM outputs	V_{OHP1}	CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
			V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Rise/fall time on PWM outputs[1)]	t_{HCPR}, t_{HCPF}	CC	–	9	ns	50 pF @ 5 V
			–	12	ns	50 pF @ 3.3 V
Rise/fall time on standard pad	t_R, t_F	CC	–	12	ns	50 pF @ 5 V
			–	15	ns	50 pF @ 3.3 V.
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	

[1] Rise/Fall time parameters are taken with 10% - 90% of power supply.

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Electrical characteristics and parameters

Table 7 Input / Output Characteristics (Operating conditions apply) (continued)

Parameter	Symbol		Values		Unit	Test Conditions
			Min.	Max.		
Pull-up/-down resistor on port pins (if enabled in software)	R_{PUP}	CC	20	50	kΩ	$V_{IN} = V_{SSP}$
Input leakage current [1)]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, T_A 105°C
Maximum current per pin standard pin	I_{MP}	SR	-10	11	mA	–
Maximum current per PWM outputs pins	I_{MP1A}	SR	-10	50	mA	–
Maximum current into V_{DDP} / out of V_{SS}	I_{MVDD} / I_{MVSS}	SR	–	260	mA	

[1] An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

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4.1.6 Analog to Digital Converter (ADC)

The following table shows the Analog to Digital Converter (ADC) characteristics. This specification applies to all analog input as given in the pin configuration list.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 8 ADC Characteristics (Operating conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage range	V_{DD} SR	3.0	–	5.5	V	
Analog input voltage range	V_{AIN} SR	V_{SSP}- 0.05	–	V_{DDP}+ 0.05	V	
Conversion time	t_{C12} CC	–	1.0	1.6	µs	
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	
Sample time	t_{sample} CC	–	200	–	ns	
RMS noise	EN_{RMS} CC	–	1.5	–	LSB12	
DNL error	EA_{DNL} CC	–	±2.0	–	LSB12	
INL error	EA_{INL} CC	–	±4.0	–	LSB12	
Gain error	EA_{GAIN} CC	–	±0.5	–	%	V_{DD} = 3.3V
Offset error	EA_{OFF} CC	–	±8.0	–	mV	

[1] All parameters are defined for the full supply voltage range if not stated otherwise.

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4.1.7 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component. Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 9 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Active mode current motor control only	I_{DDPWM} CC	–	15	40	mA	MCE clock 48MHz MPU clock 1 – 48Mhz
Active mode current motor control plus PFC	I_{DDPFC} CC	–	19	40	mA	IMC302A only
Deep Sleep mode current[1)]	I_{DDPDS} CC	–	0.54	–	mA	Both cores
Wake-up time from Sleep to Active mode	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode	t_{DSA} CC	–	290	–	µsec	

4.1.8 Flash Memory Parameters

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 10 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Data Retention Time	t_{RET} CC	10			years	Max. 100 erase / program cycles
Erase Cycles[2)]	N_{ECYC} CC			$5x10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC			$2x10^6$	cycles	

[1] CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wakeup.

[2] Sum of page erase and sector erase cycles a page sees.

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4.2 AC Parameters

4.2.1 Testing Waveforms

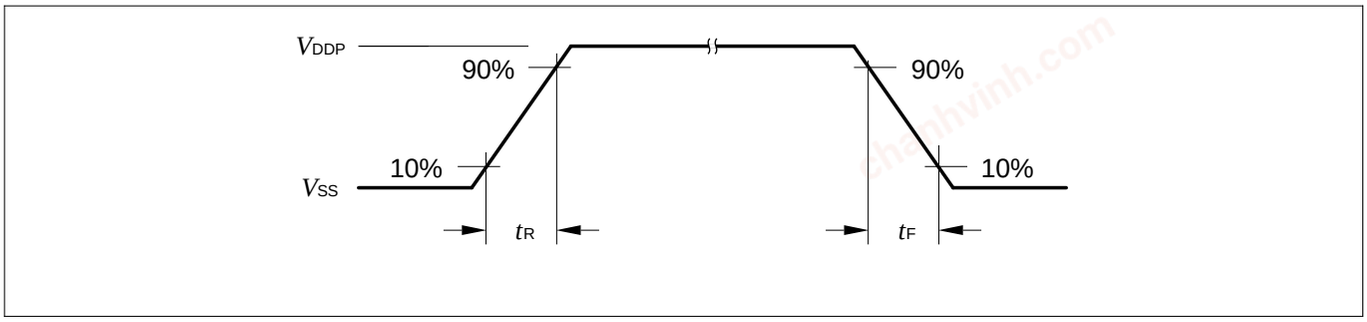


Figure 10 Rise/Fall Time Parameters

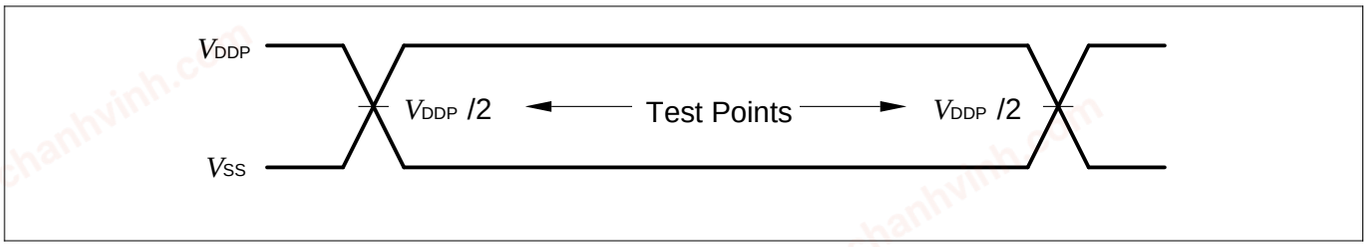


Figure 11 Testing Waveform, Output Delay

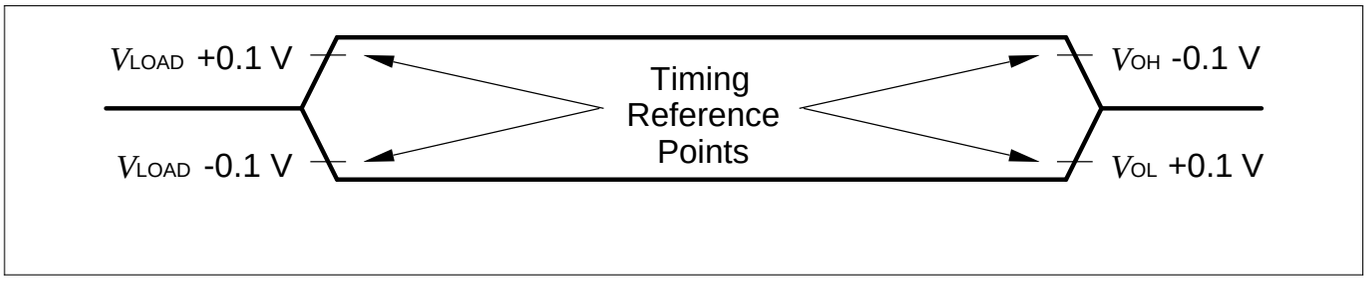


Figure 12 Testing Waveform, Output High Impedance

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4.2.2 Power-Up and Supply Threshold Characteristics

This chapter provides the characteristics of the supply threshold in IMC300.
The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.
The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Note: *Operating Conditions apply.*

Table 11 Power-Up and Supply Threshold Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$[9] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[10]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

9 A capacitor of at least 100 nF has to be added between VDDP and VSSP to fulfill the requirement as stated for this parameter.

10 Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

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Table 11 Power-Up and Supply Threshold Parameters (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
Start-up time from poweron reset	t_{SSW} CC	–	260	–	µs	Time to the first user code instruction[1)]
Start-up time to PWM on	t_{PWMON} CC	5.2	-	360	ms	Time to PWM enabled

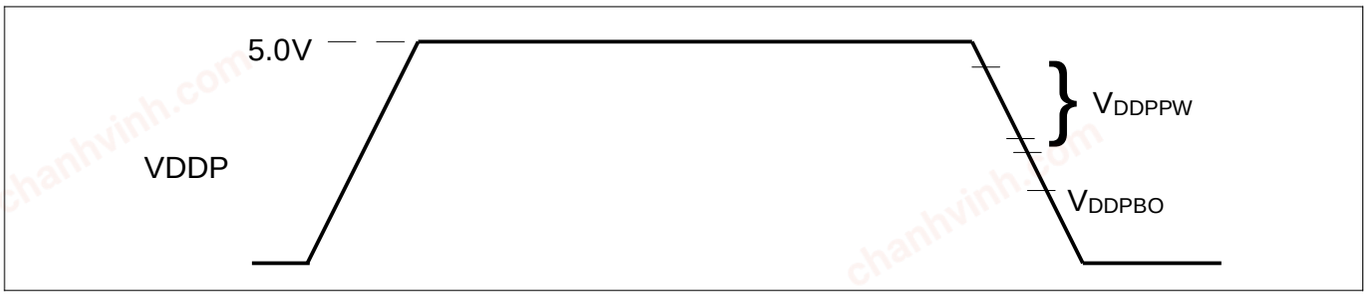


Figure 13 Supply Threshold Parameters

1 This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 48 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

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4.2.3 On-Chip Oscillator Characteristics

Table 12 provides the characteristics of the 96 MHz digital controlled oscillator DCO1. The DCO1 is used as the time base for peripherals during normal operation. The MCE core clock always runs at 48 MHz. The MCU core clock starts up at 48MHz but can be reduced to 32MHz, 16MHz or 1 MHz after startup.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Table 12 96 MHz DCO1 Characteristics

Parameter	Symbol	Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	-	96	-	MHz	under nominal conditions[1] after trimming
Accuracy with adjustment on XTAL as reference	Δf_{LTX} CC	-0.3	-	+0.3	%	with respect to f_{NOM} (typ), T_A from -40 °C to 105 °C
Accuracy with adjustment algorithm [2] based on temperature sensor	Δf_{LTTS} CC	-0.6	-	+0.6	%	with respect to f_{NOM} (typ), T_A from 0 °C to 105 °C
		-1.9	-	+1.0	%	with respect to f_{NOM} (typ), T_A from -25 °C to 105 °C
		-2.6	-	+1.3	%	with respect to f_{NOM} (typ), T_A from -40 °C to 105 °C
Accuracy	Δf_{LT} CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), T_A from 0 °C to 85 °C
		-3.9	–	4.0	%	with respect to f_{NOM}(typ), T_A from -40 °C to 105 °C

Table 13 provides the characteristics of the 32 kHz digital controlled oscillator DCO2. The DCO2 is only used internally as a secondary clock source for the internal watchdog and as a fallback in case of failure of DCO1.

Table 13 32 kHz DCO2 Characteristics

Parameter	Symbol	Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	32.5	32.75	33	kHz	under nominal conditions[1] after trimming

[1] The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.

[2] MCE version newer or equal to V1.03.00, clock adjustement algorithm for improved accuracy enabled.

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Short term frequency deviation (over V_{DDC})	Δf_{ST} CC	-1	–	1	%	with respect to f_{NOM}(typ), at 25°C
Accuracy	Δf_{LT} CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), T_A from 0 °C to 85 °C
		-3.9	–	4.0	%	with respect to f_{NOM}(typ), T_A from -40 °C to 105 °C

4.3 Motor Control Parameters

The following parameters are defined in the iMOTION™ Motion Control Engine (MCE) software.

4.3.1 PWM Characteristics

Table 14 PWM Carrier Frequency Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Motor PWM frequency	f_{PWM}	5	16	40	kHz	Ta=25 °C, VDD = nominal

4.3.2 Current Sensing Characteristics

Table 15 Motor Current Sensing Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Input range	I_{PWM}	VSS-0.05	-	VDD+0.05	V	Ta=25 °C, VDD = nominal
Configurable analog gain			1/3/6/12			
Itrip input range	$I_{PWMTRIP}$	VSS-0.05	-	VDD+0.05	V	
Itrip offset Accuraccy			±8	-	mV	
REF Input capacitance	$C_{REFIU/V/W}$	-	-	10	pF	External capacitance required on REFU,REFV, REFW

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4.3.3 Fault Timing

Table 16 Gatekill Timing

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
GK pulse width	t_{wGK}	1	-	-	µs	Ta = 25 °C, VDD = nominal
GK input to PWM shutoff	t_{GK}	-	1.3	-	µs	
Motor Fault reset timing	t_{RESET}	-	1.84	-	ms	fault reset command via UART to PWM reactivation
Itrip to PWM shutoff	t_{PWMOFF}	-	1.0	-	µs	single shunt configuration
Itrip to PWM shutoff	t_{PWMOFF}	-	1.0	-	µs	leg shunt configuration

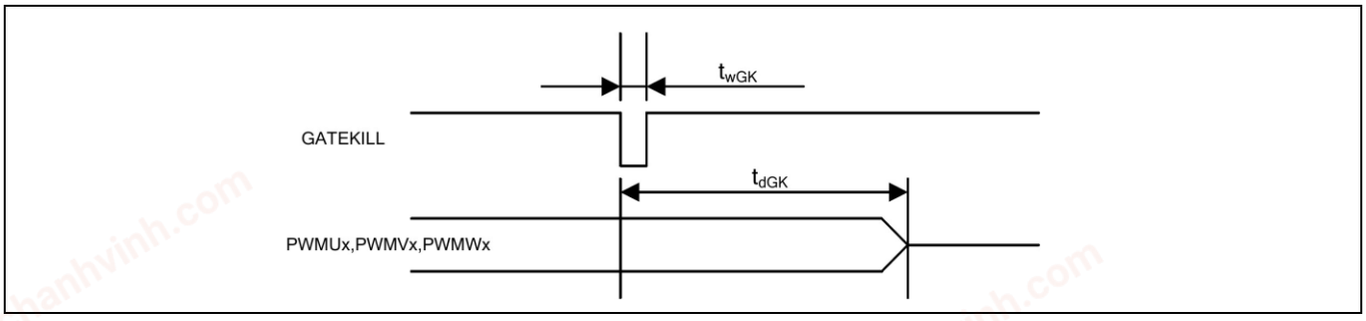


Figure 14 Fault timing

4.3.4 Analog Hall Sensing Characteristics

Table 17 Analog Hall Input Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Input range	V_H	VSS-0.05	-	VDD+0.05	V	Ta = 25 °C, VDD = nominal
Comparator Offset	V_{CMPOFF}	-	+/-3	-	mV	
Comparator Hysteresis			±15	-	mV	

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4.4 Power Factor Correction (PFC) parameters

The following parameters are defined in the iMOTION™ Motion Control Engine (MCE) software.

4.4.1 Boost PFC characteristics

Table 18 PWM Carrier Frequency Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
PFC PWM frequency	f_{PFC}	-	20	50	kHz	Motor PWM frequency within specified range

4.4.2 Totem Pole PFC characteristics

Table 19 PWM carrier frequency Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
PFC PWM frequency	f_{PFC}	-	20	50	kHz	Motor PWM frequency within specified range

4.4.3 PFC current sensing characteristics

Table 20 PFC Current Sensing Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Input range	I_{PFC}	VSS-0.05	-	VDD+0.05	V	Ta=25 °C, VDD=nominal
Configurable analog gain			1/3/6/12			
Itrip input range	$I_{PFCTRIP}$	VSS-0.05	-	VDD+0.05	V	
Itrip offset			±3	-	mV	Input voltage difference > 200mV
REF Input capacitance	$C_{REFIPFC}$	-	-	10	pF	External capacitor required on IPFCREF

4.4.4 PFC Fault timing

Table 21 PFC Fault Timing

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Itrip to PFCPWM shutoff	t_{PFCOFF}	-	1.18	-	µs	
Motor Fault reset timing	t_{RESET}	-	1.0	-	ms	Fault reset command via UART to PWM reactivation

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4.5 Control Interface Parameters (MCE)

IMC300 series provides the following communication interfaces.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

4.5.1 UART Interface

Table 22 Electrical Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
UART baud rate		1200	57600	-	BPS	
UART mode		-	8-N-1	-		Data-parity-stop bit
UART sampling filter period	$T_{UARTFIL}$	-	1/16	-	T_{BAUD}	

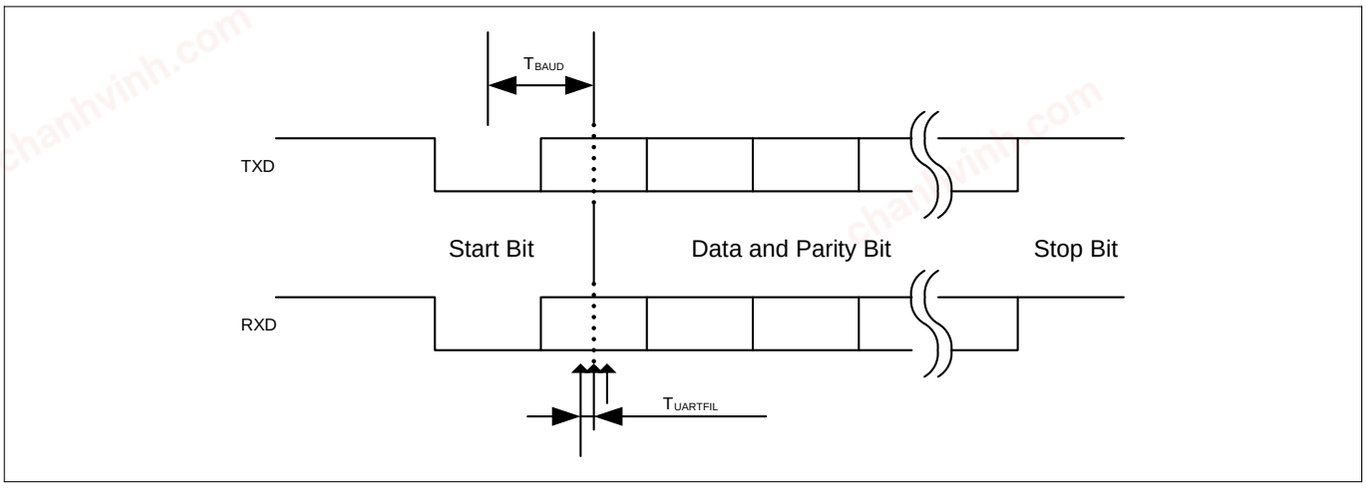


Figure 15 UART Timing

4.5.2 Over Temperature Input

The over temperature input can be used to continuously monitor an external temperature sensor like an NTC. Specific type of NTC has to be used. Refer to the MCE Reference Manual for details.

Table 23 Over temperature input

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Over temperature input threshold	V_{OT}	0.1	1.0	3.0	V	VDD = 3.3V, configurable parameter e.g. via MCEDesigner, default = 1.0V
Over temperature to PWM shutdown	t_{ot}	-	1.0	2.1	ms	

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4.5.3 Pulse Output

The IMC300 series provide an optional PGOUT pin pulse output. The pulse frequency is proportional to motor revolution. Refer to the MCE software reference manual for details.

Table 24 Pulse Output

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Pulse per revolution	*PPR*	4	-	24	PPR	
Pulse duty cycle	t_{PPR}	-	50	-	%	

4.5.4 LED Output

The IMC300 series provide an output that can be connected to an LED to give a visual indication of the status of the motor drive.

Table 25 LED Output

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Fault to LED delay	$t_{LEDFAULT}$	-	53	-	ms	
Fault reset to LED delay	$t_{LEDRESET}$	-	1.84	-	ms	
LED blinking frequency	f_{LED}	1		1000	Hz	
LED blinking duty cycle	t_{LED}	5		95	%	

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5 Quality Declaration

Table 26 Quality Parameters

Parameter	Symbol	Values		Unit	Condition
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to ANSI/ESDA/JEDEC JS-001
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to ANSI/ESDA/JEDEC JS-002
Moisture sensitivity level	*MSL* CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D

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6 Device and Package Specification

6.1 SBSL and Chip-IDs

The table below gives the IDs for the individual devices in the IMC300 family. Depending upon the mode either the SBSL-ID (secure boot loader) or the Chip-ID should be used to identify the device.

Both cores of the IMC300 family have a dedicated Chip-ID. The MCE core is programmed via a secure loader using the SBSL-IDs as given below.

For details refer to the iMOTION™ Programming Manual.

Table 27 SBSL and Chip IDs

Product Type	Core	Chip-ID	SBSL-ID
IMC301A-F048	MCE	0x1B010006	0x026add3f080ad5abfb67af2271ea4973
	ARM® Cortex®-M0	0x13011006	-
IMC301A-F064	MCE	0x1B01000B	0x0207810c349410e8be51722b81520cf8
	ARM® Cortex®-M0	0x1301100B	-
IMC302A-F048	MCE	0x1B020006	0x024747b4b61060cf95f7b14a05b1decc
	ARM® Cortex®-M0	0x13021006	-
IMC302A-F064	MCE	0x1B02000B	0x0216ebe1d4cc0767684bacceefae29b2
	ARM® Cortex®-M0	0x1302100B	-

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6.2 Package Drawings

6.2.1 PG-LQFP-48-11

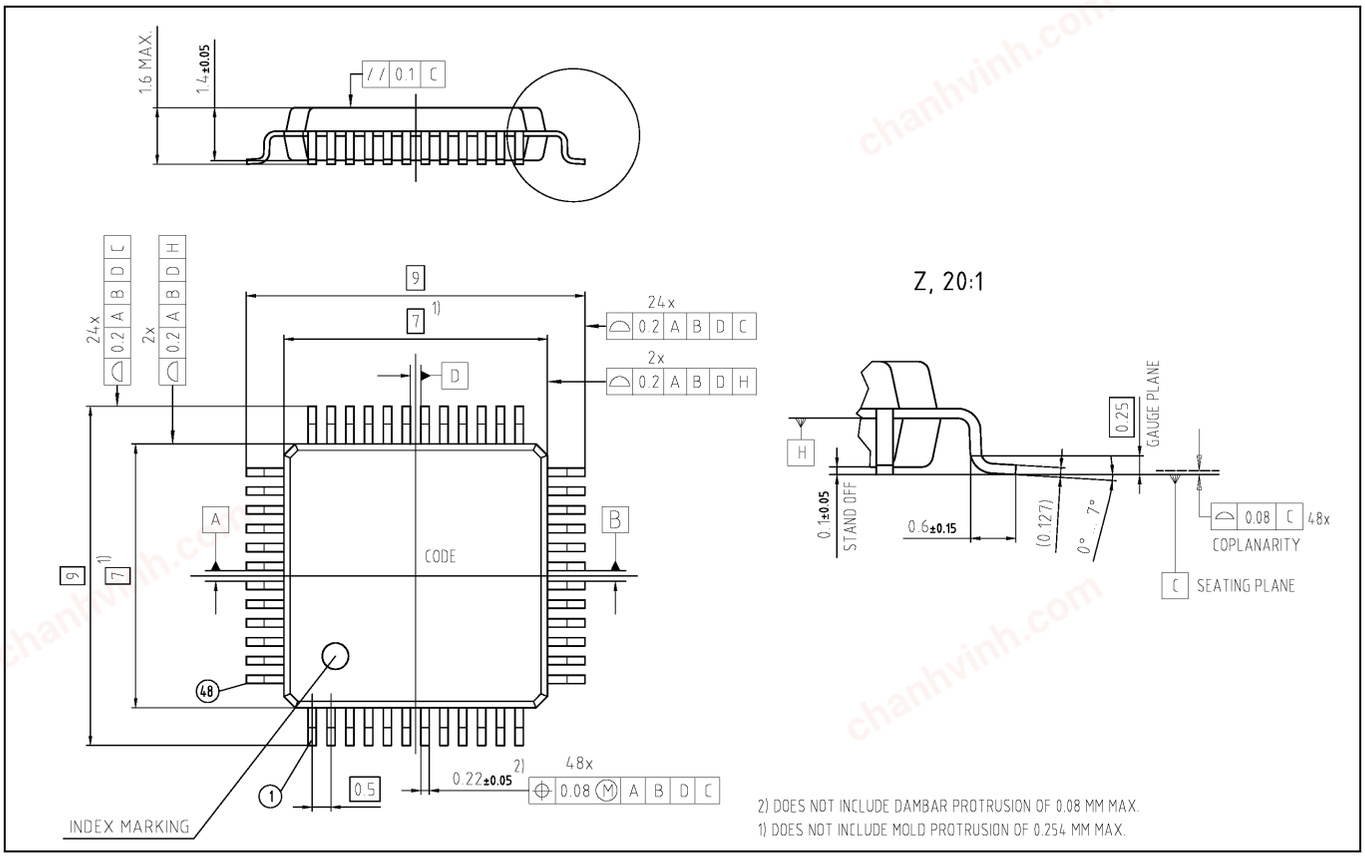


Figure 16 PG-LQFP-48-11

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6.2.2 PG-LQFP-64-29

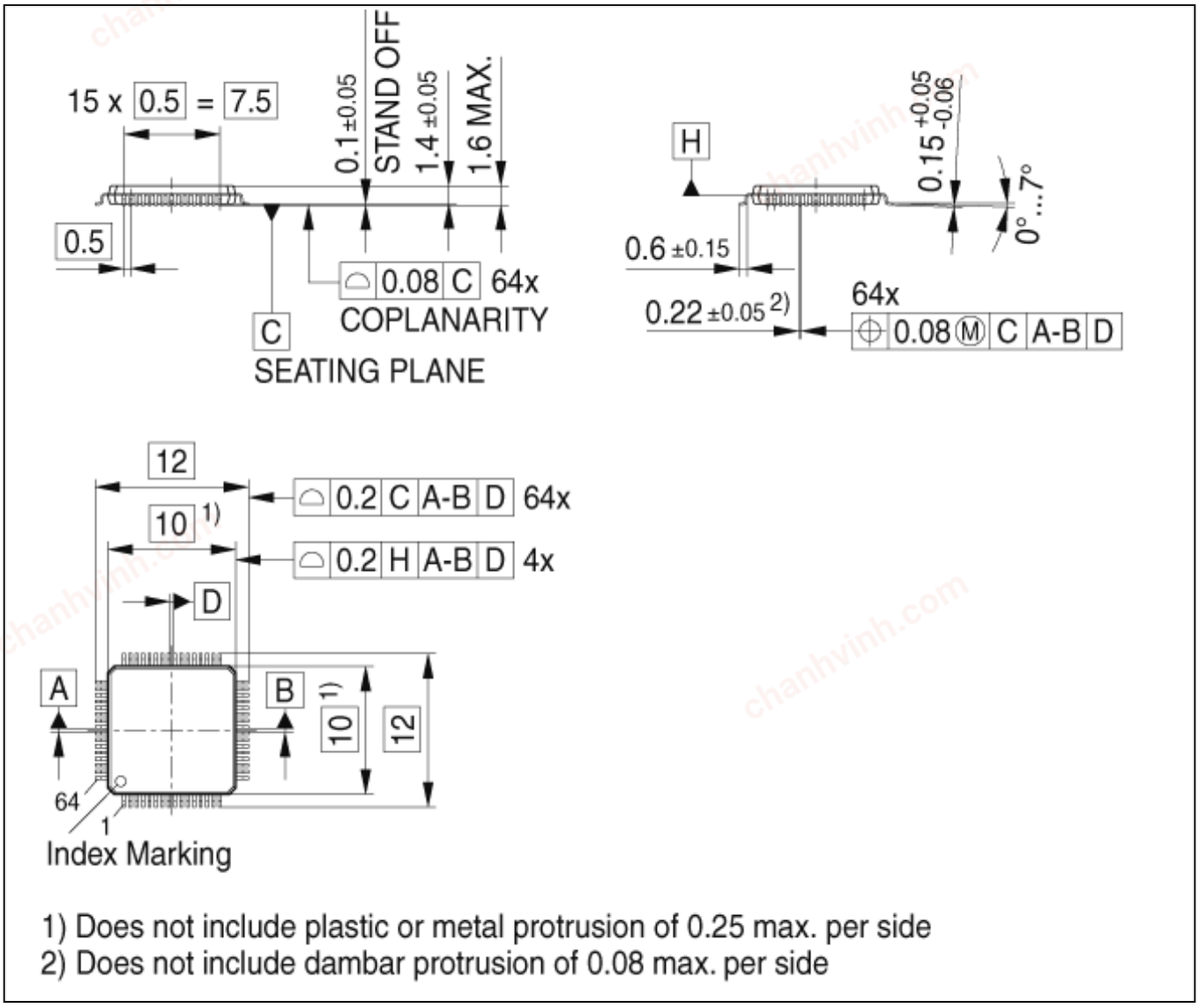


Figure 17 PG-LQFP-64-29

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6.3 Thermal Characteristics

Table 28 Package Thermal Characteristics

Parameter	Symbol	Values		Unit	Condition
		Min.	Max.		
Thermal resistance Junction-Ambient[1)]	$R_{\Theta JA}$ CC	-	66.7	K/W	PG-LQFP-64-26
		-	TBD	K/W	PG-LQFP-48-26

Note: For electrical reasons, it is required to connect the exposed pad to the board ground VSSP, independent of EMC and thermal requirements.

When operating the IMC300 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage. The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance RΘJA” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115°C. The difference between junction temperature and ambient temperature is determined by

$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DD} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

$P_{IOSTAT} = \Sigma((V_{DD} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (PIODYN) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce VDD, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

1 Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad of VQFN soldered

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6.4 Part Marking

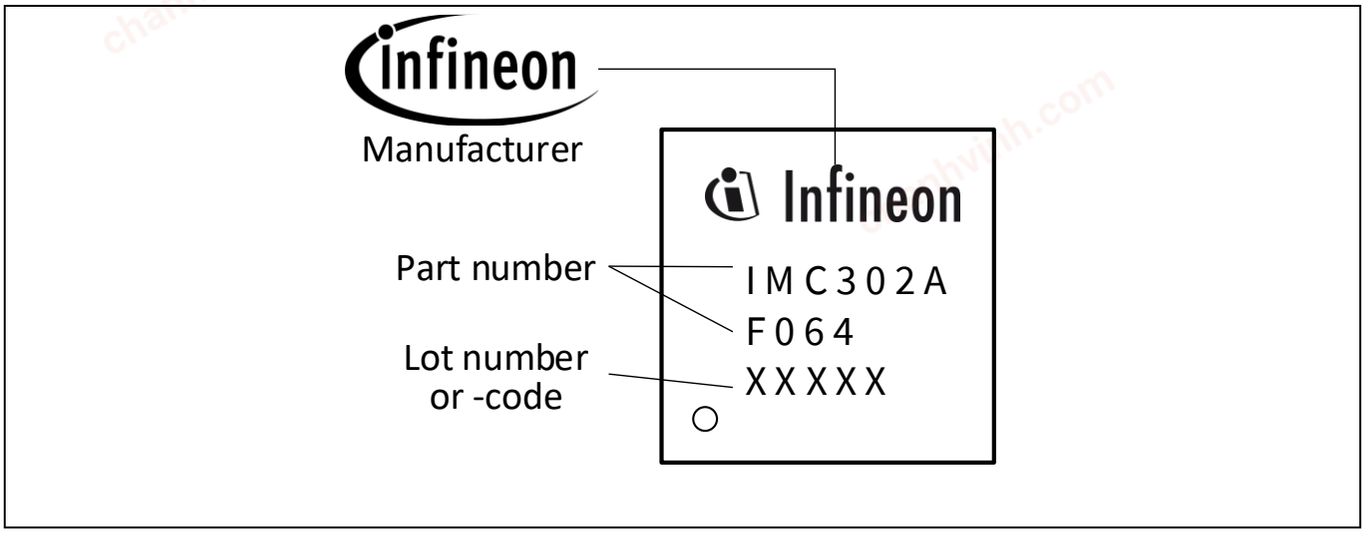


Figure 18 Part Marking

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Revision history

Document version	Date of release	Description of changes
1.2	2020-10-20	Table 1 (Pin List) updated.
1.1	2020-5-11	Figure and table numbers updated. Table 1 (Pin List) updated. Pin configuration drawings updated. Added DCO accuracy with calibration. Increased max. motor PWM frequency up to 40 kHz. Application schematics drawings in section 3 updated. Section 5 (Quality Declaration) updated.
1.0	2019-12-12	Initial version

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