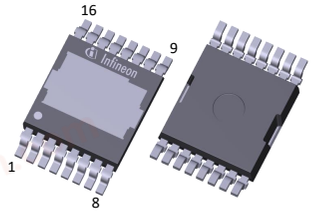
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Public

IGLT65R035D2
Final datasheet

CoolGaN™ G5

TOLT

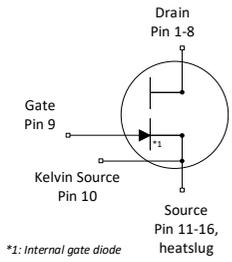


CoolGaN™ Transistor 650 V G5

Infineon's CoolGaN™ is a highly efficient gallium nitride (GaN) transistor designed for power conversion at 650 V. It enables higher power density, supports reduced system BOM cost, and facilitates miniaturized form factors. Produced using 200 mm (8 inch) wafer technology and fully automated production lines, it features narrow production tolerances and the highest product quality. This makes it suitable for a wide range of applications, from consumer electronics to industrial applications.

Features

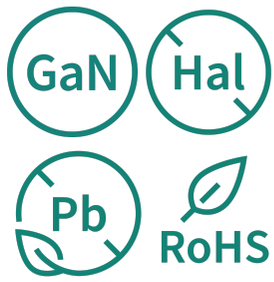
- Enhancement mode transistor
- Ultra-fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate and output charge
- Superior commutation ruggedness
- 2 kV HBM ESD standards



Benefits

- Normally OFF transistor technology ensures safe operation
- Enables rapid and precise power delivery control
- Improves system efficiency and reliability
- Ensures robust performance under challenging conditions

These features collectively make CoolGaN™ a game-changer in the realm of power conversion, offering a compelling combination of efficiency, compactness, and reliability.



Potential applications

Industrial, telecom, datacenter SMPS based on half-bridge hard and soft switching topologies such as totem pole PFC and high frequency LLC, as well as charger and adapter.

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{DS,max}$	650	V
$V_{DS,trans-max}$	900	V
$R_{DS(on),max}$	42	mΩ
$Q_{g,typ}$	7.7	nC
$I_{D,pulse}$	97	A
Q_{oss} @ 400 V	57	nC
Q_{rr}	0	nC

Type / Ordering code	Package	Marking	Related links
IGLT65R035D2	PG-HDSOP-16	65R035D2	see Appendix A

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1 Maximum ratings

at T_j = 25°C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80% of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain source voltage, continuous	$V_{DS,max}$	-	-	650	V	V_{GS} = 0 V, derating recommendation according JEDEC JEP198
Leakage current at drain source transient voltage	$I_{DS,trans}$	-	-	20	mA	V_{GS} = 0 V, $V_{DS,trans}$ = 900 V
Drain source voltage transient	$V_{DS,trans}$	-	-	900	V	<1% duty cycle, <1 µs, 1 million pulses
Drain source voltage, pulsed	$V_{DS,pulsed}$	-	-	750 650	V	T_j = 25°C; V_{GS} ≤ 0 V; cumulated stress time ≤ 1 h T_j = 125°C; V_{GS} ≤ 0 V; cumulated stress time ≤ 1 h
Switching surge voltage, pulsed	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse}$ = 750 V; turn on $I_{D,pulse}$ =44 A; T_j = 105°C; f ≤ 100 kHz, t ≤100 s (10 million pulses)
Continuous current, drain source [1]	I_D	-	-	47	A	T_C=25°C; T_j = $T_{j,max}$
Pulsed current, drain source	$I_{D,pulse}$	-97 -58	-	97 58	A	T_j=25°C; I_G=42 mA; See Diagram 3, 5 T_j=125°C; I_G=42 mA; See Diagram 4, 6
Gate current, continuous [2]	$I_{G,avg}$	-	-	32	mA	T_j=-55°C to T_j=150°C; See Table 9
Gate current, pulsed [2]	$I_{G,pulsed}$	-3.2	-	3.2	A	T_j=-55°C to T_j=150°C; t_{pulse}= 50 ns, f = 100 kHz; See Table 9
Gate source voltage, continuous [2]	V_{GS}	-10	-	-	V	T_j=-55°C to T_j=150°C; See Diagram 12
Gate source voltage, pulsed [2]	$V_{GS,pulse}$	-25	-	-	V	T_j=-55°C to T_j=150°C; t_{pulse}= 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	154	W	T_C=25°C
Operating junction temperature	T_j	-55	-	150	°C	-
Storage temperature	T_{stg}	-55	-	150	°C	Max shelf life depends on storage conditions
Drain-source voltage slew-rate	dv/dt	-	-	200	V/ns	-

[1] Limited by $T_{j,max}$. Maximum duty cycle D = 0.75

[2] We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for more details.

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2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.81	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	94	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	68	°C/W	Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thickness) copper area. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL1

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3 Electrical characteristics

at T_j=25°C, unless specified otherwise

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 -	1.2 1	1.6 -	V	I_{DS}=4.2 mA; V_{DS}=10 V; T_j=25°C I_{DS}=4.2 mA; V_{DS}=10 V; T_j=150°C
Gate-Source reverse clamping voltage	$V_{GS,\ clamp}$	-	-	-8	V	I_{GS}=-1 mA
Drain-Source leakage current	I_{DSS}	-	1.6 32	160 -	µA	V_{DS}=650 V, V_{GS}=0 V, T_j=25°C V_{DS}=650 V, V_{GS}=0 V, T_j=150°C
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.035 0.075	0.042 -	Ω	I_G=42 mA; I_D=13 A; T_j=25°C I_G=42 mA; I_D=13 A; T_j=150°C
Gate resistance	$R_{G,int}$	-	1.4	-	Ω	LCR impedance measurement; f=f_{res}, open drain;

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	540	-	pF	V_{GS}=0 V; V_{DS}=400 V, f=1 MHz
Output capacitance	C_{oss}	-	91	-	pF	V_{GS}=0 V, V_{DS}=400 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	1.3	-	pF	V_{GS}=0 V, V_{DS}=400 V, f=1 MHz
Effective output capacitance, energy related [3)]	$C_{o(er)}$	-	105	-	pF	V_{DS}=0 to 400 V
Effective output capacitance, time related [4)]	$C_{o(tr)}$	-	142	-	pF	V_{GS}=0 V; V_{DS}=0 to 400 V; I_D=const
Output charge	Q_{oss}	-	57	-	nC	V_{DS}=0 to 400 V
Coss stored energy	E_{oss}	-	8.4	.	µJ	V_{DS}=0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	I_D= 13 A; R_{ON}=3.3 Ohm; R_{OFF}=3.3 Ohm; R_{SS}=220 Ohm; C_C=5.3 nF; V_{DRV}=12 V; see Table 8
Turn-off delay time	$t_{d(off)}$	-	15	-	ns	I_D= 13 A; R_{ON}=3.3 Ohm; R_{OFF}=3.3 Ohm; R_{SS}=220 Ohm; C_C=5.3 nF; V_{DRV}=12 V; see Table 8
Rise time	t_r	-	10	-	ns	I_D= 13 A; R_{ON}=3.3 Ohm; R_{OFF}=3.3 Ohm; R_{SS}=220 Ohm; C_C=5.3 nF; V_{DRV}=12 V; see Table 8
Fall time	t_f	-	11	-	ns	I_D= 13 A; R_{ON}=3.3 Ohm; R_{OFF}=3.3 Ohm; R_{SS}=220 Ohm; C_C=5.3 nF; V_{DRV}=12 V; see Table 8

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3) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V
4) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	7.7	-	nC	V_{GS}=0 to 3 V; V_{DS}=400 V, I_D=13 A

Table 7 Reverse conduction characteristics

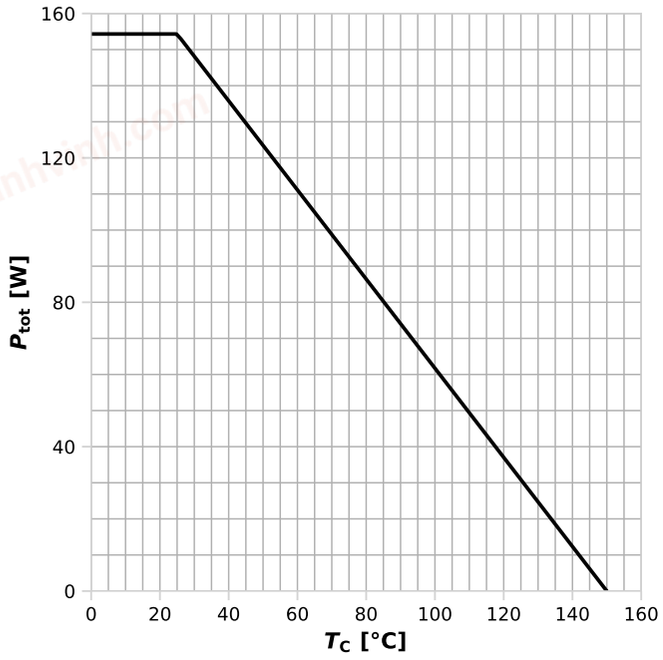
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.0	2.4	V	V_{GS}=0 V; I_{SD}=13 A
Pulsed current, reverse	$I_{SD,pulse}$	-	-	97	A	I_G=42 mA
Reverse recovery charge 5)	Q_{rr}	-	0	-	nC	I_{SD}=13 A; V_{DS}=400 V

5) Excluding Qoss

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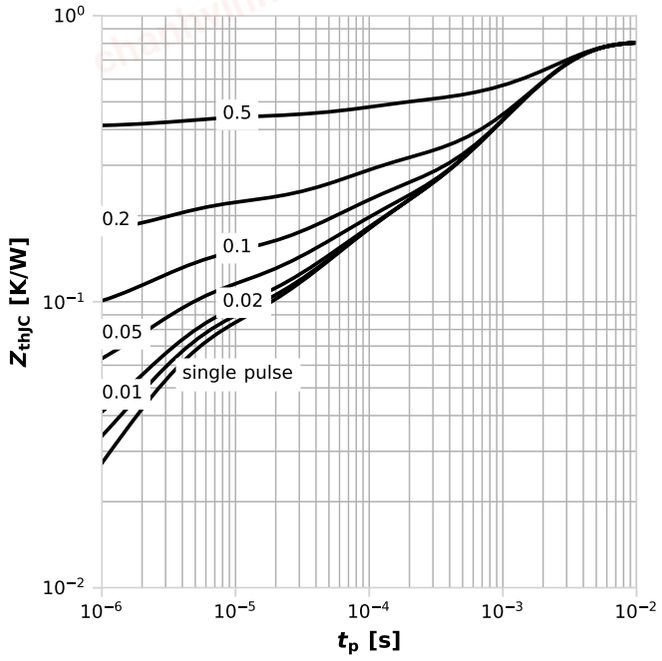
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



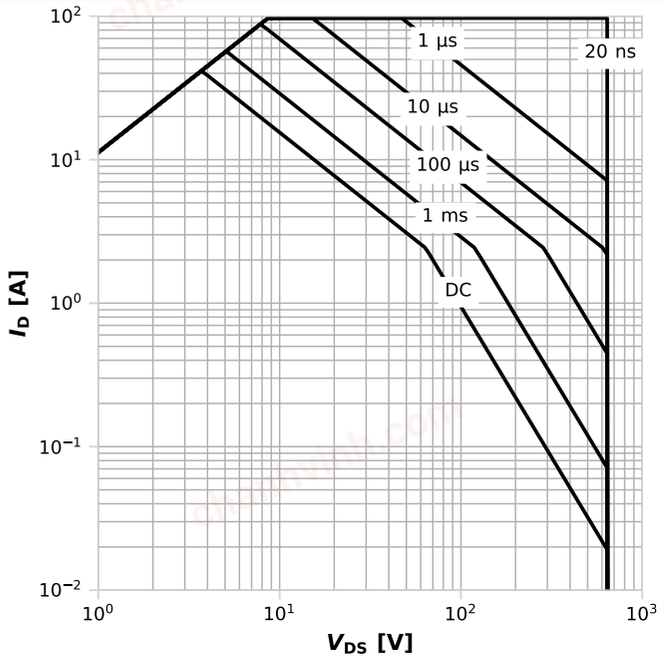
P_{tot}=f(T_C)

Diagram 2: Max. transient thermal impedance



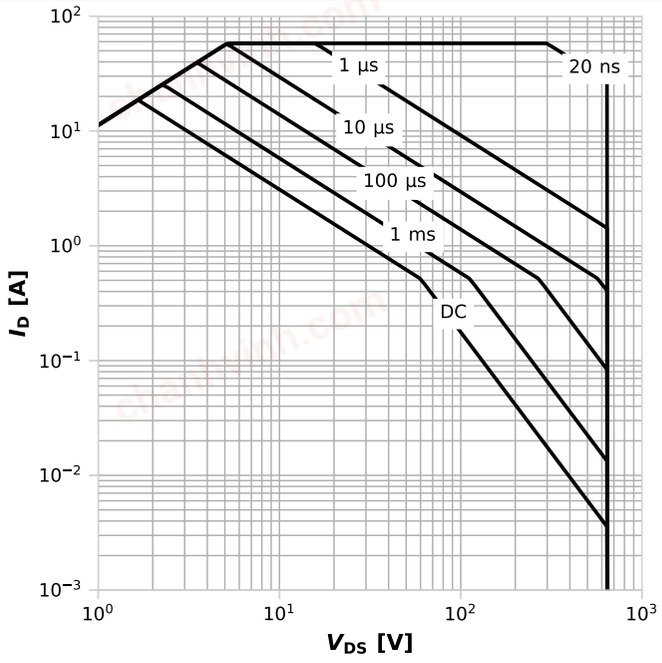
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25°C; D=0; parameter: t_p

Diagram 4: Safe operating area



I_D=f(V_{DS}); T_C=125°C; D=0; parameter: t_p

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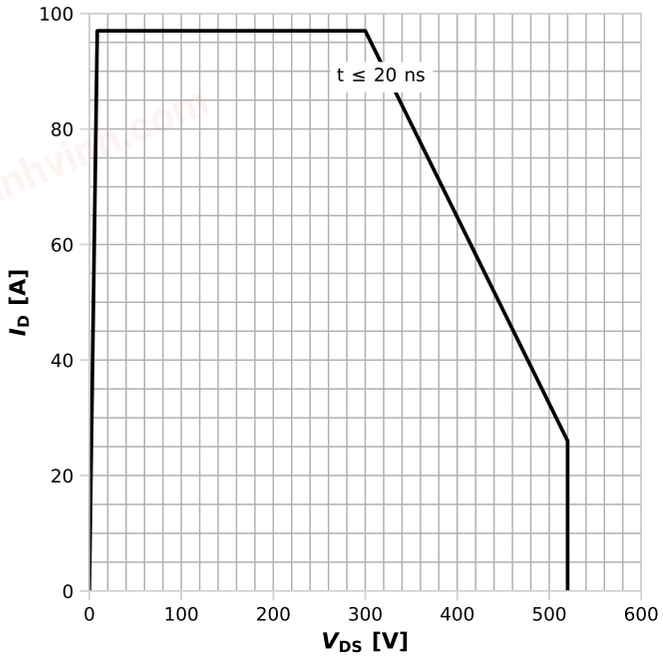
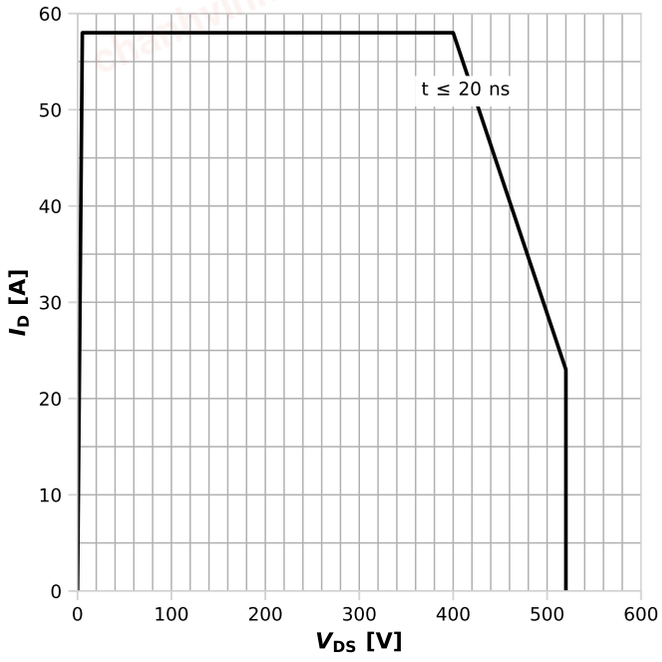
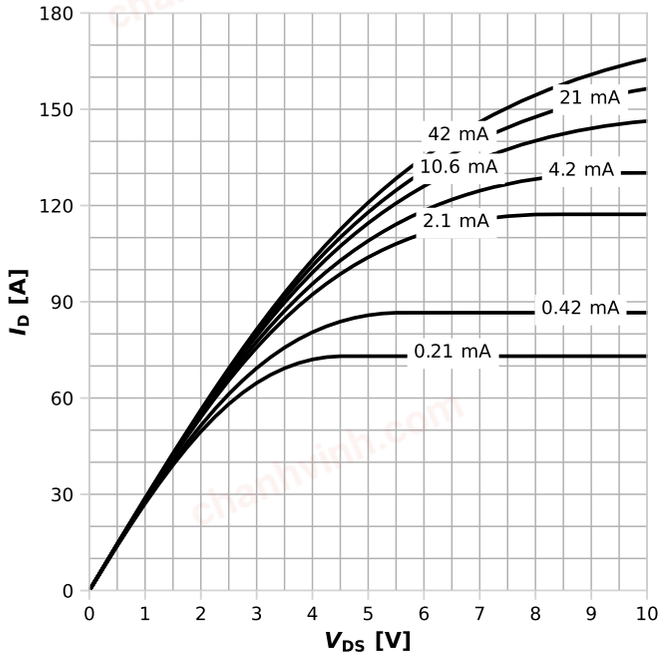
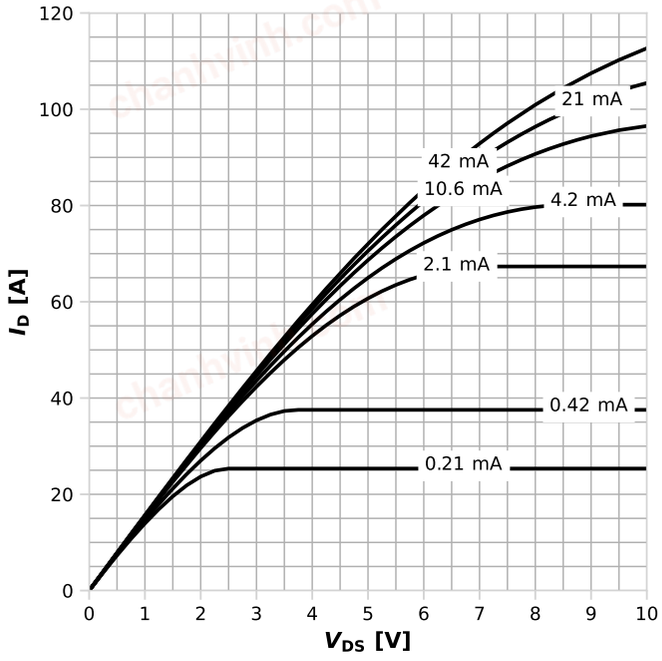
Diagram 5: Repetitive safe operating area	Diagram 6: Repetitive safe operating area
	
I_D=f(V_{DS}); T_C=25°C; T_j≤150°C; parameter: t_p	I_D=f(V_{DS}); T_C=125°C; T_j≤150°C; parameter: t_p

Diagram 7: Typ. output characteristics	Diagram 8: Typ. output characteristics
	
I_D=f(V_{DS}); T_j=25°C; parameter: I_{GS}	I_D=f(V_{DS}); T_j=125°C; parameter: I_{GS}

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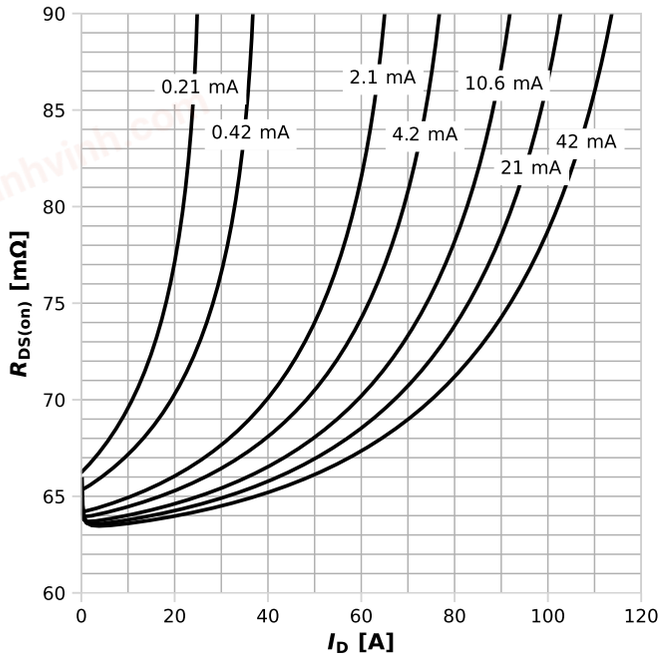
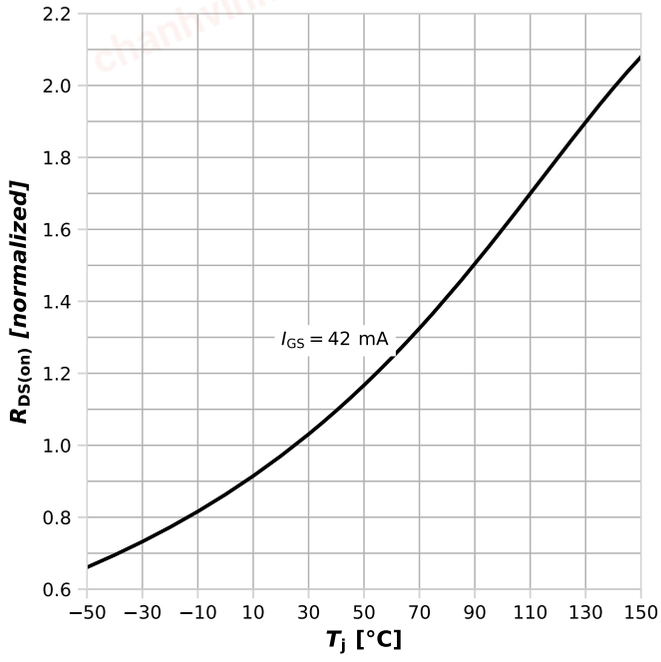
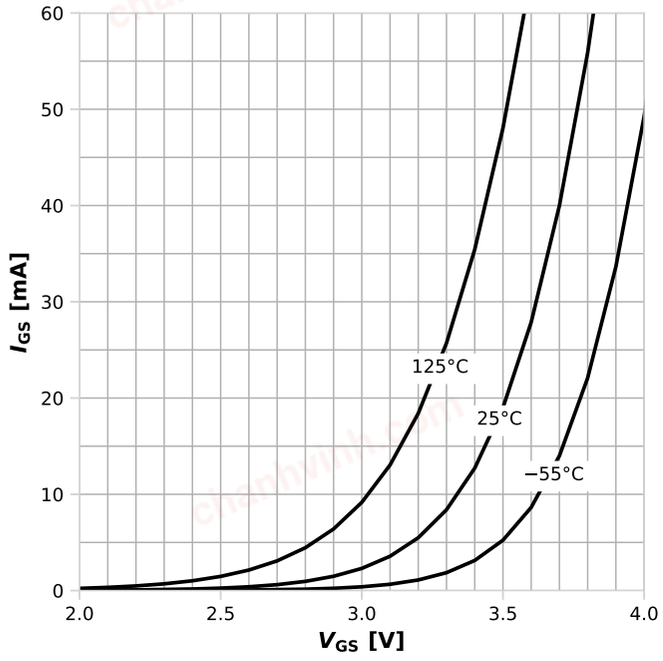
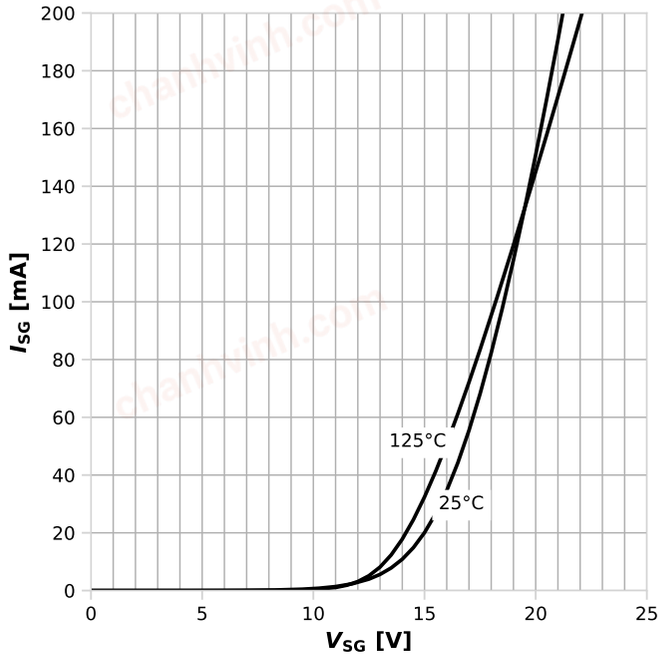
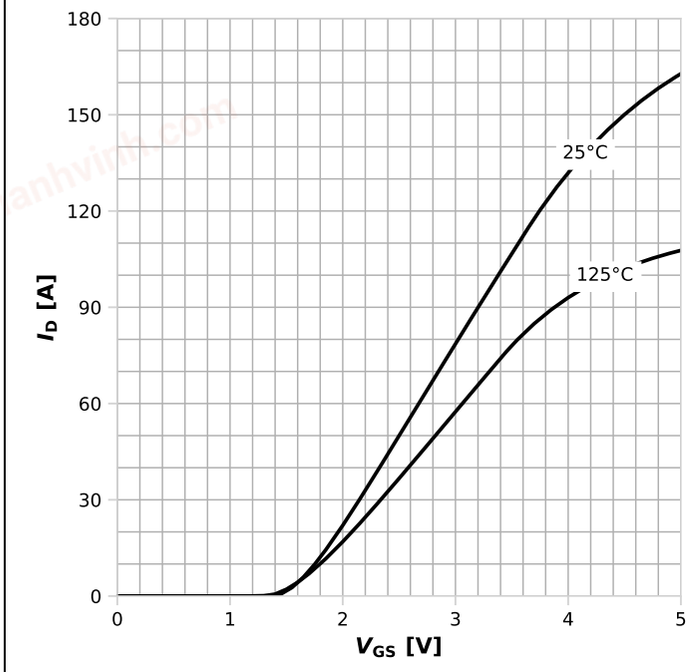
Diagram 9: Typ. Drain-source on-state resistance	Diagram 10: Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_D); T_j=125°C; parameter: I_{GS}	$R_{DS(on)}$=f(T_j); I_D=13 A

Diagram 11: Typ. gate characteristics forward	Diagram 12: Typ. gate characteristics reverse
	
I_{GS}=f(V_{GS}); open drain; parameter: T_j	I_{SG}=f(V_{SG}); parameter: T_j

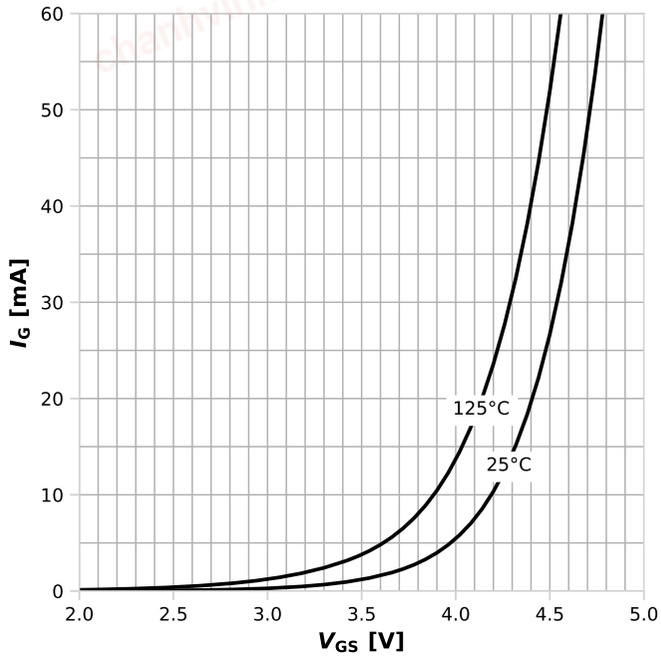
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Diagram 13: Typ. transfer characteristics



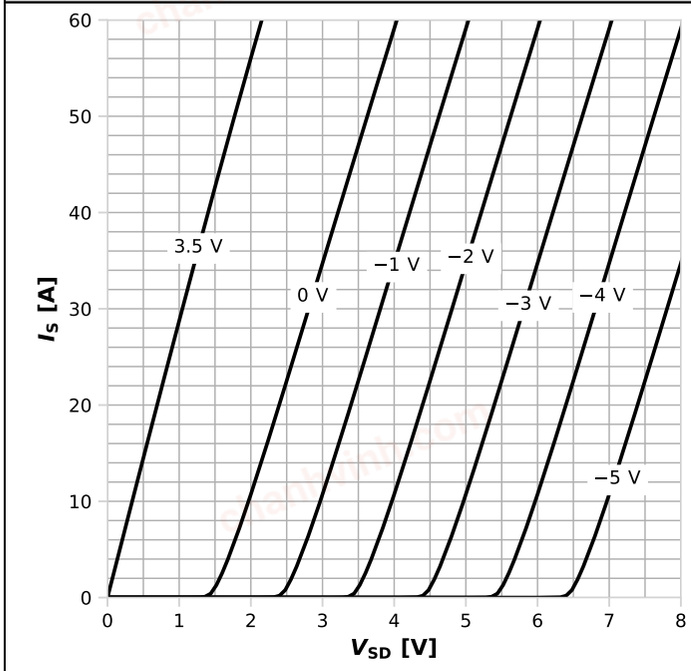
I_D=f(I_{GS}); V_{DS}=8V; parameter: T_j

Diagram 14: Typ. transfer gate current characteristic



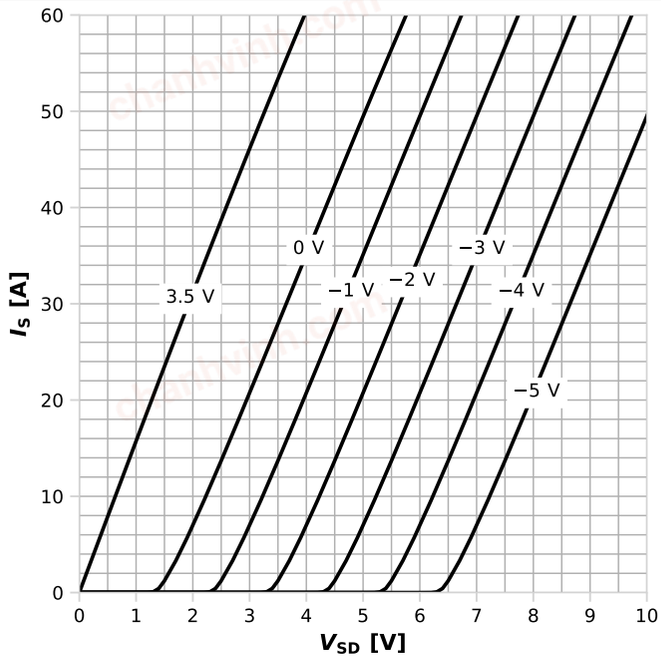
I_G=f(V_{GS}); V_{DS}=8V; parameter: T_j

Diagram 15: Typ. channel reverse characteristics



I_S=f(V_{SD}); T_j=25°C; parameter: V_{GS}

Diagram 16: Typ. channel reverse characteristics



I_S=f(V_{SD}); T_j=125°C; parameter: V_{GS}

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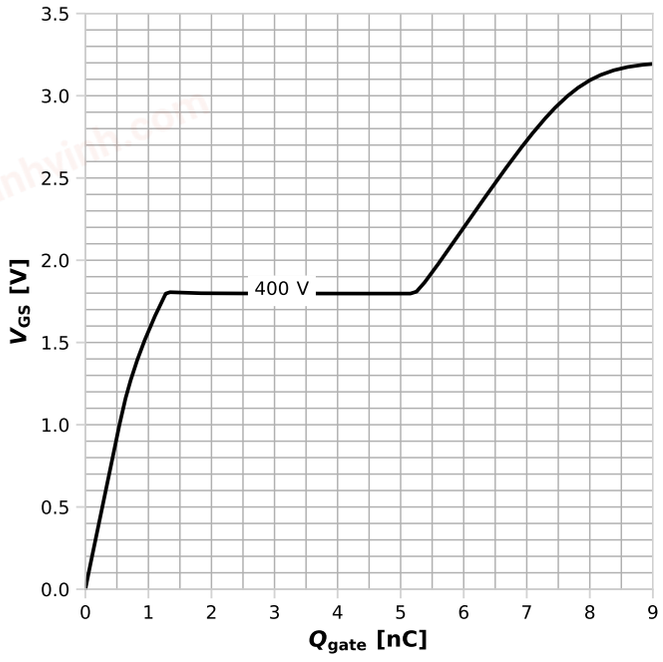
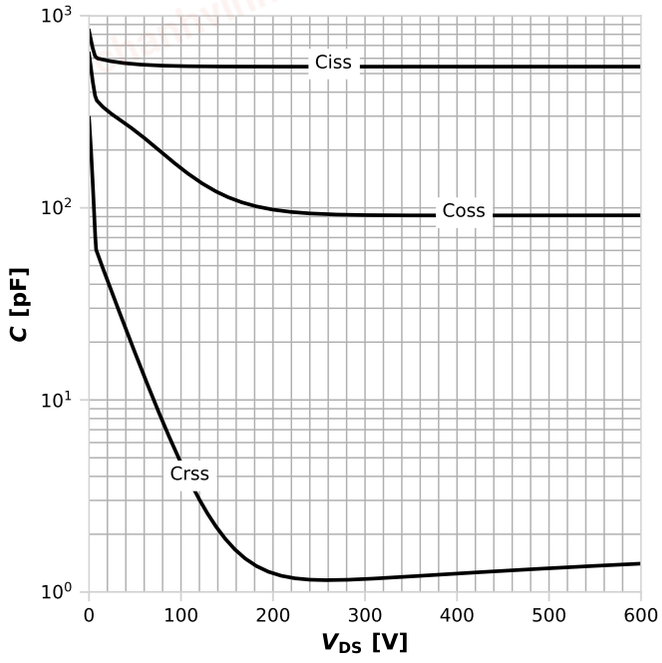
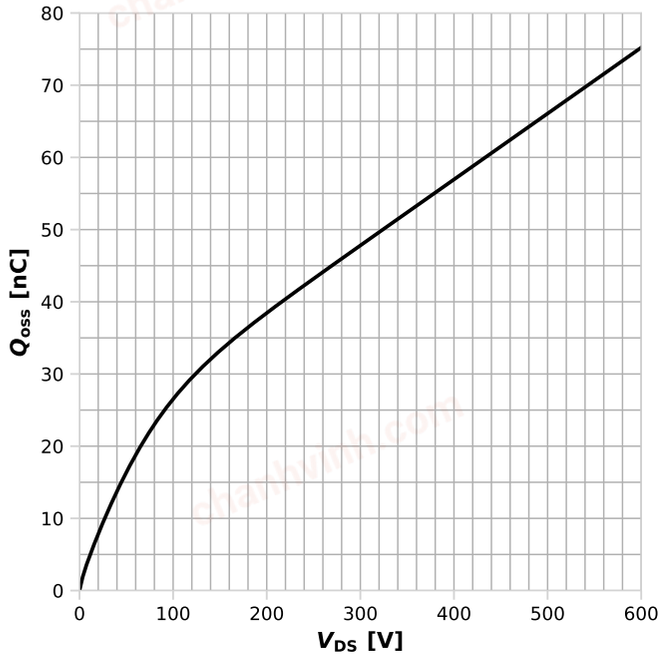
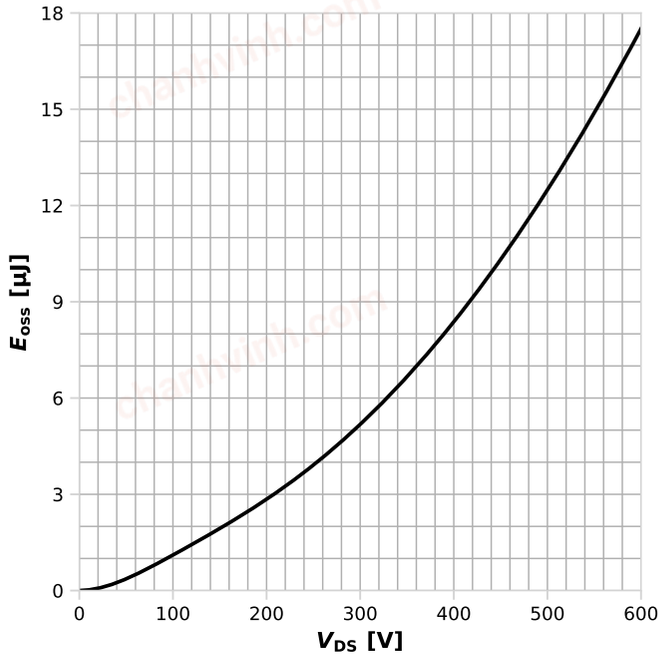
Diagram 17 Typ. gate charge	Diagram 18: Typ. capacitances
	
V_{GS}=f(Q_{gate}); I_D=13 A pulsed; I_G=4.5 mA; parameter: V_{DD}	C=f(V_{DS}); V_{GS}=0 V

Diagram 19: Typ. output charge	Diagram 20: Typ. Coss stored energy
	
Q_{oss}=f(V_{DS})	E_{oss}=f(V_{DS})

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5 Test circuits

Table 8 Reverse channel characteristics test

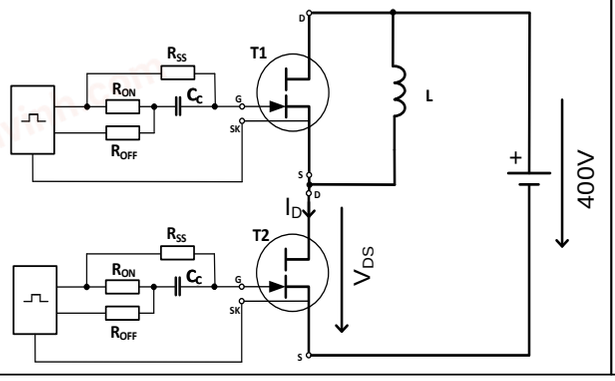
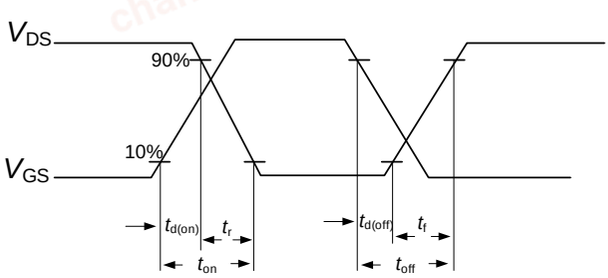
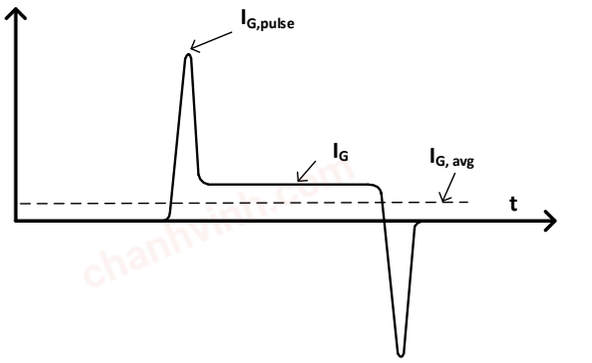
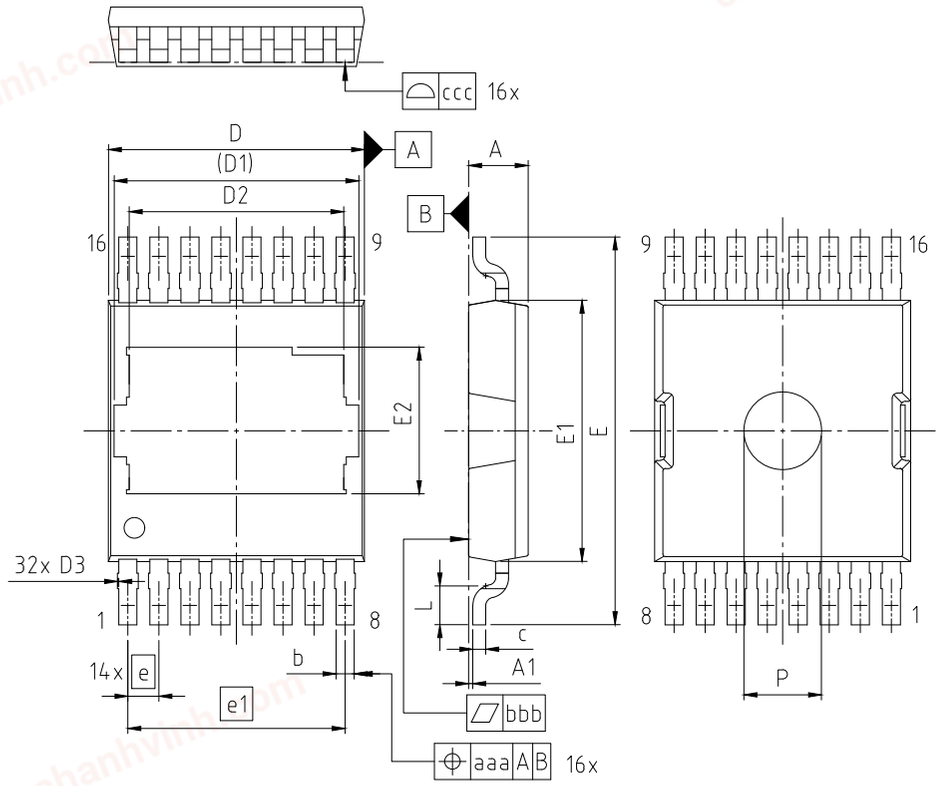
Switching times with inductive load	Switching times waveform
	

Table 9 Gate current switching waveform

Gate current switching waveform


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6 Package outlines



PACKAGE - GROUP NUMBER:	PG-HDSOP-16-U04				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	2.25	2.35	e	1.20	
A1	0.01	0.16	e1	8.40	
b	0.60	0.80	L	1.40	1.60
c	0.40	0.60	P	2.90	3.10
D	9.70	10.10	aaa	0.25	
D1	9.46		bbb	0.02	
D2	8.20	8.40	ccc	0.10	
D3	---	0.15			
E	14.80	15.20			
E1	10.00	10.30			
E2	5.57	5.77			

NOTES:
ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

Figure 1 Outline PG-HDSOP-16, dimensions in mm

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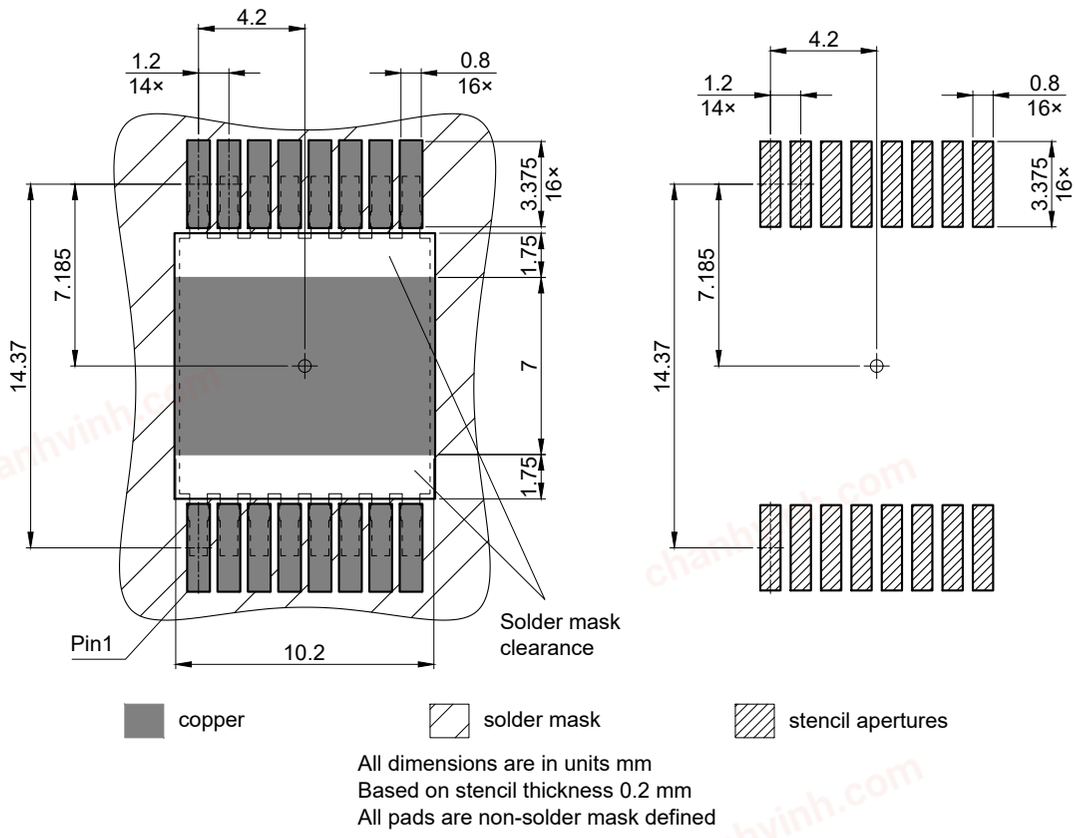
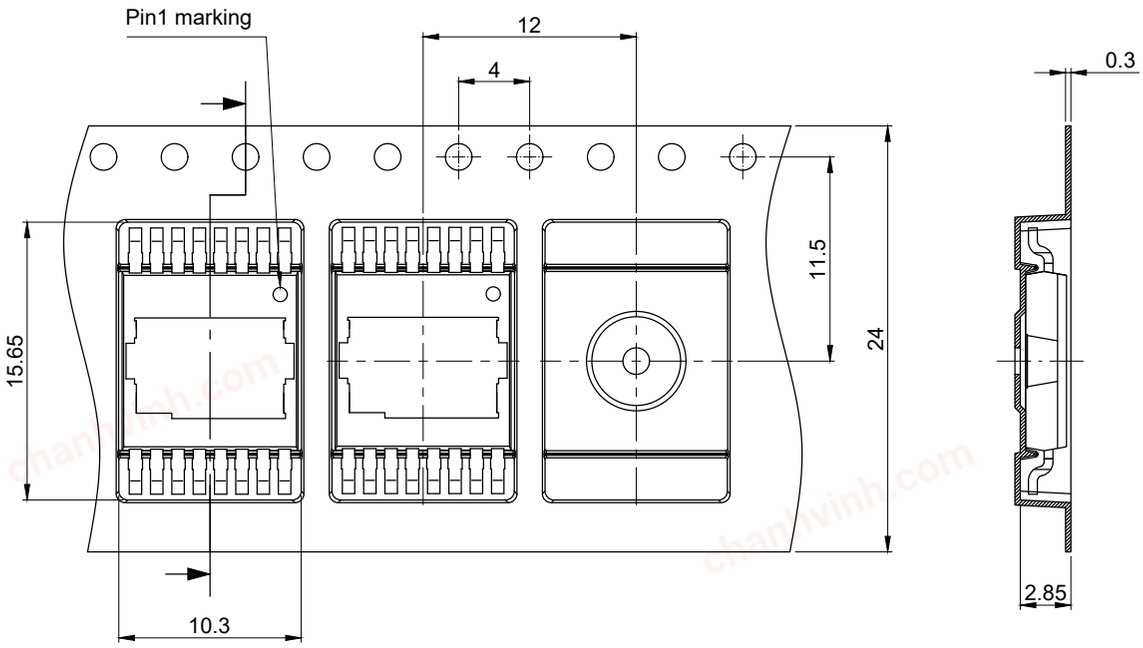


Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm

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All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 Packaging variant PG-HDSOP-16, dimensions in mm

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7 Appendix A

Table 10 Related links

- CoolGaN™ GaN 650 V webpage
- CoolGaN™ GaN 650 V reliability white paper
- CoolGaN™ GaN 650 V gate driver application note
- CoolGaN™ GaN 650 V applications information

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Revision history

IGLT65R035D2

Revision 2024-10-29, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-10-29	Release of final

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