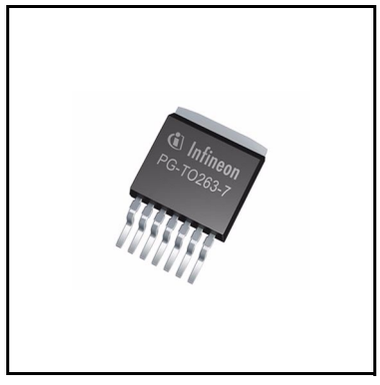
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High Current PN Half Bridge with Integrated Driver

IFX007T
Industrial & Multi Purpose NovalithIC™



1 Overview

Quality Requirement Category: Industrial

Features

- Path resistance of max. 12.8 mΩ @ 25°C (typ. 10.0 mΩ @ 25°C)
  High side: max. 6.5 mΩ @ 25°C (typ. 5.3 mΩ @ 25°C)
  Low side: max. 6.3 mΩ @ 25°C (typ. 4.7 mΩ @ 25°C)
- Enhanced switching speed for reduced switching losses
- Capable for high PWM frequency combined with active freewheeling
- Switched mode current limitation for reduced power dissipation in overcurrent
- Current limitation level of 55 A min.
- Status flag diagnosis with current sense capability
- Overtemperature shutdown with latch behavior
- Undervoltage shutdown
- Driver circuit with logic level inputs
- Adjustable slew rates for optimized EMI
- Operation up to 40 V
- Green Product (RoHS compliant)
- JESD47I Qualified

Description

The IFX007T is an integrated high current half bridge for motor drive applications. It is part of the Industrial & Multi Purpose NovalithIC™ family containing one p-channel high-side MOSFET and one n-channel low-side MOSFET with an integrated driver IC in one package. Due to the p-channel high-side switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, undervoltage, overcurrent and short circuit.

The IFX007T provides a cost optimized solution for protected high current PWM motor drives with very low board space consumption.

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Overview

Type	Package	Marking
IFX007T	PG-TO263-7-1	IFX007T

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2 Block diagram

The IFX007T is part of the Industrial & Multi Purpose NovalithIC™ family containing three separate chips in one package: One p-channel high-side MOSFET and one n-channel low-side MOSFET together with a driver IC, forming an integrated high current half-bridge. All three chips are mounted on one common lead frame, using the chip-on chip and chip-by-chip technology. The power switches utilize vertical MOS technologies to ensure optimum on state resistance. Due to the p-channel high-side switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, undervoltage, overcurrent and short circuit. The IFX007T can be combined with other IFX007Ts to form a H-bridge or a3-phase drive configuration.

2.1 Block diagram

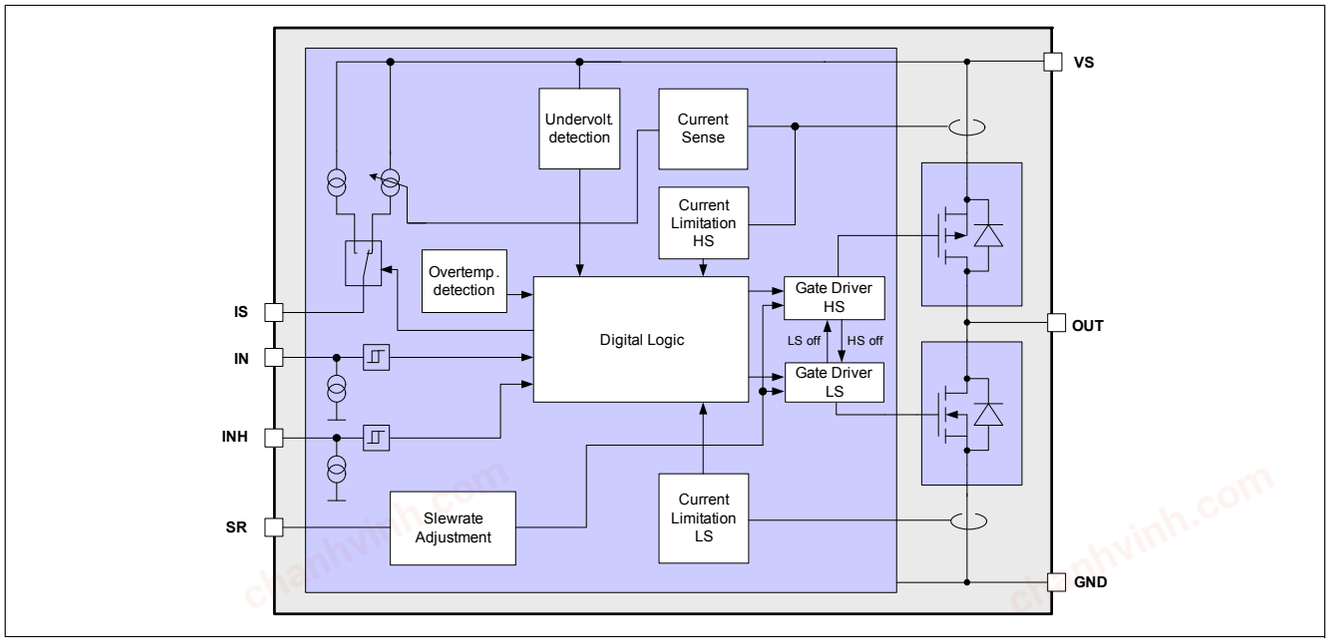


Figure 1 Block diagram

2.2 Terms

Following figure shows the terms used in this data sheet.

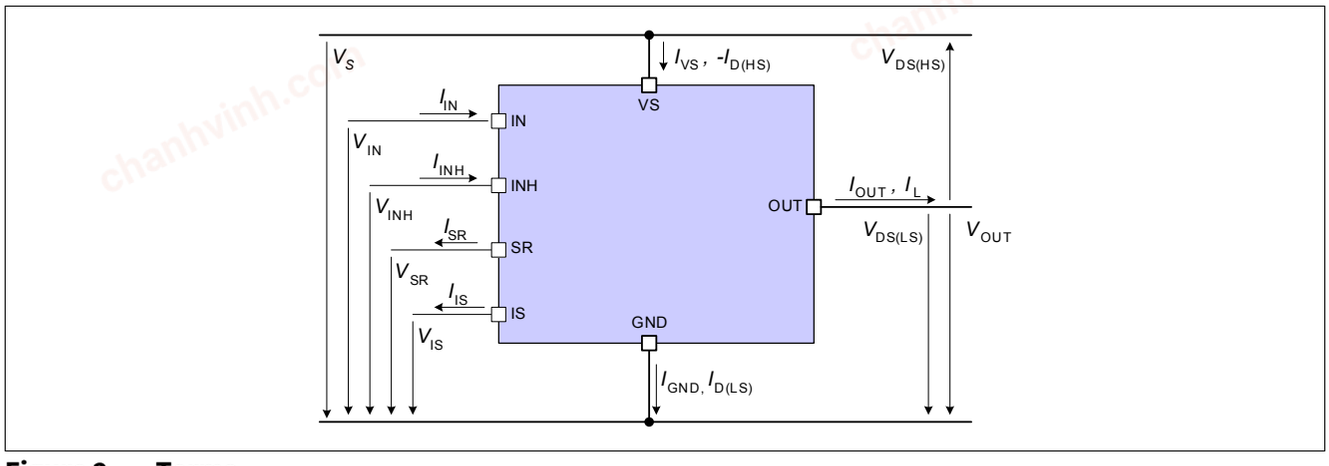


Figure 2 Terms

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3 Pin configuration

3.1 Pin assignment

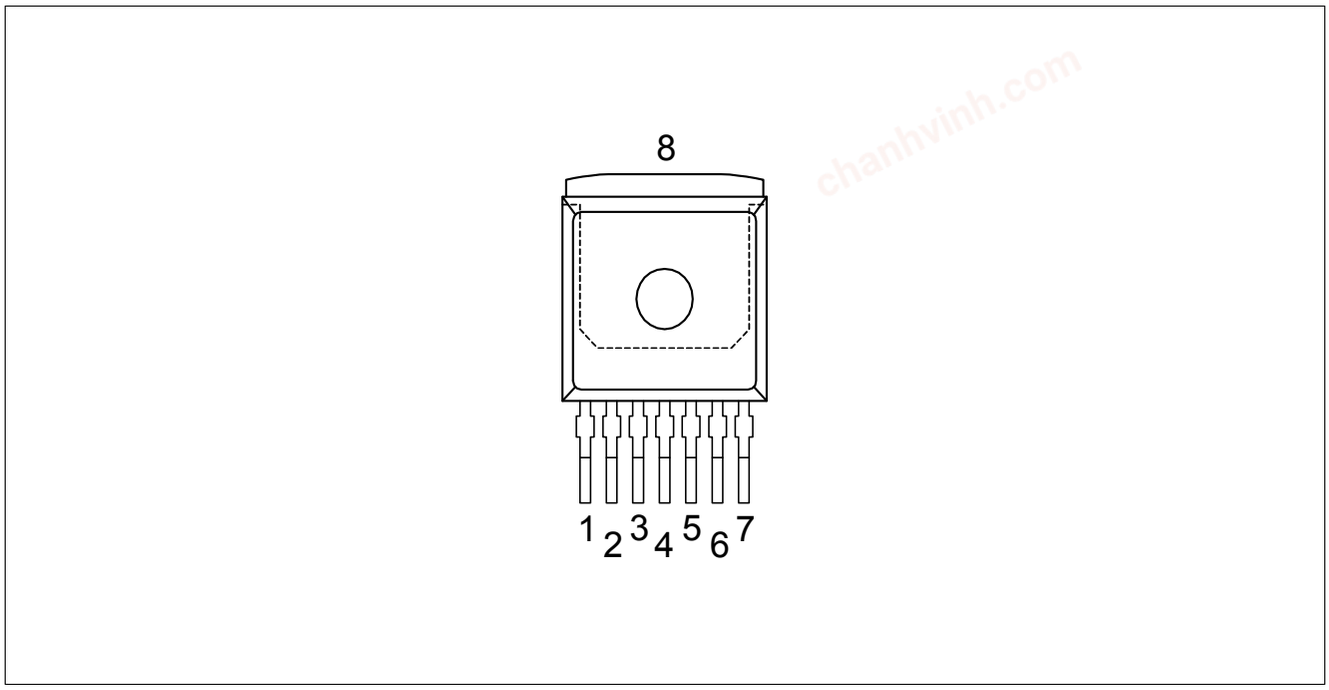


Figure 3 Pin assignment IFX007T (top view)

3.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	I/O	Function
1	**GND**	**–**	**Ground**
2	IN	I	Input Defines whether high - or low-side switch is activated
3	INH	I	Inhibit When set to low device goes in sleep mode
4,8	**OUT**	**O**	**Power output of the bridge**
5	SR	I	Slew Rate The slew rate of the power switches can be adjusted by connecting a resistor between SR and GND
6	IS	O	Current Sense and Diagnostics
7	**VS**	**–**	**Supply**

Bold type: pin needs power wiring

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4 General product characteristics

The device is intended to be used in an industrial or consumer environment. The circumstances, how the device environment must look like are described in this chapter.

4.1 Absolute maximum ratings

Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 Absolute maximum ratings[1)]

T_j = 25 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	–	P_4.1.1
Drain-source voltage high side	$V_{DS(HS)}$	-40	–	–	V	$T_j \geq 25°C$	P_4.1.2
		-38	–	–	V	$T_j < 25°C$	
Drain-source voltage low side	$V_{DS(LS)}$	–	–	40	V	$T_j \geq 25°C$	P_4.1.3
		–	–	38	V	$T_j < 25°C$	
Logic input voltage	V_{IN} V_{INH}	-0.3	–	5.3	V	–	P_4.1.4
Voltage at SR pin	V_{SR}	-0.3	–	1.0	V	–	P_4.1.5
Voltage between VS and IS pin	V_S -V_{IS}	-0.3	–	40	V	–	P_4.1.6
Voltage at IS pin	V_{IS}	-20	–	40	V	–	P_4.1.7
Voltage transient between VS and GND pin[2)]	dV_S	-1	–	1	V	Transient fall/rise time: t_{trans} > 85 ns.	P_4.1.8
Currents							
HS/LS continuous drain current	$I_{D(HS)}$ $I_{D(LS)}$	-50	–	50	A	switch active	P_4.1.9
HS/LS pulsed drain current[3)]	$I_{D(HS)}$ $I_{D(LS)}$	-117	–	117	A	t_{pulse} = 10 ms single pulse	P_4.1.10
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.11
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.12
ESD susceptibility							
ESD resistivity HBM IN, INH, SR, IS OUT, GND, VS	V_{ESD}	 -2 -6	 – –	 2 6	kV	HBM[4)]	P_4.1.13

1) Not subject to production test, specified by design.
2) “Under Voltage Shut Down” shall not be triggered.
3) Maximum reachable current may be smaller depending on current limitation level.
4) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).

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Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional range

The parameters of the functional range are listed in the following table:

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(nor)}$	8	–	40	V	$T_j \geq 25°C$	P_4.2.1
		8	–	38	V	$T_j < 25°C$	
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.2

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal resistance

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance Junction-case, high-side switch $R_{thjc(HS)} = \Delta T_{j(HS)} / P_{v(HS)}$	$R_{thJC(HS)}$	–	0.55	0.8	K/W	1)	P_4.3.1
Thermal resistance Junction-case, low-side switch $R_{thjc(LS)} = \Delta T_{j(LS)} / P_{v(LS)}$	$R_{thJC(LS)}$	–	1.1	1.6	K/W	1)	P_4.3.2
Thermal resistance Junction-ambient	R_{thJA}	–	19	–	K/W	1) 2)	P_4.3.3

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

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5 Block description and characteristics

5.1 Supply characteristics

Table 5 Supply characteristics

V_S = 24 V, T_j = 25 °C, I_L = 0 A,
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
General							
Supply current	$I_{VS(on)}$	–	2.3	2.8	mA	V_{INH} = 5 V V_{IN} = 0 V or 5 V R_{SR} = 0 Ω DC-mode normal operation (no fault condition)	P_5.1.1
Quiescent current	$I_{VS(off)}$	–	7	10	µA	V_{INH} = 0 V V_{IN} = 0 V or 5 V [1]	P_5.1.2

1) Not subject to production test, specified by design.

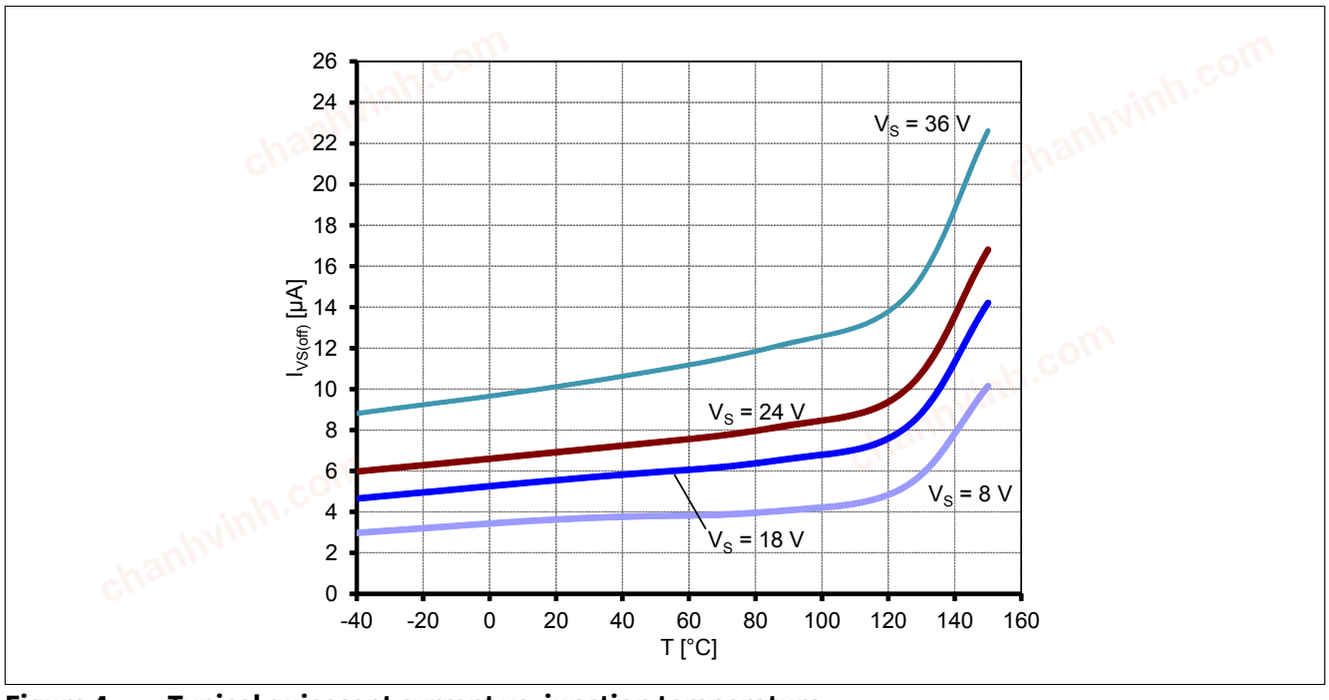


Figure 4 Typical quiescent current vs. junction temperature

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5.2 Power stages

The power stages of the IFX007T consist of a p-channel vertical DMOS transistor for the high-side switch and an n-channel vertical DMOS transistor for the low-side switch. All protection and diagnostic functions are located in a separate top chip. Both switches allow active freewheeling and thus minimizing power dissipation during PWM control.

The on state resistance R_{ON} is dependent on the supply voltage V_S as well as on the junction temperature T_j. The typical on state resistance characteristics are shown in **Figure 5** and **Figure 6**.

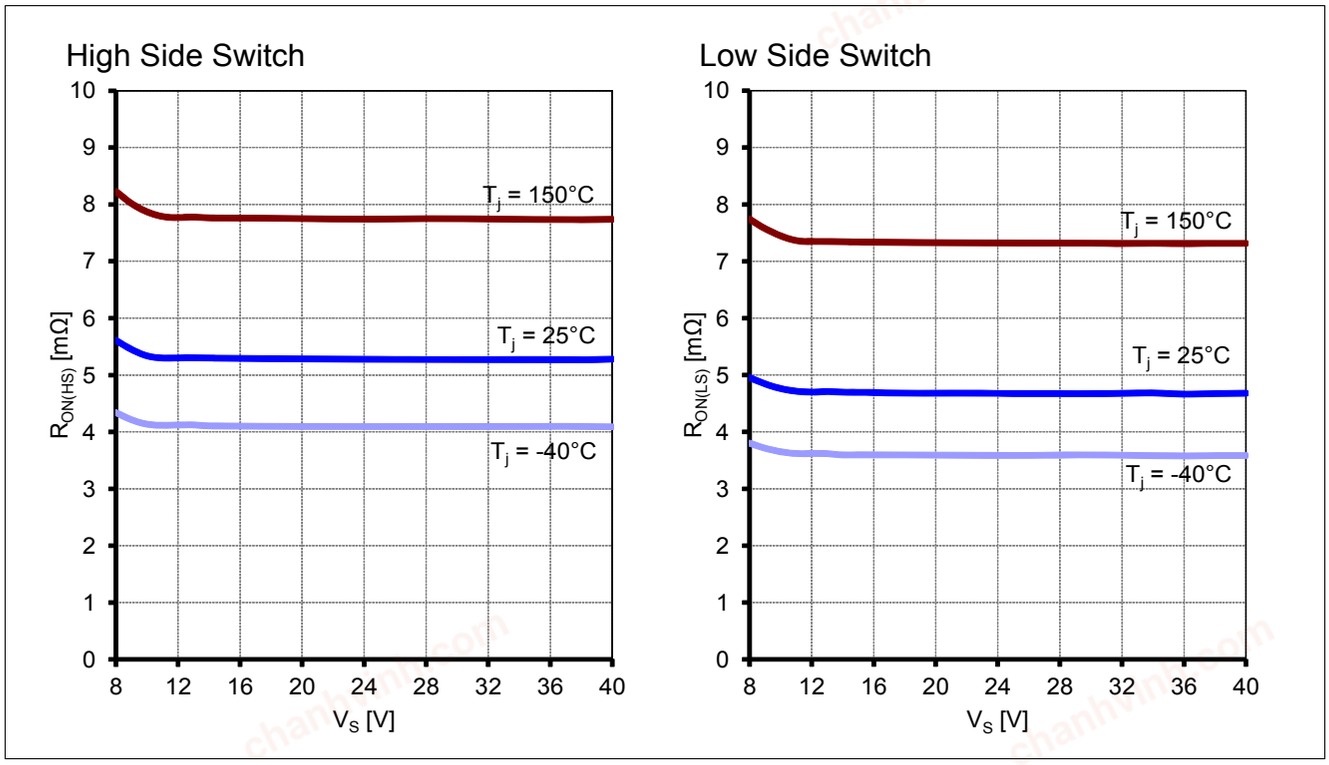


Figure 5 Typical ON-state resistance vs. supply voltage

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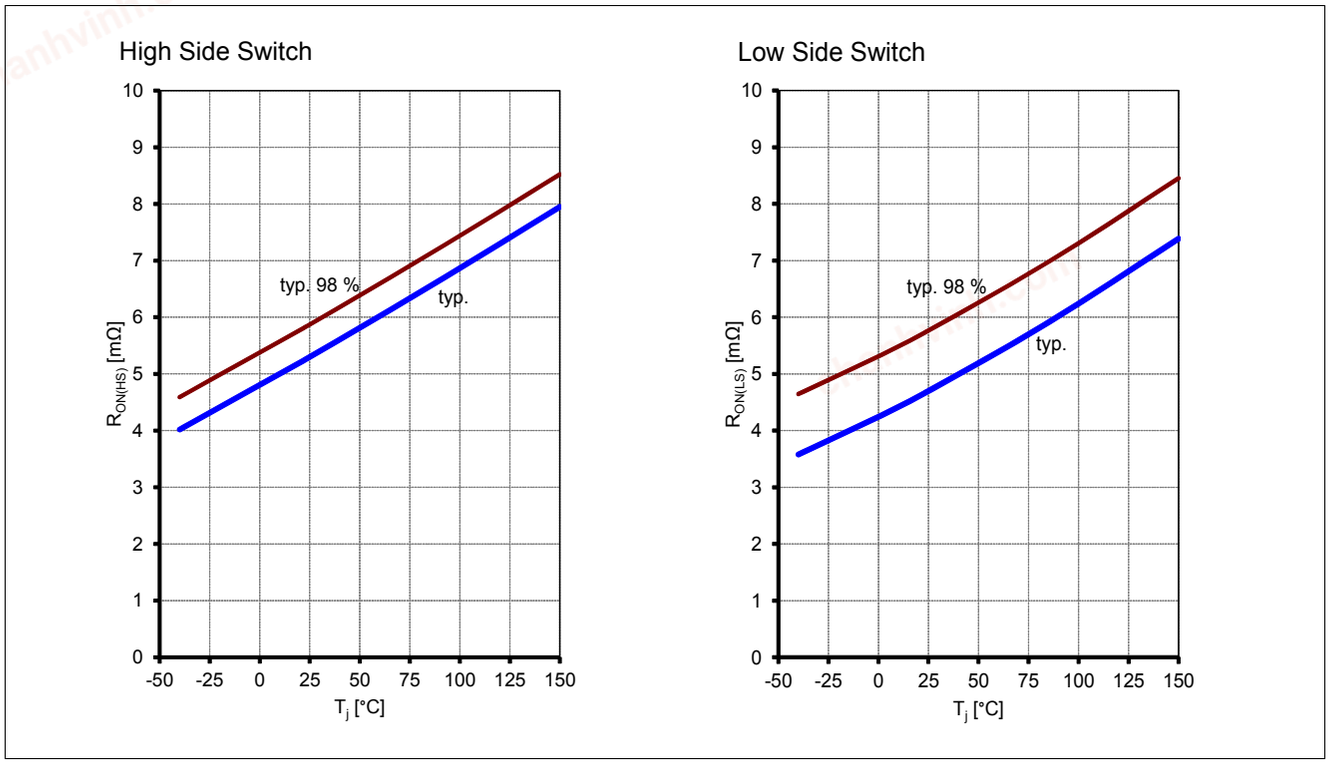


Figure 6 Typical ON-state resistance vs. junction temperature; V_S = 13.5 V; I_D = 9 A

5.2.1 Power stages - static characteristics

Table 6 Power stages - static characteristics

V_S = 24 V, T_j = 25 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High-side switch - static characteristics							
ON state high-side resistance	$R_{ON(HS)}$	–	5.3	6.5	mΩ	I_{OUT} = 9 A; V_S = 13.5 V	P_5.2.1
Leakage current high side	$I_{L(LKHS)}$	–	–	1	µA	V_{INH} = 0 V; V_{OUT} = 0 V	P_5.2.2
Reverse diode forward-voltage high side[1)]	$V_{DS(HS)}$	–	0.8	0.9	V	I_{OUT} = -9 A	P_5.2.3
Low-side switch - static characteristics							
ON-state low-side resistance	$R_{ON(LS)}$	–	4.7	6.3	mΩ	I_{OUT} = -9 A; V_S = 13.5 V	P_5.2.4
Leakage current low side	$I_{L(LKLS)}$	–	–	1	µA	V_{INH} = 0 V; V_{OUT} = V_S	P_5.2.5
Reverse diode forward-voltage low side	$-V_{DS(LS)}$	–	0.8	0.9	V	I_{OUT} = 9 A	P_5.2.6

1) Due to active freewheeling, diode is conducting only for a few µs, depending on R_{SR}.

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5.2.2 Switching times

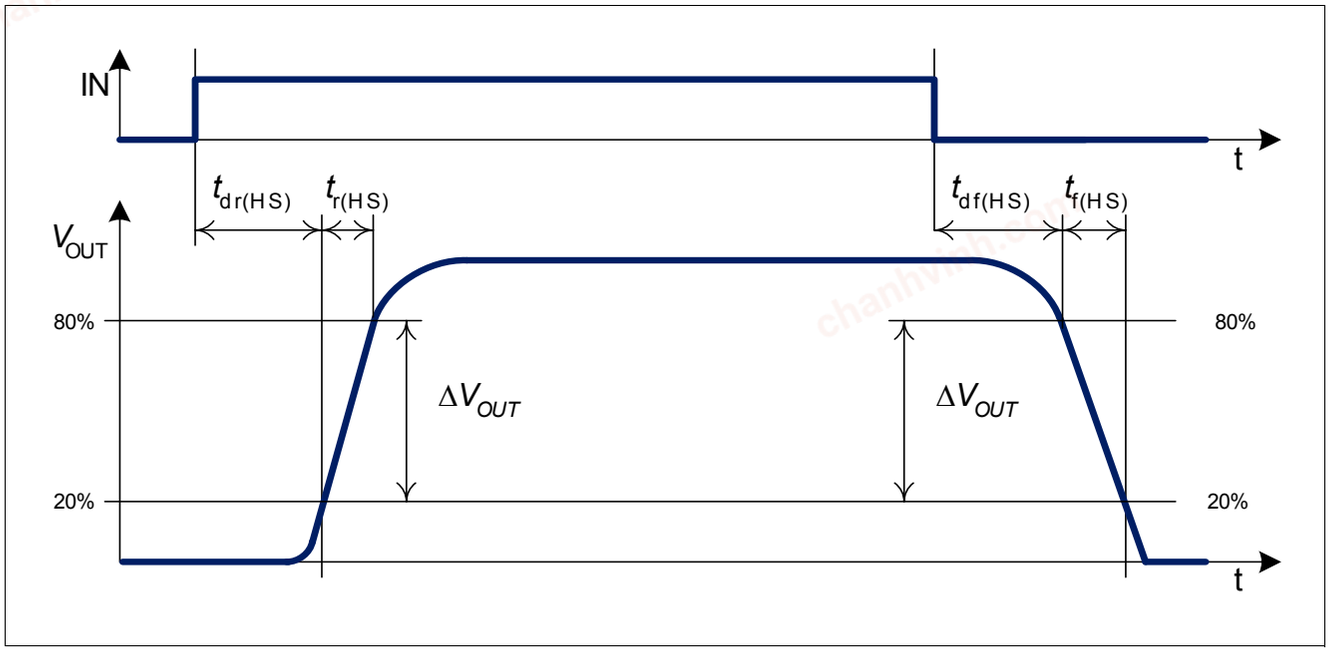


Figure 7 Definition of switching times high side (R_{load} to GND)

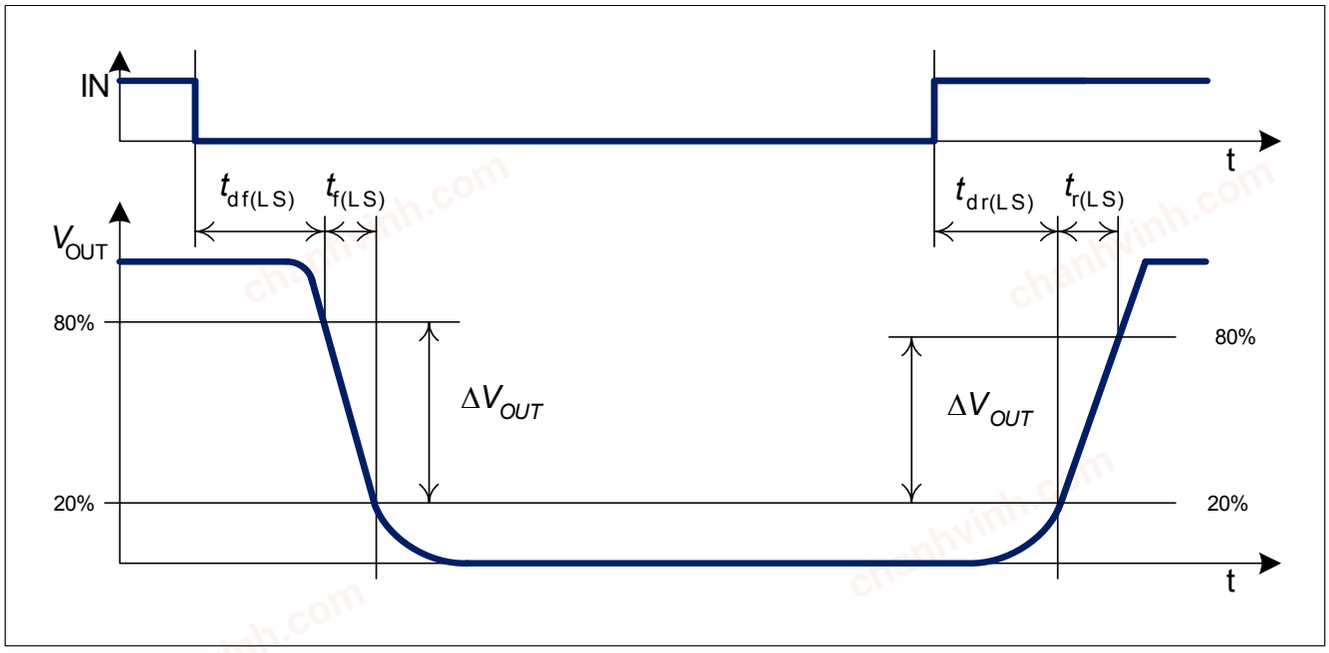


Figure 8 Definition of switching times low side (R_{load} to V_S)

Due to the timing differences for the rising and the falling edge there will be a slight difference between the length of the input pulse and the length of the output pulse. It can be calculated using the following formulas:

- $\Delta t_{HS} = (t_{dr(HS)} + 0.5\ t_{r(HS)}) - (t_{df(HS)} + 0.5\ t_{f(HS)})$
- $\Delta t_{LS} = (t_{df(LS)} + 0.5\ t_{f(LS)}) - (t_{dr(LS)} + 0.5\ t_{r(LS)})$.

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5.2.3 Power stages - dynamic characteristics

The slew rate resistor at the SR-pin shall not exceed the max. slew rate resistor value of $R_{SR} \leq 51\ k\Omega$.

Table 7 Power stages - dynamic characteristics

V_S = 24 V, T_j = 25 °C, R_{load} = 4 Ω, single pulse,
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High-side switch dynamic characteristics							
Rise-time of HS	$t_{r(HS)}$	0.05 0.22	0.25 1.3	0.75 4.7	µs	R_{SR} = 0 Ω R_{SR} = 51 kΩ	P_5.2.7
Switch-ON delay time HS	$t_{dr(HS)}$	1.5 2	3.4 15	4.6 31	µs	R_{SR} = 0 Ω R_{SR} = 51 kΩ	P_5.2.8
Fall-time of HS	$t_{f(HS)}$	0.05 0.22	0.25 1.3	0.7 4.5	µs	R_{SR} = 0 Ω R_{SR} = 51 kΩ	P_5.2.9
Switch-OFF delay time HS	$t_{df(HS)}$	0.8 1.1	2.4 9	4.1 21	µs	R_{SR} = 0 Ω R_{SR} = 51 kΩ	P_5.2.10
Low-side switch dynamic characteristics							
Rise-time of LS	$t_{r(LS)}$	0.05 0.22	0.25 1.3	0.7 4.5	µs	R_{SR} = 0 Ω R_{SR} = 51 kΩ	P_5.2.11
Switch-OFF delay time LS	$t_{dr(LS)}$	0.2 1	1.5 7	2.5 16	µs	R_{SR} = 0 Ω R_{SR} = 51 kΩ	P_5.2.12
Fall-time of LS	$t_{f(LS)}$	0.025 0.18	0.25 1.3	0.7 4.5	µs	R_{SR} = 0 Ω R_{SR} = 51 kΩ	P_5.2.13
Switch-ON delay time LS	$t_{df(LS)}$	1.6 2.0	4.2 16	5.9 36	µs	R_{SR} = 0 Ω R_{SR} = 51 kΩ	P_5.2.14

5.3 Protection functions

The device provides integrated protection functions. These are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not to be used for continuous or repetitive operation, with the exception of the current limitation (**Chapter 5.3.3**). In case of overtemperature the IFX007T will apply the slew rate determined by the connected slew rate resistor. In current limitation mode the highest slew rate possible will be applied independent of the connected slew rate resistor. Overtemperature and overcurrent are indicated by a fault current $I_{IS(LIM)}$ at the IS pin as described in the paragraph **“Status flag diagnosis with current sense capability” on Page 16** and **Figure 12**.

5.3.1 Undervoltage shutdown

To avoid uncontrolled motion of the driven motor at low voltages the device shuts off (output is tri-state), if the supply voltage drops below the switch-off voltage $V_{UV(OFF)}$. The IC becomes active again with a hysteresis $V_{UV(HY)}$ if the supply voltage rises above the switch-on voltage $V_{UV(ON)}$.

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5.3.2 Overtemperature protection

The IFX007T is protected against overtemperature by an integrated temperature sensor. Overtemperature leads to a shutdown of both output stages. This state is latched until the device is reset by a low signal with a minimum length of t_{reset} at the INH pin, provided that its temperature has decreased at least the thermal hysteresis ΔT in the meantime.

Repetitive use of the overtemperature protection impacts lifetime.

5.3.3 Current limitation

The current in the bridge is measured in both switches. As soon as the current in forward direction in one switch (high side or low side) is reaching the limit I_{CLx}, this switch is deactivated and the other switch is activated for t_{CLS}. During that time all changes at the IN pin are ignored. However, the INH pin can still be used to switch both MOSFETs off. After t_{CLS} the switches return to their initial setting. The error signal at the IS pin is reset after 2 * t_{CLS}. Unintentional triggering of the current limitation by short current spikes (e.g. inflicted by EMI coming from the motor) is suppressed by internal filter circuitry. Due to thresholds and reaction delay times of the filter circuitry the effective current limitation level I_{CLx} depends on the slew rate of the load current *dI/dt* as shown in **Figure 10**.

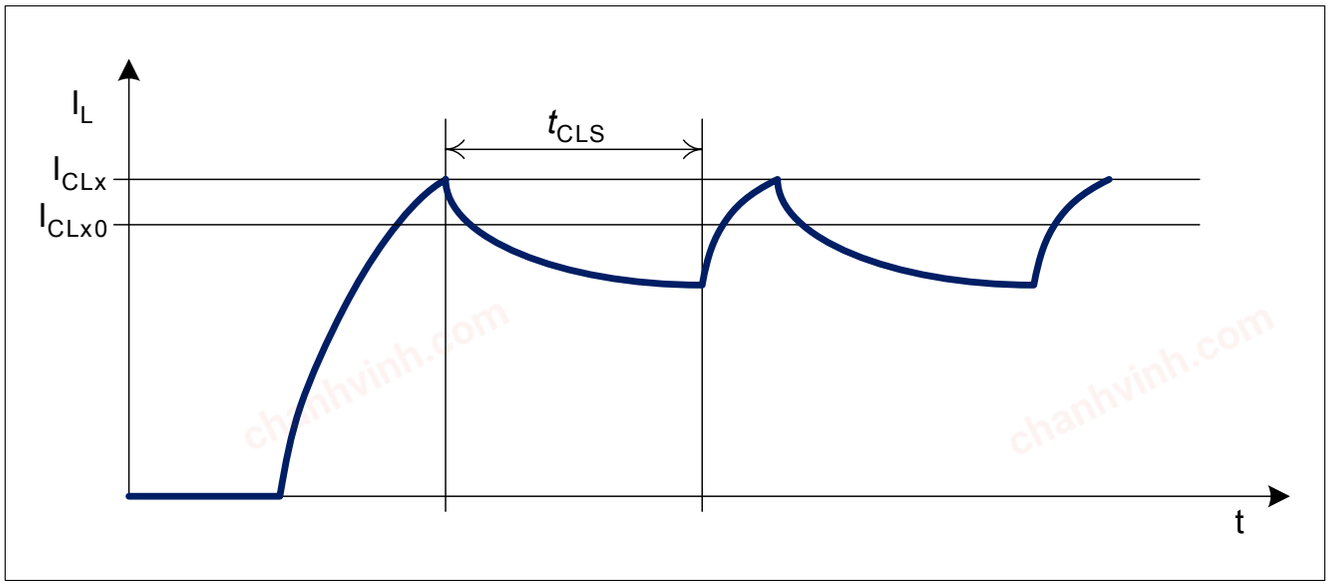


Figure 9 Timing diagram current limitation (inductive load)

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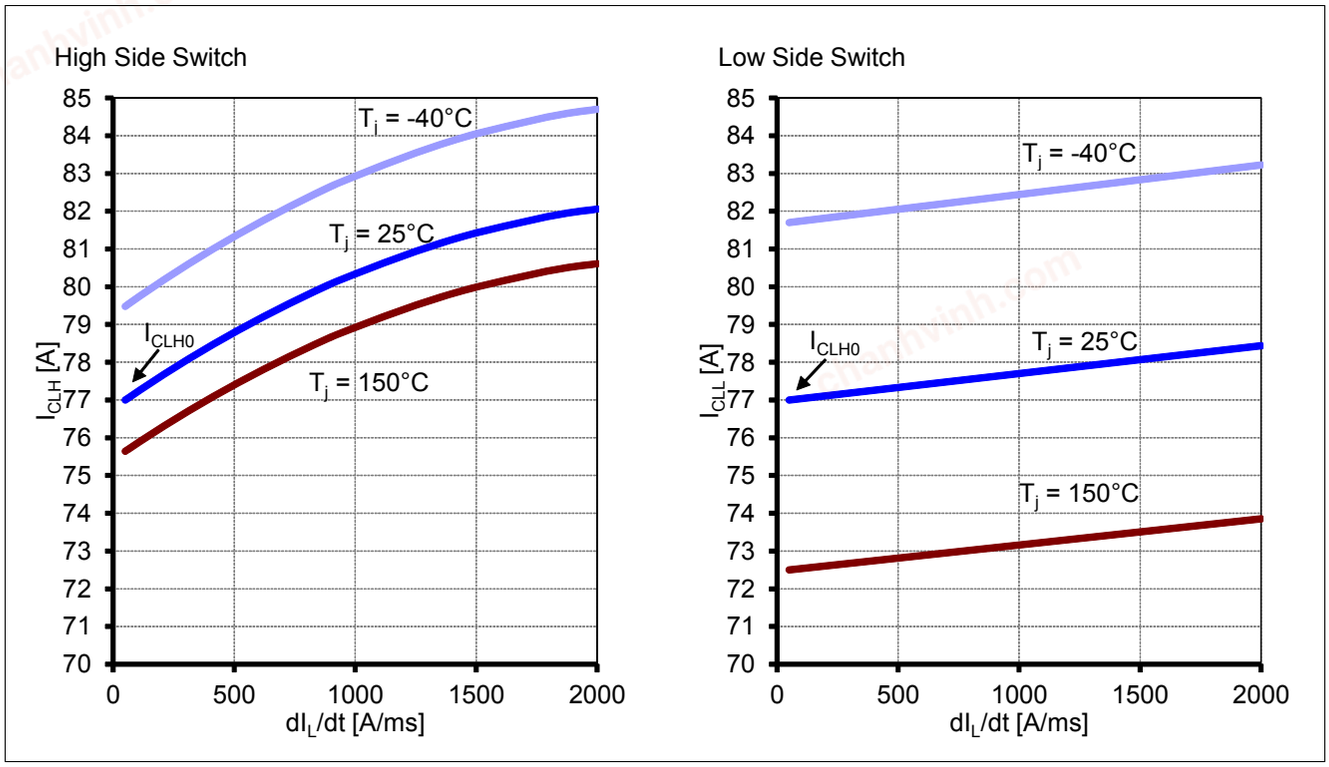


Figure 10 Typical current limitation detection level vs. current slew rate dI_L/dt

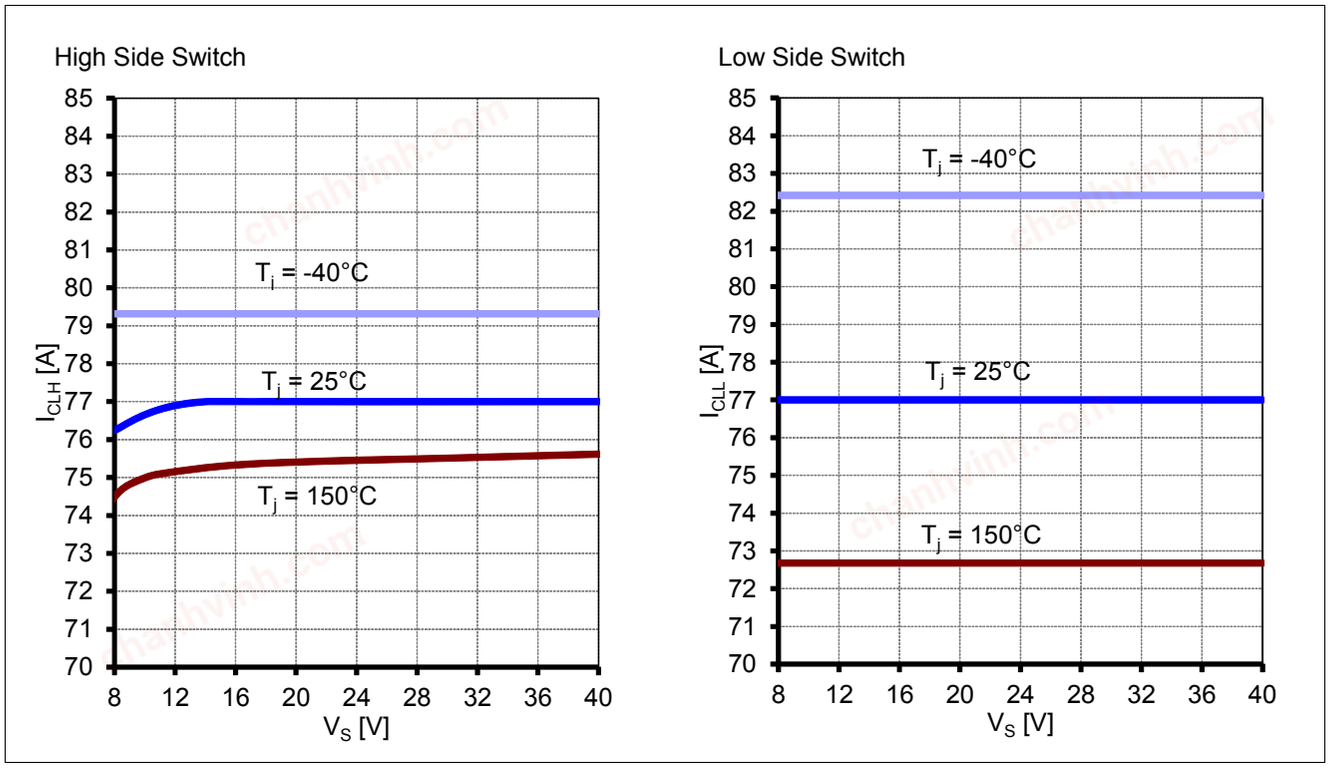


Figure 11 Typical current limitation detection levels vs. supply voltage

In combination with a typical inductive load, such as a motor, this results in a switched mode current limitation. This method of limiting the current has the advantage of greatly reduced power dissipation in the IFX007T compared to driving the MOSFET in linear mode. Therefore it is possible to use the current limitation

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for a short time without exceeding the maximum allowed junction temperature (e.g. for limiting the inrush current during motor start up). However, the regular use of the current limitation is allowed as long as the specified maximum junction temperature is not exceeded. Exceeding this temperature can reduce the lifetime of the device.

5.3.4 Short circuit protection

The device provides embedded protection functions against

- output short circuit to ground
- output short circuit to supply voltage
- short circuit of load

The short circuit protection is realized by the previously described current limitation in combination with the overtemperature shutdown of the device.

5.3.5 Electrical characteristics - protection functions

Table 8 Electrical characteristics - protection functions

V_S = 24 V, T_j = 25 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Undervoltage shutdown							
Switch-ON voltage	$V_{UV(ON)}$	–	–	5.0	V	V_S increasing	P_5.3.1
Switch-OFF voltage[1)]	$V_{UV(OFF)}$	3.3	–	4.7	V	V_S decreasing, INH = 1	P_5.3.2
ON/OFF hysteresis	$V_{UV(HY)}$	–	0.3	–	V	[2)]	P_5.3.3
Current limitation							
Current limitation detection level HS/LS	I_{CLH0} I_{CLL0}	55	77	98	A	V_S = 13.5 V	P_5.3.4
Current limitation timing							
Shut OFF time for HS and LS	t_{CLS}	70	115	210	µs	[2)]	P_5.3.5
Thermal shutdown							
Thermal shutdown junction temperature	T_{jSD}	155	175	200	°C	–	P_5.3.6
Thermal switch-ON junction temperature	T_{jSO}	150	–	190	°C	–	P_5.3.7
Thermal hysteresis	DT	–	7	–	K	[2)]	P_5.3.8
Reset pulse at INH Pin (INH low)	t_{reset}	4	–	–	µs	[2)]	P_5.3.9

1) With decreasing V_s < 5.5 V activation of the current limitation mode may occur before undervoltage shutdown.
2) Not subject to production test, specified by design.

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5.4 Control and diagnostics

5.4.1 Input circuit

The control inputs IN and INH consist of TTL/CMOS compatible schmitt triggers with hysteresis which control the integrated gate drivers for the MOSFETs. Setting the INH pin to high enables the device. In this condition one of the two power switches is switched on depending on the status of the IN pin. To deactivate both switches, the INH pin has to be set to low. No external driver is needed. The IFX007T can be interfaced directly to a microcontroller, as long as the maximum ratings in **Chapter 4.1** are not exceeded.

5.4.2 Dead time generation

In bridge applications it has to be assured that the high-side and low-side MOSFET are not conducting at the same time, connecting directly the battery voltage to GND. This is assured by a circuit in the driver IC, generating a so called dead time between switching off one MOSFET and switching on the other. The dead time generated in the driver IC is automatically adjusted to the selected slew rate.

5.4.3 Adjustable slew rate

In order to optimize electromagnetic emission, the switching speed of the MOSFETs is adjustable by an external resistor. The slew rate pin SR allows the user to optimize the balance between emission and power dissipation within his own application by connecting an external resistor R_{SR} to GND.

5.4.4 Status flag diagnosis with current sense capability

The sense pin IS is used as a combined current sense and error flag output.

In normal operation (current sense mode), a current source is connected to the status pin, which delivers a current proportional to the forward load current flowing through the active high-side switch. The sense current can be calculated out of the load current by the following equation:

$$I_{IS} = \frac{1}{dk_{ILIS}} \cdot I_L + I_{IS(offset)} \quad (5.1)$$

The other way around, the load current can be calculated out of the sense current by following equation:

$$I_L = dk_{ILIS} \cdot (I_{IS} - I_{IS(offset)}) \quad (5.2)$$

The differential current sense ratio dk_{ilis} is defined by:

$$dk_{ILIS} = \frac{I_{L2} - I_{L1}}{I_{IS}(I_{L2}) - I_{IS}(I_{L1})} \quad (5.3)$$

If the high side drain current is zero ($I_{SD(HS)}$ = 0A) the offset current $I_{IS} = I_{IS(offset)}$ still will be driven.

The external resistor R_{IS} determines the voltage per IS output current. The voltage can be calculated by $V_{IS} = R_{IS} \cdot I_{IS}$.

In case of a fault condition the status output is connected to a current source which is independent of the load current and provides $I_{IS(lim)}$. The maximum voltage at the IS pin is determined by the choice of the external resistor and the supply voltage. In case of current limitation the $I_{IS(lim)}$ is activated for 2 * t_{CLS}.

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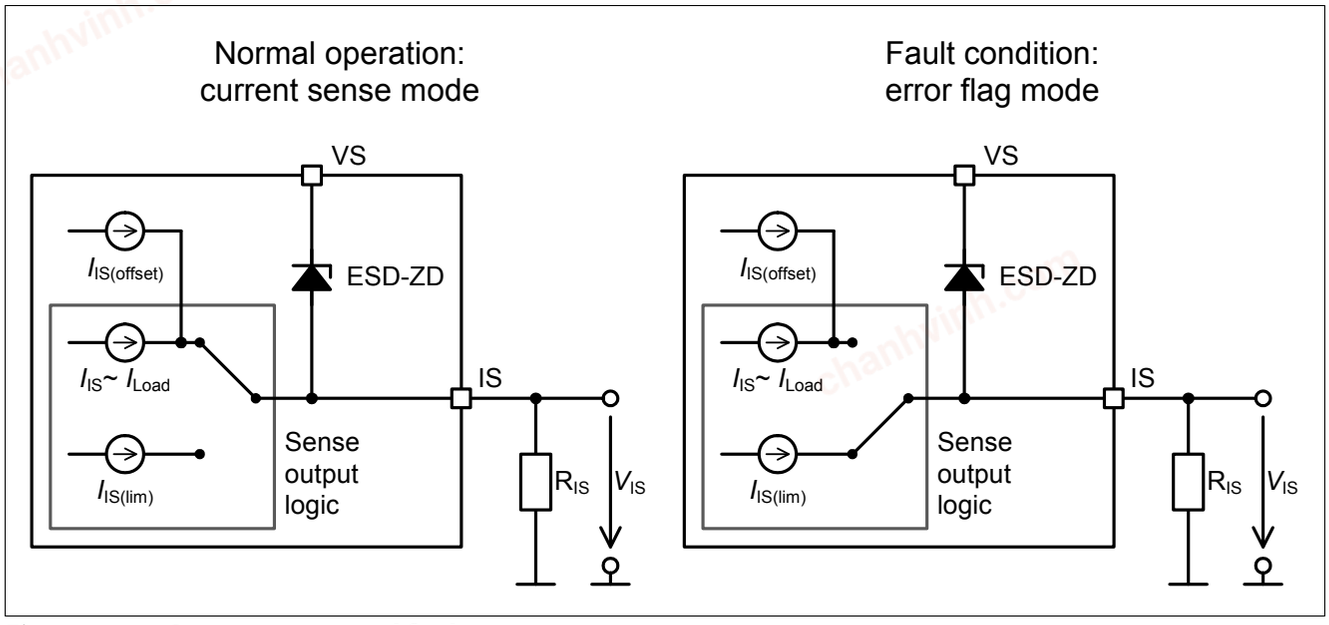


Figure 12 Sense current and fault current

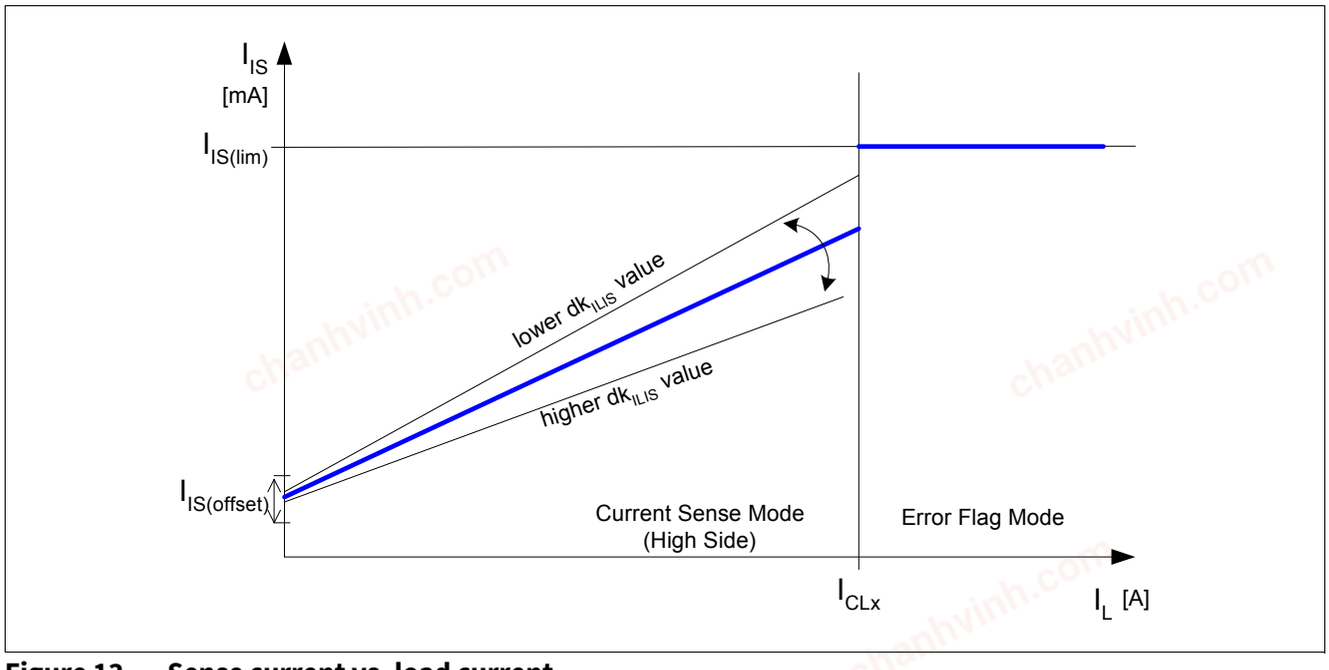


Figure 13 Sense current vs. load current

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5.4.5 Truth table

Table 9 Truth table

Device State	Inputs		Outputs			Mode
	INH	IN	HSS	LSS	IS	
Normal operation	0	X	OFF	OFF	0	Stand-by mode
	1	0	OFF	ON	$I_{IS(offset)}$	LSS active
	1	1	ON	OFF	CS	HSS active
Undervoltage (UV)	X	X	OFF	OFF	0	UV lockout, reset
Overtemperature (OT) or short circuit of HSS or LSS	0	X	OFF	OFF	0	Stand-by mode, reset of latch
	1	X	OFF	OFF	1	Shutdown with latch, error detected
Current limitation mode/ overcurrent (OC)	1	1	OFF	ON	1	Switched mode, error detected[1)]
	1	0	ON	OFF	1	Switched mode, error detected[1)]

1) Will return to normal operation after t_{CLS}; Error signal is reset after 2*t_{CLS} (see **Chapter 5.3.3**)

Table 10

Inputs	Switches	Current sense / status flag IS
0 = Logic LOW	OFF = switched off	$I_{IS(offset)}$ = Current sense - Offset (for conditions see table: **Current sense**)
1 = Logic HIGH	ON = switched on	CS = Current sense - high side (for conditions see table: **Current sense**)
X = 0 or 1		1 = Logic HIGH (error)
		0 = No output

5.4.6 Electrical characteristics - control and diagnostics

Table 11 Electrical characteristics - control and diagnostics

V_S = 24 V, T_j = 25 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Control inputs (IN and INH)							
High level voltage INH, IN	$V_{INH(H)}$ $V_{IN(H)}$	–	1.6	2	V	–	P_5.4.1
Low level voltage INH, IN	$V_{INH(L)}$ $V_{IN(L)}$	1.1	1.3	–	V	–	P_5.4.2
Input voltage hysteresis	V_{INHHY} V_{INHY}	–	300	–	mV	1)	P_5.4.3
Input current high level	$I_{INH(H)}$ $I_{IN(H)}$	15	30	100	µA	V_{IN} = V_{INH} = 5.3 V	P_5.4.4

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Table 11 Electrical characteristics - control and diagnostics (cont'd)

V_S = 24 V, T_j = 25 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input current low level	$I_{INH(L)}$ $I_{IN(L)}$	15	25	50	µA	$V_{IN} = V_{INH} = 0.4$ V	P_5.4.5
Current sense							
Differential current sense ratio in static on-condition $dk_{ILIS} = dI_L / dI_{IS}$	dk_{ILIS}	15	19.5	24	10^3	V_S = 13.5 V R_{IS} = 1 kΩ I_{L1} = 10 A I_{L2} = 40 A	P_5.4.6
Maximum analog sense current, Sense current in fault condition	$I_{IS(lim)}$	4.1	5	6.1	mA	V_S = 13.5 V R_{IS} = 1 kΩ	P_5.4.7
Isense leakage current	I_{ISL}	–	–	1	µA	V_{INH} = 0 V	P_5.4.8
Isense offset current	$I_{IS(offset)}$	30	170	385	µA	V_{INH} = 5 V $I_{SD(HS)}$ = 0 A	P_5.4.9

1) Not subject to production test, specified by design.

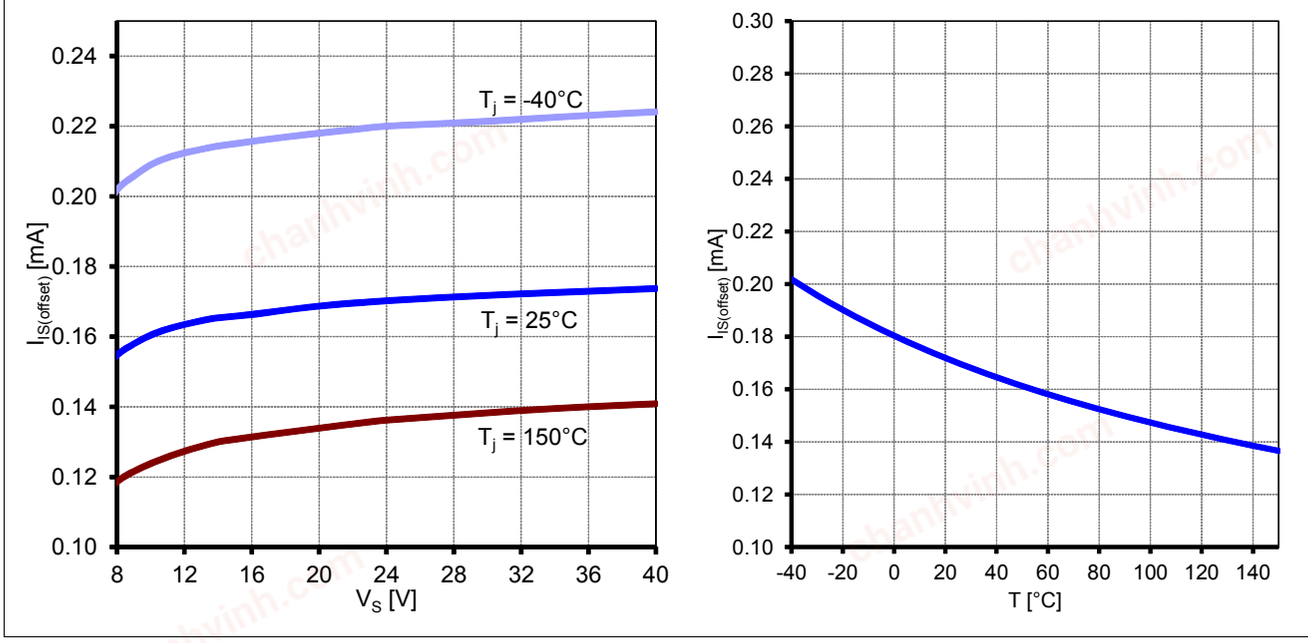


Figure 14 Typical current sense offset current

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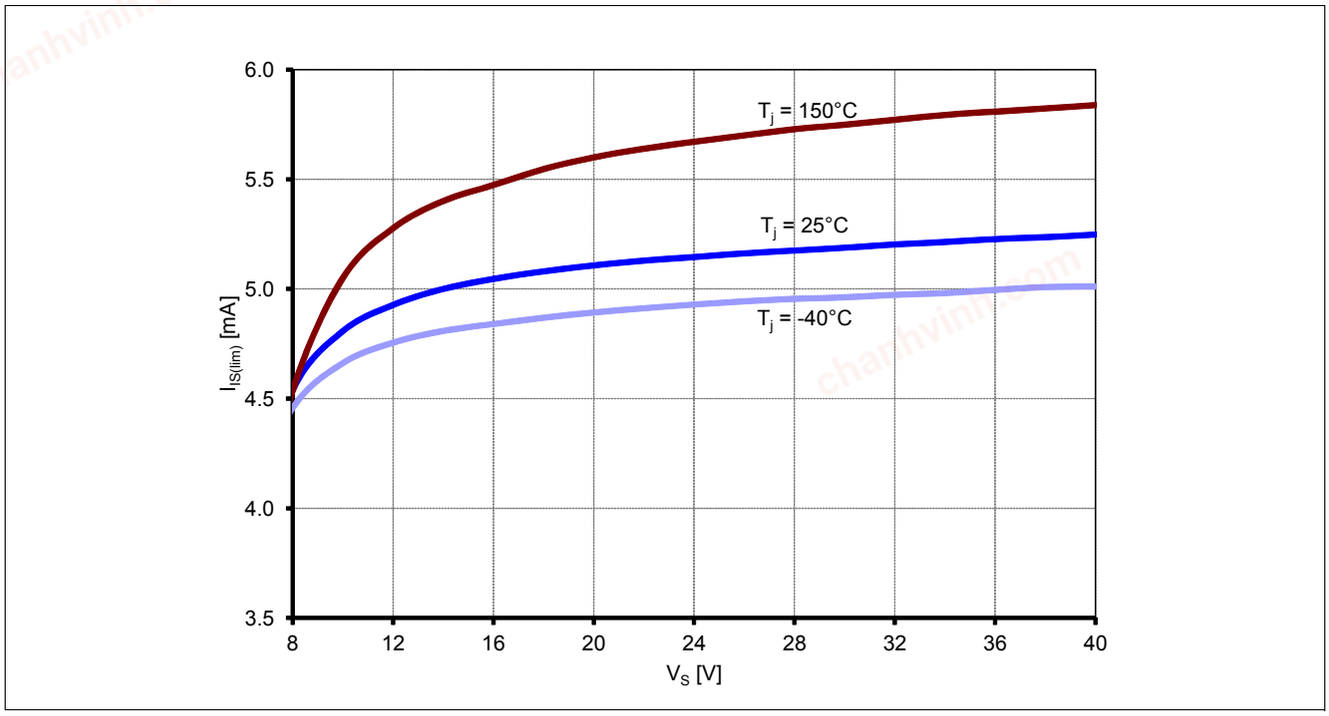


Figure 15 Typical characteristic of the maximum analog sense current in fault condition (Pos. 5.4.7.)

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6 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

6.1 Application circuit

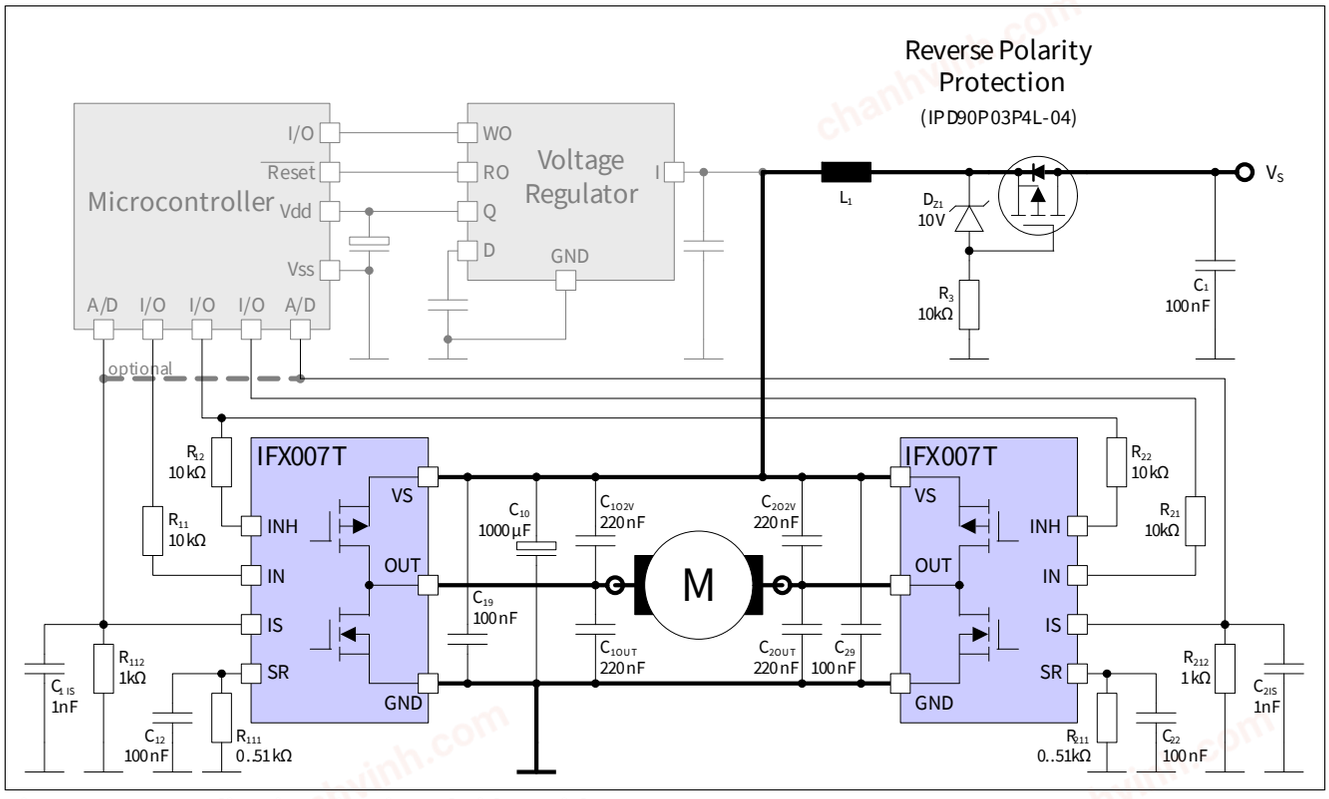


Figure 16 Application circuit: H-bridge with two IFX007T

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

6.2 Layout considerations

Due to the fast switching times for high currents, special care has to be taken to the PCB layout. Stray inductances have to be minimized in the power bridge design as it is necessary in all switched high power bridges. The IFX007T has no separate pin for power ground and logic ground. Therefore it is recommended to assure that the offset between the ground connection of the slew rate resistor, the current sense resistor and ground pin of the device (GND / pin 1) is minimized. If the IFX007T is used in a H-bridge or B6 bridge design, the voltage offset between the GND pins of the different devices should be small as well.

Due to the fast switching behavior of the device in current limitation mode a low ESR electrolytic capacitor C_{10} from VS to GND is necessary. This prevents destructive voltage peaks and drops on VS. This is needed for both PWM and non PWM controlled applications. To assure efficiency of C_{10} and C_{19}/ C_{29} the stray inductance must be low. Therefore the capacitors must be placed very close to the device pins. The value of the capacitors must be verified in the real application, taking care for low ripple and transients at the Vs pin of the IFX007T.

The digital inputs need to be protected from excess currents (e.g. caused by induced voltage spikes) by series resistors greater than 7 kΩ.

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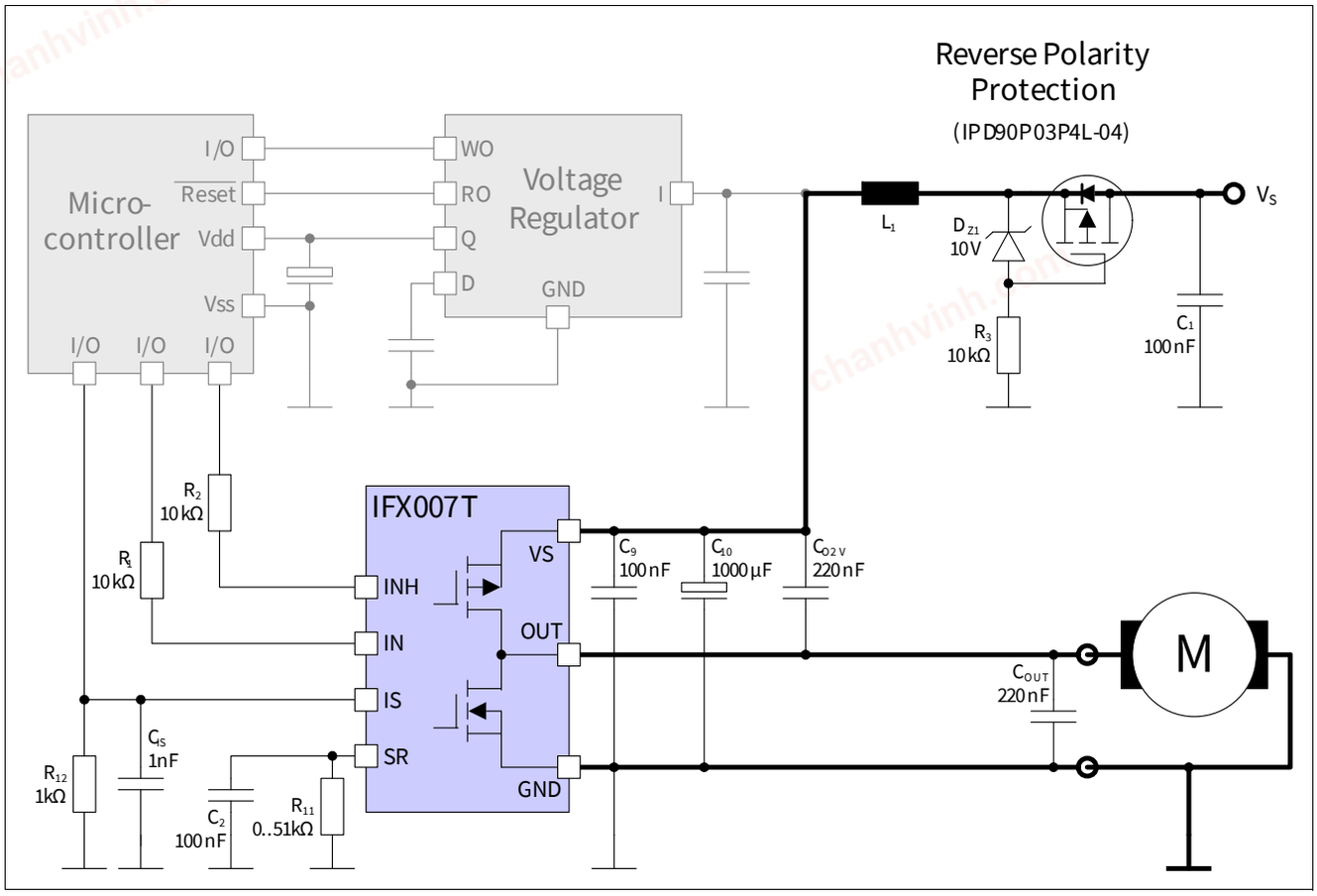


Figure 17 Application circuit: half-bridge with a IFX007T (load to GND)

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

6.3 PWM control

For the selection of the max. PWM frequency the choosen rise/fall-time and the requirements on the duty cycle have to be taken into account. We recommend a PWM-period at least 10 times the rise-time.

Example:

Rise-time = fall-time = 4 µs.

=> T-PWM = 10 * 4 µs = 40 µs.

=> f-PWM = 25 kHz.

The min. and max. value of the duty cycle (PWM ON to OFF percentage) is determined by the real fall time plus the real rise time. In this example a duty cycle make sense from approximately 20% to 80%.

If a wider duty cycle range is needed, the PWM frequency could be decreased and/or the rise/fall-time could be accelerated.

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7 Package Outlines

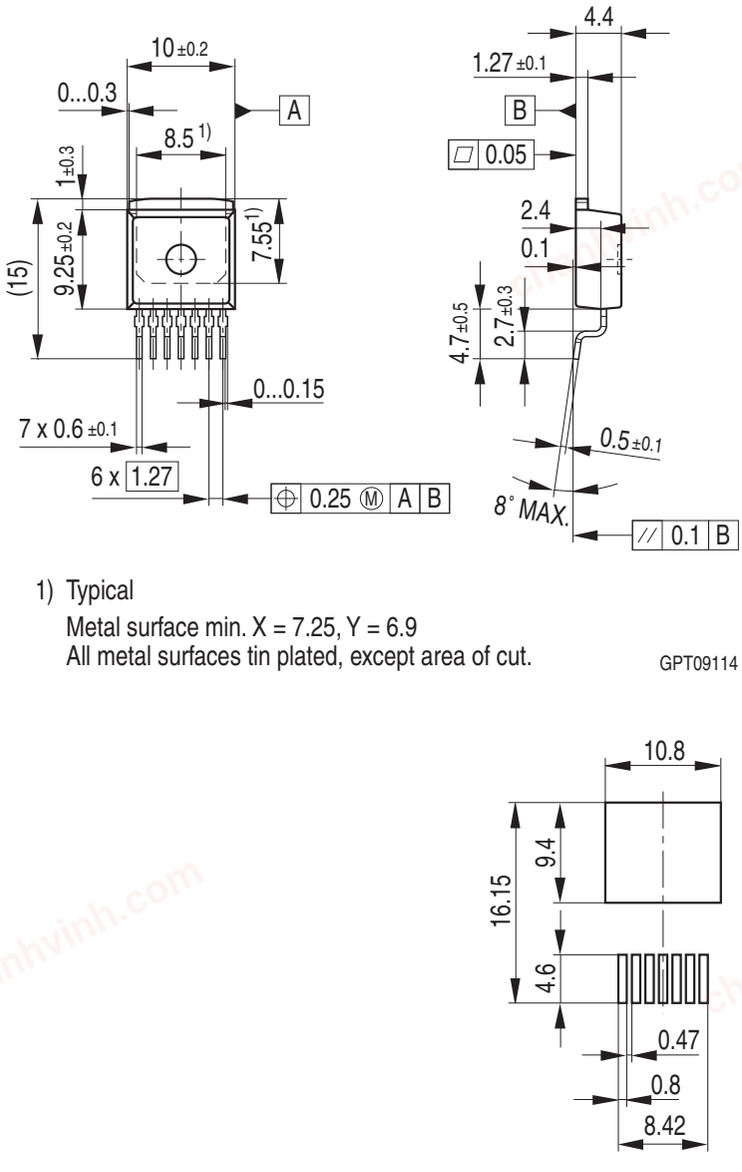


Figure 18 PG-TO263-7-1 (Plastic Green Transistor Single Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

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8 Revision History

Revision	Date	Changes
Rev. 1.0	Data Sheet	Initial release.

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