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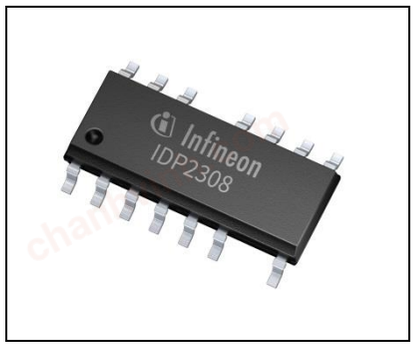
Digital Multi-Mode PFC + LLC Combo Controller

Product Highlights

- Integrated 600V startup cell
- Integrated floating driver based on coreless transformer technology
- Digital multi-mode operation for higher efficiency curve
- Supports low stand-by power by means of direct X-cap discharge function and advanced burst mode control
- Eliminates the auxiliary power supply by means of integrated startup cell and burst mode
- UART interface for communication and in-circuit configuration
- Flexible design-in by means of one time programming capability for a wide range of parameters



Description

The IDP2308 is a multi-mode PFC and LLC controller combined with a floating high side driver and a startup cell. A digital engine provides advanced algorithms for multi-mode operation to support highest efficiency over the whole load range. A comprehensive and configurable protection feature set is implemented. Only a minimum of external components are required with the low pin count DSO-14 package. The integrated HV startup cell and advanced burst mode enable to achieve low stand-by power. In addition a one-time-programming (OTP) unit is integrated to provide a wide set of configurable parameters that help to ease the design in phase.

Features

- Multi-mode PFC
- Configurable PFC gate driver
- Synchronous PFC and LLC burst mode control
- Configurable non-linear LLC VCO curve
- Configurable soft-start
- V_{AC} input voltage sensing and X cap discharge via HV pin

Applications

- LCD-TV 75W ~ 300W
- Generarl SMPS

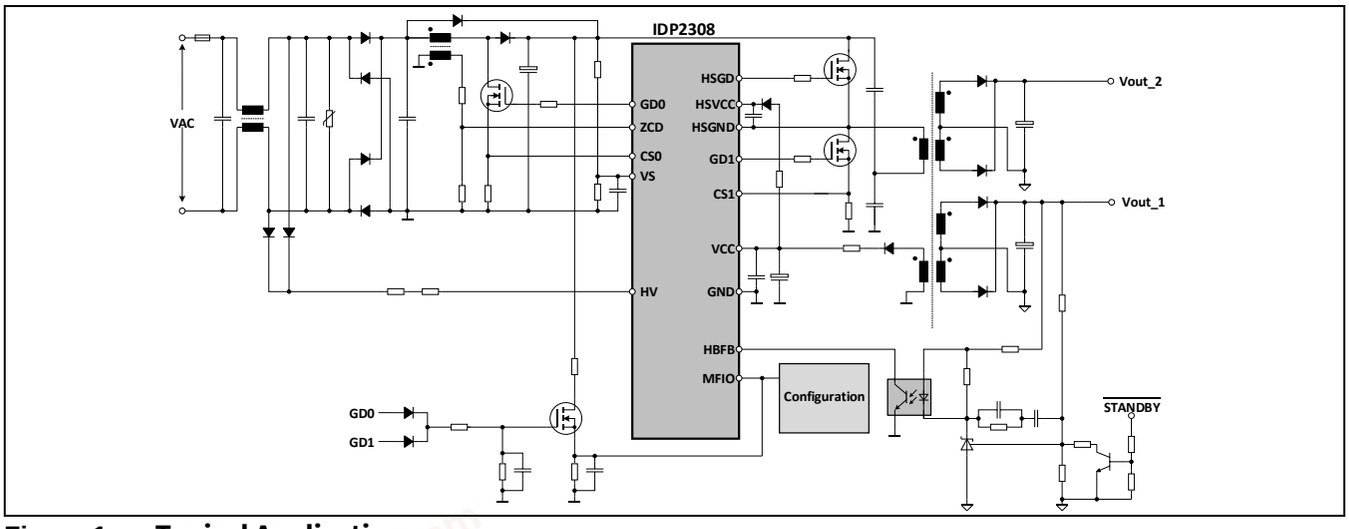


Figure 1 Typical Application

Product Type	Package	Marking
IDP2308	PG-DSO-14	DP2308

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1 Pin Configuration and Description

The pin configuration is shown in Figure 2 and Table 1. The Pin functions are described below.

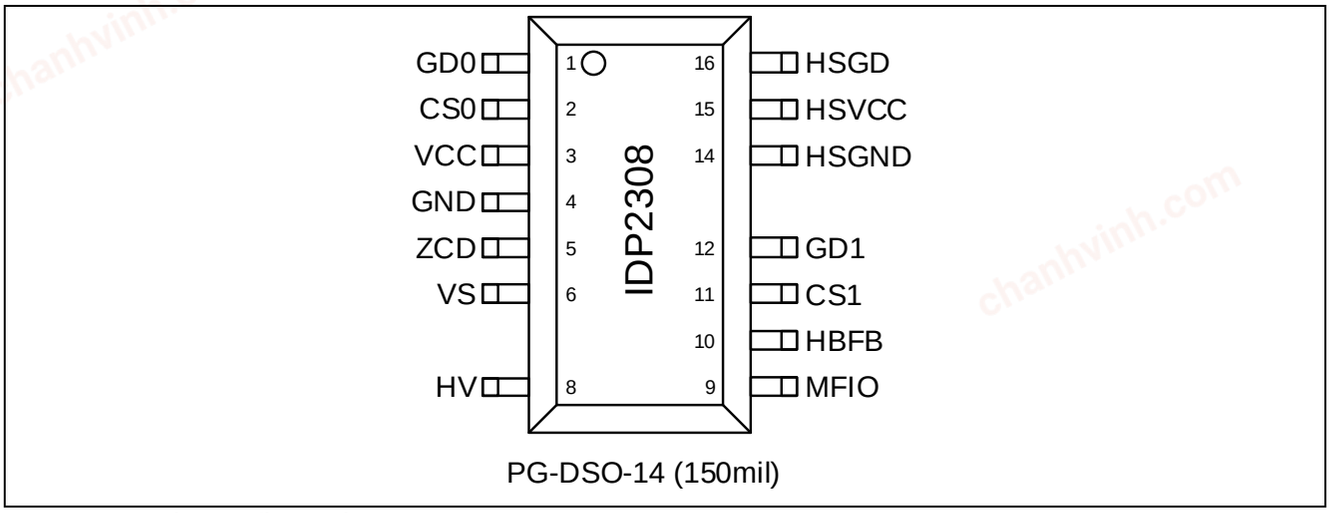

Figure 2 Pin Configuration

Table 1 Pin Definitions and Functions

Symbol	Pin	Type	Function
GD0 (PFCGD)	1	O	**Gate Driver Output 0 (PFC Gate Driver)** Output for directly driving the PFC PowerMOS. The default peak source current capability is 156 mA and the peak sink current capability is 800 mA.
CS0 (PFCCS)	2	I	**Current Sense 0 (PFC Current Sense)** Pin CS0 is connected to an external shunt resistor and the source of the PFC PowerMOS.
VCC	3	P	**Positive Voltage Supply** IC power supply
GND	4	G	**Ground** IC ground
ZCD	5	I	**Zero Crossing Detection** Pin ZCD is connected to the auxiliary winding of the PFC choke.
VS	6	I	**Voltage Sensing** Pin VS is connected to a high ohmic resistor divider for directly sensing the bus voltage.
HV	8	I	**High Voltage Input** Pin HV is connected to the AC input via an external resistor and 2 diodes. There is a 600 V HV startup-cell internally connected that is used for initial VCC charge. It is also used to discharge the x-capacitors of the EMI network. Furthermore sampled high voltage sensing is supported for brownin/brownout detection.
MFIO	9	I	**MFIO** Pin MFIO provides a half duplex UART communication IO interface for parameter configuration. It also can be used for PFC output redundant over voltage protection. In that case it is recommended to use a BSS127 transistor as shown in Figure 1 and the described in section 3.4.3.4.
HBFB	10	I	**Half Bridge Feedback** Pin HBFB is connected to an optocoupler for the feedback path to control the LLC switching frequency.

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Symbol	Pin	Type	Function
CS1 (HBCS)	11	I	**Current Sense 1 (Hallf Bridge current Sense)** Pin CS1 is connected to an external shunt resistor and the source of the PowerMOS in the half-bridge stage.
GD1 (LSGD)	12	O	**Gate Driver Output 1 (Half Bridge Low Side Gate Driver)** Output for directly driving the lowside PowerMOS in the half-bridge. The peak source current capability is 120 mA and the peak sink current capability is 500 mA.
HSGND	14	G	**High side Ground** Ground for floating high side driver
HSVCC	15	P	**High side VCC** Power supply of the high side floating driver, supplied via bootstrap
HSGD	16	O	**High side floating Gate Driver** Output for directly driving the high side PowerMOS in the half-bridge. The peak source current capability is 0.52 A and the peak sink current capability is 1.3 A. Refer to item 4.4.9 for more details.

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2 Representative Blockdiagram

A simplified functional block diagram is given in Figure 3. Note that this figure only represents the principle functionality.

IDP2308 digital combo-PFC & LLC controller consists of an Infineon 66MHz (f_{MCLK}) NanoDSP processor to actualize both the power factor correction (PFC) and a half-bridge resonant function. The PFC and LLC controllers function with their configured parameter to optimize the performance. The current sense, zero-crossing and voltage sense provide the controller as well as the processor inputs for its control.

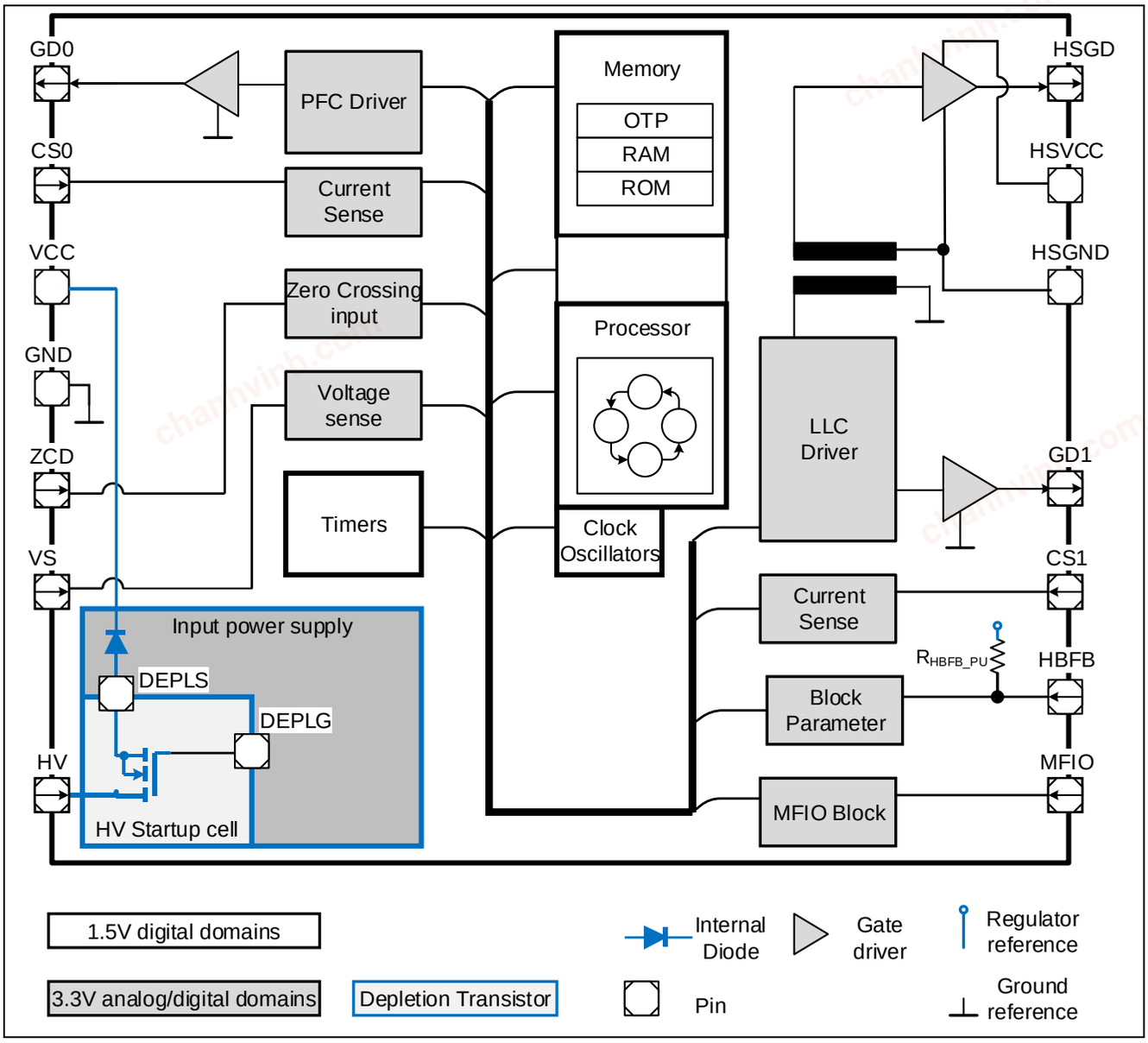

Figure 3 Representative Blockdiagram

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3 Functional Description

The functional description gives an overview about the integrated functions and features and their relationship. The mentioned parameters and equations are based on typical values at T_A = 25°C. The correlated minimum and maximum values are shown in the electrical characteristics in Chapter 4.

This chapter contains following main descriptions:

- Introduction (Chapter 3.1)
- Overview Controller Features (Chapter 3.2)
- General control features (Chapter 3.3)
- PFC Controller (Chapter 3.4)
- Half-bridge LLC Controller (Chapter 3.5)
- Operation Flow (Chapter 3.6)
- Overview Protection Features (Chapter 3.7)
- Fixed and configurable parameters (Chapter 3.8)

3.1 Introduction

The IDP2308 is a digital Combo-LLC controller to support application topologies with a multi-mode PFC and half-bridge LLC stage. The IC consists of a smart digital core that provides advanced algorithms for multi-mode operation and a variety of protection features. A high degree of forward integration is realized by implementing a floating HV gate driver and a HV startup cell in a slim PG-DSO-14 package. Multifunctional pins ensure a very low component count in the application. General controller features are summarized in Table 2.

The IC supports highest design-in flexibility in the application by means of an advanced set of configurable parameters. The configuration can be done via a half duplex UART interface at pin MFIO.

3.2 Overview Controller Features

- General Controller Features (Table 2)
- PFC Controller Features (Table 5)
- LLC Controller Features (Table 6)

3.3 Overview Controller Features

This chapter provides an overview of functional blocks for Figure 3. The general control features are

Table 2 General Controller Features

System and Devices overview	Chapter 3.3.1
IC Power System and High Voltage Startup Cell	Chapter 3.3.2
Direct AC input monitoring combined with VCC startup function	Chapter 3.3.2.1
X-cap discharge function via the integrated HV startup-cell	Chapter 3.3.2.2
Standby Mode with synchronous PFC-LLC burst operation	Chapter 3.3.3
IC protection	Chapter 3.3.4
Auto restart mode	Chapter 3.3.4.4
AC detection	Chapter 3.3.5

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3.3.1 System and Device overview

The device is dominantly used in an AC/DC application with a working scenario as illustrated below. The device on powering-up enters start-up and soft-start stage. Once the voltage at the primary side and secondary side of the transformer stabilizes, depending on the load condition, the device operates in extremely light load or normal operation.

In extremely light load condition, the device operates in burst, meaning the gate drivers are driven at a lower frequency ranges and switching on periodically only to maintain the supply voltage and the VCC of the device.

In normal operating condition, the device actively switches its gate driver to regulate the voltage and current supplies to the load.

In Figure 4, when overcurrent protection mechanism is triggered, the device shall shut down its LLC and PFC controller and enter a restart of the system and attempt to re-power the system. There are many protection and shut-down scenario. For further detail, please refer to Chapter 3.7.

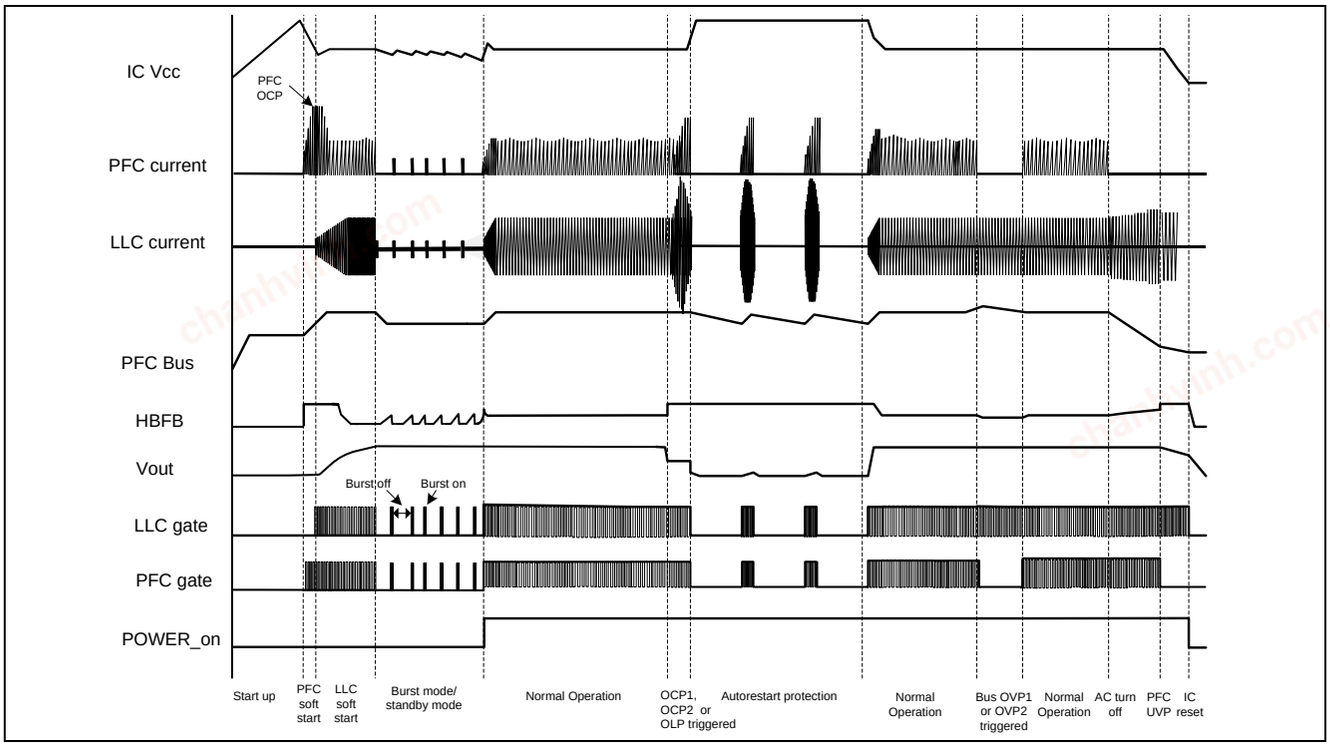

Figure 4 IDP2308 Operation Overview

3.3.1.1 Processor and memory operations

This chapter describes the IC power processor function and its operation.

On powering up, the device's processor initializes and loads its configuration from its one-time-programmable memory and configures the device to its application needs. The timer for the scheduler is programmed and the processor run within a scheduler timing function to continuous monitor for any protection event as well as optimize the parameter for the PFC and LLC controllers.

The processor runs in an active scheduler mode when the PFC and the LLC controller are running and runs in the following mode in specific condition of the system.

- HV-startup: System "cold start" with VCC startup via the integrated HV startup cell.
- Standby: System operates in synchronous PFC-LLC burst operation to keep output voltage regulated and yet maintain very low system power consumption

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- Auto-restart: A protection mode that stops all PFC and LLC switching operations, puts the IC into a suitable sleep mode, and initiates a new startup after a configurable break time[1].

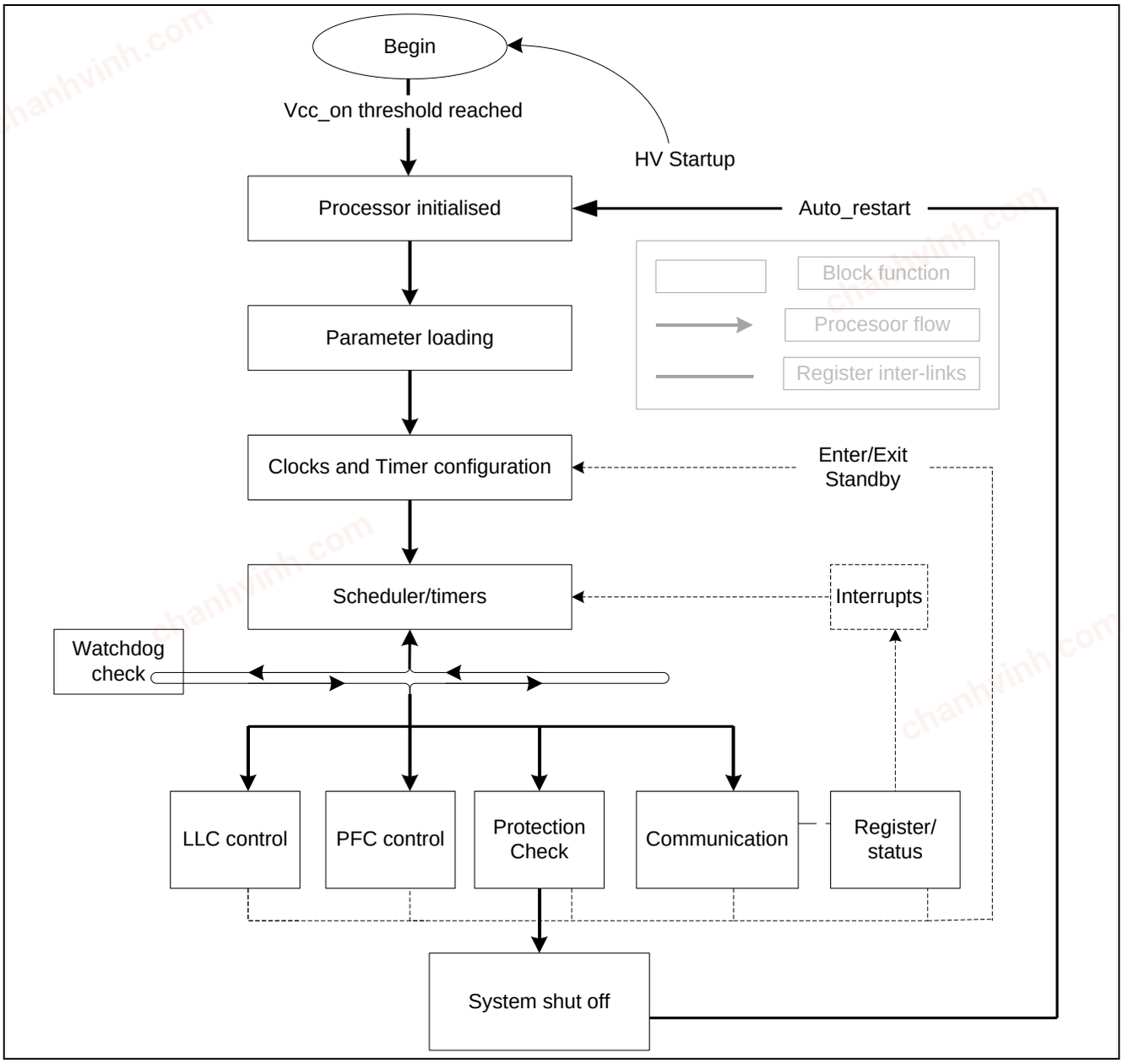

Figure 5 Overview of Processor operations

The processor runs its program from its Read Only Memory (ROM) with random access memory (RAM) as main data space for computation and control-flow state records during operation.

The processor monitors and processes the analog-to-digital (ADC) data. The processed data is provided to control the power-factor-correction (PFC) and Resonant LLC converter. The processor also monitors the input line (AC), its own monitoring lines as well as the output load feedback voltage for protection condition and mitigates according to the conditions with the protection function. All the information are registered and interrupts are triggered when interrupt event occurs.

[1] Please refer to Chapter 4.7 for more detail about the protection mechanisms.

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3.3.1.2 Communication interface

The communication to external host is via the MFIO pin and is handled by the processor in firmware. A half-duplex UART communication data between the host and the device is transferred through internal UART.

3.3.1.3 Voltage and current sensors

IDP2308 sensing nodes are multiplexed to an analog-to-digital (ADC) module to allow the device to monitor the system behavior and its internal behavior. The voltage and current sensors are multiplexed to the ADC as well.

Each of the sensing node samples its voltage or current and the sampling is multiplexed onto the ADC where the digital read-out is measured.

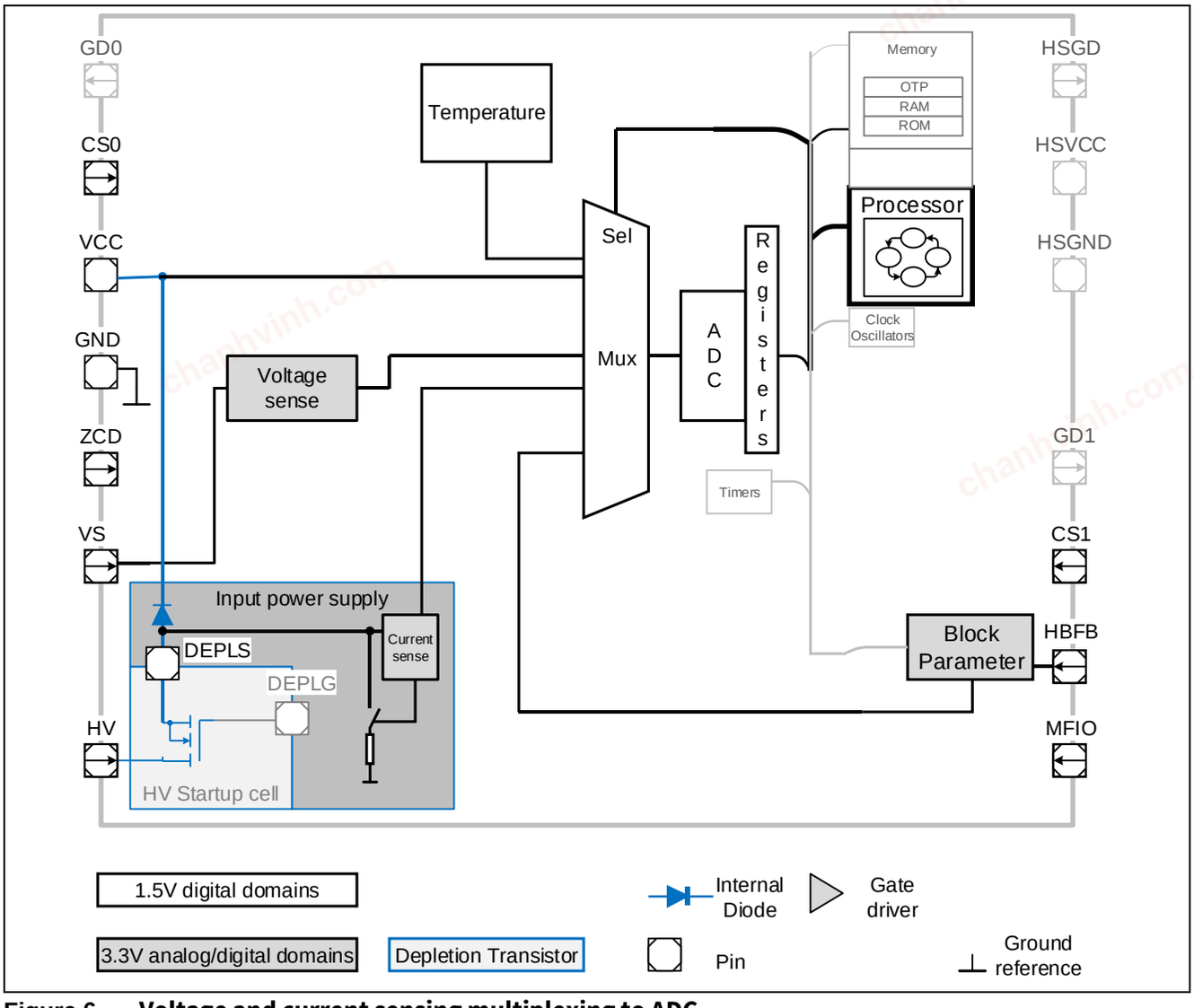

Figure 6 Voltage and current sensing multiplexing to ADC

Figure 6 shows the sensing paths that are multiplexed to the ADC. The ADC sensing is time-multiplexed to the sensing nodes and is managed internally by the processor. Timers are used to enable and disable the sample and hold circuit in the current sense block. Within each of the sensing block, there are sub-sensing nodes that allow measurement for each specific function. See Chapter 4.4.3 and Chapter 4.4.4 for further details.

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3.3.2 IC Power Supply and High Voltage Startup Cell

This chapter describes the IC power supply approach and the functions correlated with the high voltage startup cell for Figure 1. The functions supported by the high voltage startup cell are

- Direct AC input monitoring combined with VCC startup function (Chapter 3.3.2.1)
- X-cap discharge function via the integrated HV startup-cell (3.3.2.2)

IDP2308 contains four power supply pins VCC, GND, HSVCC and HSGND. The VCC is the main low voltage supply input at the IC. All the internal circuits except the integrated floating driver are connected to pin VCC and pin GND, which is the common ground. A capacitor needs to be placed directly at the pins VCC and GND to provide a proper buffering of the IC power supply voltage.

The pins HSVCC and HSGND are the power supply pins for the integrated floating high side driver. The high side driver is supplied by an external bootstrap buffer capacitor that also needs to be connected close to pins HSVCC and HSGND. The external bootstrap capacitor is charged via an external bootstrap diode and resistor which are connected in serial to the VCC supply.

3.3.2.1 Direct AC input monitoring combined with VCC startup function

There are two main functions supported at pin HV, with the connection of the AC input voltage via a resistor, R_{HV} (51kΩ) and two diodes (See Figure 8).

The integrated HV startup-cell is switched on during the VCC startup phase, when the IC is inactive. A current is flowing from pin HV to pin VCC via an internal diode, which charges the capacitor at pin VCC. This current is limited by the R_{HV} and the $R_{DS(on)}$ of the HV startup-cell. Once the voltage at pin VCC exceeds the VCC on- threshold, the active operating phase is entered.

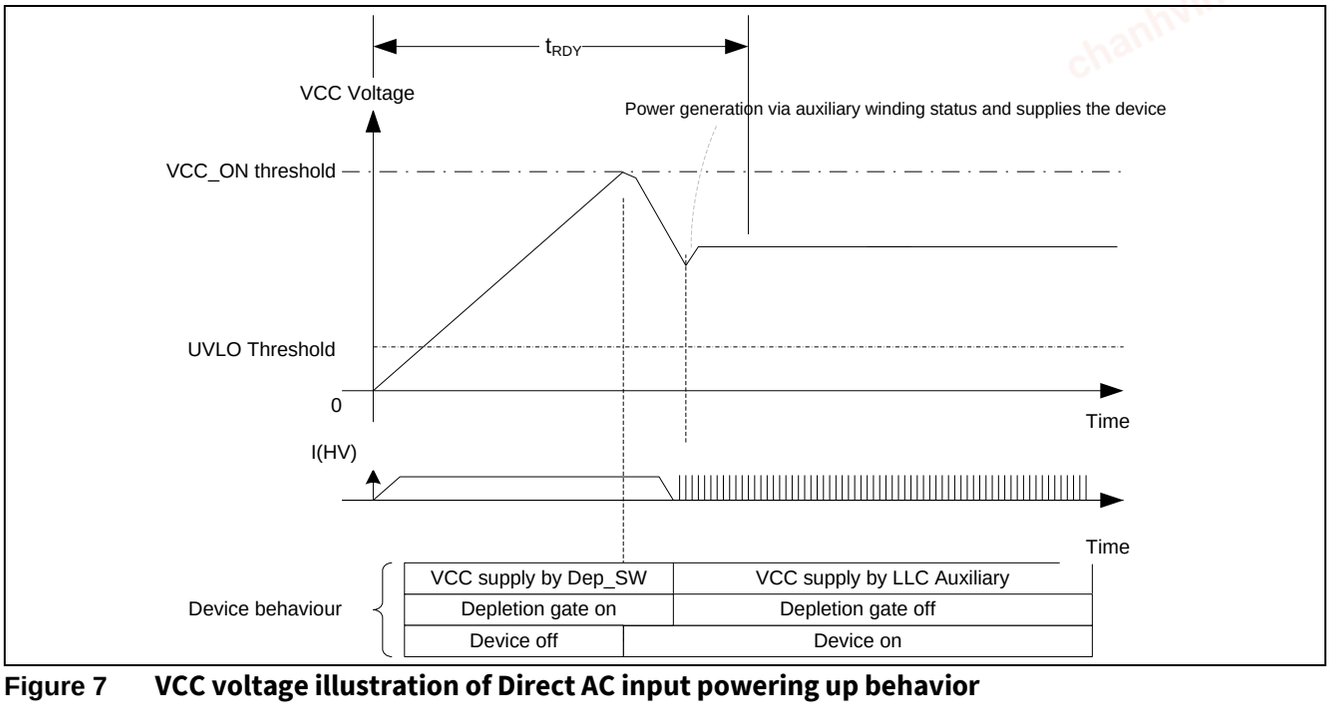

Figure 7 VCC voltage illustration of Direct AC input powering up behavior

Within the device, a direct AC input monitoring is supported by a resistive sense that is switched on periodically by an internal timer. The timer switches on the HV startup cell and the switch T2 for a very short time after a defined period. During this short on-time, the voltage across R_{SH} is sensed to estimate the HV voltage (See Figure 8).

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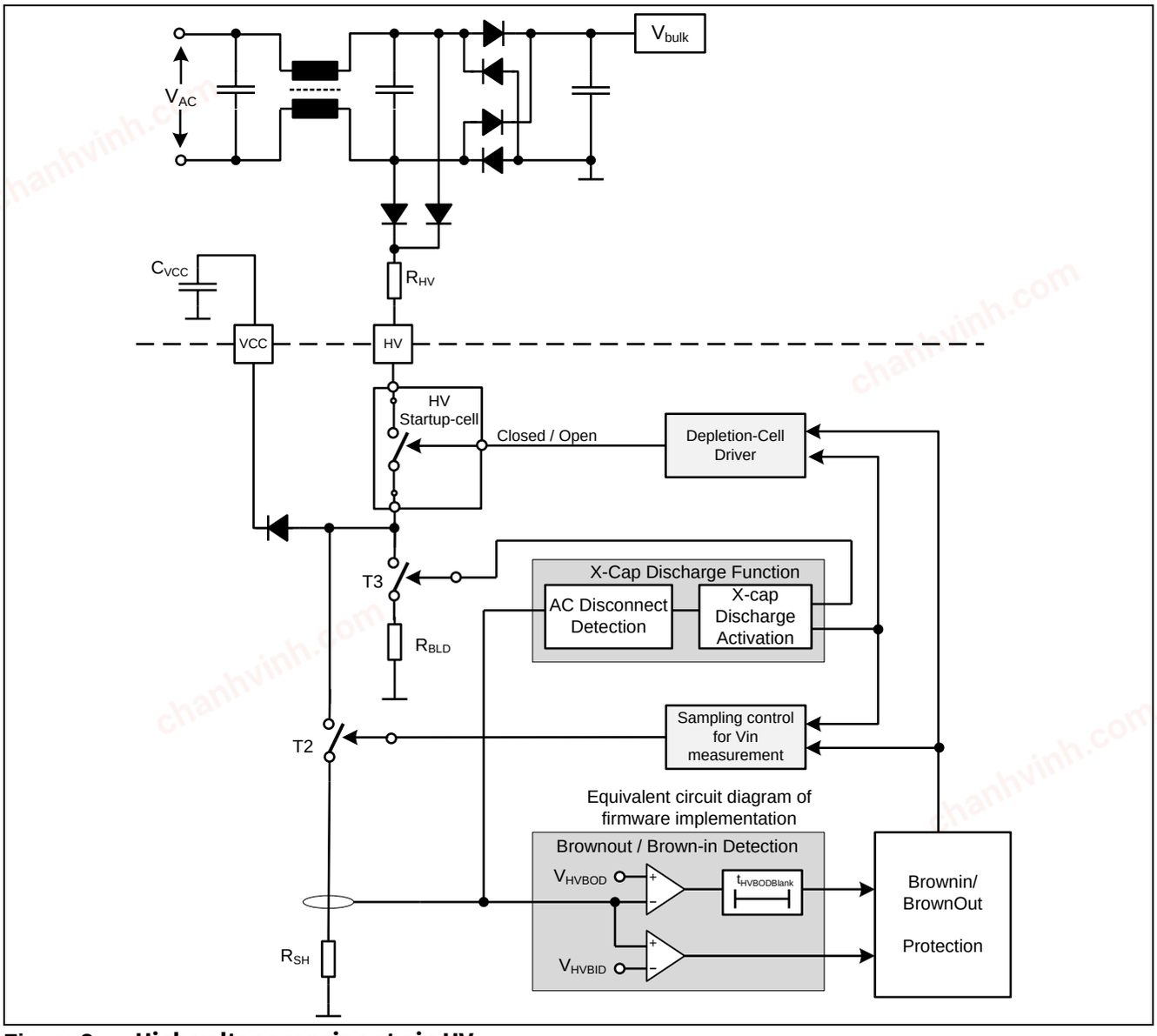

Figure 8 High voltage sensing at pin HV

3.3.2.2 X-cap discharge function via the integrated HV startup-cell

Safety standard requires X-caps to be discharged within one second once the switching mode power supply is disconnected from the AC line.

The AC waveform is closely monitored by the HV pin through external resistor R_{HV} (51 kΩ). An AC detection algorithm checks if there is an alternating voltage at the converter input. This function works reliably for input voltages as specified in Table 3. As soon as the voltage stops alternating an AC unplug event is detected and input capacitors (XCAPs) are getting discharged via the depletion cell of IDP2303B between pins HV and GND. AC unplug detection time is typically within a few hundred Milliseconds and maximum 800 ms. The maximum discharge time constant for the maximum XCAP capacitance value of 2µF (see Table 4) is then appr. 104 ms (with R_{HV} = 51kΩ and the IC internal resistance of about 1kΩ). Therefore the XCAPs are safely discharged within 1s to ES1 or SELV limits according to IEC62368 and IEC60950.

The X-caps are then discharged to fulfil the safety standard. The discharging current is determined by the external resistor R_{HV} (51 kΩ) and R_{BLD} (see Figure 8). The X-cap discharge function is a configurable parameter.

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Table 3 Input voltage ratings for reliable AC detection

Parameters		Min.	Max.	Unit	Remarks
Input voltage		90	264	VAC	
Frequency	Range 1	47	53	Hz	
	Range 2	57	63	Hz	

Table 4 XCAP discharge component ratings

Parameters	Min.	Max.	Unit	Remarks
Total capacitance of all XCAPs	0.1	2	µF	
Total discharge resistance from AC voltage to HV pin	51	60	kΩ	Default R_{HV} 51 kΩ

3.3.3 Standby Mode with synchronous PFC-LLC burst operation

For IDP2308, a “STANDBY” signal from the application will trigger the start to enter standby mode. The “STANDBY” signal will cause a change in resistor divider ratio such that the rated output voltage is regulated at lower voltage in standby mode. If V_{HBFB} is less than $V_{_burst_enter}$ for a blanking time of $t_{_blk_burst}$, both PFC and LLC will stop switching immediately. The IC is put into power saving mode. The controller enters into burst pause phase of standby mode.

During the standby mode, the HBFB pin is monitored to control the burst mode operation. When the HBFB voltage rises up and reaches the burst on threshold $V_{_burst_on}$, or VCC drops below $V_{VCC_burst_off}$, the device will wake up and start burst mode operation. LLC burst on time $t_{_burst_on_max}$ is constant and configurable with soft-start and soft-stop. After LLC completes one full busrt on switching, the device will stop switching and enters sleep mode to save the power consumption.

The LLC busrt frequency $f_{_sw_busrt}$ and $t_{_burst_on_max}$ are optimized at typical standby power load in order to achieve lowest input power and output ripple. Meanwhile, under ultra light load condition, e.g. no load condition, LLC will increase burst frequency adaptively according burst off time. In the end, burst frequency is stabilized so as to regulate busrt off time around maximum burst off time $t_{_burst_off_max}$. By setting proper $t_{_burst_off_max}$, LLC can deliver right-fit energy adaptively to different load and avoid deep saturation of feedback loop, which is able to reduce output ripple, minimize power consumption at secondary feedback path and perform excellent dynamic load response.

When heavy load comes, the HBFB voltage will rise up and hit the leaving burst mode threshold $V_{_burst_exit}$. Then the device will leave burst mode operation. Another leaving burst mode condition is when the burst off time reaches the minimum burst off time limit $t_{_burst_off_min}$.

3.3.4 IC protection

3.3.4.1 Undervoltage lockout for VCC

There is an undervoltage lockout unit (UVLO) implemented, that ensures a defined enabling and disabling of the IC operation depending on the supply voltage at pin VCC. The UVLO contains a hysteresis with the voltage thresholds V_{VCCon} for enabling the IC and V_{VCCoff} for disabling the IC.

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3.3.4.2 Overvoltage protection for VCC

Overvoltage protection at VCC is triggered when V_{VCC} exceeds a threshold of $V_{_VCCOVP}$ for a blanking time of $t_{_VCCOVP}$. The system enters into auto restart mode then.

3.3.4.3 Over temperature protection

When the internal temperature exceeds the over temperature protection level $T_{_OTP}$, the system enters into latch mode. System restarts operation after VCC recycle (VCC < V_{VCC_PD}).

3.3.4.4 Auto Restart Mode

Once the auto restart mode is entered, the IC stops both PFC and LLC switching operations and enters sleep mode. During this auto restart off-phase the HV startup-cell is activated to maintain the VCC voltage. After the configurable auto restart breaktime $t_{_AR}$ the IC initiates a new start-up.

3.3.5 AC detection

This feature is used for detecting AC unplug condition during standby mode and is implemented via a combination of built-in hardware and firmware. The figure below shows the configuration of the EMI filter and where input voltage is sensed through the HV pin.

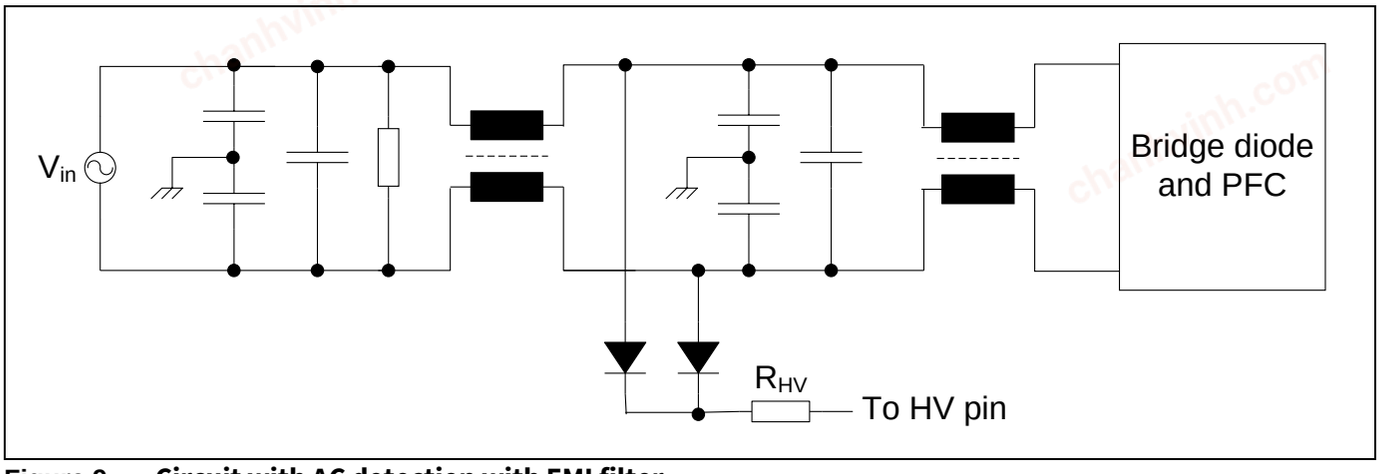

Figure 9 Circuit with AC detection with EMI filter

During standby mode, low power consumption is the main challenge. IDP2308 makes use of the AC detection function to detect the AC unplug quicky and reliably. With the AC detection, it neither needs to sample the AC voltage too often nor needs to trigger the wakeup of the IC too often and hence it can maintain low standby power consumption. Having detected the AC unplugged, the X-cap discharge function would be triggered. In the AC detection function, IDP2308 would take AC samples after defined time intervals and based on proprietary algorithm it determines the decision of unplug condition.

3.4 PFC Controller

The PFC controller turns on and off the PFC gate driver so that a desired bus voltage is maintained while the AC input current is approximately proportional to the AC line voltage resulting in high power factor and low THD. A gate driver switching cycle has divided into three phases:

- the on-time, t_{on}, where the PFC MOSFET is turned on, and the PFC choke current increases
- the freewheeling time, t_f, where the PFC MOSFET is turned off, the choke current decreases and charges the PFC output capacitor via the freewheeling diode

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- the waiting time t_w, which starts when the choke current decreased to zero and an oscillation is observed at the drain-source voltage of the switching MOSFET and the voltage at the auxiliary winding.

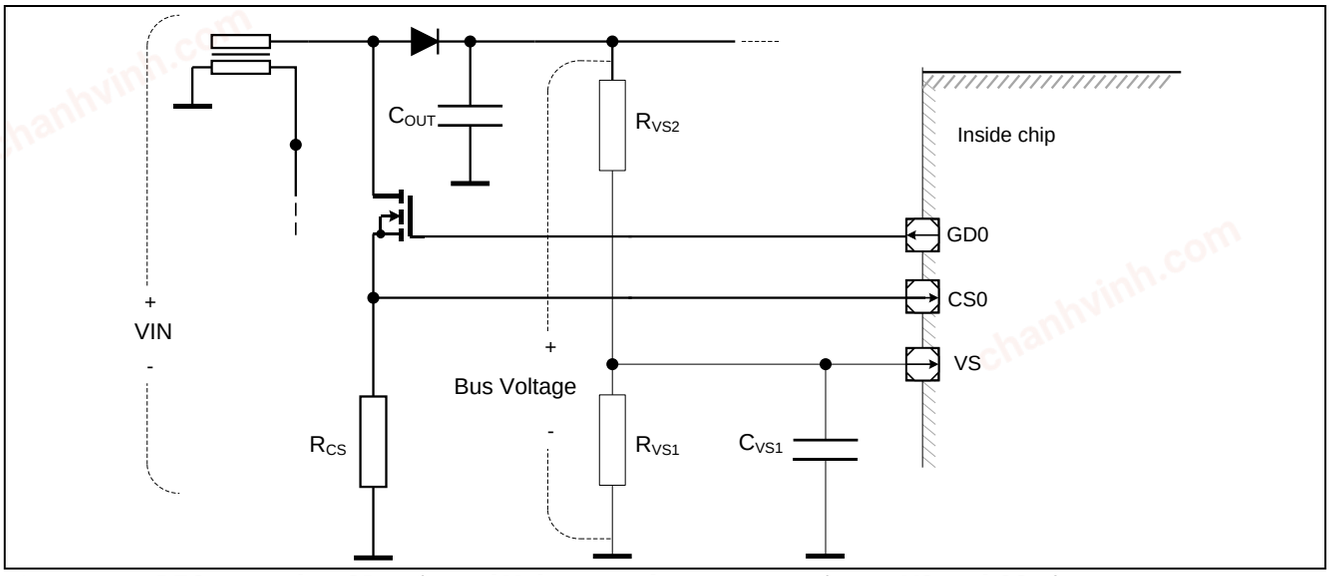

Figure 10 PFC control at GD0 pin and Voltage and current sensing at VS and CS pins

The following PFC functionality of the controller is described:

Table 5 PFC Controller Features

PFC Softstart	Chapter 3.4.1
Multi-mode PFC control	Chapter 3.4.2
PFC Protection	Chapter 3.4.3
PFC Open Control Loop Protection (PFCOLP)	Chapter 3.4.3.1
PFC Inductor Over Current Protection (PFCOCP)	Chapter 3.4.3.2
PFC Output Over Voltage Protection (PFCOVP)	Chapter 3.4.3.3
PFC Output Redundant Over Voltage Protection (PFCROVP)	Chapter 3.4.3.4
PFC Output Under Voltage Protection (PFCUVP)	Chapter 3.4.3.5
PFC Brownin Protection for AC Input Line (PFCBID)	Chapter 3.4.3.6
PFC Brownout Protection for AC Input Line (PFCBOD)	Chapter 3.4.3.7
PFC Long Time Continuous Conduction Mode Protection (PFCCCMP)	Chapter 3.4.3.8

3.4.1 PFC Softstart

PFC softstart, a PI controller calculates the on-time as a function of the difference between the reference bus voltage and the actual PFC bus voltage. To compensate for the on-time and hence line dependency of the boost power stage, the output of the PI controller is multiplied with on-time. The PFC operates in fixed QR-1 operation with minimum on-time. With the minimum on-time multiplied to the output of the PI controller, it will form an exponential softstart ramp for on-time that limits the switching frequency and startup current. Once the desired PFC bus voltage is reached, it resumes to normal multimode PFC operation.

3.4.2 PFC Multi-mode operation

For PFC operating in critical conduction mode CrCM, the MOSFET is turned on with a constant on-time throughout the complete AC half cycle and the off-time is varying during the AC half cycle depending on the instantaneous input voltage applied. Thus, the switching frequency is varying within each AC half cycle with the lowest switching frequency at the peak of the AC input voltage and the highest switching frequency near the zero crossings of the input voltage. A new switching cycle starts immediately when the inductor current reaches zero.

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CrCM is also equivalent to quasi-resonant switching at first inductor current valley or QR1 operation. The switching period of CrCM operation is given by

$$T_{sw} = t_{cyc} = t_{on} + t_{off} \quad (1)$$

CrCM is ideal for full load operation, where the constant on-time is large. However, the constant on-time reduces at light load, resulting in very high switching frequency particularly near the zero crossings of the input voltage. The high switching frequency will increase the switching losses, resulting in poor efficiency at light load.

The new multimode PFC control algorithm implemented in IDP2308 can lower the switching frequency by adding an additional delay into each switching cycle through selecting further inductor current valleys to achieve QR2, QR3 and up to QR10 operation. In this way, the switching frequency is limited between a minimum and maximum value. The switching period of the multimode PFC operation, consisting of QR1 to QR10 operation and DCM, is given by

$$T_{sw} = t_{cyc} + t_w \quad (2)$$

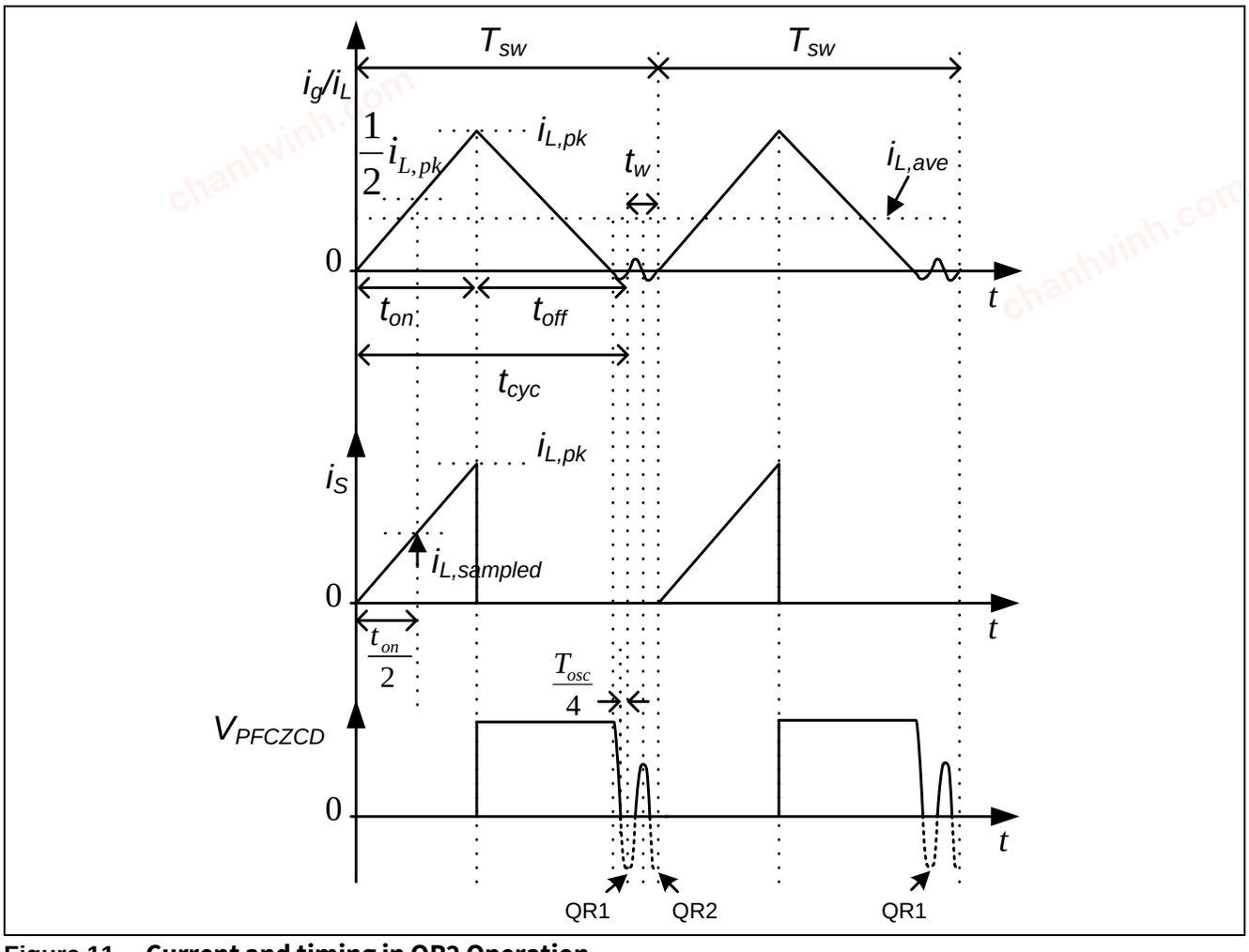

Figure 11 Current and timing in QR2 Operation

Introduction of the delay helps to reduce switching frequency but it also distorts the input current waveform and thus affects the PFC THD performance. The multimode PFC control also consists of an algorithm that optimizes the applied on-time on a cycle by cycle basis so as to ensure good input current shaping and improve PFC THD performance.

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3.4.3 PFC Protection

The PFC stage is protected against:

- PFC Open Control Loop Protection (PFCOCLP) (Chapter 3.4.3.1)
- PFC Inductor Over Current Protection (PFCOCP) (Chapter 3.4.3.2)
- PFC Output Over Voltage Protection (PFCOVP) (Chapter 3.4.3.3)
- PFC Output Redundant Over Voltage Protection (PFCROVP) (Chapter 3.4.3.4)
- PFC Output Under Voltage Protection (PFCUVP) (Chapter 3.4.3.5)
- PFC Brownin Protection for AC Input Line (PFCBID) (Chapter 3.4.3.6)
- PFC Brownout Protection for AC Input Line (PFCBOD) (Chapter 3.4.3.7)
- PFC Long Time Continuous Conduction Mode Protection (PFCCCMP) (Chapter 3.4.3.8)

3.4.3.1 PFC Open Control Loop Protection (PFCOCLP)

Open control loop is detected if the voltage value at pin VS is lower than the threshold $V_{_OlpPFC}$. This may happen in case that the voltage sensing loop is highside open circuit or the input voltage is too low. If open loop is detected at the IC startup, both the PFC and the HB LLC controller do not start up. If this open loop condition is detected during system operation, the system enters into auto restart mode.

3.4.3.2 PFC Inductor Over Current Protection (PFCOCP)

In the converter system, the peak current through the MOSFET is monitored via the PFC shunt resistor R_{PCS} to minimise stress for the MOSFET, the inductor L_{PFC} and the diode D_{PFC}. Once the voltage across the shunt resistor exceeds the over current threshold $V_{_CS0ocpset}$, the MOSFET gate is turned off. Afterwards, the ZCD signal, or the PFC maximal period time-out signal, initializes the next switching cycle. This protection mechanism is active in every switching cycle.

3.4.3.3 PFC Output Over Voltage Protection (PFCOVP)

A two stage overvoltage protection scheme is implemented where a slower average measurement of the bus voltage shall trigger a shutdown of the PFC under OVP1 of a lower threshold by firmware, and a faster immediate measurement of the bus voltage shall also trigger a shutdown of the PFC under OVP2 by hardware. For OVP1, if the average sensed PFC bus voltage exceeds the threshold $V_{_OvpSwSetPFC}$, the PFC will stop switching while the LLC continues to run. OVP2 is implemented by hardware. The threshold of this comparator is fixed at $V_{_OvpHwSetPFC}$ =2.8V. Once the sensed bus voltage exceeds this threshold for a configurable filter delay time, the PFC will stop switching while the LLC continues to run. Once the average sensed PFC bus voltage reduces and reaches the reference bus voltage $V_{_RefPFC}$, the PFC converter resumes normal operation.

3.4.3.4 PFC Output Redundant Over Voltage Protection (PFCROVP)

For ROVP, if the PFC bus voltage exceeds $V_{_ROVP_set}$, one ROVP count is recorded. The PFC will stop switching but the LLC continues to run. Once the average sensed PFC bus voltage reduces and reaches the reference bus voltage $V_{_ROVP_reset}$, the PFC converter resumes to normal operation. If another ROVP is recorded within $t_{_ROVP}$ (8s), it is recorded as 2nd ROVP count. The PFC will stop switching again but the LLC continues to run. However, the ROVP count will be reset to zero if a next ROVP event occurs after $t_{_ROVP}$ (8s). The $t_{_ROVP}$ (8s) starts counting when the last occurring ROVP event is triggered. Whenever the ROVP count accumulates to maximum ROVP count $n_{_ROVP}$ (10), the IC enters auto-restart mode.

In normal operations, the ROVP acts similar to the behavior of OVP1. When either OVP1 at VS pin or ROVP at MFIO pin is triggered, the same behavior occurs. In event that the OVP1 resistor divider has faulty resistance level, if VS voltage is lower, the PFC bus voltage would increase. In this case, the ROVP triggers to protect the system. Since

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the faulty resistance level remains unchanged, the ROVP will re-trigger again and again once the bus voltage drops to normal level when the switching is stopped and results in auto-restart mode.

This feature is disabled by default, which is selectable in the configurable parameters. Since the MFIO pin is a multifunction pin, not dedicated for high impedance bus voltage sensing, it is recommended to use the proposed solution with BSS127 shown in Figure 1 to ensure almost lossless ROVP function, not effecting standby performance.

3.4.3.5 PFC Output Under Voltage Protection (PFCUVP)

The PFC undervoltage protection (UVP) is a protection for the LLC converter from entering capacitive operation range. Since UVP is detected by sensing the PFC bus voltage, it is placed under PFC protection features. UVP is implemented by firmware. If the average sensed PFC bus voltage falls below a configurable UVP threshold $V_{_UvpSetPFC}$ for a blanking time of $t_{_UvpBlkPFC}$, PFC undervoltage is detected. PFC and LLC will stop switching.

3.4.3.6 PFC Brownin Protection for AC Input Line (PFCBIP)

PFC brownin protection is implemented by firmware and it utilizes HV pin for AC input voltage sampling for better input voltage measurement.

The desired brownin input voltage threshold is $V_{_HVBID}$. If $V_{ACrms} > V_{_HVBID}$, brown-in is detected and the system enters into startup.

3.4.3.7 PFC Brownout Protection for AC Input Line (PFCBOP)

The PFC brownout protection prevents the system from operating at very low input voltage that is out of the normal operating range. This helps to protect the system from high current stress or device failures at very low input voltage. PFC brownout protection is implemented by firmware and it utilizes HV pin for AC input voltage sampling for better input voltage measurement.

The desired brownout input voltage threshold is $V_{_HVBOD}$. If $V_{AC,rms} < V_{_HVBOD}$ and after a blanking time of $t_{_HVBODblank}$, brownout is detected. PFC will stop switching and LLC will continue switching.

3.4.3.8 PFC Long Time Continuous Conduction Mode Protection (PFCCCMP)

Continuous conduction mode (CCM) operation may occur during PFC startup for limited time duration. It is considered as a failure in the system only if CCM operation of the PFC converter is observed over a longer period of time. The PFC converter may run into CCM operation for a longer period due to shorted bypass diode, heavy load step that is out of specification or very low input voltage that is out of the normal operating range.

When CCM occurs, the magnetizing current in the PFC choke does not have a chance to decay to zero before the MOSFET turns on. There will be no quasi-resonant oscillation observed at the ZCD signal before the maximum switching period time-out is reached that turns the MOSFET on. This turn-on event without ZCD oscillation is monitored to protect the PFC converter from continuous CCM operation. The long time CCM protection is implemented by firmware.

At every sampling period, if the maximum switching period time-out occurs before any quasi-resonant oscillation is observed at the ZCD signal, the CCM time counter is increased by 1. If the PFC switching period is less than the time-out period, the CCM time counter is decreased by 1. Once the CCM time counter exceeds $t_{_CcmpPFC}$, the system enters into auto restart mode. The long time CCM protection is active only if the PFC on-time is above the threshold $t_{_OnMinPFC}$ by 200ns.

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3.5 Half-bridge LLC Controller

Following LLC functionality is described:

Table 6 Half-bridge LLC Controller Features

LLC Softstart (Time Controlled Oscillator TCO)	Chapter 3.5.1
LLC Normal Operation (Voltage Controlled Oscillator VCO)	Chapter 3.5.2
LLC Smooth Transition of Frequency Control From TCO to VCO	Chapter 3.5.3
LLC Half-bridge Protection	Chapter 3.5.4
LLC Open Control Loop Protection (LLCOCLP)	Chapter 3.5.4.1
LLC Over Load Protection (LLCOLP)	Chapter 3.5.4.2
LLC Over Current Protection Level 1 (LLCOCP1)	Chapter 3.5.4.3
LLC Over Current Protection Level 2 (LLCOCP2)	Chapter 3.5.4.4

3.5.1 LLC Softstart (Time Controlled Oscillator TCO)

The half-bridge LLC controller enters softstart for every VCC power up and upon recovering from certain protection mode provided the bus voltage is in the proper range. In softstart, the switching frequency changes with the elapsing time (a time controlled oscillator - TCO), as shown in Figure 12.

The switching frequency starts at a maximum value and decrease with a defined frequency step change at every 2ms. The initial frequency step change is larger and the frequency step change will gradually decrease at every 2ms until it reaches the minimum frequency step change value.

Once the softstart switching frequency is close to the switching frequency output of the free-running voltage controlled oscillator (VCO), the external secondary side LLC bus voltage controller and VCO will take over the regulation of the LLC output voltage. The LLC enters into normal operation.

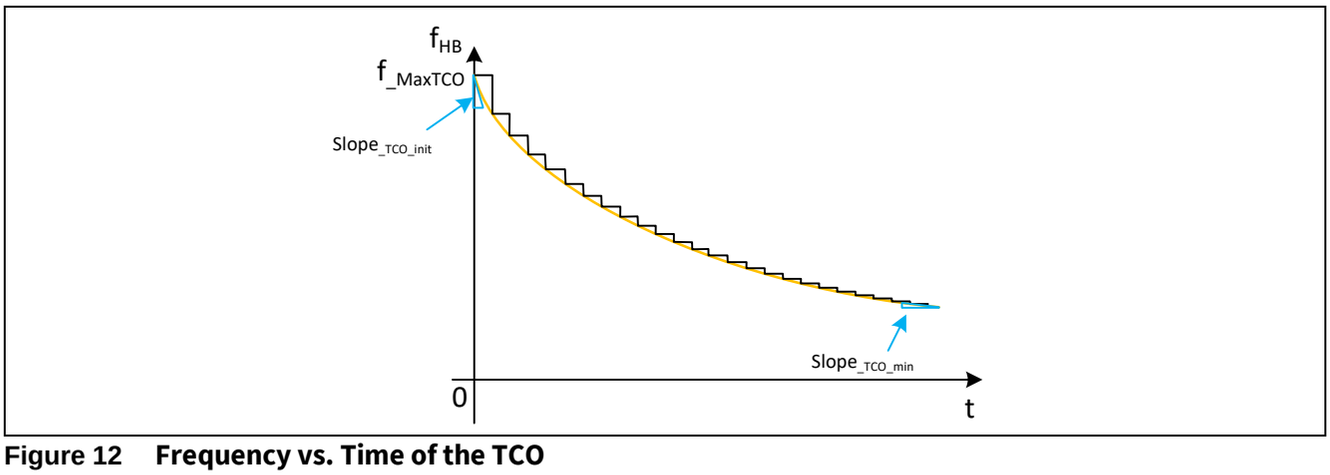

Figure 12 Frequency vs. Time of the TCO

3.5.2 LLC Normal Operation (Voltage Controlled Oscillator VCO)

During normal operation, a voltage controlled oscillator (VCO) generates the HB LLC converter switching frequency f_{HB} based on the HB feedback voltage V_{HBFB}. In this controller, the curve of the HB switching frequency f_{HB} in response to the feedback voltage V_{HBFB} is schematically shown as in Figure 13.

The VCO switching period vs. feedback voltage inside this controller consists of three pieces of direct line with different slew rate. As shown in Figure 13, the line in area II (normal operation) has much lower slew rate than the area I (Light Load) and III (Heavy Load). Therefore, the VCO in the area II has a much better frequency resolution than in the area I and III. In this way, fine frequency resolution around the nominal operating point

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V_{NomHB} is realized, while a wide operating frequency range can be covered with fast response to the load change in both heavy and light load is realized.

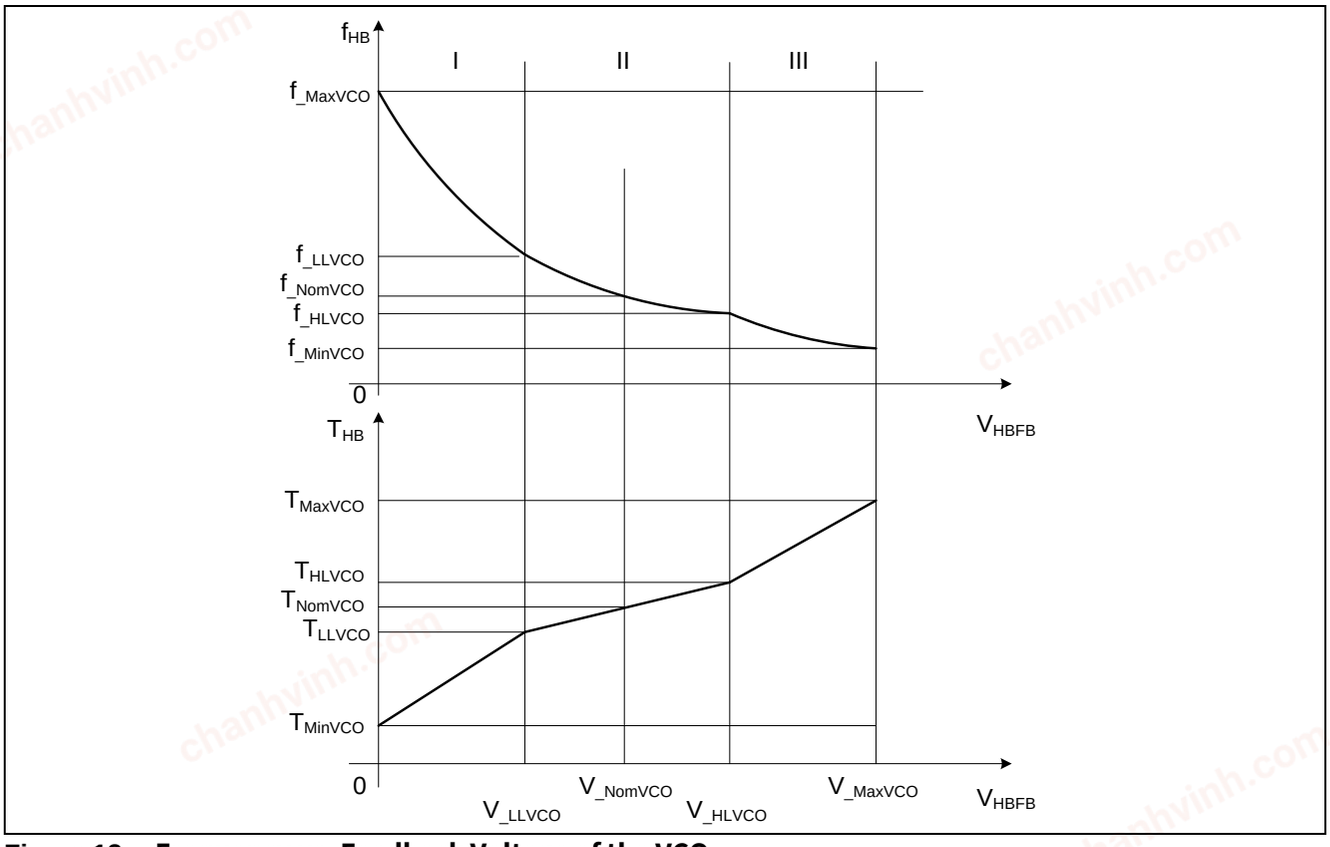

Figure 13 Frequency vs. Feedback Voltage of the VCO

The switching period curve is defined by following key points: feedback origin (0, T_{MinVCO}), VCO light load ($V_{_LLVCO}$, $T_{_LLVCO}$), VCO nominal point (V_{NomVCO}, T_{NomVCO}), VCO heavy load ($V_{_HLVCO}$, $T_{_HLVCO}$) and feedback maximal point ($V_{_MaxVCO}$, $T_{_MaxVCO}$). In this controller, all values are calculated based on the VCO nominal frequency $f_{_NomVCO}$ and nominal feedback voltage $V_{_NomVCO}$ with certain factors, as:

the minimal and maximal HB LLC switching frequency $f_{_MinVCO}$ and $f_{_MaxVCO}$:

$$f_{_MinVCO} = k_{fMinVCO} \cdot f_{_NomVCO} \quad (3)$$

$$f_{_MaxVCO} = k_{fMaxVCO} \cdot f_{_NomVCO} \quad (4)$$

the frequency at the corners:

$$f_{_HLVCO} = k_{fHLVCO} \cdot f_{_NomVCO} \quad (5)$$

$$f_{_LLVCO} = k_{fLLVCO} \cdot f_{_NomVCO} \quad (6)$$

and the feedback voltages:.

$$V_{_HLVCO} = k_{vHLVCO} \cdot V_{_NomVCO} \quad (7)$$

$$V_{_LLVCO} = k_{vLLVCO} \cdot V_{_NomVCO} \quad (8)$$

Once these points are defined, the switching period is calculated by a linear interpolation of the switching period to the feedback voltage, and the switching frequency curve over the whole feedback range is resulted, which is naturally non-linear function of the feedback voltage, as shown in Figure 13.

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For an optimal HB LLC operation, the frequency $f_{_NomVCO}$ should be set as the resonant frequency of the LLC resonant tank, while the respected feedback voltage $V_{_NomVCO}$ is taken at the middle of the regulation feedback range.

3.5.3 LLC Smooth Transition of Frequency Control from TCO to VCO

With built-in HB LLC softstart, the output voltage rises up smoothly and feedback voltage V_{HBFB} is available once the output voltage reaches in the regulation range. During the startup, LLC leaves the softstart mode and enters normal operation mode if the switching frequency determined by the VCO is equal to or higher than the switching frequency determined by the TCO, then the voltage controlled oscillator (VCO) takes over the frequency control.

3.5.4 LLC Half-bridge Protection

The LLC half-bridge is protected against:

- LLC Open Control Loop Protection (LLCOCLP) (Chapter 3.5.4.1)
- LLC Over Load Protection (LLCOLP) (Chapter 3.5.4.2)
- LLC Over Current Protection 1 (LLCOCP1) (Chapter 3.5.4.3)
- LLC Over Current Protection 2 (LLCOCP2) (Chapter 3.5.4.4)

In this controller, the HB LLC converter is protected against HB open loop and over load (OLP), over current

3.5.4.1 LLC Open Control Loop Protection (LLCOCLP)

Open control loop may happen due to open circuit in opto-coupler either at the diode or at the transistor, open circuit in HB feedback pin or the broken connection of the IC pin to the opto-coupler transistor source terminal. In this case, the HB feedback V_{HBFB} stays at high. After the end of the softstart, the averaged value of the feedback voltage V_{HBFB} over time period of $N_{_AccHB} * t_{_SrHB}$ is compared with the threshold $V_{_OlpHB}$. If the measured value is higher than the threshold for time $t_{_OlpHB}$, then the open loop protection is triggered and the whole system enters auto-restart mode. The system will be stopped and a time break $t_{_AR}$ follows. After this time break, the HB LLC converter restarts again with softstart. This is open loop protection.

3.5.4.2 LLC Over Load Protection (LLCOLP)

Over load at the HB LLC output during normal operation leads to rise of the feedback voltage V_{HBFB}. Once the averaged value of the feedback voltage V_{HBFB} over time period of $N_{_AccHB} * t_{_SrHB}$ is high than the threshold $V_{_OlpHB}$ for time $t_{_OlpHB}$, the over load protection is triggered and the HB controller, together with PFC, enters auto-restart mode. The HB LLC converter will be stopped and a time break $t_{_AR}$ follows. After this time break, the HB LLC converter restarts again with softstart.

3.5.4.3 LLC Over Current Protection Level 1 (LLCOCP1)

LLC OCP1 is implemented with hardware comparator and firmware handling and the condition is checked at every LLC switching. The voltage across the shunt resistor R_{HB} at the low-side MOSFET is sensed via the CS1 pin.

There are three different over current protection thresholds $V_{_Ocp1_norm}$, $V_{_Ocp1_burst}$ and $V_{_Ocp1_startup}$ to cover various operation conditions. The threshold $V_{_Ocp1_startup}$ is applied during startup, the threshold $V_{_Ocp1_burst}$ is applied during leaving burst mode transition to avoid the OCP1 mis-triggered and the relatively lower threshold $V_{_Ocp1_norm}$ is applied during normal operation.

If the voltage across the shunt resistor R_{HB} at the low-side MOSFET exceeds the OCP1 threshold, OCP1 protection is triggered to increase the current switching frequency t at rate of $t_{_Slope_after\ OCP1}$ to limit the power. The higher switching frequency results in reduced current flowing in the LLC tank and limits the output power transfer. If the sensed current falls below the OCP threshold, the LLC switching frequency starts to be reduced. At the point

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where the calculated LLC switching frequency based on the HBFB signal is higher than the switching frequency as defined by the OCP1 protection, the LLC converter resumes control under VCO.

If above scenario occurs continuously more than $N_{_Ocp1_max}$ times, then there will be a serious fault condition, IC will enter auto restart protection mode to protect the whole system. In the meantime, due to the limited power transfer during OCP1 protection, the open loop protection or overload protection could also be triggered to enter auto restart protection mode.

Table 7 LLC Overcurrent protection 1 parameters [1]

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
LLC OCP1 detection during startup [2]	$V_{Ocp1_startup}$	-	550	-	mV	[1] [3]
LLC OCP1 detection during leaving burst mode [2]	V_{Ocp1_burst}	-	750	-	mV	[1] [3]
LLC OCP1 detection during normal operation mode [4]	V_{Ocp1_norm}	-	427.5	-	mV	
Maximum overcurrent count for overcurrent protection to trigger	N_{Ocp1_max}	-	8	-	-	

[1] This setting is application specific and is changed accordingly for application. Please check setting when application varies.
[2] Voltage level triggered only during start up and burst mode.
[3] Parameter is not tested in production test.
[4] Applicable in normal operation only. Voltage level not triggered for soft-start and burst mode.

3.5.4.4 LLC Over Current Protection Level 2 (LLCOCP2)

LLC OCP2 could be triggered by a large primary side current through the shunt resistor. OCP2 is implemented by hardware via the OCP2 comparator. The status of OCP2 hardware can be read by firmware to detect if OCP2 event has occurred for subsequent action to be taken. If the voltage across the shunt resistor is higher than the threshold V_{Ocp2}, the system enters into auto restart mode.

3.6 Operation Flow

In this chapter the control flow of the IC are described. Operating flowchart is shown in Figure 14.

- IC Initialization (Section 4.6.1)
- Operation flow of the PFC Controller (Section 4.6.2)
- Operation flow of the HB LLC Controller (Section 4.6.3)

3.6.1 IC Initialization

As mentioned previously, once the VCC is above the turn-on threshold, the IC is active. The IC enters initialization state immediately after the VCC is powered up. In the initialization state, the correct setup values are assigned to the control units and then both PFC and HB are enabled. Also refer to Figure 5 for scheduler.

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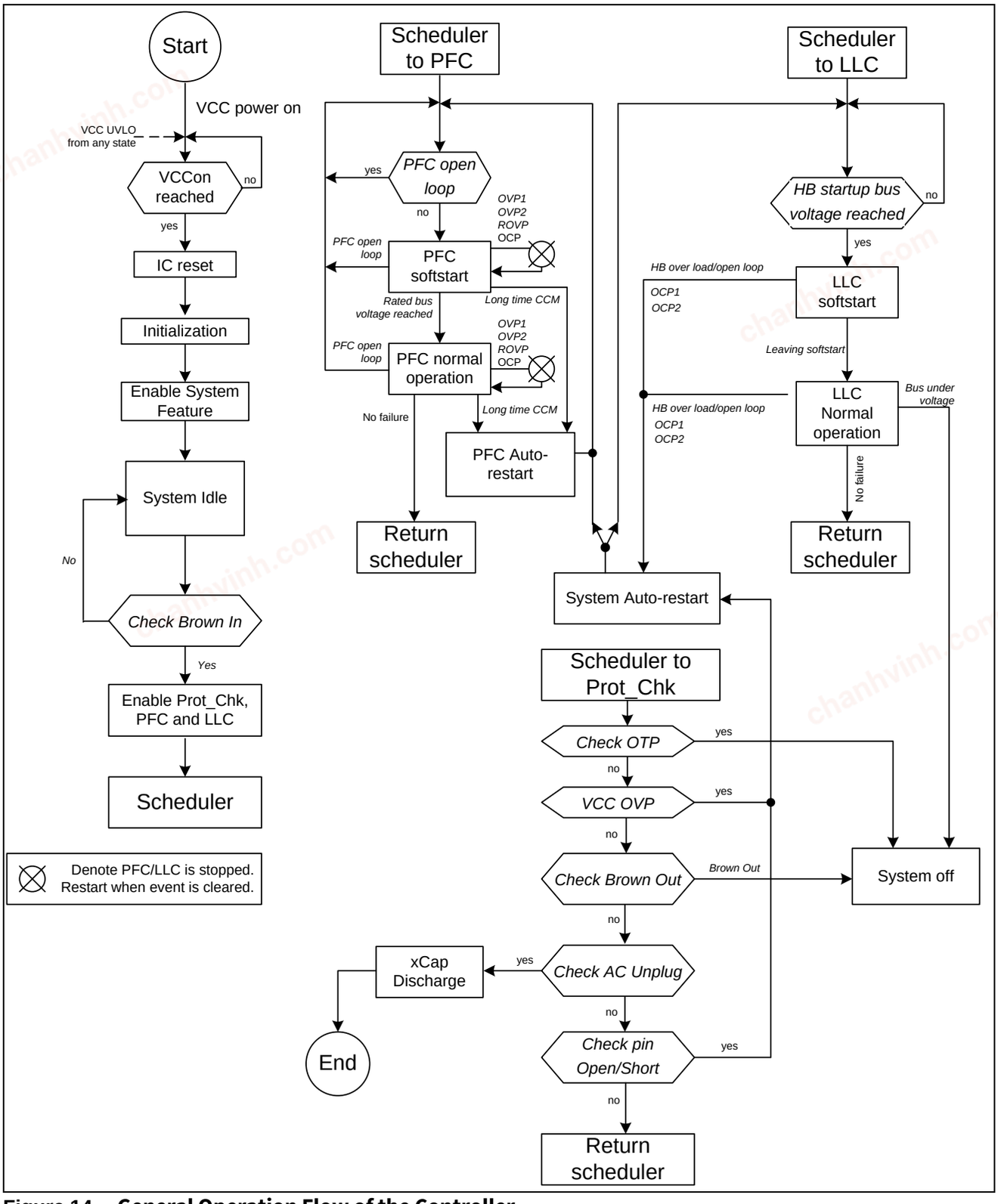

Figure 14 General Operation Flow of the Controller

3.6.2 Operation Flow of the PFC Controller

If the PFC is disabled, there is no sensing of any PFC related signal and no switching of the PFC gate driver, the PFC MOSFET gate is actively pulled down to ground.

Once the PFC is enabled, the bus voltage is checked against open loop. If no open loop is detected, the PFC begins its operation with softstart.

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During PFC softstart, the PFC starts its operation according to the sensed signals at ZCD, CS0, and VS. The voltage control loop (PI regulator) is kept fast enough and the integrator of the PI regulator growth is limited to avoid output voltage overshoot. As soon as the bus voltage is getting close to the rated value, the PFC enters normal operation state where it is regulated to improve the power factor.The bus voltage is regulated to its rated value.

From the PFC protections, OCP does not cause any break of the PFC converter operation but OVP1 and OVP2 will cause a short break of the PFC operation. After the bus voltage comes back to the rated value, the PFC resumes its operation immediately. In case of long time CCM operation, the PFC enters auto-restart state. After the auto-restart time break, the PFC restarts with softstart.

3.6.3 Operation Flow of the Halfbridge LLC Controller

If the HB LLC is disabled, there is no sensing of any HB LLC converter related signal and no switching of the high and low side gate driver. The MOSFET gates are actively pulled down to ground.

Once the HB LLC is enabled, the controller checks the bus voltage against the HB startup bus voltage V_{HBstrt}. After the HB startup voltage at the PFC bus is reached, the HB LLC controller enters softstart state. In this state, the HB LLC converter switching frequency is controlled by TCO and decreases with time. The output will be built up and feedback signal should be available within the softstart time, t_{ss_max}. Once the feedback voltage reaches a certain value that the frequency determined by VCO is equal to current frequency determined by the TCO, the controller enters normal operation state, feedback signal is then used for the output regulation by the VCO.

Some failures may stop the HB operation and lead the controller back to valid bus voltage check, i.e. by bus under voltage, or the softstart state after the HB auto-restart time break, i.e. by open loop or over load. In case of the over current protection 2 (OCP2), the HB LLC converter enters system auto-restart mode.

A comprehensive set of protection is integrated inside this controller for PFC and HB LLC converter. Some of them have just influence on the PFC or HB LLC only while some have influence on the other part of the controller. This information is summarized as in the Table 8 and Table 9.

Table 8 PFC Protections If Enabled

Protection	Effect on PFC converter	Effect on HB converter
Bus over voltage protection 1	$V_{VS} > V_{_OvpSwSetPFC}$: blocks gate signal; $V_{VS} < V_{_RefPFC}$: releases gate signal	no influence
Bus over voltage protection 2	$V_{VS} > V_{_OvpHwSetPFC}$: blocks gate signal $V_{VS} < V_{_RefPFC}$: releases gate signal	no influence
Bus under voltage	$V_{VS} < V_{_UvpSetPFC}$: stops operation	$V_{VS} < V_{UvpSetPFC}$: LLC continues switching
VS open loop protection	$V_{VS} < V_{_OlpPFC}$ for : no startup of PFC	no start up
PFC over current protection	$V_{CS0} > V_{_CS0ocpSet}$ for $t_{_OcpLebPFC}$: stops gate immediately; next gate turn-on triggered by ZCD or $t_{_maxPFC}$	no effect
PFC minimal on-time	PFC on time from regulator $t_{on} < t_{_OnMinPFC}$: blocks PFC gate signal; $t_{on} > t_{_OnMinPFC}$: releases PFC gate signal	no effect
PFC maximal on-time	$t_{on} > t_{_OnMaxPFC}$: $t_{on} = t_{OnMaxPFC}$	no effect
PFC Brownin	$V_{ACrms} > V_{_HVBID}$: Enters startup	no effect
PFC Brownout	$V_{ACrms} < V_{_HVBOD}$: After a blanking time of $t_{_HVBODblank}$, stops PFC operation	LLC continues switching
PFC long time CCM protection	CCM operation for longer than $t_{_CcmpPFC}$: system Auto-restart	

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Table 9 LLC Protections If Enabled

Protection	Effect on PFC converter	Effect on HB converter
HB over current protection 1	$V_{CS1} > V_{_OCP1}$ for $N_{_Ocp1_max}$: system Auto-restart	
HB over current protection 2	$V_{CS1} > V_{_OCP2}$: system Auto-restart	
HB open control loop protection	$V_{HBFB} > V_{_OlpHB}$ for $t_{_OlpHB}$: system Auto-restart	
HB over load protection		

3.7 Overview Protection Features

The following table provides an overview about the complete protection feature set. The corresponding default actions are listed for the cases where a protection feature is triggered.

If the application requires different behavior for the items in the table 8, please contact Infineon representatives.

Table 10 Overview Protection Features

Protection Fatures	Symbol	Default Action	Description
Undervoltage Lockout for VCC	ULVO	PFC and LLC stop switching	Chapter 3.7.1
Overvoltage Protection for VCC	VCCOVP	Auto restart	Chapter 3.7.2
Overtemperature Protection by means of internal Temperature Detection	OTP	Latch	Chapter 3.7.3
PFC Open Control Loop Protection	PFCOCLP	Auto restart	Chapter 3.4.3.1
PFC Inductor Over Current Protection	PFCOCP	PFC turns off switch immediately	Chapter 3.4.3.2
PFC Output Over Voltage Protection	PFCOVP	PFC stops switching	Chapter 3.4.3.3
PFC Output Redundtant Over Voltage Protection	PFCROVP	Auto restart	Chapter 3.4.3.4
PFC Output Under Voltage Protection	PFCUVP	PFC stops switching while LLC continues switching	Chapter 3.4.3.5
PFC Brownin Protection for AC Input Line (PFCBIP)	PFCBIP	IC starts switching operation after threshold exceeded	Chapter 3.4.3.6
PFC Brownout Protection for AC Input Line	PFCBOP	PFC stops switching while LLC continues switching	Chapter 3.4.3.7
PFC Long Time Continuous Conduction Mode Protection	PFCCMP	Auto restart	Chapter 3.4.3.8
LLC Open Control Loop Protection	LLCOCLP	Auto restart	Chapter 3.5.4.1
LLC Over Load Protection	LLCOLP	Auto restart	Chapter 3.5.4.2
LLC Over Current Protection 1	LLCOCP1	Frequency increases	Chapter 3.5.4.3
LLC Over Current Protection 2	LLCOCP2	Auto restart	Chapter 3.5.4.4

3.7.1 Undervoltage Lockout for VCC

There is an undervoltage lockout unit (UVLO) implemented, that ensures a defined enabling and disabling of the IC operation depending on the supply voltage at pin VCC. The UVLO contains a hysteresis with the voltage thresholds V_{VCCon} for enabling the IC and V_{VCCoff} for disabling the IC.

Once the mains input voltage is applied, a current is flowing through an external resistor into pin HV via the integrated diode to pin VCC. The IC is enabled once VCC exceeds the threshold V_{VCCon} and enters normal operation if no fault condition is detected. In this phase V_{VCC} will drop until the self supply via the auxiliary winding takes

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over the supply at pin VCC. The self supply via the auxiliary winding must be therefore in place before V_{VCC} undershoots the V_{VCCoff} threshold.

3.7.2 Overvoltage Protection for VCC

There is an over voltage detection at pin VCC implemented. The detection function consists of a threshold $V_{_VCCOVP}$ and a blanking time of $t_{_VCCOVP}$. The IC is disabled once the overvoltage protection is triggered at pin VCC.

3.7.3 Overtemperature Protection by means of internal Temperature Detection

There is an over temperature protection implemented, that initiates a thermal shutdown once the internal temperature level $T_{_OTP}$ is exceeded. Subsequently system enters latch mode, and only VCC recycle can restart the system.

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3.8 Fixed and Configurable Parameters

In this chapter all the fixed and configurable parameters are shown. The list of parameters shown in the following tables is default value and has been verified in a reference design system.

3.8.1 Fixed Parameters

The below parameters are fixed and cannot be changed.

Table 11 General Parameters

Parameter Symbol	Parameter Description	Pin	Fixed Value	Unit
$V_{_VCCOVP}$	VCC OVP	VCC	23.5	V
$t_{_HVBODBlank}$	AC brownout blanking time	-	120	ms
$T_{_OTP}$	IC OTP	-	125	°C

Table 12 PFC Parameters

Parameter Symbol	Parameter Description	Pin	Fixed Value	Unit
$V_{_OlpPFC}$	PFC open loop	VS	0.39	V
$V_{_startup}$	PFC startup voltage	VS	0.59	V
$V_{_RefPFC}$	PFC control_normal	VS	2.45	V
$t_{_ZCDfilter}$	PFC ZCD filter time	ZCD	160	ns
$t_{_ringsup}$	PFC Ringing suppression time	ZCD	400	ns
$n_{_valley_min}$	Minimum PFC valley number for multimode operation	-	1	-
$n_{_valley_max}$	Maximum PFC valley number for multimode operation	-	10	-
$t_{_CcmpPFC}$	PFC Blanking time for CCM protection	-	60	ms
$t_{_maxPFC}$	PFC max switching periodtosc	-	40	µs
$t_{_OcpLebPFC}$	Blanking time for PFC OCP	CS0	0	s

Table 13 LLC Parameters

Parameter Symbol	Parameter Description	Pin	Fixed Value	Unit
$Step_{_LLC_VCO_decrease}$	LLC VCO frequency decrement step	HBFB	3	$1/f_{MCLK}$
$Step_{_LLC_VCO_increase}$	LLC VCO frequency increment step	HBFB	20	$1/f_{MCLK}$
$t_{_Ocp1_leb}$	LLC LEB of OCP1	CS1	0.4	µs
$t_{_Ocp2_filter}$	LLC noise blanking CS1 OCP2	CS1	110	ns
$Slope_{_after\ OCP1}$	LLC softstart slope after OCP1 event	CS1	80	ns/32µs
$V_{_burst_on}$	LLC HBFB voltage burst on in burst mode	HBFB	1.65	V
$t_{_Ocp1_blk_Leave_burst}$	LLC OCP1 blanking time during burst mode to normal mode transition	CS1	200	ms
$t_{_ss_max}$	LLC max. soft start duration	-	131	ms

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3.8.2 Configurable Parameters

Table 14 The below parameters are defined and can be configured.General Parameters

Parameter Symbol	Parameter Description	Pin	Default	Range	Unit
$V_{_HVBID}$ [1]	AC brownin	HV	70	1 ~ 255	Vac
$V_{_HVBOD}$ [1]	AC brownout	HV	60	1 ~ 255	Vac
$t_{_AR}$	Auto restart break time	-	2	0.01~2.08	s
$t_{_VCCOVP}$	VCC OVP blanking time	-	9	1~17	ms

[1] AC brownin/brownout is based on R_{HV} 51kΩ

Table 15 PFC Parameters

Parameter Symbol	Parameter Description	Pin	Default	Range	Unit
$V_{_GD0H}$ [1]	PFC GD0 drive voltage	GD0	10.5	4.5 ~ 15	V
$I_{_GD0H}$ [1]	PFC GD0 drive current	GD0	0.156	0.087 ~ 0.36	A
$V_{_UvpSetPFC}$	PFC bus under voltage	VS	1.77	0.1 ~ 2.3	V
$V_{_RefPFC_burst}$	PFC control_burst	VS	2.2	0.1 ~ 2.3	V
$V_{_HBstrt}$	LLC enter soft start	VS	2.05	0.1 ~ 2.3	V
$t_{_UvpBlkPFC}$	PFC blanking time for bus under voltage	VS	3	0.128 ~ 8388	ms
$t_{_ovc}$	PFC over voltage comparator filter time	VS	10000	0 ~ 31500	ns
$V_{_OvpSwSetPFC}$	PFC bus over voltage	VS	2.572	2 ~ 2.8	V
$V_{_OvpSwClearPFC}$	PFC bus over voltage clear	VS	2.45	2 ~ 2.8	V
$V_{_CS0ocpSet}$ [2]	PFC over current	CS0	0.6	0.05 ~ 1.15	V
$f_{_sw_max_pfc}$	PFC max switching frequency	-	120	1 ~ 300	kHz
$f_{_sw_min_pfc}$	PFC min switching frequency	-	60	1 ~ 300	kHz
$svp_{_startup}$	PFC PIT1 P-coe during startup	-	4	0 ~ 7	-
Svp	PFC PIT1 P-coe	-	6	0 ~ 7	-
Svi	PFC PIT1 I-coe	-	7	0 ~ 7	-
Svt	PFC PIT1 T-coe	-	4	0 ~ 7	-
$t_{_OnMinPFC}$	PFC min on time	-	0.1	0.016 ~ 63.98	µs
$t_{_OnMaxPFC}$	PFC max on time	-	20	0.016 ~ 63.98	µs

[1] Refer to 5.4.6 for limits

[2] Refer to 5.4.4 for limits

Table 16 LLC Parameters

Parameter Symbol	Parameter Description	Pin	Default	Range	Unit
$V_{_GD1H}$ [1]	LLC GD1 drive voltage	GD1	10.5	4.5 ~ 15	V
$I_{_GD1H}$ [1]	LLC GD1 drive current	GD1	0.12	0.026 ~ 0.12	A
$V_{_Ocp1_norm}$ [1]	LLC OCP1 during steady state	CS1	0.4275	0.05 ~ 1.15	V
$V_{_Ocp1_start}$ [1]	LLC OCP1 during softstart	CS1	0.55	0.05 ~ 1.15	V
$V_{_Ocp1_burst}$ [1]	LLC OCP1 during burst mode	CS1	0.75	0.05 ~ 1.15	V
$N_{_Ocp1_max}$	LLC max number of OCP1 events	CS1	8	1 ~ 255	-
$f_{_Ocp1}$	LLC switching frequency during OCP1	CS1	200	100 ~ 600	kHz
$V_{_burst_enter}$	LLC HBFB voltage when entering a burst mode	HBFB	0.3	0.1 ~ 2.3	V
$V_{_burst_exit}$	LLC HBFB voltage when exiting burst mode	HBFB	2.05	0.1 ~ 2.3	V

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Parameter Symbol	Parameter Description	Pin	Default	Range	Unit
$V_{_OlpHB}$	LLC open-loop / overload protection	HBFB	2	0.1 ~ 2.3	V
$V_{_HLVCO}$	LLC VCO heavy load voltage	HBFB	2	0.1 ~ 2.3	V
$V_{_LLVCO}$	LLC VCO light load voltage	HBFB	0.45	0.1 ~ 2.3	V
$f_{_MaxVCO}$	LLC VCO max frequency	-	250	1 ~ 300	kHz
$f_{_LLVCO}$	LLC VCO light load frequency	-	140	1 ~ 300	kHz
$f_{_NomVCO}$	LLC nominal operating frequency	-	100	1 ~ 300	kHz
$f_{_HLVCO}$	LLC VCO heavy load frequency	-	85	1 ~ 300	kHz
$f_{_MinVCO}$	LLC VCO minimal frequency	-	82	1 ~ 300	kHz
$f_{_sw_burst_start}$	LLC starting frequency in burst mode	-	200	80 ~ 300	kHz
$f_{_sw_burst_stop}$	LLC ending frequency in burst mode	-	200	80 ~ 300	kHz
$f_{_sw_burst}$	LLC switching frequency during burst mode	-	130	50 ~ 200	kHz
$f_{_MaxTCO}$	LLC max. soft start frequency	-	270	100 ~ 300	kHz
$t_{_Ocp1_blk_startup}$	LLC OCP1 blanking time from startup threshold to low threshold during startup	-	200	0.032 ~ 2097	ms
$t_{_Ocp1_release}$	LLC releasing OCP1 lapse time	CS1	100	0.032 ~ 2097	ms
$t_{_Ocp1_filter}$	LLC blanking filter time CS1 OCP1	CS1	0	0 ~ 984	ns
$t_{_blk_Ocp2}$	LLC blanking time for OCP2	CS1	0	0 ~ 984	ns
$t_{_dead_llc}$	LLC dead time	-	0.5	0.0157 ~ 0.984	µs
$t_{_OlpHB}$	LLC blanking time before open-loop / overload protection	-	100	0.032 ~ 2097	ms
$t_{_blk_burst}$	Blanking time to enter burst mode	-	20	0.032 ~ 2097	ms
$t_{_burst_off_min}$	Minimum burst off time		0.1	0.08 ~ 20.4	ms
$Slope_{_TCO_init}$	LLC initial slope during soft start	-	0.85	0.0157 ~ 3.984	µs /128 µs
$Slope_{_TCO_min}$	LLC min slope during soft start	-	0.36	0.0157 ~ 3.984	µs /128 µs
$N_{_burst_sstart}$	LLC soft start steps	-	4	1 ~ 218	-
$N_{_burst_sstop}$	LLC soft stop steps	-	4	1 ~ 218	-
$T_{_burst_on_max}$	LLC burst on time (excluding soft stop time)	-	160	32 ~8160	us
$Slope_{_burst_leave}$	LLC slope of soft start when leaving burst mode	HBFB	0.32	0.0157 ~ 3.984	µs /128 µs
$T_{High_limit\ Burst_off_time}$	High limit of burst off time for adaptive minimum frequency during burst on	-	120	20 ~ 200	ms

[1] Refer to 5.4.6 for limits

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4 Electrical Characteristics

All signals are measured with respect to ground pin GND, except the highside signals at pins HSVCC and HSGD, which are measured with respect to pin HSGND. The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note : Stresses above the values listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.These values are not tested during production test. For the same reason make sure that any capacitors that will be connected to pins VCC and HSVCC are discharged before assembling the application circuit.

Table 17 Absolute Maximum Ratings

Parameters	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltage externally supplied to pin VCC	V_{VCCEXT}	- 0.5	26	V	
Voltage at pin GDx	V_{GDx}	-0.5	V_{VCC} + 0.3	V	
Junction temperature	T_J	- 40	125	°C	
Storage temperature	T_S	- 55	150	°C	
Soldering temperature	T_{SOLD}	—	260	°C	Wave Soldering [1]
Latch-up capability	I_{LU}	—	150	°C	[2] Pin voltages acc. to abs. max. ratings
ESD capability HBM	V_{HBM}	—	2000	V	[3]
ESD capability CDM	V_{CDM}	—	500	V	[4]
Input Voltage Limit for pin MFIO, HBFB, VS, CS, ZCD	V_{IN_DC}	- 0.5	3.6	V	
Maximum permanent clamping current for pin ZCD and CS	$-I_{CLN_DC}$	—	2.5	mA	RMS
Maximum transient clamping current for pin ZCD and CS	$-I_{CLN_TR}$	—	10	mA	pulse < 500ns
Maximum negative transient input voltage for ZCD	$-V_{IN_ZCD}$	—	1.5	V	pulse < 500ns
Maximum negative transient input voltage for CS	$-V_{IN_CS}$	—	3.0	V	pulse < 500ns
Maximum permanent positive clamping current for CS	I_{CLP_DC}	—	2.5	mA	RMS
Maximum transient positive clamping current for CS	I_{CLP_TR}	—	10	mA	pulse < 500ns
Maximum voltage at pin HV	V_{HV}	- 0.3	600	V	
Maximum current at pin HV	I_{HV}	—	10	mA	
Voltage at pins HSVCC, HSGD and HSGND	V_{HSx}	-650	+650	V	Isolation voltage, referred to IC GND

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[1] According to JESD22-A111 Rev A.
[2] Latch-up capability according to JEDEC JESD78D, TA= 85°C.
[3] ESD-HBM according to ANSI/ESDA/JEDEC JS-001.
[4] ESD-CDM according to JESD22-C101F.

4.2 Package Characteristics

Table 18 Package Characteristics

Parameters	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Thermal resistance	R_{thJA}	—	119	K/W	
Creepage distance HV vs. GND-related pins.	D_{CRHV}	2.1	—	mm	
Creepage distance HSGND vs. GND-related pins	D_{CRHS}	2.1	—	mm	

4.3 Operating Conditions

Table 19 Operating Range

Parameters	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Junction Temperature	T_J	-40	125	°C	
Lower VCC limit	V_{VCC}	V_{UVOFF}	—	V	device is held in reset when $V_{VCC} < V_{UVOFF}$
Voltage externally supplied to VCC pin	V_{VCCEXT}	—	24	V	maximum voltage that can be applied to pin VCC by an external voltage source
Gate driver pin voltage	V_{GD}	-0.5	V_{VCC} + 0.3	V	

4.4 DC Electrical Characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range, T_J from -40 °C to +125 °C.

Typical values represent the median values related to T_A = 25 °C. All voltages refer to GND, and the assumed supply voltage is V_{VCC} = 18 V, if not specified otherwise.

Not all values given in the tables are tested during production test. The values not tested are explicitly marked.

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4.4.1 Power Supply Characteristics

Table 20 Electrical Characteristics of the Power Supply

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
VCC Turn_On threshold	V_{VCCon}	19	20.5	22	V	dV_{CC}/dt = 0.2 V/ms
VCC active current in normal mode with open gates	$I_{VCCactive}$	—	18	—	mA	
VCC Turn_Off [1] threshold	V_{VCCoff}	7.12	7.5	7.88	V	
VCC Tun_Off [1] threshold in burst off mode [2]	$V_{VCCoff_burst_off}$	9.97	10.5	11.03	V	VCC Tun_Off [1] threshold in burst off mode [2]
VCC quiescent current in burst off mode [2], not include current drawn from HBFB pin [3]	$I_{VCC_burst_off}$	—	0.6	1.4	mA	$T_j \leqslant 85°C$
		—	—	3.3	mA	$T_j \leqslant 125°C$
IC Power down threshold	V_{VCC_PD}	5.7	6	6.3	V	
VCC quiescent current in Power down mode	I_{VCC_PD}	5	20	40	µA	$V_{VCC} < V_{VCC_PD}$(min) – 0.3V

[1] VCC Turn_Off means IC is in UVLO mode and the startup cell is turned on.

[2] Burst on and burst off mode are both in burst mode while the current consumption of the IC is same as in normal mode during burst on mode and the processor is turned off in burst off mode (refer to Figure 4).

[3] Total current in burst off mode = $I_{VCC_burst_off} + V_{HBFB_open}/R_{HBFB_PU}$, refer to Figure 3 for internal connection of HBFB pin.

4.4.2 Characteristics of the MFIO Pin

Table 21 Electrical Characteristics of the MFIO Pin

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Output low voltage	V_{OL}	—	—	0.8	V	I_{OL} = 2 mA
Output high voltage	V_{OH}	2.2	—	—	V	I_{OH} = –2 mA
Output sink current	I_{OL}	—	—	2	mA	
Output source current	$-I_{OH}$	—	—	2	mA	
Output rise time (0 → 1)	t_{RISE}	—	—	25	ns	20 pF load, push/pull output [1]
Output fall time (1 → 0)	t_{FALL}	—	—	25	ns	20 pF load, push/pull or open-drain output [1]

[1] Not tested in production test.

4.4.3 Characteristics of the HBFB Pin

Table 22 Electrical Characteristics of the HBFB Pin [1]

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
HBFB open voltage	V_{HBFB_open}	3.04	3.20	3.36	V	
Pull-up resistor	R_{HBFB_PU}	—	9	—	kΩ	
Pull-up resistor tolerance	ΔR_{HBFB_PU}	—	—	± 20	%	

[1] Not tested in production test.

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4.4.4 Characteristics of the Current Sense Inputs CSx

Table 23 Electrical Characteristics of the CSx Pin

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
OCP2 threshold voltage	V_{OCP2}	—	1.2	—	V	
OCP2 threshold tolerance	Δ_{VOCP2}	—	—	±5	%	voltage divider tolerance
OCP, OCP1 threshold tolerance	ΔV_{OCP1}	—	—	±6.2	%	
Delay from V_{CSx} crossing $V_{CSxOCP1}$ to CSx_OCP1 rising edge, 1.2V range	t_{CSOCP1}	20	320	620	ns	[1] input signal slope dV_{CS}/dt = 10 mV/µs [2]
		90	170	250	ns	[1] input signal slope dV_{CS}/dt = 150mV/µs [2]
		90	140	210	ns	[1] input signal slope dV_{CS}/dt = 300mV/µs [2]

[1] Not tested in production test.

[2] This slope represents a use case of a switch-mode power supply with minimum input voltage.

4.4.5 Characteristics of the Zero Crossing Input ZCD

Table 24 Zero-Crossing Comparator Characteristics

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Zero-crossing threshold	V_{ZCTHR}	15	40	70	mV	
Comparator propagation delay	t_{ZCPD}	30	50	70	ns	dV_{ZCD}/dt = 4V/µs
Input voltage negative clamping level	$-V_{INPCLN}$	140	180	220	mV	

4.4.6 Characteristics of the Gate Driver Pins GDx

Table 25 Electrical Characteristics of the Gate Driver Pins GD0 and GD1

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
APD low voltage (Active Pull Down while device is not powered or gate driver is not enabled)	V_{APD}	—	—	1.6	V	I_{GDx} = 5mA [1]
R_{PPD} tolerance	ΔR_{PPD}	—	—	± 25	%	permanent pull-down resistor inside gate driver
Driver Output low impedance for GD0	R_{GDL}	—	—	4.4	Ω	$T_J \leq$ 125°C, I_{GD} = 0.1 A
Driver Output low impedance for GD1	R_{GDL}	—	—	7.0	Ω	$T_J \leq$ 125°C, I_{GD} = 0.1 A
Output voltage tolerance	ΔV_{GDxH}	—	—	±5	%	tolerance of programming options if V_{GDH} > 10V

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Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Rail-to-rail output high voltage	V_{GDxHRR}	V_{VCC} - 0.5	—	V_{VCC}	V	if V_{VCC} < programmed V_{GDH} and output at high state
Output high current tolerance in PWM mode	ΔI_{GDxH}	—	—	±15	%	
Discharge current for GD0	I_{GD0DIS}	800	—	—	mA	V_{GD} = 4 V and driver at low state [1]
Discharge current for GD1	I_{GD1DIS}	500	—	—	mA	V_{GD} = 4 V and driver at low state [1]
Output low reverse current	$-I_{GDREVL}$	—	—	100	mA	applies if V_{GD} < 0 V and driver at low state [1]
Output high reverse current in PWM mode	I_{GDREVH}	—	1/6 of I_{GDH}	—	mA	applies if V_{GDxH} < V_{GD} and driver at high state [1]

[1] Not tested in production test

4.4.7 Characteristics of the High-Voltage Pin HV

Table 26 Electrical Characteristics of the HV PIN

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Leakage current at HV pin	I_{HVleak}	—	—	10	µA	V_{HV} = 600 V HV startup cell off
Resistor value for bleeding path	$R_{HV_discharge}$	200	—	1000	Ω	Overall resistance between VIN to GND
Current charging capability for VCC cap.	I_{LD}	3.2	5	7.5	mA	V_{VCC} < V_{VCCon} -0.3V

4.4.8 Characteristics of the VS Pin

Table 27 Electrical Characteristics of the VS pin

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input leakage current, no pull device	$\|I_{LK}\|$	—	—	200	nA	$V_{VS} \leqslant$ 2.9V [1]
PFC Overvoltage protection 2, OVP2	$V_{OvpHwSetPFC}$	2.70	2.8	2.90	V	

[1] Pad leakage verified with guard bands at T_A = 25°C.

4.4.9 Characteristics of the HSGD Pin

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range, T_J from -40 °C to +125 °C. Typical values represent the median values related to T_J = 25 °C. All voltages refer to HSGND, and the assumed supply voltage is V_{HSVCC} = 14 V, if not specified otherwise.

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Table 28 Electrical Characteristics of the HSGD pin

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Operating voltage range	V_{HSVCC}	—	—	24	V	lower limit defined by $V_{HSVCCon}$, $V_{HSVCCoff}$
HSVCC turn on threshold	$V_{HSVCCon}$	8.7	9.2	9.7	V	
HSVCC turn off threshold	$V_{HSVCCoff}$	6.2	6.7	7.2	V	
HSVCC turn on/off hysteresis	$V_{HSVCChy}$	2	2.5	3	V	
Output voltage at low state	$V_{HSGDlow}$	—	25	100	mV	I_{HSGD} = 20 mA (sink)
		—	125	500	mV	I_{HSGD} = 100 mA (sink)
	$-V_{HSGDlow}$	—	25	100	mV	I_{HSGD} = -20 mA (src)
Output voltage at high state	$V_{HSGDhigh}$	10	11	12	V	I_{HSGD} = -20 mA (src)
		7	—	—	V	I_{HSGD} = -20 mA (src) V_{HSVCC} = 8 V
Output voltage at active shutdown	$V_{HSGDuvlo}$	—	25	200	mV	I_{HSGD} = 20 mA (sink) V_{HSVCC} = 5 V
Output low impedance	R_{HSGDLS}	—	—	5	Ω	I_{HSGD} = 20 mA (sink)
Peak source current	$I_{HSGDpksrc}$	0.13	—	0.52	A	[1]
Peak sink current	$-I_{HSGDpksnk}$	0.45	—	1.3	A	[1]
Output low reverse current	$-I_{HSGDREVL}$	—	—	100	mA	applies if V_{HSGD} < 0 V and driver at low state [1]
Rising time 2V < V_{HSGD} < 8V	$t_{HSGDrise}$	20	60	140	ns	C_{LOAD} = 3.3 nF, R_{LOAD} = 6.8 Ω [1]
Falling time 8V > V_{HSGD} > 2V	$t_{HSGDfall}$	4	20	40	ns	C_{LOAD} = 3.3 nF, R_{LOAD} = 6.8 Ω [1]

[1] Not tested in production test

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5 Outline Dimensions and Marking

5.1 Outline Dimensions

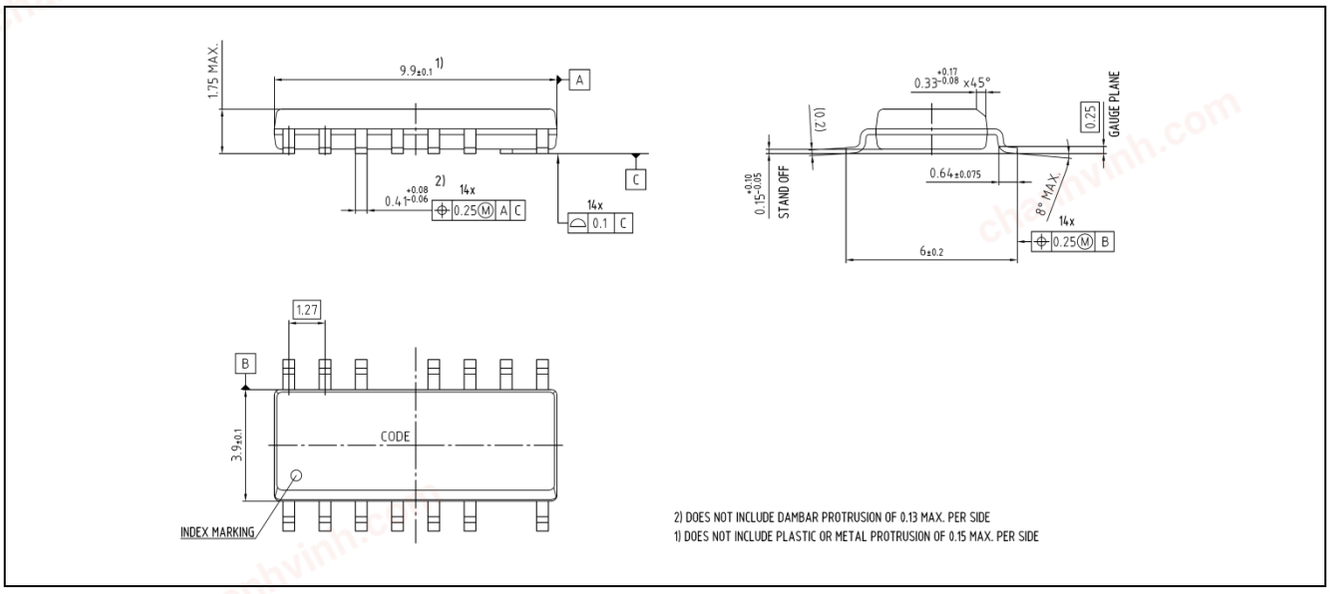

Figure 15 PG-DSO-14

Note: Please read the Getting Started guide to learn how to use the macro's and styles in this template.

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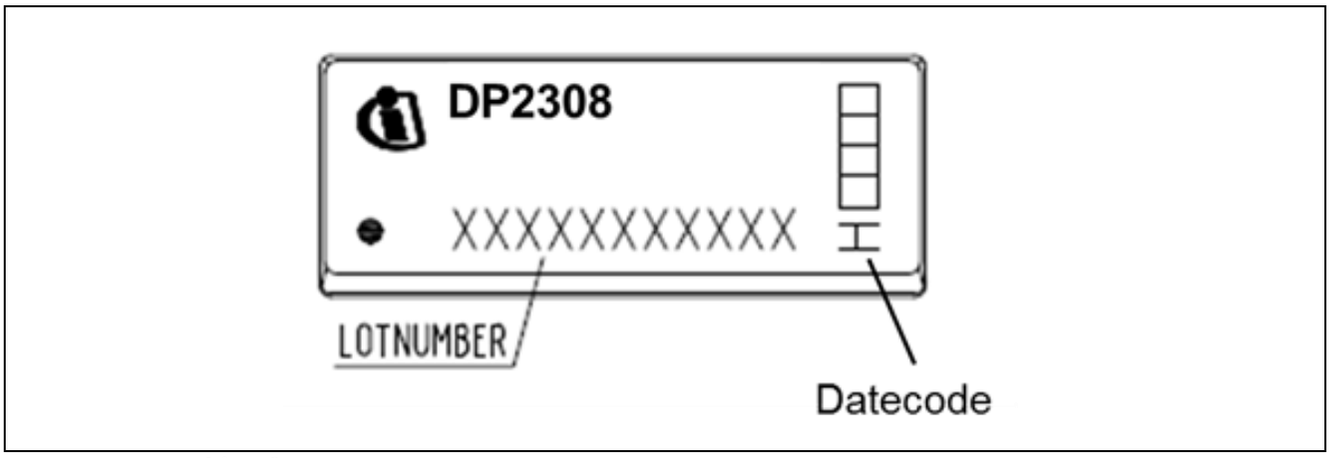

Figure 16 Marking for IDP2308

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Revision History

Major changes since the last revision

Page or Reference	Description of change
13	Max R_{HV} in Table 4 changed to 60 kΩ
14, 25, 26, 27	Update description on over temperature protection (OTP)

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