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ICB2FL03G

2nd Generation FL Controller for Fluorescent Lamp Ballasts

Data Sheet

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Final

Power Management & Multimarket

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page 52	changed min value for $T_{HSGDRise}$ from 140ns to 120ns typo correction: $T_{HSGDRise}$ & $T_{HSGDFall}$ --> $t_{HSGDRise}$ & $t_{HSGDFall}$

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2nd Generation FL-Controller for Fluorescent Lamp Ballasts

Product Highlights

- Lowest count of external components
- 650 V half-bridge driver with coreless transformer technology
- Supports Customer In-Circuit Test Mode for reduced tester time
- Supports multi-lamp designs (series connection)
- Integrated digital timers up to 40 seconds
- Numerous monitoring and protection features for highest reliability
- Very high accuracy of frequencies and timers over the whole temperature range
- Very low standby losses

PFC Features

- Discontinuous mode PFC for load range 0 to 100%
- Integrated digital compensation of PFC control loop
- Improved compensation for low THD of AC input current, also in DCM operation
- Adjustable PFC current limitation

Lamp Ballast Inverter Features

- Adjustable detection of overload and rectifier effect (EOL)
- Detection of capacitive load operation
- Improved ignition control allows operation close to the magnetic saturation of the lamp inductors
- Restart with skipped preheating on short interruptions of line voltage (for emergency lighting)
- Parameters adjustable by resistors only
- Pb-free lead plating; RoHS-compliant

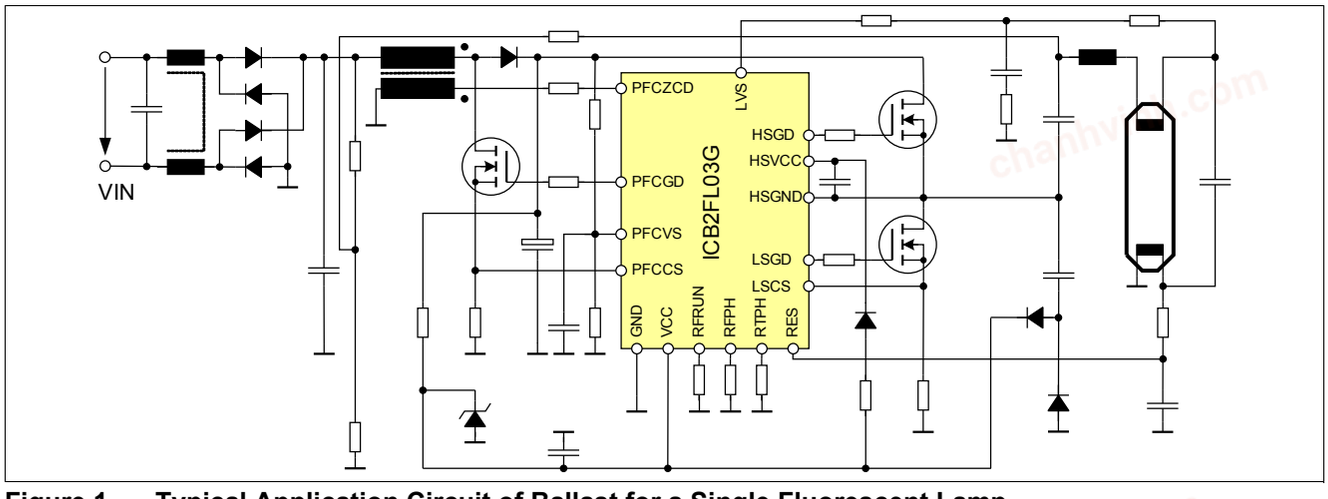


Figure 1 Typical Application Circuit of Ballast for a Single Fluorescent Lamp

Description

The FL controller ICB2FL03G is designed to control fluorescent lamp ballast, including a discontinuous mode Power Factor Correction (PFC), lamp inverter control and a high-voltage level shift half-bridge driver.

The control concept covers requirements for T5 lamp ballasts for single and multi-lamp designs (series connection supported). ICB2FL03G is based on the 2nd-generation FL controller technology, is easy to use and simple to design in. This makes the ICB2FL03G a basis for cost-effective solutions for fluorescent lamp ballasts with high reliability. **Figure 1** shows a typical application circuit of ballast for a single fluorescent T8 lamp with current mode preheating.

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1 Pin Configuration and Functionality

1.1 Pin Configuration

Table 1 Pin Configuration for PG-DSO-16

Pin	Symbol	Function
1	LSGD	Low side gate drive (inverter)
2	LSCS	Low side current sense (inverter)
3	VCC	Supply voltage
4	GND	Low side ground
5	PFCGD	PFC gate drive
6	PFCCS	PFC current sense
7	PFCZCD	PFC zero current detector
8	PFCVS	PFC voltage sense
9	RFRUN	Set R for run frequency
10	RFPH	Set R for preheat frequency
11	RTPH	Set R for preheating time
12	LVS	Lamp voltage sense
13	RES	Restart after lamp removal
14	HSGND	High side ground
15	HSVCC	High side supply voltage
16	HSGD	High side gate drive (inverter)

1.2 PG-DSO-16 Package

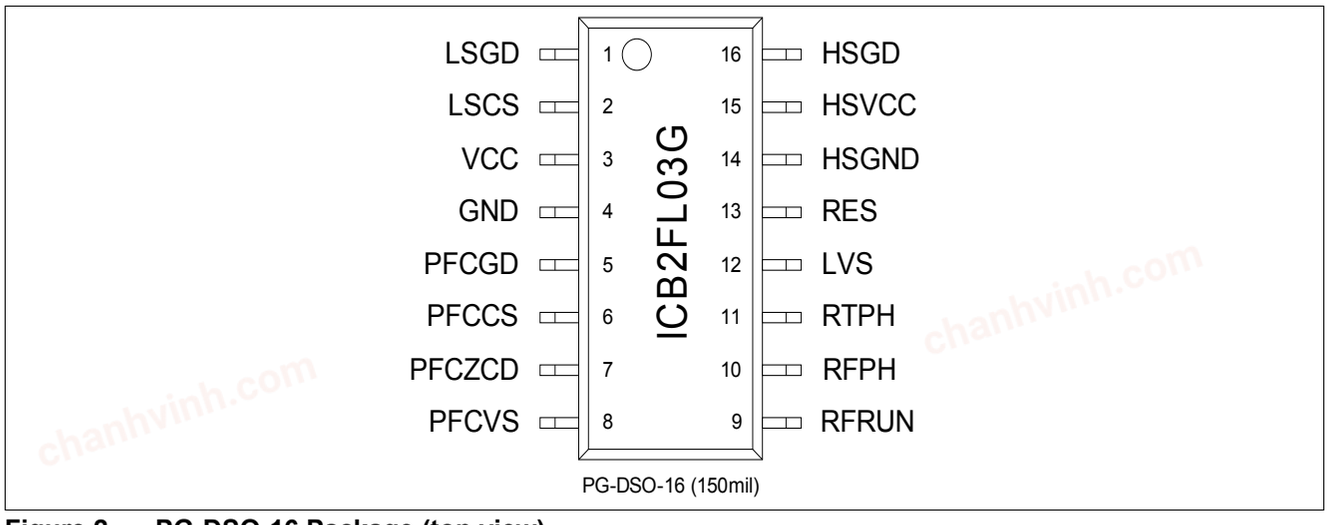


Figure 2 PG-DSO-16 Package (top view)

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1.3 Pin Functionality

LSGD (low-side gate drive, pin 1)

The gate of the low-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO (under voltage lockout) and limitation of the max H-level at 11.0 V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt); the gate voltage typically rises within 245 ns from L-level to H-level. The fall time of the gate voltage is less than 50 ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode parallel to a resistor in the gate drive loop. It is recommended to use a resistor of typically 10 Ω between drive pin and gate in order to avoid oscillations and in order to shift the power dissipation of discharging the gate capacitance into this resistor. The dead time between the LSGD signal and HSGD signal is self-adapting between 1.05 µs and 2.1 µs.

LSCS (low-side current sense, pin 2)

This pin is directly connected to the shunt resistor which is located between the source terminal of the low-side MOSFET of the inverter and ground.

Internal clamping structures and filtering measures allow for sensing the source current of the low-side inverter MOSFET without additional filter components.

The first threshold is 0.8 V. If this threshold is exceeded for longer than 500 ns during preheat or run mode, an inverter overcurrent is detected and causes a latched shutdown of the IC. The ignition control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8 V threshold. This stops the frequency decrease and waits for ignition. The ignition control is now continuously monitored by the LSCS PIN. The ignition control is designed to handle choke operation in saturation during ignition in order to reduce the choke size.

If the sensed current signal exceeds a second threshold of 1.6 V for longer than 500 ns during start-up, soft start, ignition mode and pre-run, the IC changes over into latched shutdown.

There are further thresholds active at this pin during run mode that detect capacitive mode operation. An initial threshold at 50 mV needs to sense a positive current during the second 50 % on-time of the low-side MOSFET for proper operation (cap. load 1). A second threshold of -50mV senses the current before the high-side MOSFET is turned on. A voltage level below this threshold indicates faulty operation (cap. load 2). Finally a third threshold at 2.0 V senses even short overcurrent during turn-on of the high-side MOSFET, typical for reverse recovery currents of a diode (cap. load 2). If any of these three comparator thresholds indicates incorrect operating conditions for longer than 620 µs (cap. load 2) or 2500 ms (cap. load 1) in run mode, the IC turns off the gates and changes into fault mode due to detected capacitive mode operation (non-zero voltage switching).

The threshold of -50 mV is also used to adjust the dead time between turn-off and turn-on of the half-bridge drivers in a range of 1.05 µs to 2.1 µs during all operating modes.

Vcc (supply voltage, pin 3)

This pin provides the power supply of the ground related section of the IC. There is a turn-on threshold at 14.0 V and an UVLO threshold at 10.6 V. The upper supply voltage level is 17.5 V. There is an internal zener diode clamping V_{CC} at 16.3 V (at I_{VCC} = 2 mA typically). The maximum zener current is internally limited to 5 mA. An external zener diode is required for higher current levels. Current consumption during UVLO and during fault mode is less than 170 µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for gate drive and logic signal currents. In order to skip preheating after short interruptions to the mains supply it is necessary to feed the start-up current (160 µA) from the bus voltage. Note: for external V_{CC} supply, see notes in the flowchart (**Section 3.3**).

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GND (ground, pin 4)

This pin is connected to ground and represents the ground level of the IC for supply voltage, gate drive and sense signals.

PFCGD (PFC gate drive, pin 5)

This pin controls the gate of the MOSFET in the PFC preconverter designed in boost topology. There is an active L-level during UVLO and limitation of the max H-level at 11.0 V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate drive voltage rises within 245 ns from L-level to H-level. The fall time of the gate voltage is less than 50 ns in order to turn off quickly.

A resistor of typically 10 Ω between the drive pin and gate is recommended in order to avoid oscillations and in order to shift the power dissipation of discharging the gate capacitance into this resistor.

The PFC section of the IC controls a boost converter as a PFC preconverter in discontinuous conduction mode (DCM). Control usually starts with gate drive pulses with a fixed on-time of typically 4.0 µs at V_{ACIN} = 230 V, increasing up to 24 µs and with an off-time of 47 µs. As soon as sufficient zero current detector (ZCD) signals are available, the operation mode changes from fixed frequency operation to operation with variable frequency. The PFC works in critical conduction mode operation (CritCM) when rated and / or medium load conditions are present. This means triangular-shaped currents in the boost converter choke without gaps and variable operating frequency. During low loads (detected by an internal compensator) operation is in discontinuous conduction mode (DCM) – i.e., triangular-shaped currents in the boost converter choke with gaps when reaching the zero current level and variable operating frequency in order to avoid steps in the consumed line current.

PFCCS (PFC current sense, pin 6)

The voltage drop across a shunt resistor located between the source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1.0 V for longer than 200 ns, the PFC gate drive is turned off as long as the zero current detector (ZCD) enables a new cycle. If no ZCD signal is available within 52 µs after turn-off of the PFC gate drive, a new cycle is initiated from an internal start-up timer.

PFCZCD (PFC zero current detector, pin 7)

This pin senses the point of time when the current through boost inductor becomes zero during off-time of the PFC MOSFET in order to initiate a new cycle.

The moment of interest appears when the voltage of the separate ZCD winding changes from the positive to negative level, which represents a voltage of zero at the inductor windings and therefore the end of current flow from the lower input voltage level to the higher output voltage level. There is a threshold with hysteresis – for increasing level 1.5 V, for decreasing level 0.5 V – which detects the change in inductor voltage.

A resistor, connected between ZCD winding and pin 7, limits the sink and source current of the sense pin when the voltage of the ZCD winding exceeds the internal clamping levels (6.3 V and -2.9 V typically @ 5 mA) of the IC.

If the sensed voltage level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 52 µs after turn-off of the PFC gate drive. The source current flowing out of this pin during the on-time of the PFC-MOSFET indicates the voltage level of the AC supply voltage. During low input voltage levels the on-time of the PFC-MOSFET is increased in order to minimize gaps in the line current during zero crossing of the line voltage and improve the THD (Total Harmonic Distortion) of the line current. Optimization of the THD is possible by trimming of the resistor between this pin and the ZCD winding.

PFCVS (PFC voltage sense, pin 8)

The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for rated bus voltage is 2.5 V. There are further thresholds at 0.3125 V (12.5 % of the rated bus voltage) for the detection of open control loop, at 1.875 V (75 % of the rated bus voltage) for the detection of undervoltage, and at 2.725 V (109 % of the rated bus voltage) for the detection of overvoltage. The

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overvoltage threshold operates with a hysteresis of 100 mV (4 % of the rated bus voltage). For the detection of successful start-up, the bus voltage is sensed at 95 % (2.375 V). It is recommended to use a small capacitor between this pin and GND as a spike suppression filter.

In run mode, a PFC overvoltage stops the PFC gate drive within 5 µs. As soon as the bus voltage is less than 105 % of the rated level, the gate drives are enabled again. If the overvoltage lasts for longer than 625 ms, inverter overvoltage is detected and the inverter turns off the gate drives also. This causes powerdown and powerup when V_{BUS} < 109 %.

A bus undervoltage (V_{BUS} > 75 %) or inverter overvoltage during run mode is handled as a fault U. In this situation the IC changes into powerdown mode and generates a delay of 100 ms by an internal timer. Then startup conditions are checked and if valid, a further startup is initiated. If startup conditions are not valid, a further delay of 100 ms is generated.

This procedure is repeated a maximum of seven times. If startup is successful within these seven cycles, the situation is interpreted as a short interruption of the mains supply and the preheating is skipped. Any further startup attempt is initiated to include the preheating.

RFRUN (set R for run frequency, pin 9)

A resistor from this pin to ground sets the operating frequency of the inverter during run mode. The typical run frequency range is 20 kHz to 120 kHz. The set resistor R_RFRUN can be calculated, based on the run frequency f_{RUN} according to the equation:

$$R_{FRUN} = \frac{5 \cdot 10^8 \Omega Hz}{f_{RUN}}$$

RFPH (set R for preheat frequency, pin 10)

A resistor from this pin to ground, together with the resistor at pin 9, sets the operating frequency of the inverter during preheating mode. The typical preheating frequency range is from the run frequency (as a minimum) to 150 kHz. The set resistor R_RFPH can be calculated, based on the preheating frequency f_{PH} and the resistor R_{RFRUN} according to the equation:

$$R_{RFPH} = \frac{R_{RFRUN}}{\frac{f_{PH} \cdot R_{RFRUN}}{5 \cdot 10^8 \Omega Hz} - 1}$$

RTPH (set R for preheating time, pin 11)

A resistor from this pin to ground sets the preheating time of the inverter during preheating mode. A set resistor range from zero to 25 kΩ corresponds to a range of preheating times from zero to 2500 ms subdivided into 127 steps, as expressed below:

$$R_{RTPH} = \frac{t_{PreHeating}}{100 \frac{ms}{k\Omega}}$$

LVS (lamp voltage sense, pin 12)

Before startup this pin senses a current fed from the rectified line voltage via resistors through the high-side filaments of the lamp for detection of an inserted lamp.

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The sensed current fed into the LVS pin has to exceed 12 μA typically at a voltage level of 6.0 V at the LVS pin. The reaction on the high side filament detection is mirrored at the RES pin (see pin 13). In addition, the detection of available mains supply after an interruption is sensed by this pin. Together with the RES pin, the IC can monitor the lamp removal of one lamp path (series connection of lamps is possible). If the functionality of this pin is not required, it can be disabled by connecting this pin to ground.

During run mode the lamp voltage is monitored with this pin by sensing a current proportional to the lamp voltage via resistors. An overload is indicated by an excessive lamp voltage. If the peak-to-peak lamp voltage causes a peak-to-peak current above a threshold of 210 μA_{PP} for longer than 620 μs, a fault EOL1 (end-of-life) is assumed. If the DC current at the LVS pin exceeds a threshold of ±42 μA for longer than 2500 ms, a fault EOL2 (rectifier effect) is assumed. The levels of AC sense current and DC sense current can be set separately by an external RC network. Note that in the case of deactivation of the LVS PIN, reactivation starts when the voltage at the LVS pin exceeds $V_{LVSEnable1}$ in RUN Mode.

RES (restart, pin 13)

A source current flowing out of this pin via resistor and filament to ground monitors the existence of the low-side filament of the fluorescent lamp for restart after lamp removal. A capacitor from this pin directly to ground eliminates a superimposed AC voltage that is generated as a voltage drop across the low-side filament. With a second sense resistor, the filament of a parallel lamp can be included in the lamp removal sensing. Note that during startup the chip supply voltage V_{cc} has to be below 14.0 V before V_{RES} reaches the filament detection level.

During typical start-up with connected filaments of the lamp a current source I_{RES3} (-21.3 μA) is active as long as V_{CC} > 10.6 V and V_{RES} < V_{RES1} (1.6 V). An open low-side filament is detected when V_{RES} > V_{RES1}. Such a condition will prevent the start-up of the IC. In addition, the comparator threshold is set to V_{RES2} (1.3 V) and the current source changes to I_{RES4} (-17.7 μA). The system is then waiting for a voltage level lower than V_{RES2} at the RES pin to indicate a connected low-side filament, which will enable the start-up of the IC.

An open high-side filament is detected when there is no sink current $I_{LVSSINK}$ (< 12 μA typ.) into the LVS pin before the V_{CC} start-up threshold is reached. Under these conditions the current source at the RES pin is I_{RES1} (-42.6 μA) as long as V_{CC} > 10.6 V and V_{RES} < V_{RES1} (1.6 V) and the current source is I_{RES2} (-35.4 μA) when the threshold has changed to V_{RES2} (1.3 V). In this way, the detection of the high-side filament is mirrored at the levels on the RES pin.

There is a further threshold of 3.2 V active at the RES pin during run mode. If the voltage level rises above this threshold for longer than 620 μs, the IC changes over into latched fault mode.

In any case of fault detection with different reaction times the IC turns off the gate drives and changes into powerdown mode with a current consumption of 170 μA max. An internal timer generates a delay time of 200 ms before start-up conditions are checked again. As soon as start-up conditions are valid, a second start-up attempt is initiated. If this second attempt fails, the IC remains in latched fault mode until a reset is generated by UVLO or lamp removal. The RES PIN can be deactivated by setting the PIN to GND (durable).

HSGND (high-side ground, pin 14)

This pin is connected to the source terminal of the high-side MOSFET, which is also the node of the high-side and low-side MOSFET. This pin represents the floating ground level of the high-side driver and the high-side supply.

HSVCC (high-side supply voltage, pin 15)

This pin provides the power supply of the high-side ground-related section of the IC. An external capacitor between pins 14 and 15 acts like a floating battery, which has to be recharged cycle by cycle via the high-voltage diode from low-side supply voltage during on-time of the low-side MOSFET. There is a UVLO threshold with hysteresis that enables the high-side section at 10.4 V and disables it at 8.6 V.

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HSGD (high-side gate drive, pin 16)

The gate of the high-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO and limitation of the max H-level at 11.0 V during normal operation. The switching characteristics are the same as described for LSGD (pin 1). It is recommended to use a resistor of about 10 Ω between the drive pin and gate in order to avoid oscillations and in order to shift the power dissipation of discharging the gate capacitance into this resistor. The dead time between LSGD signal and HSGD signals is self-adapting between 1.05 µs and 2.1 µs (typically).

2 Functional Description

This section describes applications and functionality of the chip.

2.1 Typical Application Circuitry

The schematic shown in **Figure 3** shows a typical application for a T5 single fluorescent lamp. It is designed for universal input voltage from 90 V_{AC} up to 270 V_{AC}. The following sections explain the components in reference to this schematic.

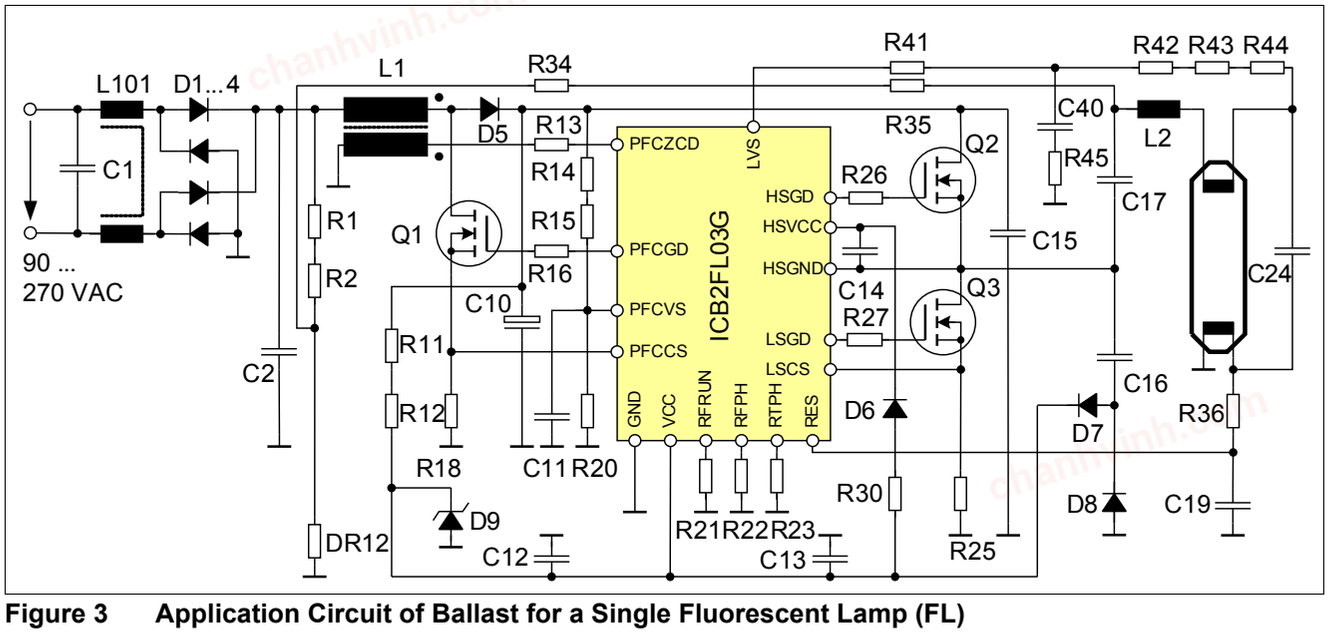


Figure 3 Application Circuit of Ballast for a Single Fluorescent Lamp (FL)

2.2 Normal Startup

This section describes the basic operation flow (8 phases) from the UVLO (Under Voltage Lock Out) into run mode without any error detection. For detailed information see **Section 2.2.1** and **Section 2.2.2**. **Figure 4** shows the 8 different phases during a typical start from UVLO (phase 1, **Figure 4**) to run mode (phase 8, **Figure 4**) and then into normal operation (no failure detected).

If the AC line input is switched ON, the V_{CC} voltage rises to the UVLO threshold V_{CC} = 10.6 V (no IC activity during UVLO). If V_{CC} exceeds the first threshold of V_{CC} = 10.6 V, the IC starts the first level of detection activity, the high and low side filament detection during the start-up hysteresis (phase 2, **Figure 4**).

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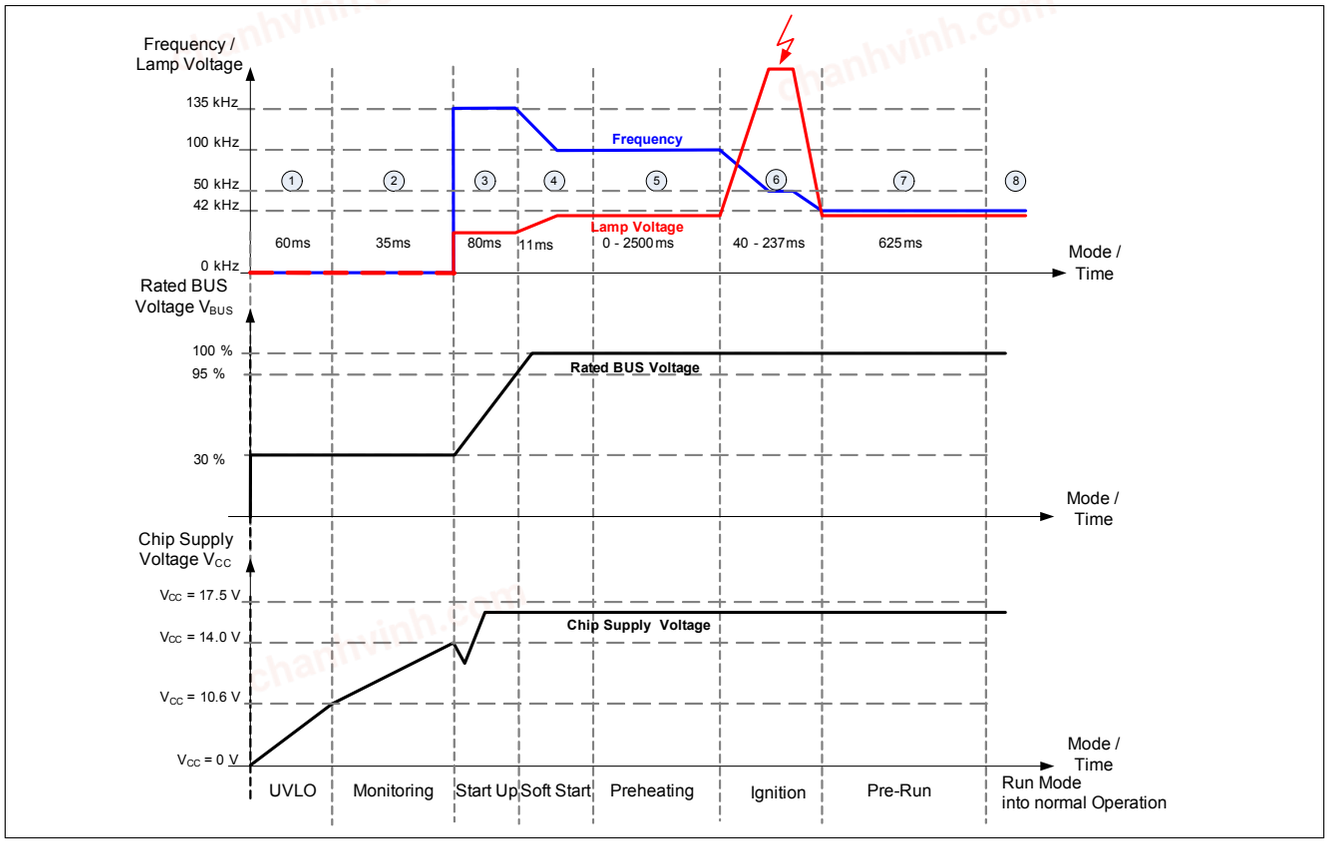


Figure 4 Typical Startup Procedure in Run Mode (in Normal Operation)

Followed at the end of the start-up hysteresis (phase 2, **Figure 4**) V_{CC} > 14.0 V and before phase 3 is active, a second level of detection activity senses for 130 µs (propagation delay of the IC) whether the bus voltage is between 12.5 % and 105 %. If the previous bus voltage conditions are fulfilled and the filaments are detected, the IC starts the operation with an internally fixed startup frequency of typically 135 kHz (all gates are active). If the bus voltage reaches a level of 95 % of the rated bus voltage within 80 ms at the latest (phase 3, **Figure 4**), the IC enters the soft start phase. During soft start (phase 4 , **Figure 4**), the start-up frequency shifts from 135 kHz down to the set preheating frequency (**Section 2.2.2**). In the soft start phase, the lamp voltage rises and the chip supply voltage reaches its working level from 10.6 V < V_{CC} < 17.5 V. After the soft start has finished, the IC enters the preheating mode (phase 5, **Figure 4**) for preheating the filaments (adjustable time) in order to extend the life cycle of the FL filaments. On finishing preheating, the controller starts ignition (phase 6, **Figure 4**). During the ignition phase, the frequency decreases from the set preheating frequency down to the set operation frequency (adjustable, see **Section 2.2.2**). If ignition is successful, the IC enters the pre-run mode (phase 7, **Figure 4**).

This mode is provided in order to prevent a malfunction of the IC due to an unstable system – e.g., the lamp parameters are not in a steady state condition. After finishing the 625 ms pre-run phase, the IC switches over to the run mode (phase 8, **Figure 4**) with complete monitoring.

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2.2.1 Operating Levels from UVLO to Soft Start

This section describes the operating flow from phase 1 (UVLO) to phase 4 (soft start) in detail. The control of the ballast is able to start the operation within less than 100 ms (IC in active mode). This is achieved by a small start-up capacitor (about 1 µF C12 and C13 – fed by start-up resistors R11 and R12 in **Figure 3**) and the low current consumption during the UVLO (I_{VCC} = 130 µA – phase 1, **Figure 5**) and start-up hysteresis (I_{VCC} = 160 µA – defines the start-up resistors – phase 2, **Figure 5**) phases. The chip supply stage of the IC is protected against overvoltage via an internal Zener clamping network, which clamps the voltage at 16.3 V and allows a current of 2.5 mA. For clamping currents above 2.5 mA, an external Zener diode (D9, **Figure 3**) is required.[1)]

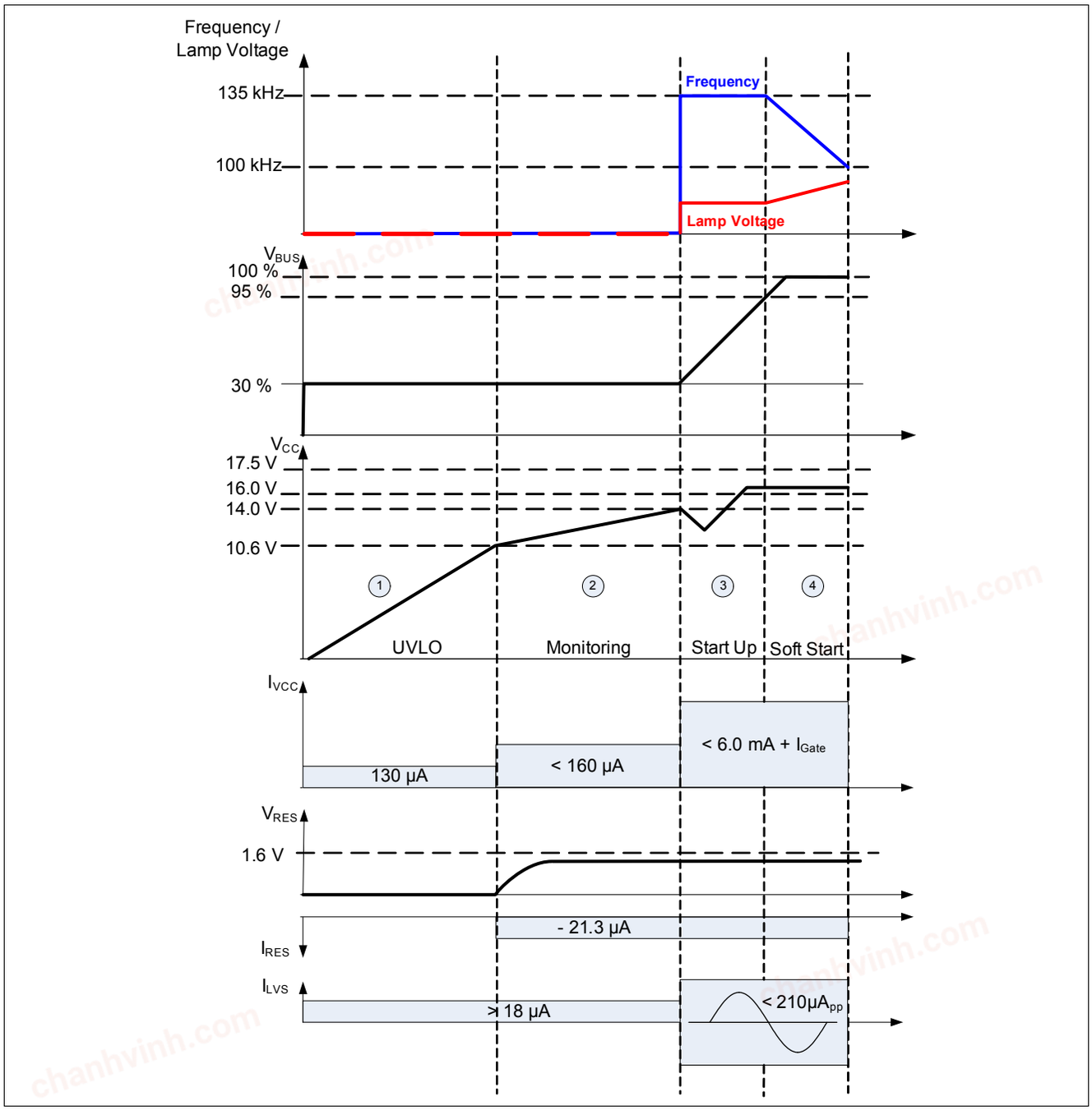


Figure 5 Typical Startup Procedure in Run Mode (in Normal Operation)

1) I_{Gate} depends on MOSFET

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If V_{CC} exceeds the 10.6 V level and stays below 14.0 V (start-up hysteresis – phase 2, **Figure 5**), the IC checks whether the lamps are assembled by detecting a current across the filaments.

The low side filaments are checked from a source current of typical I_{RES3} = - 21.3 µA flowing out of pin 13 RES (**Figure 5** I_{RES}). This current produces a voltage drop of V_{RES} < 1.6 V (filament is ok) at the low side filament sense resistor (R 36 in **Figure 3**), connected to GND (via low side filament). An open low side filament is detected (see **Section 2.3.2**), when the voltage at the RES pin exceeds the V_{RES} > 1.6 V threshold (**Figure 5** V_{RES}).

The high side filaments are checked by a current of I_{LVS} > 12 µA typically via resistors R41, R42, R43 and R44 (**Figure 3**) into the LVS pin 12 (for a single lamp operation). An unused LVS pin has to be disabled via connection to GND. An open high side filament is detected (see **Section 2.3.3**) when there is no sink current into the LVS pin. This causes a higher source current out of the RES pin (typically 42.6 µA / 35.4 µA) in order to exceed V_{RES} > 1.6 V. In the case of defective filaments, the IC keeps monitoring until an adequate current from the RES or the LVS pin is present (e.g. in case of removal of a defective lamp).

When V_{CC} exceeds the 14.0 V threshold – by the end of the start-up hysteresis in phase 2 , **Figure 5** – the IC waits for 130 µs and senses the bus voltage. If the rated bus voltage is in the corridor of 12.5 % < $V_{BUSrated}$ < 105 %, the IC powers up the system and enters phase 3 (**Figure 5** $V_{BUSrated}$ > 95 % sensing); if not, the IC initiates a UVLO until the chip supply voltage falls below V_{CC} < 10.6 V. As soon as the condition for a power-up is fulfilled, the IC starts the inverter gate operation with an internal fixed start-up frequency of 135 kHz. The PFC gate drive starts with a delay of approx. 300 µs. Next, the bus voltage will be checked for a rated level above 95 % for a duration of 80 ms (phase 3, **Figure 5**). When leaving phase 3, the IC enters the soft start phase and shifts the frequency from the internal fixed start-up frequency of 135 kHz down to the set preheating frequency – e.g. f_{RFPH} = 100 kHz.

2.2.2 Operating Levels from Soft Start to Run Mode

This section describes the operating flow from phase 5 (preheating mode) to phase 8 (run mode) in detail. In order to extend the lifetime of the filaments, the controller enters – after the soft start phase – the preheating mode (phase 5, **Figure 6**). The preheating frequency is set by resistors R22 pin R_{FPH} to GND in combination with R21 (**Figure 3**) typ. 100 kHz e.g. R22 = 8.2 kΩ in parallel to R21 = 11.0 kΩ (see **Figure 3**, RFRUN pin). The preheating time can be selected by the programming resistor (R23 in **Figure 3**) at pin RTPH from 0 ms up to 2500 ms (phase 5, **Figure 6**).

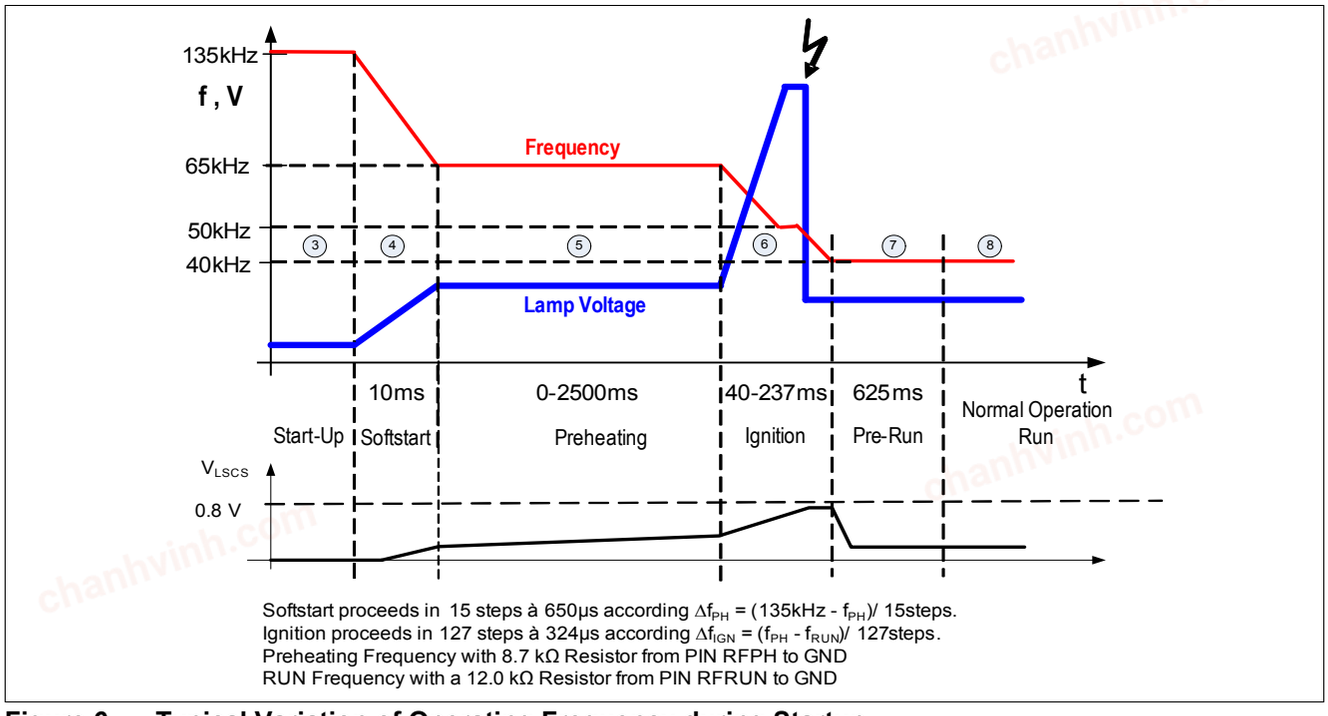


Figure 6 Typical Variation of Operating Frequency during Startup

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During ignition (phase 6, **Figure 6**), the operating frequency of the inverter is shifted downward in t_{typ} = 40 ms (t_{max} = 237 ms) to the run frequency set by a resistor (R21 in **Figure 3**) at pin RFRUN to GND (typically 45 kHz with an 11.0 kΩ resistor). During this frequency shifting, the voltage and current in the resonant circuit will rise when the operation is close to the resonant frequency with increasing voltage across the lamp. The ignition control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8 V threshold. This stops the decrease of the frequency and waits for ignition. The ignition control is now continuously monitored by the LSCS pin. The maximum duration of the ignition procedure is limited to 237 ms. If there is no ignition within this time frame, the ignition control is disabled and the IC changes over into the latched fault mode.

Furthermore, in order to reduce the size of the lamp choke, the ignition control is designed to operate with a lamp choke in magnetic saturation during ignition. For operation in magnetic saturation during ignition; the voltage at the shunt at the LSCS pin 2 has to be V_{LSCS} = 0.75 V when the ignition voltage is reached. If ignition is successful, the IC enters the pre-run mode (phase 7, **Figure 6**). The pre-run mode is a safety mode in order to prevent a malfunction of the IC due to an unstable system – e.g., the lamp parameters are not in a steady state condition. After 625 ms pre-run mode, the IC changes to the run mode (phase 8, **Figure 6**). The run mode monitors the complete system regarding bus over- and undervoltage, open loop, overcurrent of PFC and / or inverter, lamp overvoltage (EOL1) and rectifier effect (EOL2) (see **Section 2.5**) and capacitive loads 1 and 2 (see **Section 2.6**).

Figure 8 shows the lamp voltage versus the frequency during the different phases from preheating to the run mode. The lamp voltage rises by the end of the preheating phase with decreasing frequency (e.g., 100 kHz to 50 kHz) up to, for example, 700 V during ignition. After ignition, the lamp voltage drops down to its working level with continuous decreasing of the frequency (**Figure 8**) down to its working level e.g. 45 kHz (set by a resistor at the RFRUN pin to ground). After decreasing of the frequency stops, the IC enters the pre-run mode.

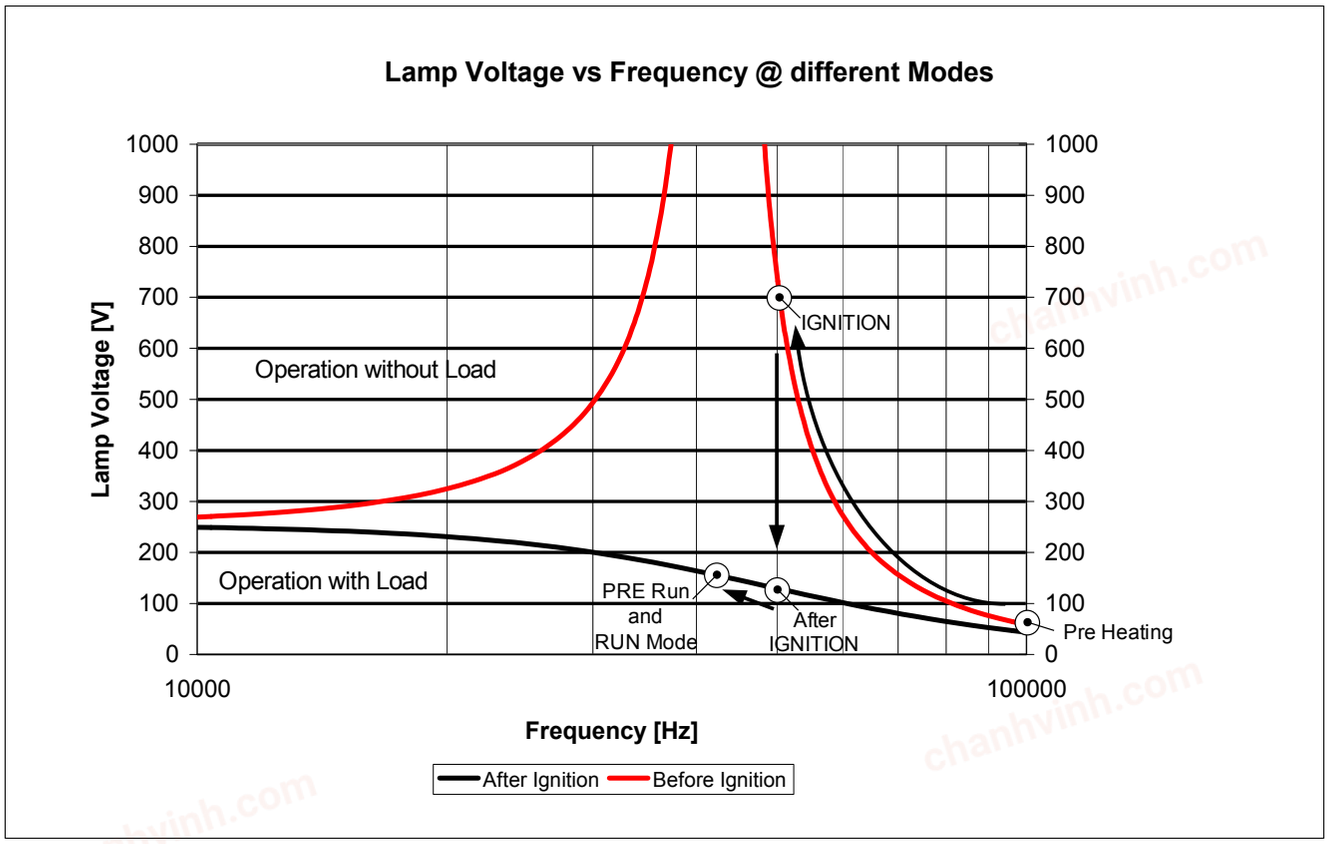


Figure 7 Lamp Voltage versus Frequency during the different Startup Phases

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2.3 Filament Detection during Start-Up and Run Mode

The low and high side filament detection is sensed via the RES and the LVS pins. The low side filament detection during start-up and run mode is detected via the RES pin only. An open high side filament during start-up will be sensed via the LVS and the RES pins.

2.3.1 Start-Up with broken Low Side Filament

A source current of I_{RES3} = -21.3 µA from the RES pin (13) monitors the existence of a low side filament during a start-up (also in run mode). In the case of an open low side filament during the start-up hysteresis (10.6 V < V_{CC} < 14.0 V) a capacitor (C19 in **Figure 3**) will be charged up via I_{RES3} = -21.3 µA. When the voltage at the RES pin (13) exceeds V_{RES1} = 1.6 V, the controller prevents a power up and clamps the RES voltage internally at V_{RES} = 5.0 V. The gate drives of the PFC and inverter stage do not start working.

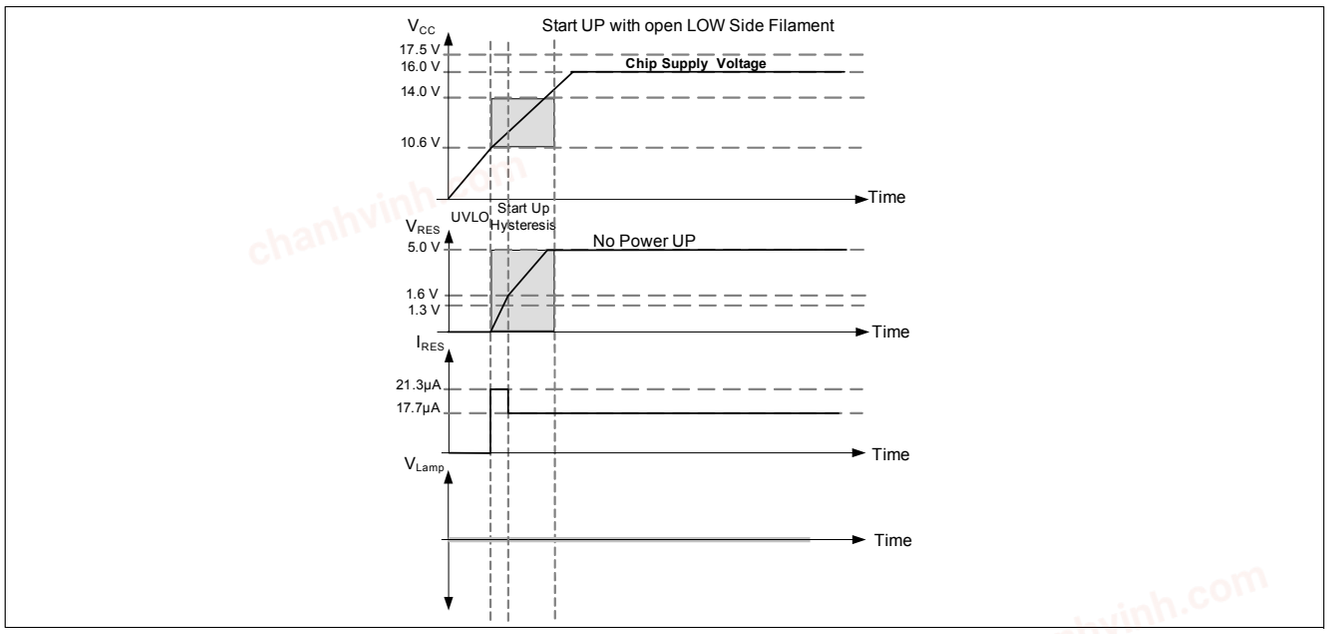


Figure 8 Start-Up with Open Low Side Filament

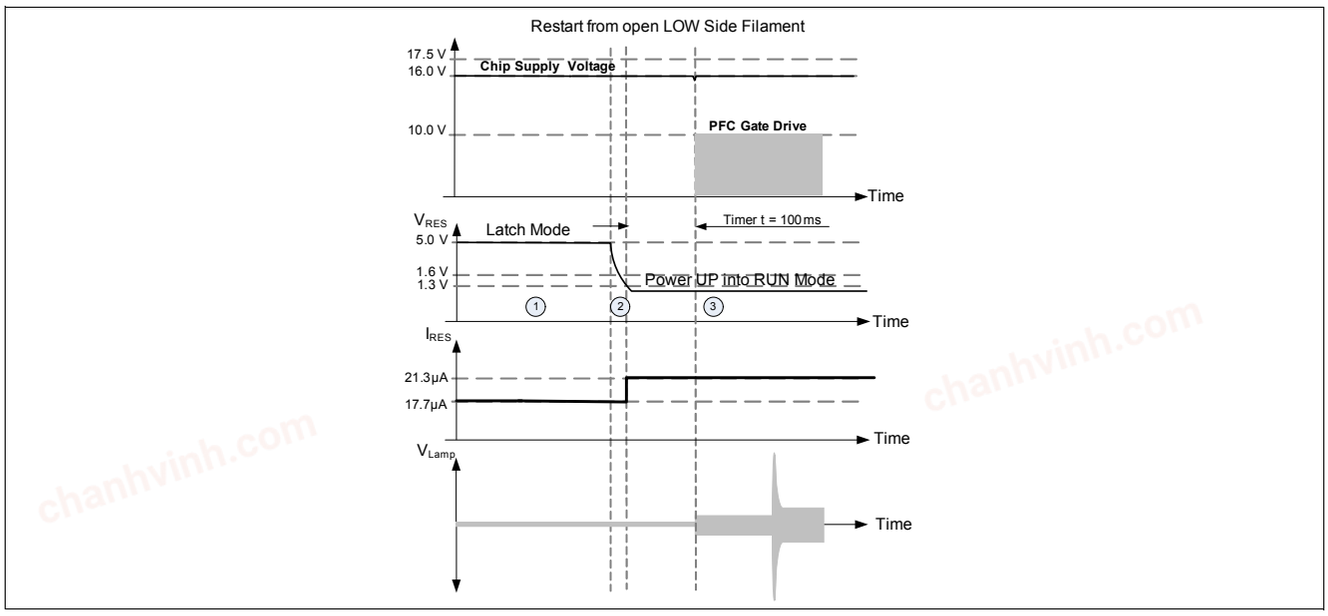


Figure 9 Restart from Open Low Side Filament

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The IC comparators are then set to a threshold of V_{RES1} = 1.3 V and to I_{RES4} = - 17.7µA, the controller waits until the voltage at the RES pin drops below V_{RES1} = 1.3 V.

When a filament is present (**Figure 9**, section 2), the voltage drops below 1.3 V and the value of the source current out of the RES pin is set from I_{RES4} = -17.7 µA up to I_{RES3} = -21.3 µA. The controller then powers up the system, including soft start and preheating, into the run mode.

2.3.2 Low Side Filament Detection during Run Mode

In the case of an open low side filament during run mode, the current flowing out of the RES pin I_{RES3} = -21.3 µA charges up the capacitor C19 in **Figure 3**. If the voltage at the RES pin exceeds the V_{RES3} = 3.2 V threshold, the controller detects an open low side filament and stops the gate drives after a delay of t = 620 µs of an internal timer.

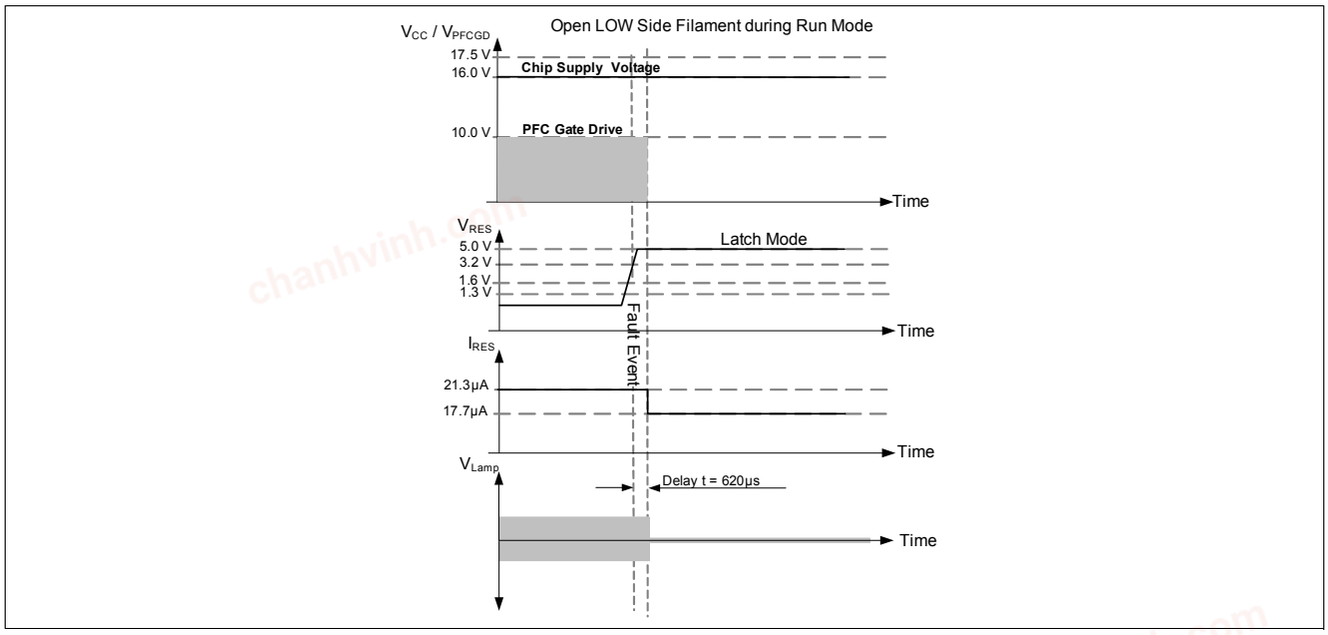


Figure 10 Open Low Side Filament Run Mode

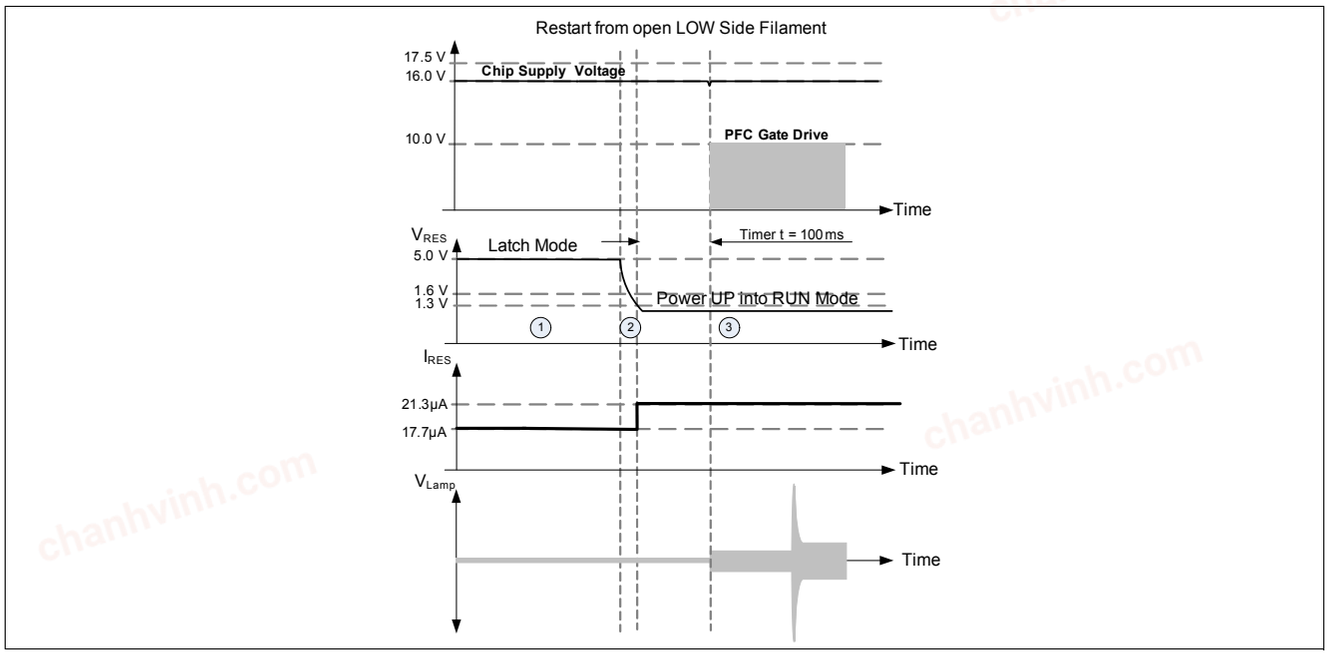


Figure 11 Restart from Open LS Filament

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A restart is initiated when a filament is detected e.g. in the case of a lamp removal. If a filament is present (**Figure 11**, section 2), the voltage drops below 1.3 V and the value of the source current flowing out of the RES pin is set from I_{RES4} = -17.7 µA up to I_{RES3} = -21.3 µA. The controller powers up the system, including soft start and preheating, into the run mode (**Figure 11**, section 3).

2.3.3 Start-Up with Broken High Side Filament

An open high side filament during the start-up hysteresis (10.6 V < V_{CC} < 14.0 V) is detected when the current into the LVS pin 12 is below I_{LVS} = 12 µA (typically). In that case, the current flowing out of the RES pin 13 rises up to I_{RES1} = -42.6 µA. This causes the voltage at the RES pin to cross V_{RES1} = 1.6 V. The source current is now set to I_{RES2} = -35.4 µA and another threshold of V_{RES2} = 1.3 V is active. The controller prevents a power-up (see **Figure 12**), and the gate drives of the PFC and inverter stage do not start working.

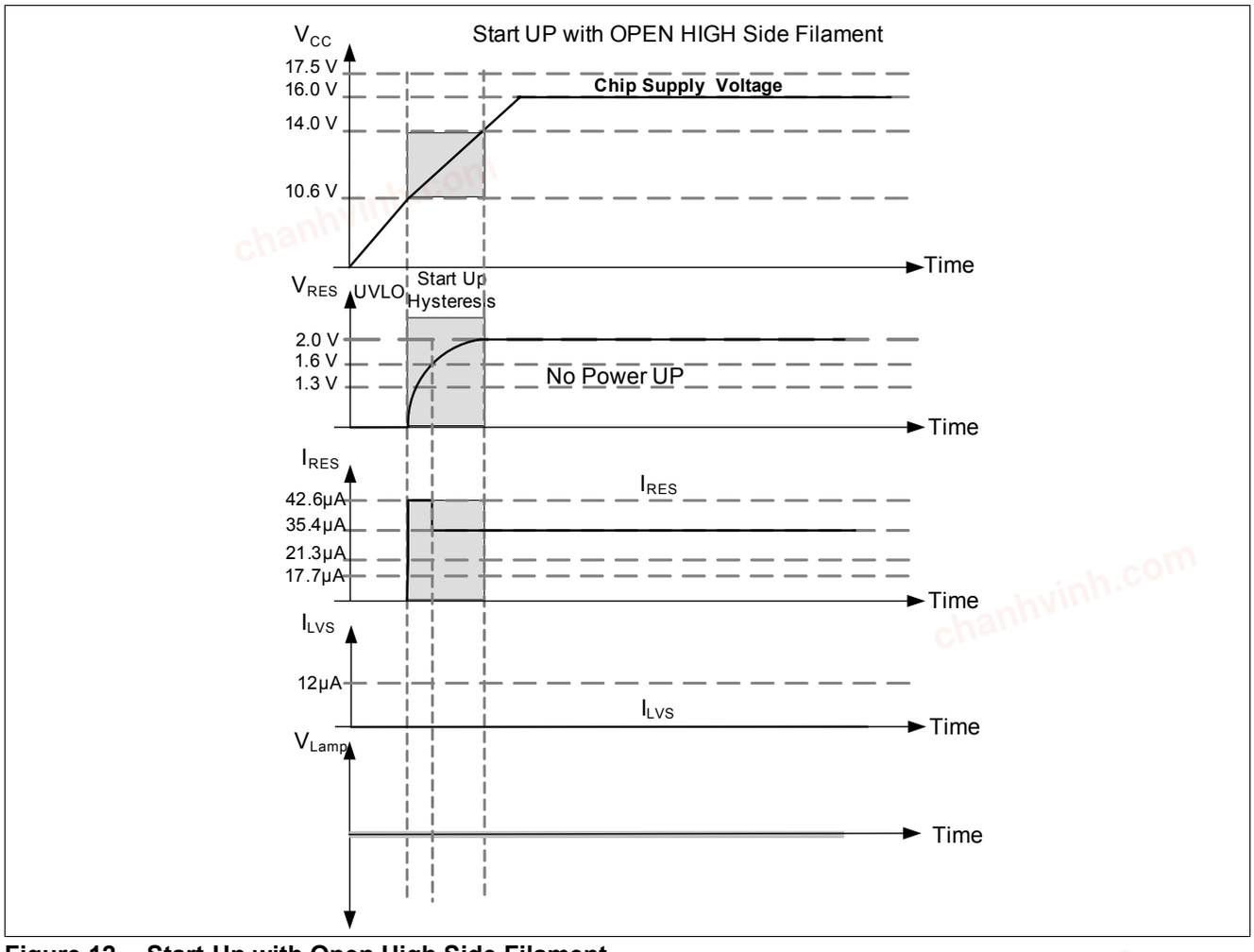


Figure 12 Start-Up with Open High Side Filament

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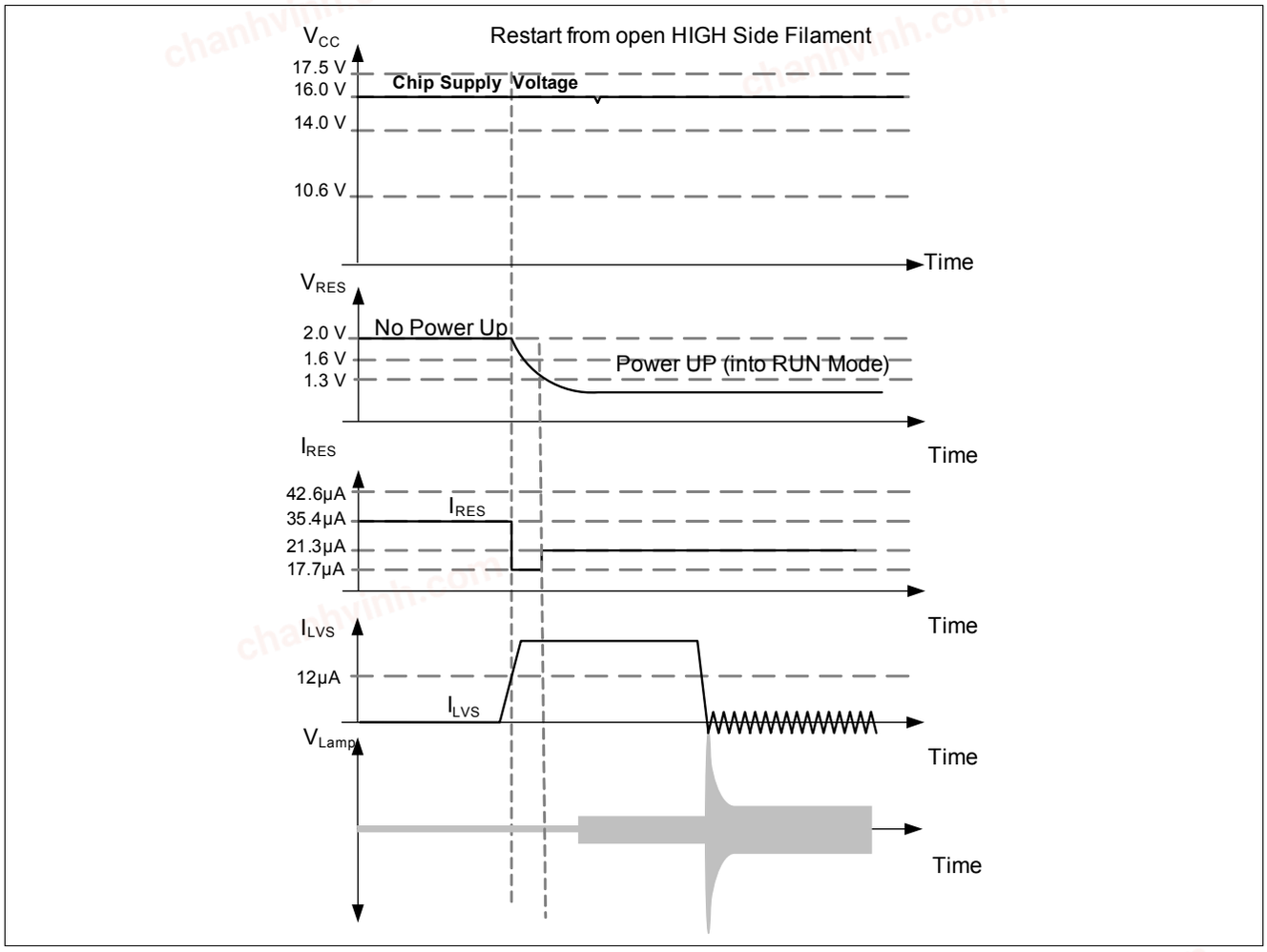


Figure 13 Restart from Open High Side Filament

When the high side filament is present, e.g. insertion of a lamp, the current of the active LVS pin exceeds I_{LVS} > 12 µA (typically), the RES current drops from I_{RES2} = -35.4 µA down to I_{RES4} = -17.7 µA (**Figure 13**). The controller then senses the low side filament. If a low side filament is also present, and the controller drops (after a short delay due to a capacitor at the RES pin) below V_{RES2} = 1.3 V, the RES current is set to I_{RES3} = -21.3 µA, and the controller powers up the system.

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2.4 PFC Preconverter

2.4.1 Discontinuous Conduction and Critical Conduction Mode Operation

The digitally controlled PFC preconverter starts with an internally fixed ON time of typically t_{ON} = 4.0 µs and a variable frequency. The ON time is increased every 280 µs (typical) up to a maximum ON time of 24 µs. The control switches practically immediately from the discontinuous conduction mode (DCM) to critical conduction mode (CritCM) as soon as a sufficient ZCD signal becomes available. The frequency range in CritCM is 22 kHz to 500 kHz depending on the power (**Figure 14**), with a variation of the ON time from 24 µs > t_{ON} > 0.5µs.

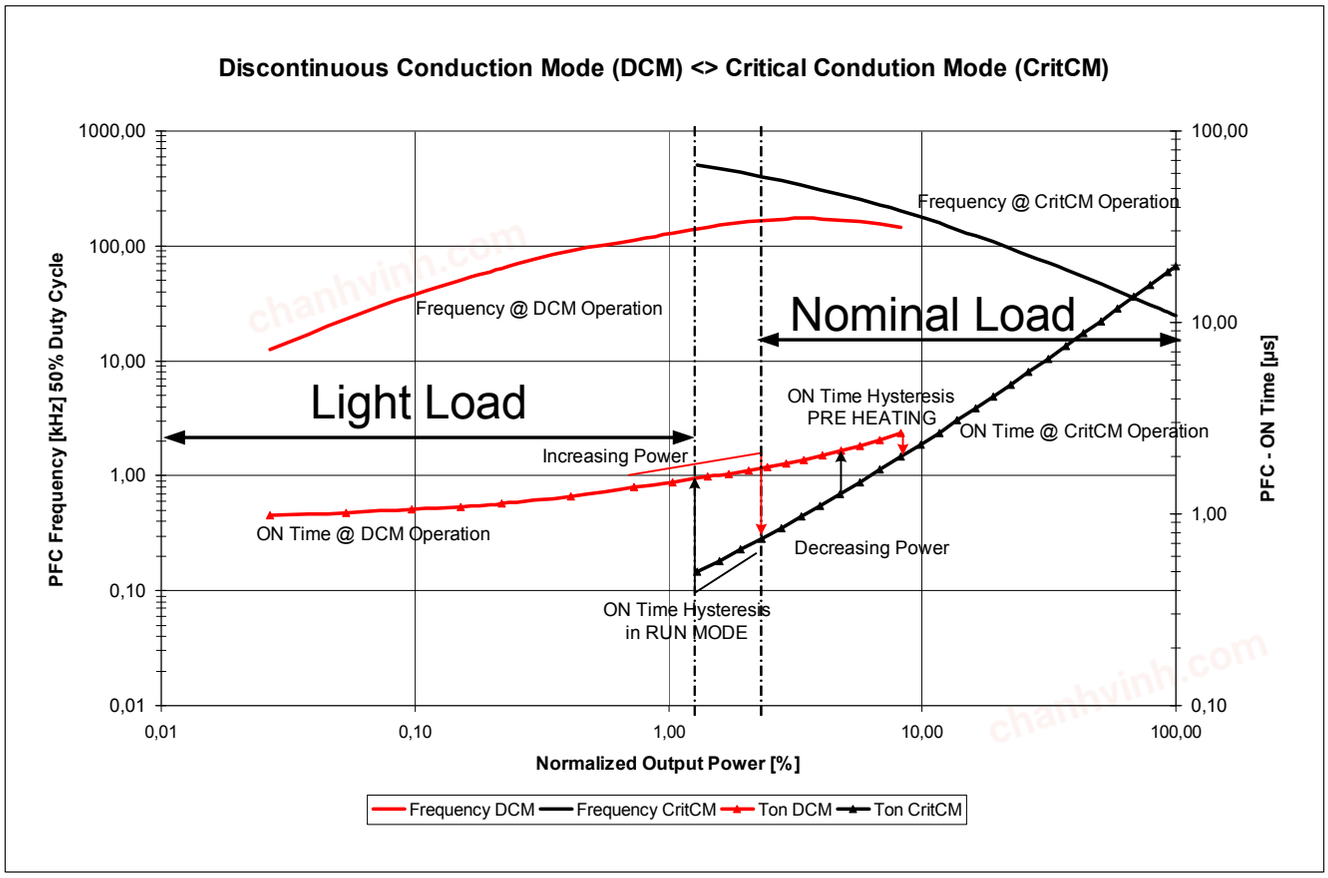


Figure 14 Operating Frequency and ON Time versus Power in DCM and CritCM Operation

For lower loads ($P_{OUTNorm}$ < 8 % from the normalized load[1)]) the control operates in discontinuous conduction mode (DCM) with an ON time from 4.0 µs and increasing OFF time. The frequency during DCM is variable in a range from 144 kHz down to typically 22 kHz @ 0.1 % load (**Figure 14**). With this control method, the PFC converter enables stable operation from 100 % load down to 0.1 %. **Figure 14** shows the ON time range in DCM and CritCM (Critical Conduction Mode) operation. In the overlapping area of CritCM and DCM there is a hysteresis of the ON time which causes a negligible frequency change.

2.4.2 PFC Bus Voltage Sensing

Overvoltage, open loop, bus 95 % and undervoltage states (**Figure 15**) of the PFC bus voltage are sensed at the PFCVS pin via the network R14, R15, R20 and C11 – **Figure 3** (C11 acts as a spike suppression filter).

1) Normalized power @ low line input voltage and maximum load

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2.4.2.1 Bus Overvoltage and PFC Open Loop

The bus voltage loop control is completely integrated (**Figure 16**) and provided by an 8-bit sigma/delta A/D converter with a typical sampling rate of 280 µs and resolution of 4 mV/bit. After leaving phase 2 (monitoring), the IC starts power-up (V_{CC} > 14.0 V). After power-up, the IC senses the bus voltage below 12.5 % (open loop) or above 105 % (bus overvoltage) for 130 µs. In the case of bus overvoltage ($V_{BUSrated}$ > 109 %) or open loop ($V_{BUSrated}$ < 12.5 %) in phases 3 to 8, the IC shuts off the gate drives of the PFC within 5 µs or 1 µs respectively. In this case, the PFC restarts automatically when the bus voltage is within the corridor (12.5 % < $V_{BUSrated}$ < 105 %) again. Is the bus voltage valid after 130 µs, the bus voltage sensing is set to 12.5 % < $V_{BUSrated}$ < 109 %. If these thresholds are exceeded for longer than 1 µs (open loop) or 5 µs (overvoltage), the PFC gate drive stops working until the voltage drops below 105 % or exceeds the 12.5 % level. If the bus overvoltage (> 109 %) lasts for longer than 625 ms in run mode, the inverter gates also shut off and a power-down with complete restart is attempted (**Figure 15**).

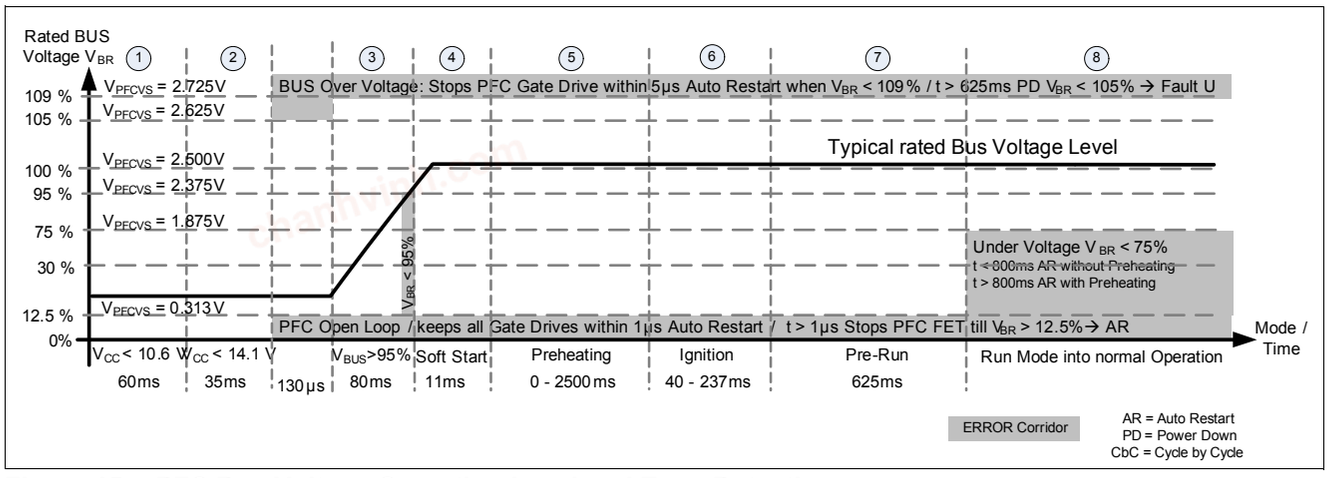


Figure 15 PFC Bus Voltage Operating Level and Error Detection

2.4.2.2 Bus Voltage 95 % and 75 % Sensing

When the rated bus voltage is in the corridor of 12.5 % < $V_{BUSrated}$ < 109 %, the IC will check whether the bus voltage exceeds the 95 % threshold (**Figure 15**, phase 3) within 80 ms before entering the soft start phase 4. Another threshold is activated when the IC enters the run mode (phase 8). If the rated bus voltage drops below 75 % for longer than 84 µs, a power-down with a complete restart is attempted when a counter exceeds 800 ms. In the case of short-term bus undervoltage (the bus voltage reaches its working level in run mode before exceeding typically 800 ms (min. 500 ms)) the IC skips phases 1 to 5 and starts with ignition (see **Section 2.7.1** for conditions for emergency lighting). The internal reference level of the bus voltage sense V_{PFCVS} is 2.5 V (100 % of the rated bus voltage) with a high accuracy. A surge protection is activated in the case of a rated bus voltage of V_{BUS} > 109 % and a low side current sense voltage of V_{LSCS} > 1.6 V in pre-run mode, or V_{LSCS} > 0.8 V in run mode for longer than 500 ns.

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2.4.3 PFC Structure of Mixed Signals

A digital NOTCH filter eliminates the input voltage ripple independently of the mains frequency. A subsequent error amplifier with PI characteristic ensures stable operation of the PFC preconverter (**Figure 16**).

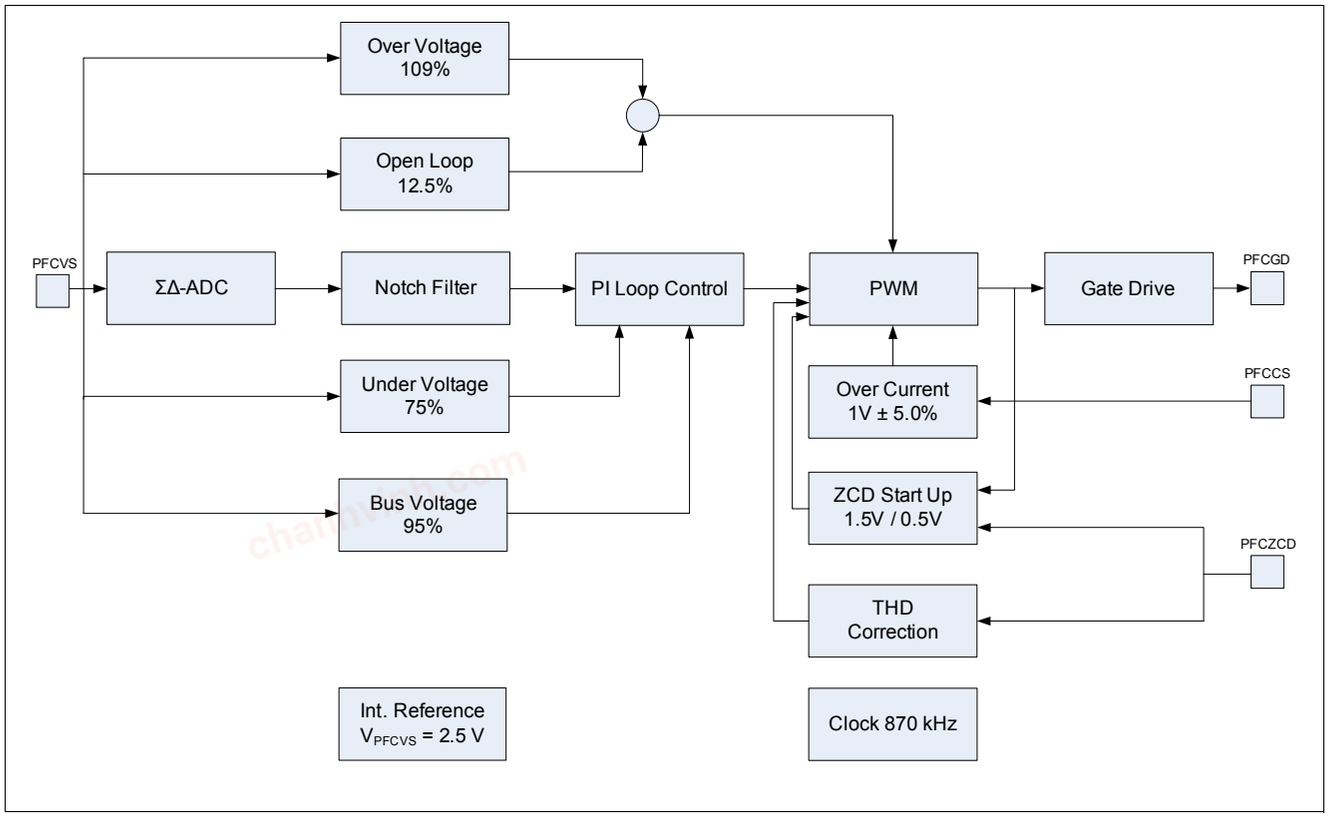


Figure 16 Structure of the Mixed Digital and Analog Control of the PFC Preconverter

The zero current detection (ZCD) is sensed by the PFCZCD pin via R13 (**Figure 3**). Notification of finished current flow during demagnetization is required in CritCM and in DCM also. The input is equipped with a special filtering system, including blanking of typically 500 ns and a large hysteresis of typically 0.5 V and 1.5 V V_{PFCZCD} (**Figure 16**).

2.4.4 THD Correction via ZCD Signal

An additional feature is the THD correction (**Figure 16**). In order to optimize the improved THD (especially in the zones A shown in **Figure 17** ZCD @ AC Input Voltage), there is a possibility to extend the pulse width of the gate signal (blue part of the PFC gate signal in **Figure 17**) with the variable PFC ZCD resistor (see resistor R13 in **Figure 3**) in addition to the gate signal controlled by the V_{PFCVS} signal (gray part of the PFC gate signal in **Figure 17**).

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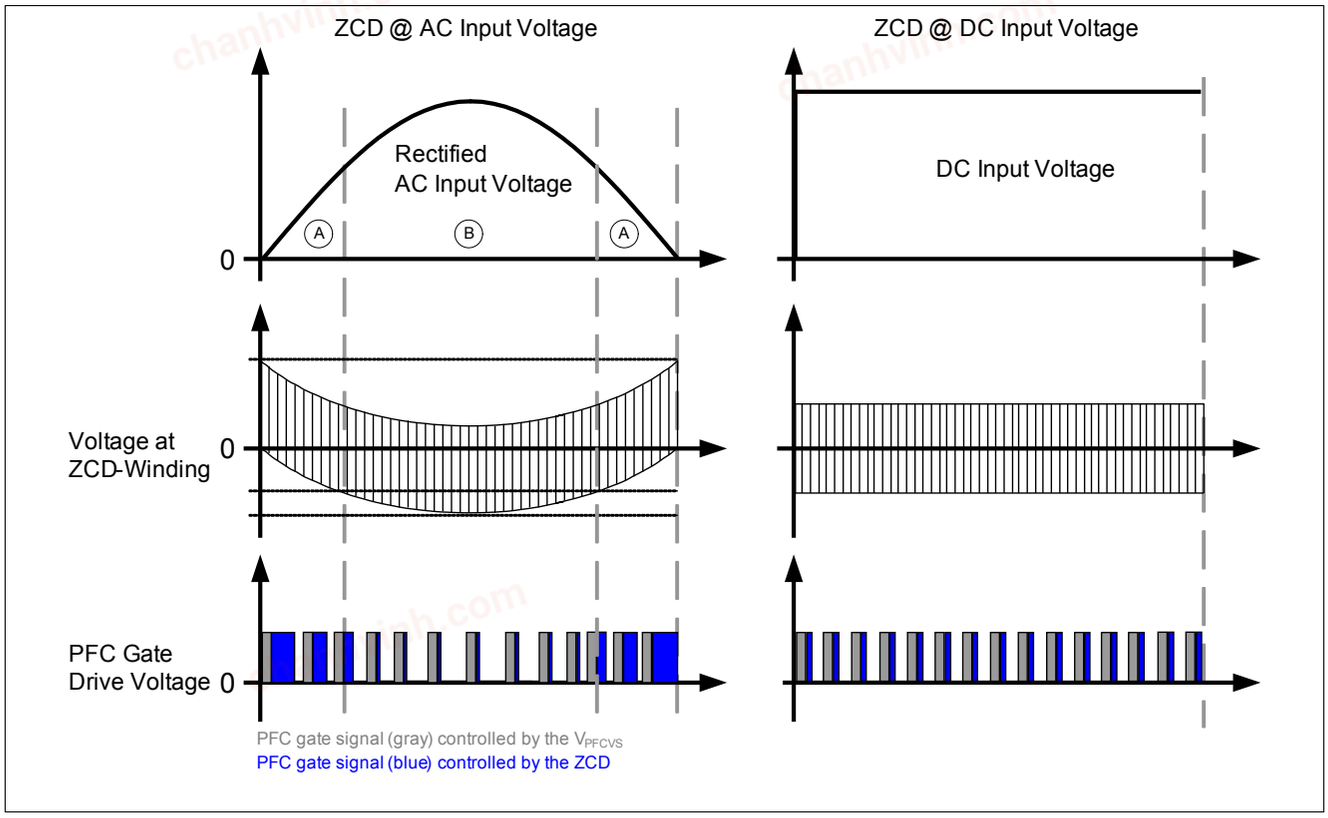


Figure 17 THD Optimization using adjustable Pulse Width Extension

In the case of DC input voltage (see DC input voltage in **Figure 17**), the pulse width gate signal is fixed as a combination of the gate signal controlled by the V_{PFCVS} pin (gray) and the additional pulse width signal controlled by the ZCD pin (blue) shown in **Figure 17** ZCD @ DC input voltage.

The PFC current limitation at pin PFCCS interrupts the ON time of the PFC MOSFET if the voltage drop at the shunt resistors R18 (**Figure 3**) exceeds V_{PFCCS} = 1.0 V (**Figure 16**). This interrupt will restart after the next sufficient signal from ZCD becomes available (Auto Restart). The first value of the resistor can be calculated by the ratio of the PFC mains choke and ZCD winding by the bus voltage and a current of typically 1.5 mA (see equation below for a good practical value of resistance of ZCD). An adjustment of the ZCD resistor causes an optimized THD.

$$R_{ZCD} = \frac{\frac{N_{ZCD}}{N_{PFC}} * V_{BUS}}{1.5mA}$$

2.5 Detection of End-of-Life and Rectifier Effect

Two effects are present by End of Life (EOL): lamp overvoltage (EOL1) and a rectifier effect (EOL2).

After ignition (see 1 in **Figure 18**), the lamp voltage breaks down to its run voltage level with decreasing frequency. On reaching the run frequency, the IC enters the pre-run mode for 625 ms. During this period, the EOL detection is still disabled. In the subsequent run mode (2 in **Figure 18**) the detection of EOL1 (lamp overvoltage; see 3, **Figure 18**) and EOL2 (rectifier effect; see 4, **Figure 18**) is enabled completely.

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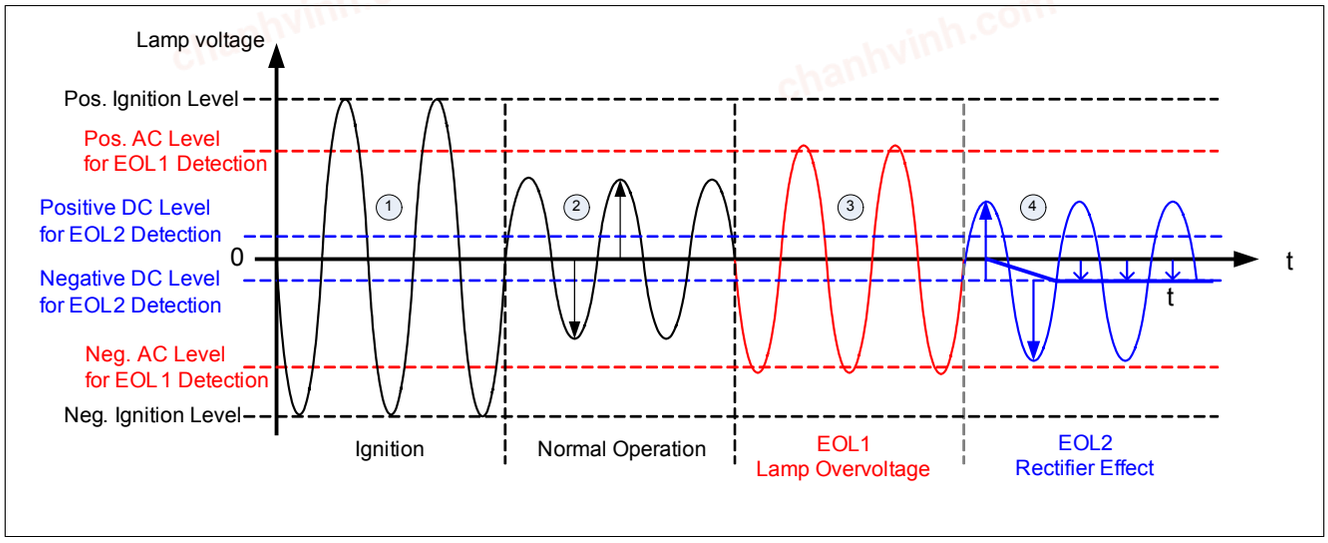


Figure 18 End of Life and Rectifier Effect

2.5.1 Detection of End of Life 1 (EOL1) – Lamp Overvoltage

The event of EOL1 is detected by measuring the positive and negative peak levels of the lamp voltage via an AC current fed into the pin LVS (**Figure 19**). This AC current is fed into the LVS pins via the network R41, R42, R43, R44 and the low pass filter C40 and R45 – see **Figure 3**. If the sensed AC current exceeds 210 μA_{PP} for longer than 620 µs, the status of end-of-life (EOL1) is detected (lamp overvoltage/overload; see **Figure 19** LVSAC current). The EOL1 fault results in a latched power-down mode (after trying a single restart). The controller continuously monitors the status until the EOL1 status changes – e.g. a new lamp is inserted.

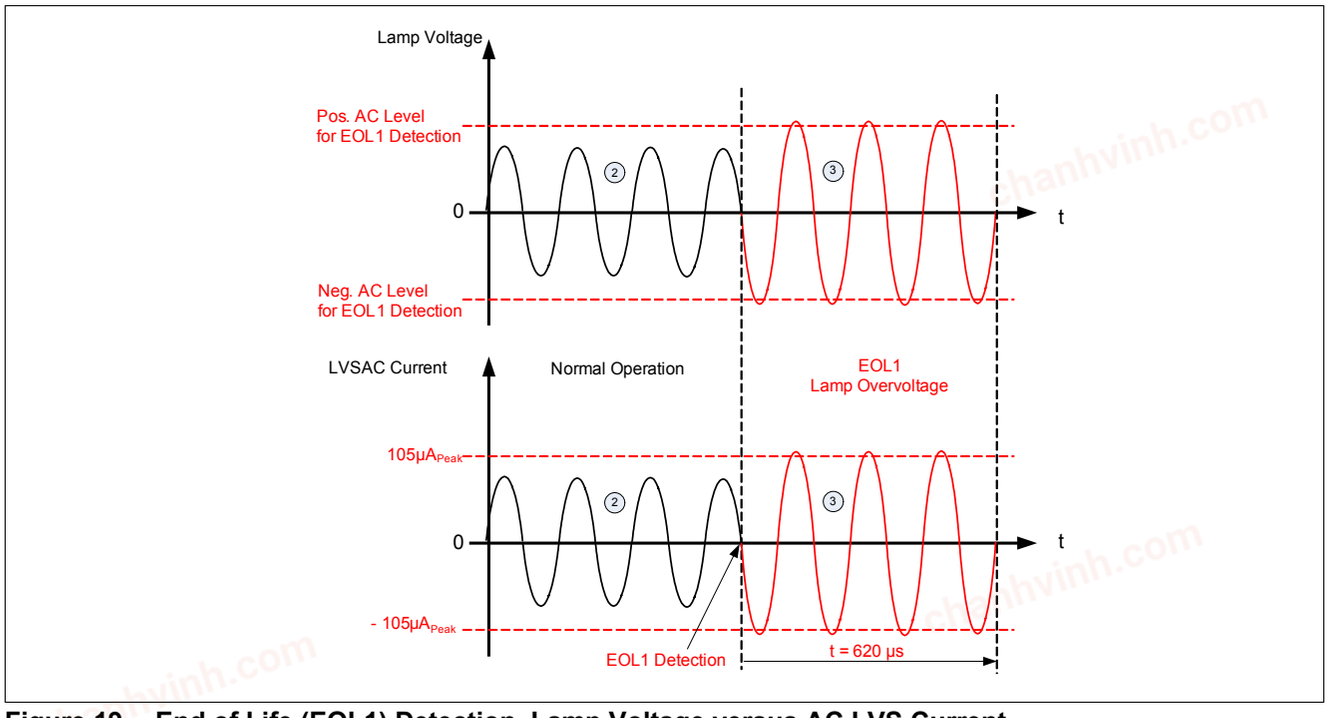


Figure 19 End of Life (EOL1) Detection, Lamp Voltage versus AC LVS Current

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2.5.2 Detection of End of Life 2 (EOL2) – Rectifier Effect

The rectifier effect (EOL2) is detected by measuring the positive and negative DC levels of the lamp voltage via a current fed into the LVS pin (**Figure 20**). This current is fed into the LVS pin via the network R41, R42, R43 and R44 (see **Figure 3**). If the sensed DC current exceeds ± 42 µA (**Figure 20** LVSDC current) for longer than 2500 ms, the status of end-of-life (EOL2) is detected. The EOL2 fault results in a latched power-down mode (after trying a single restart) and the controller is continuously monitoring. The insertion of a new lamp or an interruption of the input voltage resets the status of the IC.

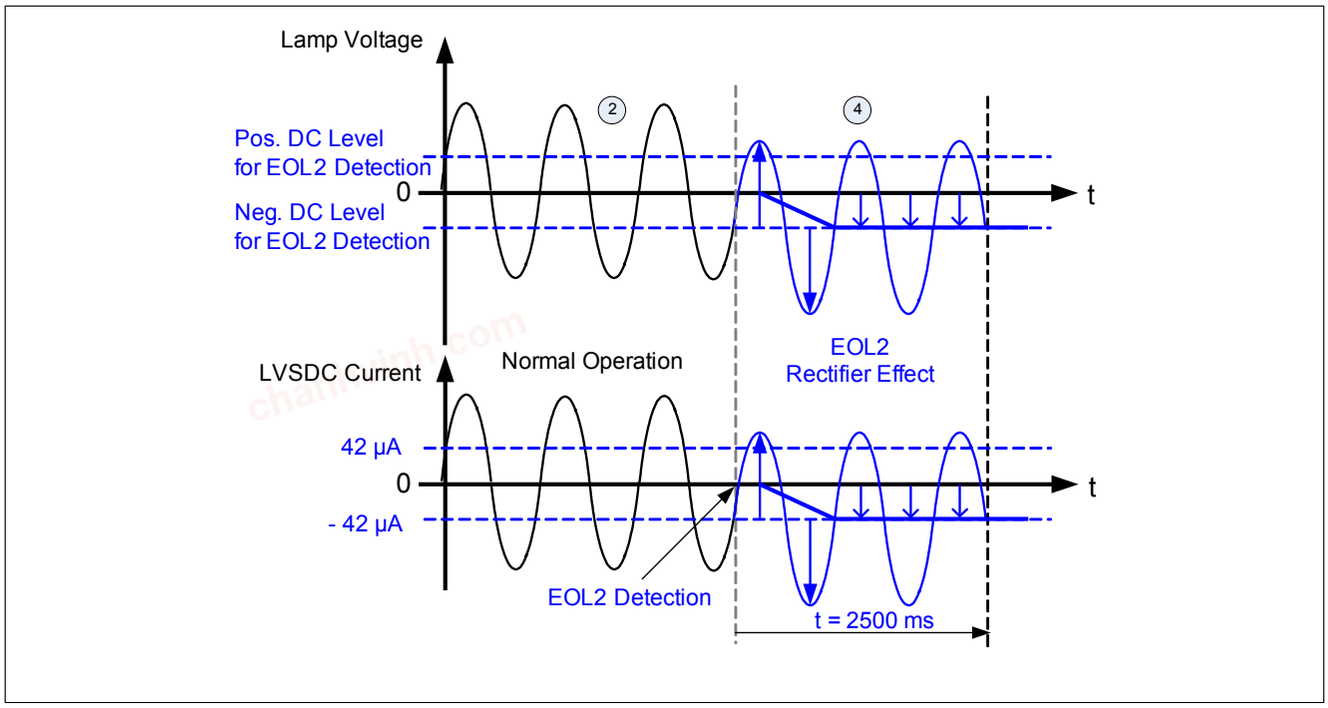


Figure 20 End of Life (EOL2) Detection, Lamp Voltage versus DC LVS Current

2.6 Detection of Capacitive Load

In order to prevent a malfunction in the area of capacitive load (see **Figure 21**) during run mode due to certain deviations from the normal load (e.g. harmed lamp, sudden break of the lamp tube …), the IC has three integrated thresholds – sensed only via the LSCS (pin 2). The controller distinguishes between two different states of capacitive load: detection of working without load (idling detection, CapLoad 1) and working with short overcurrent (CapLoad 2). This state (CapLoad 2) affects operation below the resonance in the capacitive load area (**Figure 23**). In both cases, the IC results in a latched power-down mode after a single restart. After latching the power-down mode, the controller continuously monitors the input voltage and lamp filaments, and restarts after interruption of the input voltage or insertion of a new lamp.

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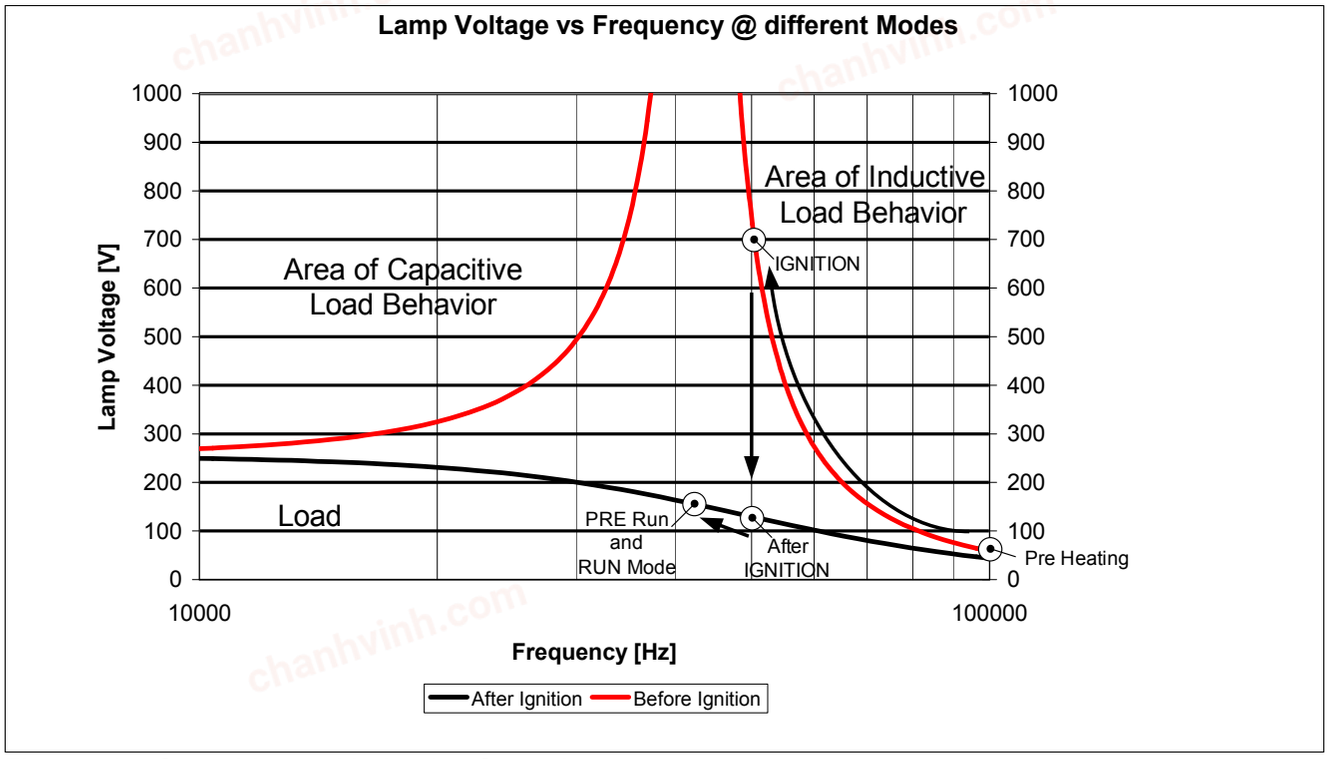


Figure 21 Capacitive and Inductive Operation

2.6.1 Capacitive Load 1 (Idling Detection – Current Mode Preheating)

A capacitive load 1 operation (idling) is detected when the voltage at the LSCS pin is below +50 mV during the second 50 % ON time of the low side MOSFET (see capacitive load 1 (idling) in **Figure 22**). If this status is present for longer than 2500 ms, the controller triggers a latched power-down mode after trying a single restart. The controller keeps monitoring the status continuously until an adequate load is present (e.g. lamp removal); then the IC changes to normal operation.

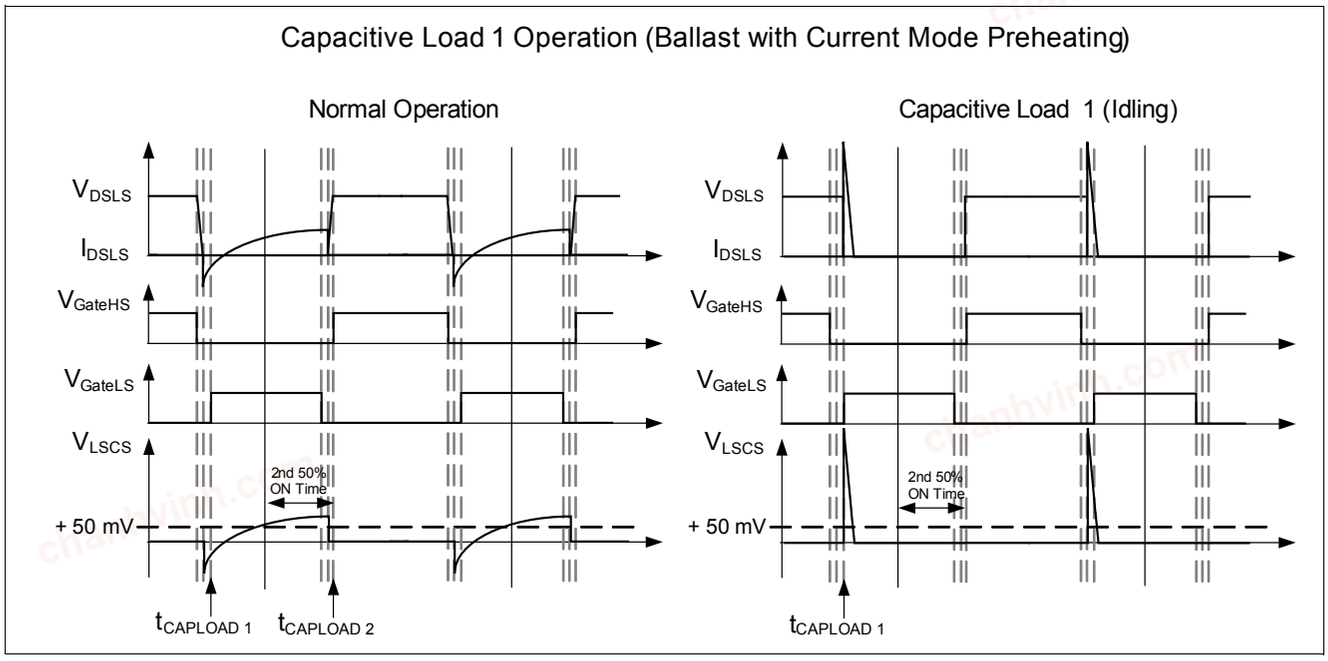


Figure 22 Capacitive Mode 1 Operation without Load during Run Mode

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2.6.2 Capacitive Load 2 (Overcurrent / Operation below Resonance)

A capacitive load 2 operation is detected if the voltage at the LSCS pin drops below a second threshold of V_{LSCS} = –50 mV directly before the high side MOSFET is turned on or exceeds a third threshold of V_{LSCS} = 2.0 V during ON switching of the high side MOSFET. If this overcurrent is present for longer than 620 µs, the IC triggers a latched power-down mode after trying a single restart. The controller keeps monitoring the status continuously until an adequate load is present e.g. a new lamp is inserted; then the IC changes to normal operation.

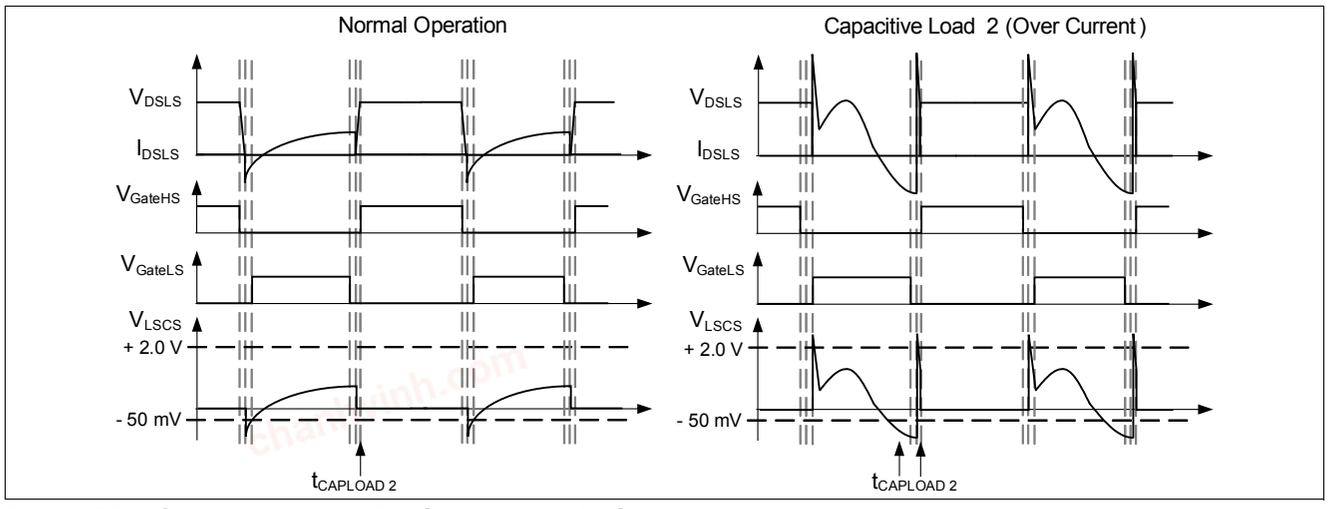


Figure 23 Capacitive Mode 2 – Operation with Overcurrent

2.6.3 Adjustable Self-adapting Dead Time

The dead time between the turn OFF and turn ON of the half-bridge drivers is adjustable (C16, see **Figure 3**) and is detected via a second threshold (–50 mV) of the LSCS voltage. The range of the dead time adjustment is 1.05 µs up to 2.1 µs during all operating modes. The start of the dead time measurement is the OFF switching of the high side MOSFET. The end of the dead time measurement is when V_{LSCS} drops for longer than typically 200 ns (internal fixed propagation delay) below –50 mV. This time will be stored (stored dead time) and the low side gate driver switches ON. The high side gate driver turns ON again after OFF switching of the low side switch and the stored dead time.

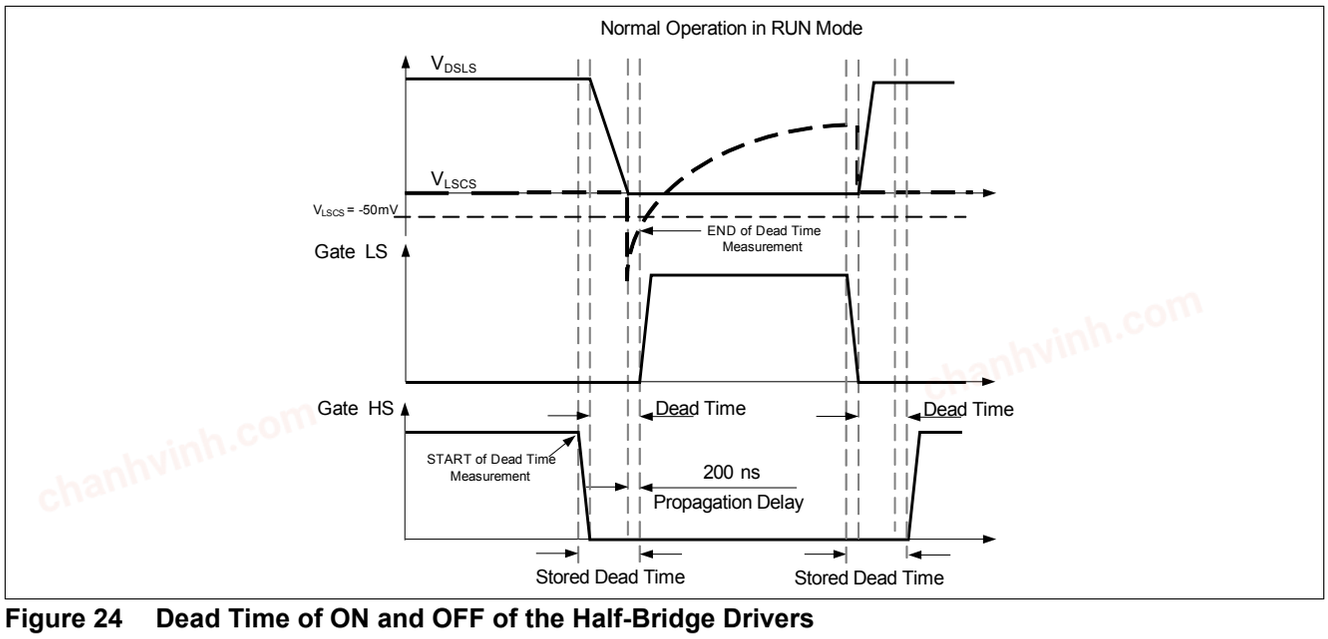


Figure 24 Dead Time of ON and OFF of the Half-Bridge Drivers

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2.7 Emergency Lighting

Line interruptions (bus voltage drops) are detected by the PFCVS. If the rated PFC bus voltage drops below $V_{BUSRated}$ < 75 % during run mode, the controller detects PFC bus undervoltage. In order to meet the emergency lighting standards, the controller distinguishes between two different states of PFC bus undervoltage: short- and a long-term PFC bus undervoltage. A timer increases the time as long as bus undervoltage is present. Short-term bus undervoltage is detected if the timer value stays below t < 800 ms typical (500 ms min.) after the bus voltage reaches the nominal level again. This causes a restart without preheating (emergency standard of VDE0108) – see **Figure 25**. If the timer exceeds t > 800 ms, the controller forces a complete restart of the system due to long-term bus undervoltage (**Figure 26**).

2.7.1 Short-term PFC Bus Undervoltage

Short-term PFC bus undervoltage (**Figure 25**) is detected if the duration of the undervoltage does not exceed 800 ms (timer stays below t < 800 ms, see **Figure 25**). In that case, the PFC and inverter drivers are immediately switched off and the controller continuously monitors the status of the bus voltage in a latched power-down mode (I_{CC} < 170 µA). If the signal at the LVS pin exceeds 18 µA and the rated bus voltage is above 12.5 % while the timer is below t < 800 ms, the controller restarts from power up without preheating. The timer resets to 0 when entering run mode.

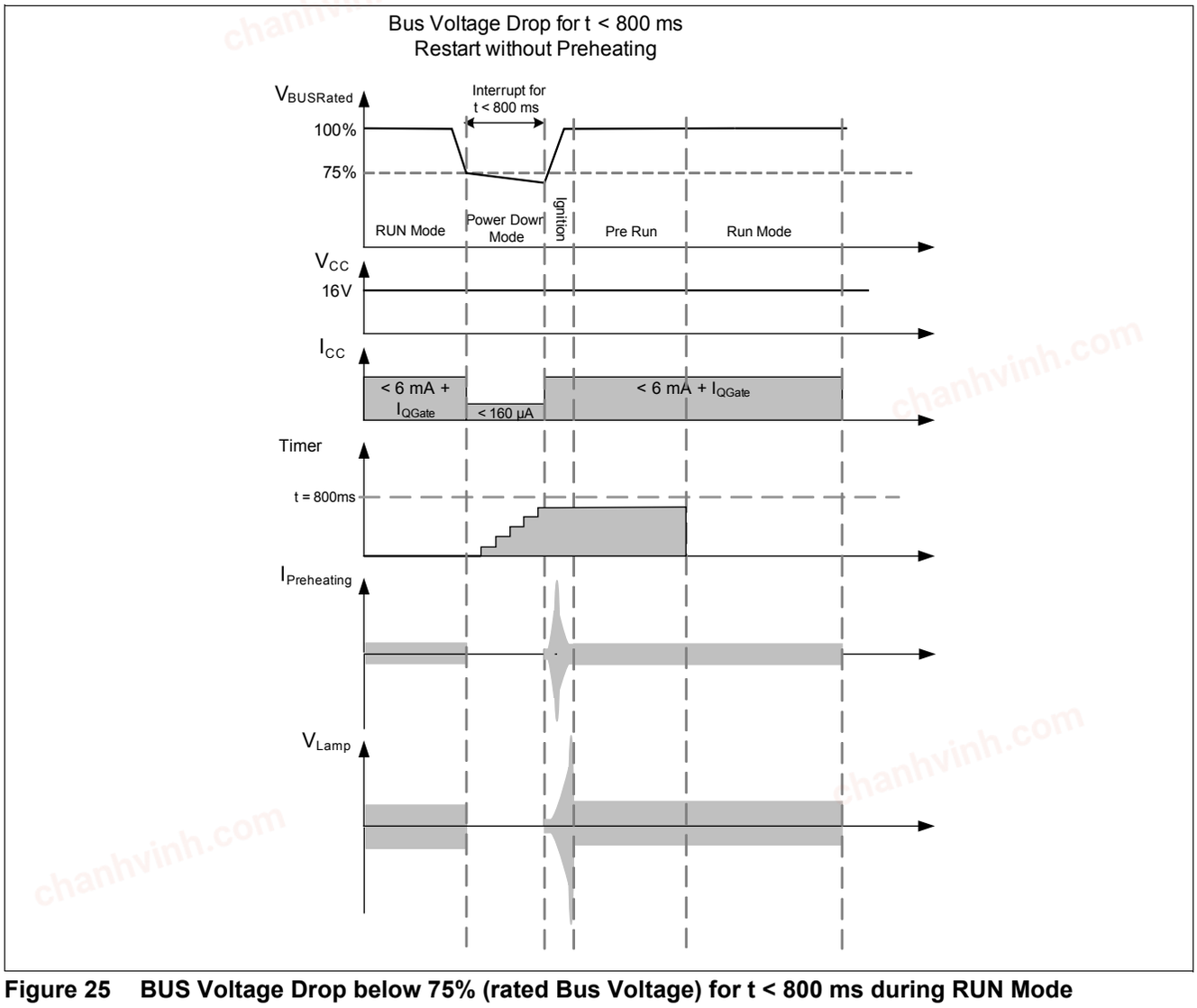


Figure 25 BUS Voltage Drop below 75% (rated Bus Voltage) for t < 800 ms during RUN Mode

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2.7.2 Long-term PFC Bus Undervoltage

If the duration of the bus undervoltage exceeds t > 800 ms (see **Figure 26**), the controller forces an undervoltage lockout (UVLO). The chip supply voltage drops below V_{CC} = 10.6 V and the chip supply current is below I_{CC} < 130 µA. When the Vcc voltage exceeds the 10.6 V threshold again, the IC current consumption is below I_{CC} < 160 µA. In that case, the controller resets the timer and restarts with the full start-up procedure, including monitoring, power-up, start-up, soft start, preheating, ignition, pre-run and run modes, as shown in **Figure 26**.

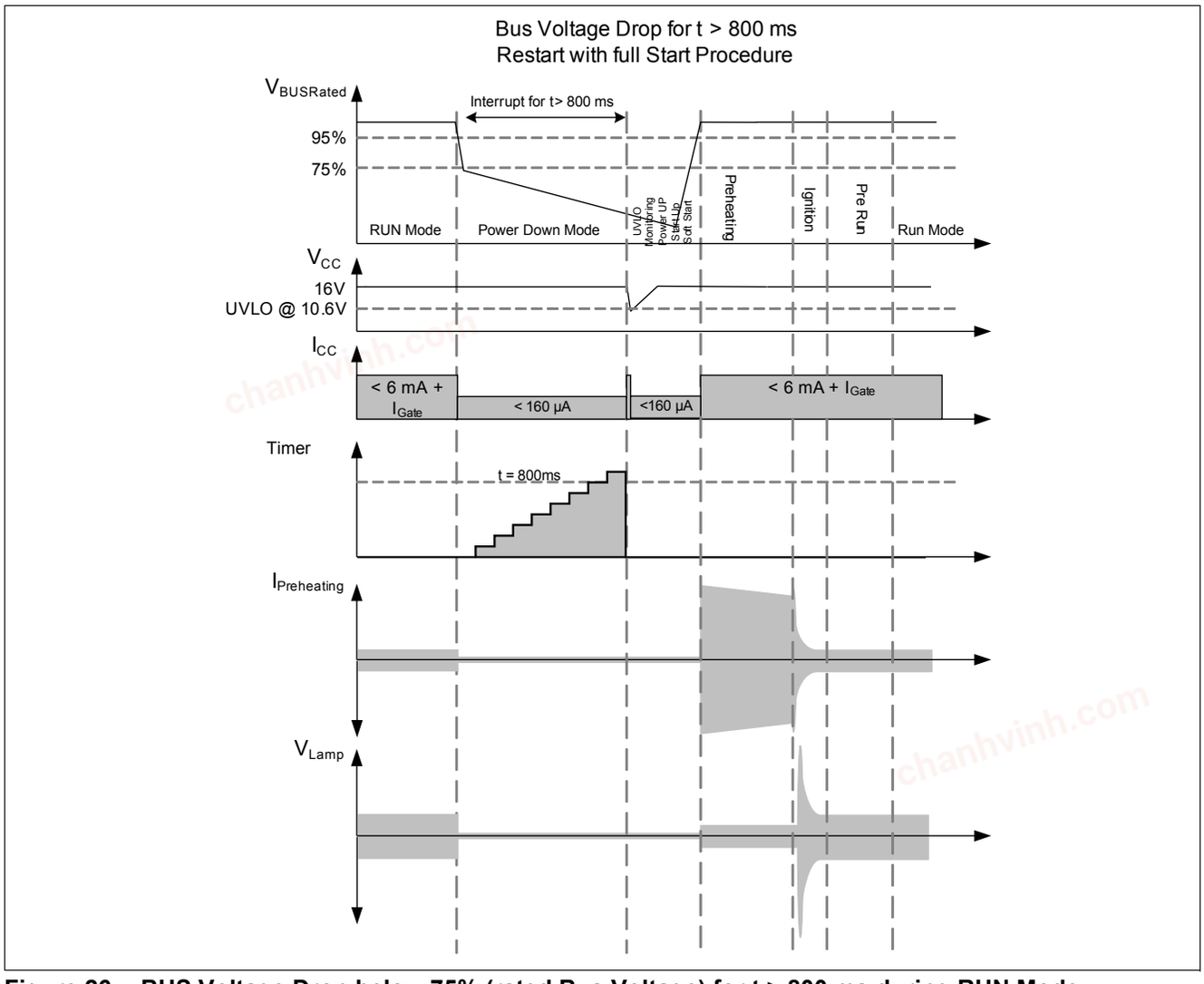


Figure 26 BUS Voltage Drop below 75% (rated Bus Voltage) for t > 800 ms during RUN Mode

2.8 Built-in Customer Test Mode Operation

In order to decrease the final ballast testing time for customers, the 2nd generation of ballast IC supports an integrated built-in Customer Test Mode and several functions to disable some features and states of the IC.

2.8.1 Preheating Test Mode

This feature forces the IC to stay in the preheating mode (see **Section 2.8.1.2**) or to start ignition immediately without any preheating (see **Section 2.8.1.1**). A resistor at this pin defines the duration of the preheating phase. Normally, the preheating phase is in a range of 0 ms up to 2500 ms set via a resistor R_{RTPH} = 0 Ω up to 25 kΩ from the RTPH pin to GND. The preheating phase is skipped when the RTHP pin is set to GND. If the signal at this pin is V_{RTPH} > 5.0 V, the IC remains in the preheating mode.

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2.8.1.1 Skip the Preheating Phase – Set RTPH Pin to GND

Figure 27 shows a standard start-up with a preheating time set via resistor at the RTPH pin 11 to GND (e.g. 8.2 kΩ – this is equal to a preheating phase of approx. 820 ms). The preheating phase can be skipped by setting the RTPH pin 11 directly to GND. In this case, ignition takes place directly after the soft start phase (see Figure 28).

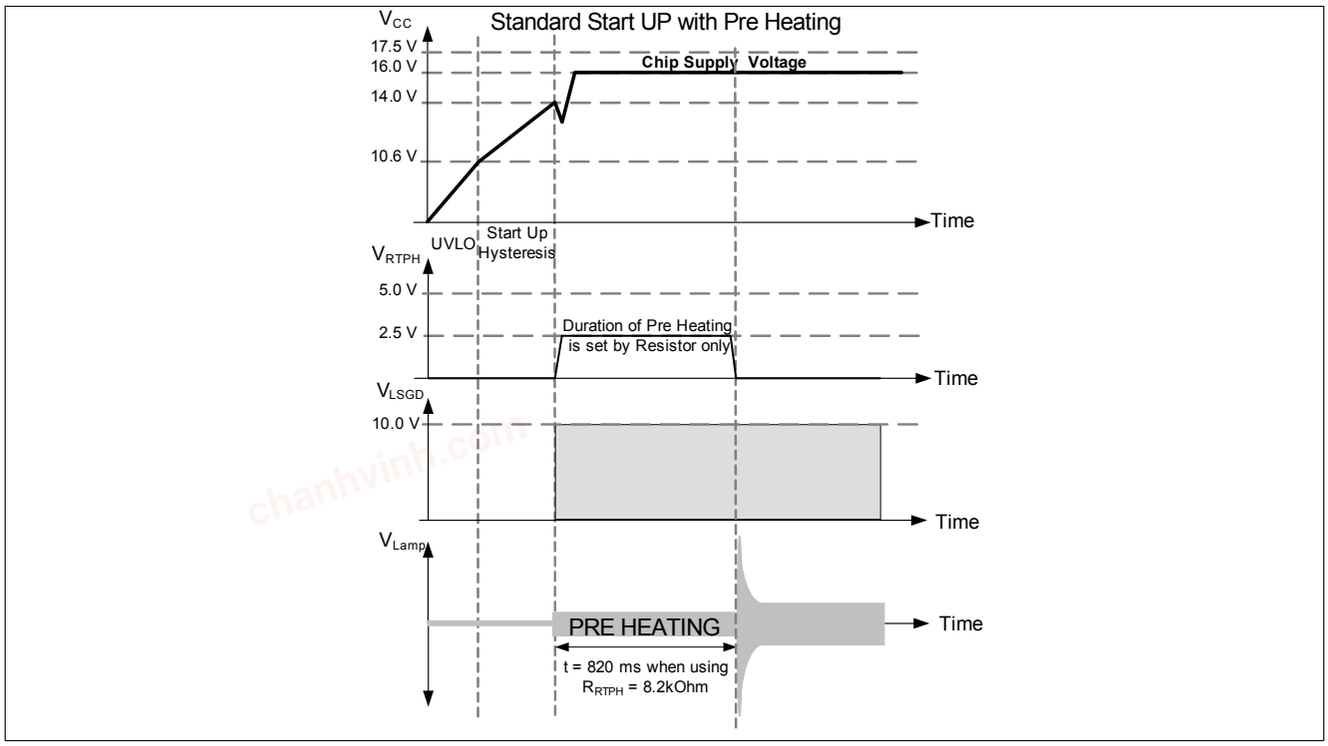


Figure 27 Start-Up WITH Preheating

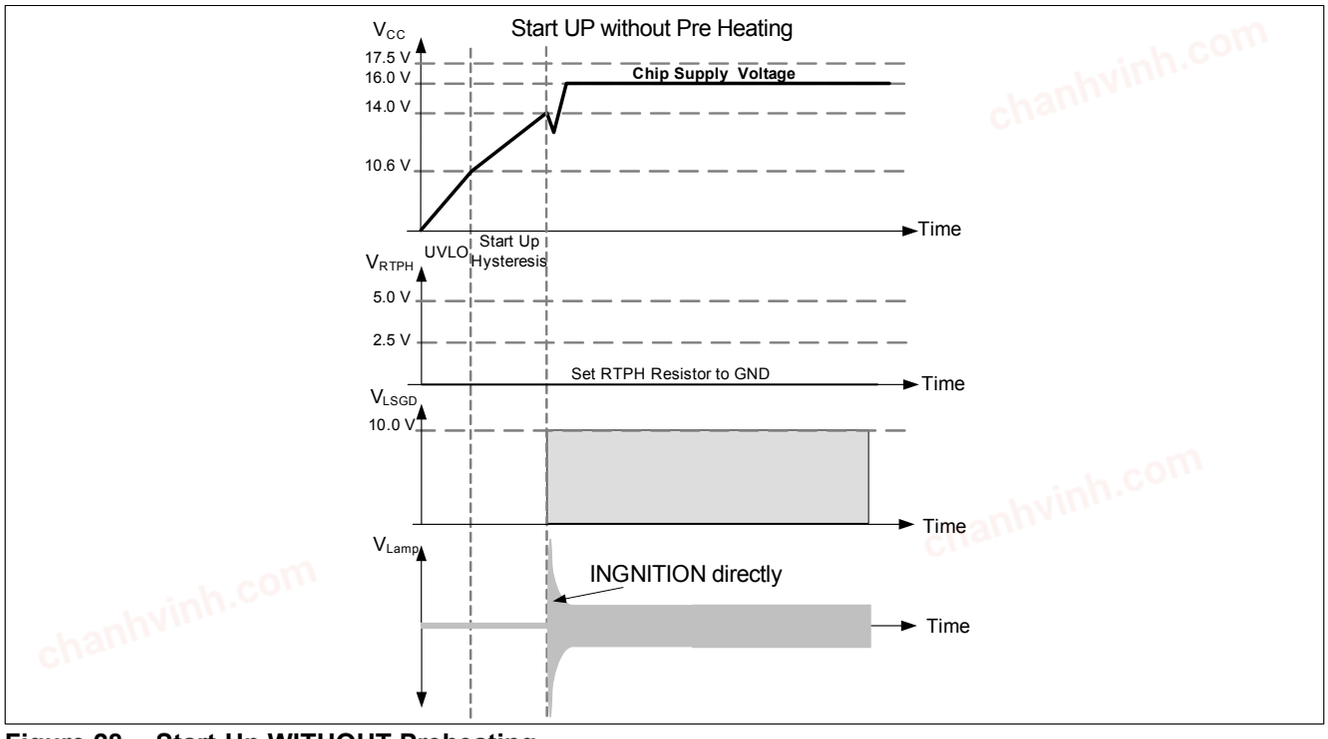


Figure 28 Start-Up WITHOUT Preheating

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2.8.1.2 IC Remains in Preheating Phase

This feature gives the customer the flexibility to align the preheating frequency to the filament power in the preheating phase. **Figure 29** shows a standard start-up with the set preheating time of, for example, 820 ms with an 8.2 kΩ resistor at the RTPH pin 11. To force the IC to remain in preheating, the voltage level at the RTPH pin 11 has to be set to 5.0 V. The duration of this 5.0 V signal defines the time of the preheating (see $I_{PreHeat}$ in **Figure 30**).

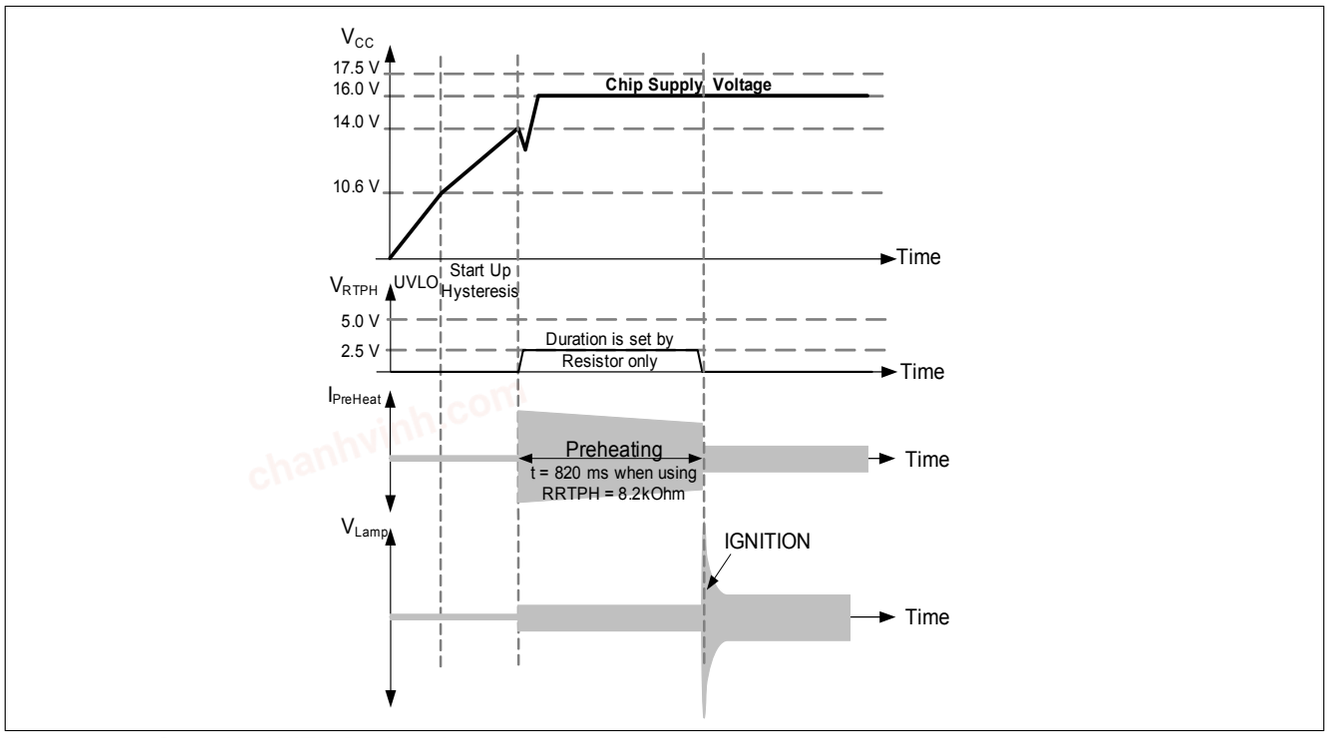


Figure 29 Start-Up WITH Preheating

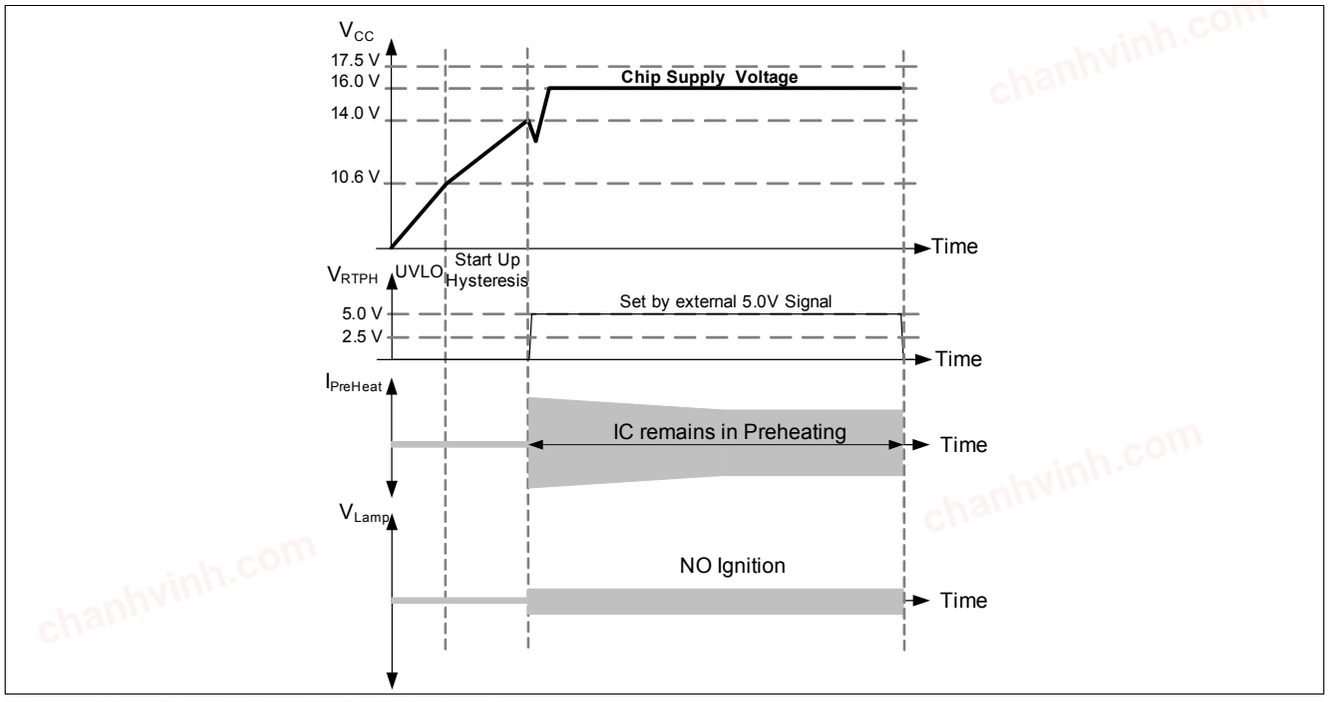


Figure 30 Start-Up WITHOUT Preheating

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2.8.2 Deactivation of the Filament Detection

In order to deactivate the filament detection of the low or high side filament, set the RES pin 13 or the LVS pin to GND. In this case, the IC starts up in normal operation without checking the filaments – e.g. when using an equivalent lamp resistive load instead of a load.

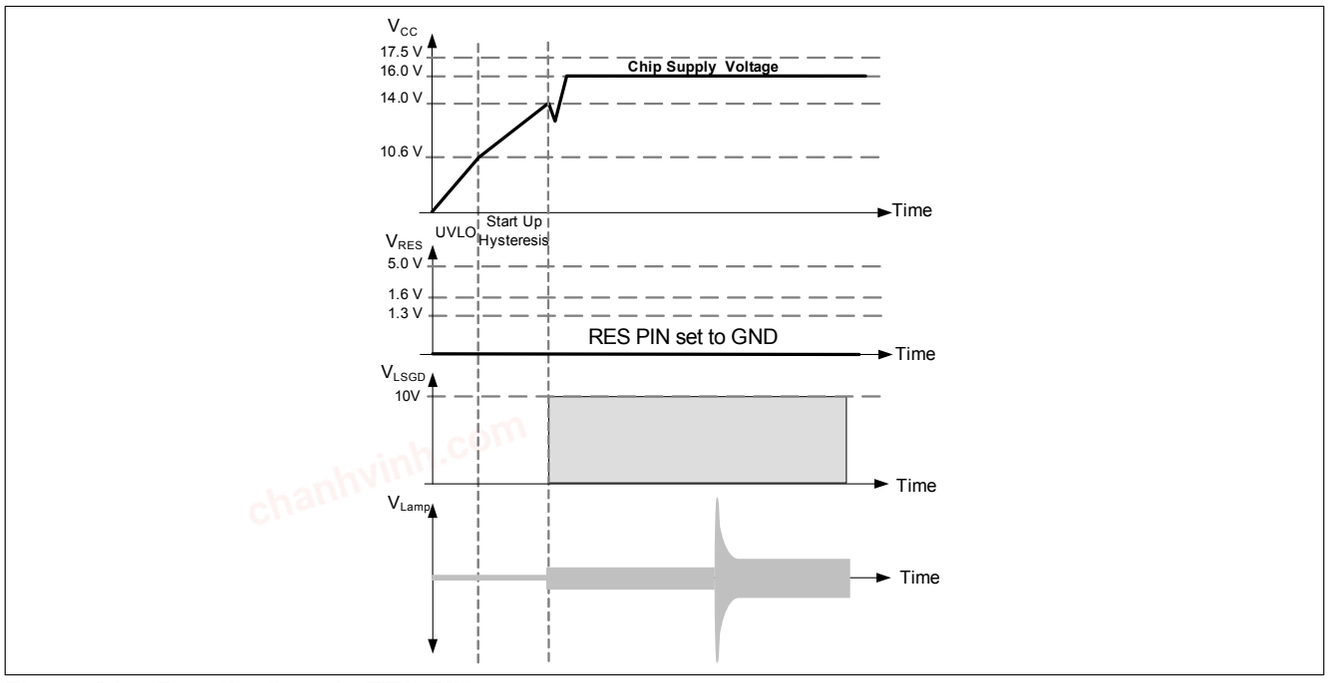


Figure 31 Deactivation via RES PIN

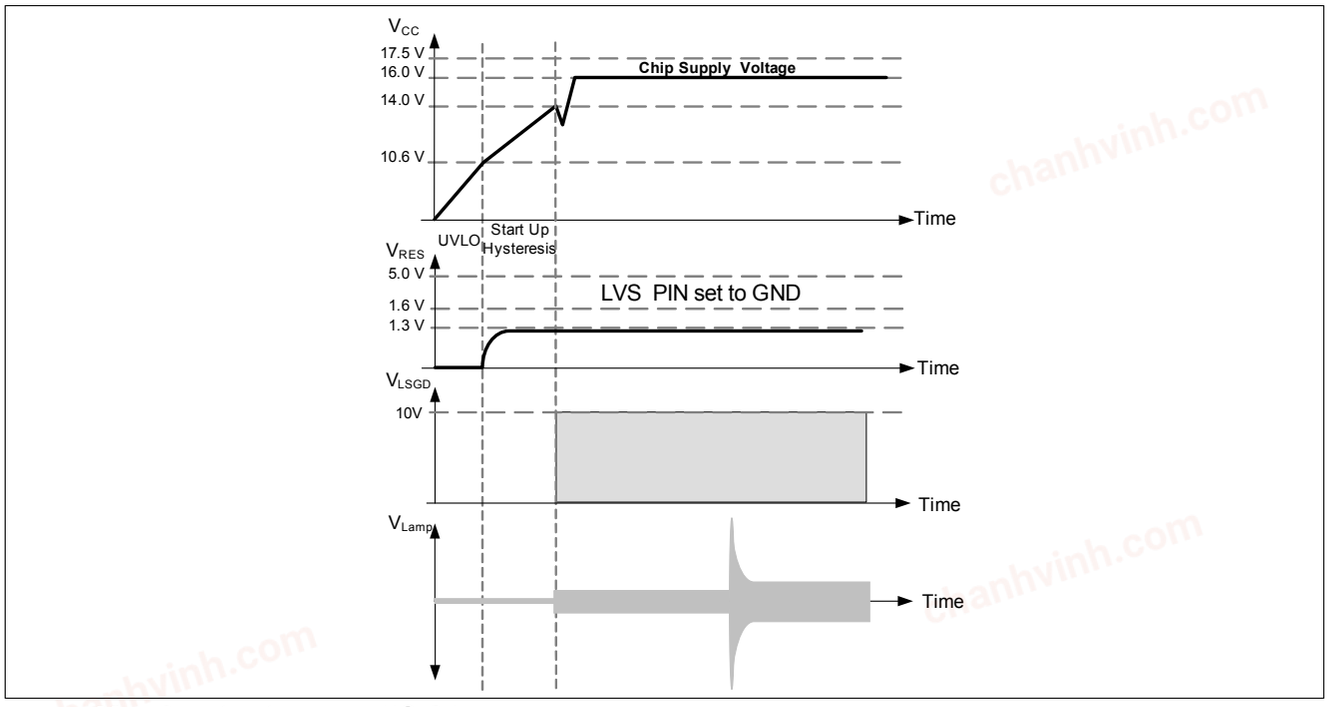


Figure 32 Deactivation via LVS PIN

Figure 31 shows the deactivation of the low and high side filament via set the RES pin 13 to GND. **Figure 32** shows the deactivation of the high side filament detection via set the LVS pin to GND.

Note: An unused LVS pin has to be set to GND.

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2.8.3 Built-in Customer Test Mode (Clock Acceleration)

The built-in customer test mode, supported by this IC, saves testing time for customers in terms of ballast end test. In this mode, the IC accelerates the internal clock in order to reduce the time of the 4 different procedures by the following factors (see **Table 2**).

Table 2 Specified Acceleration Factors

Phase	Duration for Test [ms]	Acceleration Factor	Nominal Duration [ms]
Preheating	625	4	2500 (max)
Time Out Ignition	118.5	2	237
Pre Run Mode	41.7	15	625
EOL2	41.7	60	2500

2.8.3.1 Enabling of the Clock Acceleration

The clock acceleration (Built-in Customer Test Mode) is activated when the chip supply voltage exceeds V_{CC} > 14.0 V and the voltages at the run and preheating frequency pins are set to V_{RFRUN} = V_{RFPH} = 5.0 V (± 5 %) – see **Figure 33**. A RES pin voltage of V_{RES} > 3.5 V up to 5.0 V (± 5 %) prevents a power-up of the IC, the IC remains in a mode before powering up as long as the voltage at the RES pin is V_{RES} > 3.5 V up to 5.0 V (± 5 %) – no power-up.

Note: After the activation of the clock acceleration mode, the voltage level of 5.0 V at the run and preheating frequency pins (V_{RFRUN} = V_{RFPH}) can be released.

2.8.3.2 Starting the Chip with Accelerated Clock

In order to start the IC with an accelerated clock, set the voltage at the RES pin to GND (V_{RES} = 0 V), see **Figure 33**. The IC powers up the system and starts working with an accelerated clock. The duration of the different modes are accelerated by the factors shown in **Table 2**.

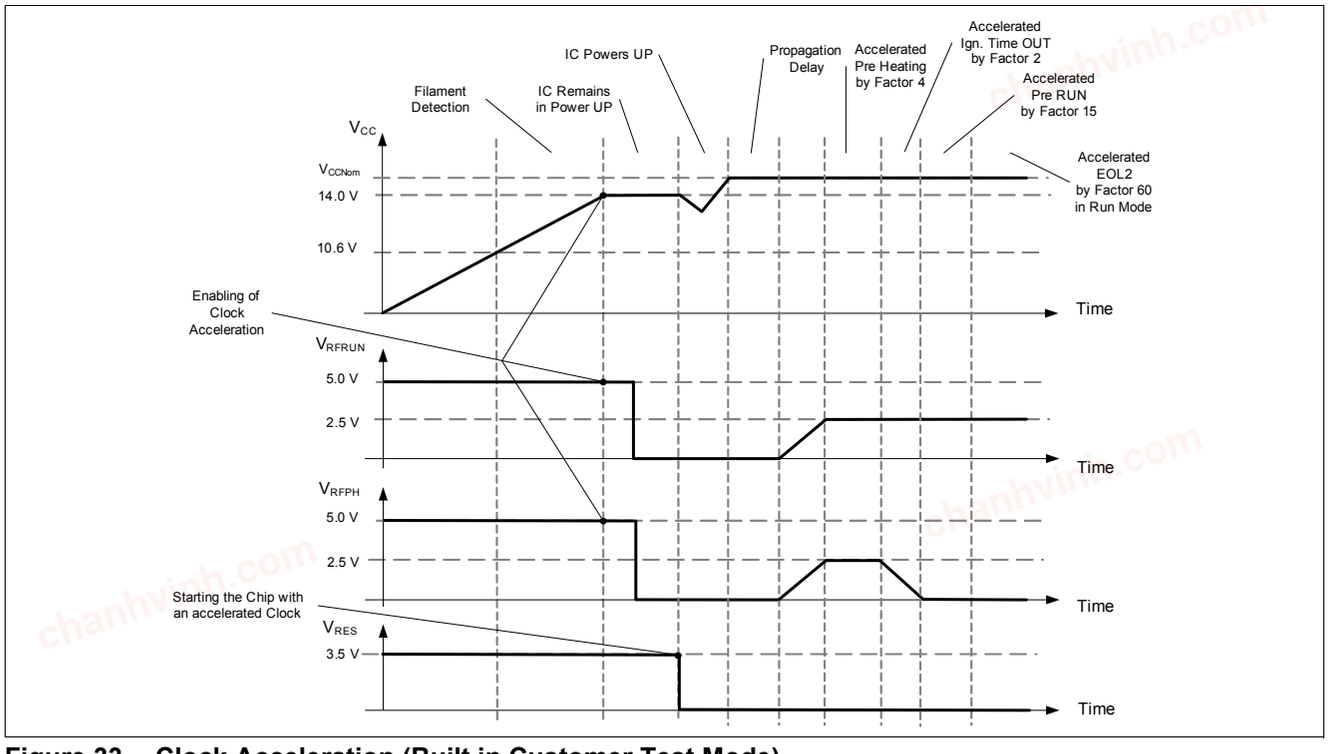


Figure 33 Clock Acceleration (Built in Customer Test Mode)

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3 State Diagram

3.1 Features during Different Operating Modes

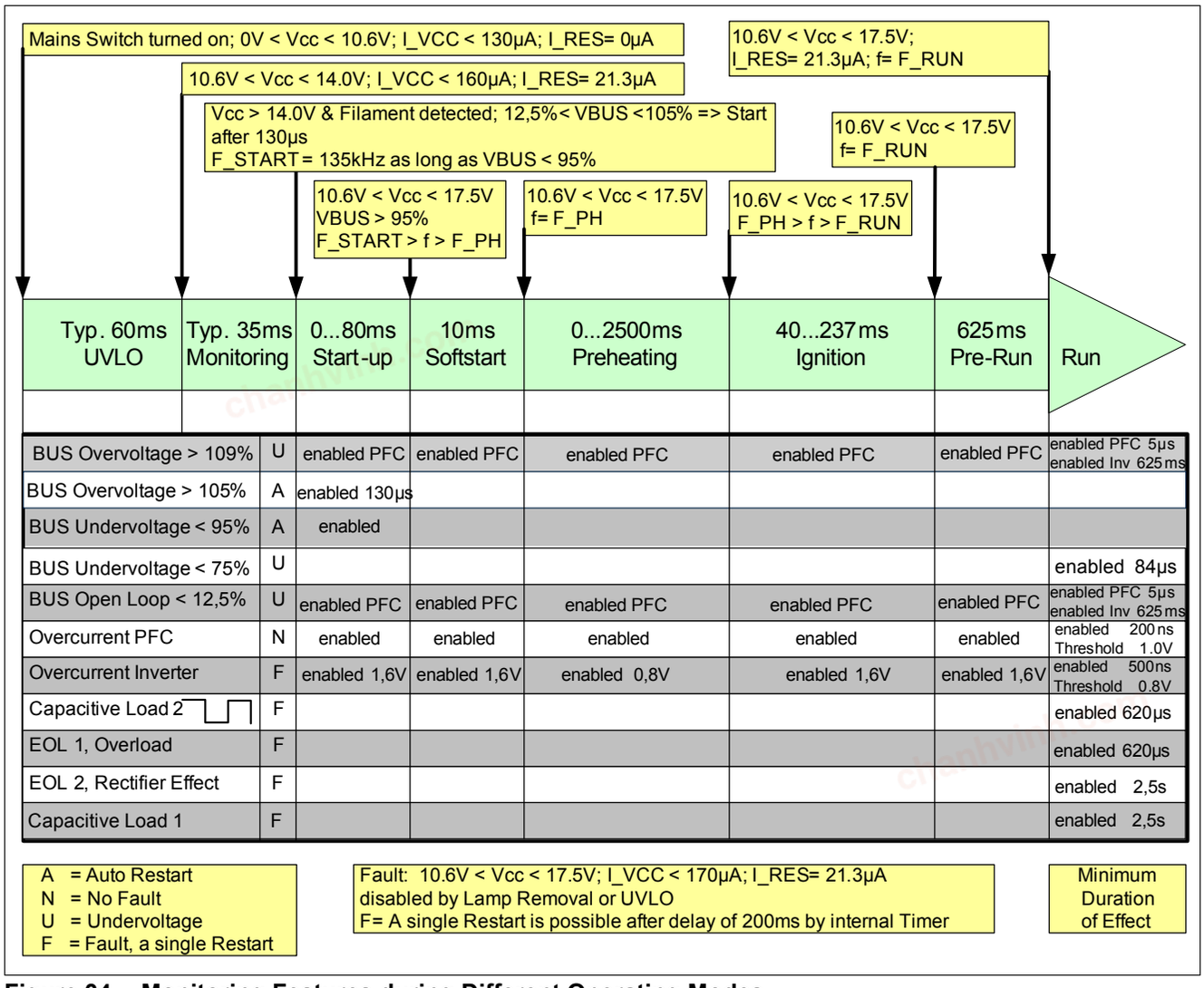


Figure 34 Monitoring Features during Different Operating Modes

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3.2 Operating Flow of the Start-Up Procedure into Run Mode

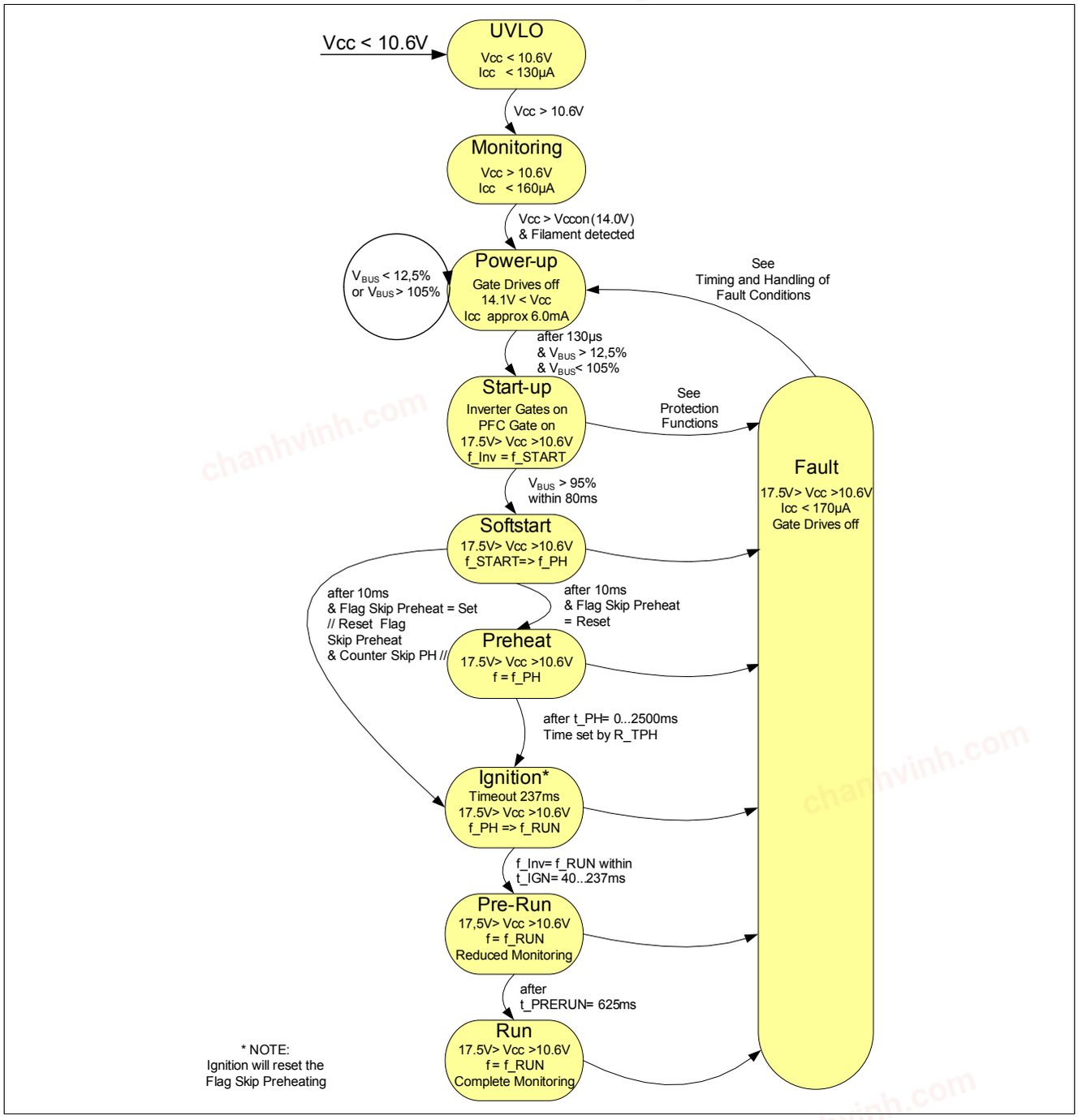


Figure 35 Operating Flow during Start-Up Procedure

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3.3 Auto Restart and Latched Fault Condition Mode

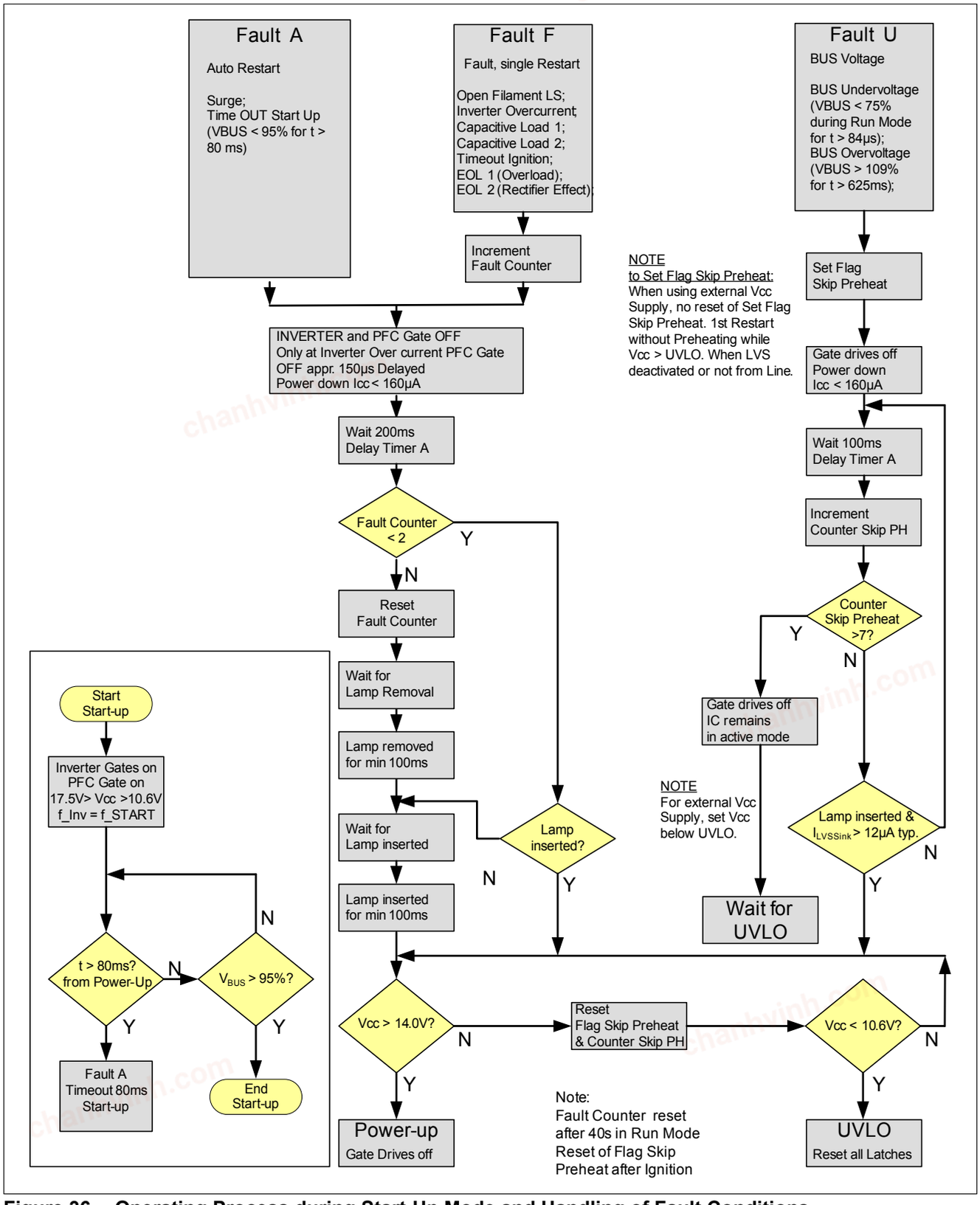


Figure 36 Operating Process during Start-Up Mode and Handling of Fault Conditions

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4 Protection Functions Matrix

Table 3 Protection Functions Matrix

Description of Fault	Characteristics of Fault			Operating Mode Detection Active								Consequence
	Name of Fault	Type of fault	Minimum Duration of effect	Monitoring	Power-up 130 µs	Start-up until V_{BUS} > 95%	Softstart 10ms	Preheat Mode 0 – 2500ms	Ignition Mode 40 – 237ms	Pre-Run Mode 625ms	Run Mode	
Supply voltage V_{cc} < 14.0 V before power-up	Below start-up threshold	S	1µs	X								Prevents power-up
Supply voltage V_{cc} < 10.6 V after power-up	Below UVLO threshold	S	5µs	X	X	X	X	X	X	X	X	Power-down, reset failure latch
Current into LVS pin < 12µA (typ.) before power-up	Open filament HS	S	100µs	X								Prevents power-up
Voltage at RES pin > 1.6 V before power-up	Open filament LS	S	100µs	X								Prevents power-up
Voltage at RES pin > 3.2 V	Open filament LS	F	620µs								X	Power down, latched fault mode, 1 restart
Bus voltage < 12.5% of rated level 10 µs after power-up	Open loop detection	S	1µs		X							Keep Gate drives off, re-start after V_{cc} hysteresis
Bus voltage < 12.5 % of rated level	Open loop detection	N	1µs			X	X	X	X	X	X	Stops PFC FET until V_{BUS} > 12.5%
Bus voltage < 12.5% of rated level	Shut-down option	U	625ms								X	Power down, restart when V_{BUS}> 12.5%
Bus voltage < 75% of rated level add. shut down delay 120µs	Under-voltage	U	84µs								X	Power down, 100ms delay, restart, skip pre-heating max 7 times
Bus voltage < 95% of rated level during start-up	Timeout max start-up time	A	80ms			X						Power down, 200ms delay, restart
Bus voltage > 105% of rated level 10µs after power-up	Over-voltage	S	5µs		X							Keep Gate drives off, re-start after Vcc hysteresis
Bus voltage > 109% of rated level in active operation	PFC overvoltage	N	5µs			X	X	X	X	X	X	Stops PFC FET until V_{BUS}< 105%
Bus voltage > 109% of rated level in active operation	Inverter overvoltage	U	625ms								X	Power down, restart when V_{BUS}<105%
+/- peak level of lamp voltage at pin LVS above threshold	EOL 1 overvoltage	F	620µs								X	Power down, latched fault mode, 1 restart
DC level of lamp voltage above +/- threshold	EOL 2 rect. effect	F	2500ms								X	Power down, latched fault mode, 1 restart
Capacitive load 1	Cap load 1 idling	F	2500ms								X	Power down, latched fault mode, 1 restart
Capacitive load 2, operation below resonance	Cap. load 2 overload	F	620µs								X	Power down, latched fault mode, 1 restart

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Table 3 Protection Functions Matrix (cont'd)

Description of Fault	Characteristics of Fault			Operating Mode Detection Active								Consequence
	Name of Fault	Type of fault	Minimum Duration of effect	Monitoring	Power-up 130 µs	Start-up until V_{BUS} > 95%	Softstart 10ms	Preheat Mode 0 – 2500ms	Ignition Mode 40 – 237ms	Pre-Run Mode 625ms	Run Mode	
Run frequency cannot be achieved	Timeout ignition	F	237ms						X			Power down, latched fault mode, 1 restart
Voltage at PFCCS pin >1.0V	PFC overcurrent	N	200ns			X	X	X	X	X	X	Stops on-time of PFC FET immediately
Voltage at LSCS pin >0.8V	Inverter current lim	N	200ns						X			Activates ignition control
Voltage at LSCS pin >0.8V	Inverter overcurrent	F	500ns					X			X	Power down, latched fault mode, 1 restart
Voltage at LSCS pin >1.6V	Inverter overcurrent	F	500ns			X	X		X	X		Power down, latched fault mode, 1 restart
Inverter overcurrent & VBUS > 109% (Surge)	Surge	A	500ns							X	X	Power-down, restart when V_{BUS} < 109 %
After jump into latched fault mode F wait			200ms	A single restart attempt after delay of internal timer								
Reset of failure latch in run mode after			40s	Reset of failure latch by UVLO or 40 s in run mode								
S = Start-up condition, N = No fault, A = Auto restart , U = Undervoltage												
F = Fault with a single restart; a second F leads to a latched fault *Note: All values @ typical 50 Hz mains frequency*												

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5 Electrical Characteristics

All voltages without the high side signals are measured with respect to ground (pin 4). The high side voltages are measured with respect to pin 17. The voltage levels are valid if other ratings are not violated.

5.1 Absolute Maximum Ratings

Absolute maximum ratings are defined as ratings, which when exceeded may lead to destruction of the integrated circuit. For the same reason, ensure that any capacitor to be connected to pin 3 (V_{CC}) or pin 15 (HSV_{CC}) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
LSCS Voltage	V_{LSCS}	–5	6	V	
LSCS Current	I_{LSCS}	–3	3	mA	
LSGD Voltage	V_{LSGD}	–0.3	V_{cc}+0.3	V	Internally clamped to 11 V
LSGD Peak Source Current	$I_{LSGDsomax}$	–75	5	mA	< 500 ns
LSGD Peak Sink Current	$I_{LSGDsimax}$	–50	400	mA	< 100 ns
VCC Voltage	V_{VCC}	–0.3	18.0	V	
VCC Zener Clamp Current	$I_{VCCzener}$	–5	5	mA	IC in Power Down Mode
PFCGD Voltage	V_{PFCGD}	–0.3	V_{cc}+0.3	V	
PFCGD Peak Source Current	$I_{PFCGDsomax}$	–150	5	mA	< 500 ns
PFCGD Peak Sink Current	$I_{PFCGDsimax}$	–100	700	mA	< 100 ns
PFCCS Voltage	V_{PFCCS}	–5	6	V	
PFCCS Current	I_{PFCCS}	–3	3	mA	
PFCZCD Voltage	V_{PFCZCD}	–3	6	V	
PFCZCD Current	I_{PFCZCD}	–5	5	mA	
PFCVS Voltage	V_{PFCVS}	–0.3	5.3	V	
RFRUN Voltage	V_{RFRUN}	–0.3	5.3	V	
RFPH Voltage	V_{RFPH}	–0.3	5.3	V	
RTPH Voltage	V_{RTPH}	–0.3	5.3	V	
RES Voltage	V_{RES}	–0.3	5.3	V	
LVS Voltage	V_{LVS}	–6	7	V	
LVS Current1	I_{LVS_1}	–1	1	mA	IC in Power Down Mode
LVS Current2	I_{LVS_2}	–3	3	mA	IC in active Mode
HSGND Voltage	V_{HSGND}	–650	650	V	Referring to GND[1)]
HSGND Voltage Transient	dV_{HSGND}/dt	–40	40	V/ns	
HSVCC Voltage	V_{HSVCC}	–0.3	18.0	V	Referring to HSGND
HSGD Voltage	V_{HSGD}	–0.3	V_{HSVCC}+ 0.3	V	Internally clamped to 11V
HSGD Peak Source Current	$I_{HSGDsomax}$	–75	0	mA	< 500 ns
HSGD Peak Sink Current	$I_{HSGDsimax}$	0	400	mA	< 100 ns
Junction Temperature	T_J	–25	150	°C	

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Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Storage Temperature	T_S	–55	150	°C	
Maximum Power Dissipation	P_{TOT}	–	1	W	PG_DSO-16 T_{amb}=25°C
Thermal Resistance (Both Chips) Junction-Ambient	R_{thJA}	–	125[2)]	K/W	PG_DSO-16
Soldering Temperature Wave		–	260	°C	Wave Soldering[3)]
Soldering Temperature Reflow		–	[4)]	°C	Reflow Soldering
ESD Capability HBM	V_{ESD_HBM}	–	2	kV	Human Body Model[5)]
ESD Capability CDM	V_{ESD_CDM}	–	1	kV	Charged Device Model[6)]
Rated Bus Voltage (95%)	$V_{PFCVS95}$	2.33	2.43	V	

1) Limitation due to voltage capability in end test
2) @Ta = 85°C & PCB area >30mmx20mm
3) According to JESD22A111
4) According to J-STD-020D
5) According to EIA/JESD22-A114-B
6) According to JESD22-C101

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5.2 Operating Range

The IC operates as described in the functional description once the values listed here lie within the operating range.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
HSVCC Supply Voltage	V_{HSVCC}	$V_{HSVCCOff}$	17.5	V	Referring to HSGND
HSGND Voltage	V_{HSGND}	–650	650	V	Referring to GND[1)]
VCC Voltage @ 25°C	V_{VCC}	V_{VCCOff}	17.5	V	T_J = 25°C
VCC Voltage @ 125°C	V_{VCC}	V_{VCCOff}	18.0	V	T_J = 125°C
LSCS Voltage Range	V_{LSCS}	–4	5	V	In active mode
PFCVS Voltage Range	V_{PFCVS}	0	4	V	
PFCCS Voltage Range	V_{PFCCS}	–4	5	V	In active mode
PFZCD Current Range	I_{PFCZCD}	–3	3	mA	In active mode
LVS Voltage Range	V_{LVS}	–6	6[2)]	V	
LVS Current Range	I_{LVS}	[3)]	210	µA	IC Power Down Mode
LVS Current Range	I_{LVS}	–2.5	2.5	mA	IC active mode
RFPH Frequency	$F_{RFPHrange}$	F_{RUN}	150	kHz	
RFPH Source Current Range	I_{RFPH}	–500	0	µA	@ V_{RFPH} = 2.5 V
RTPH Voltage Range	V_{RTPH}	0	2.5	V	
Junction Temperature	T_j	–25	125	°C	
Adjustable Preheating Freq.	F_{RFPH}	F_{RFRUN}	150	kHz	Range set by RFPH
Adjustable Run Frequency	F_{RFRUN}	20	120	kHz	Range set by RFRUN
Adjustable Preheating Time	t_{RTPH}	0	2500	ms	Range set by RTPH
Set Resistor for Run Feq.	R_{RFRUN}	4	25	kΩ	
Set Resistor for Preheat Feq.	R_{RFPH}	4	–	kΩ	R_{RFRUN} parallel to R_{RFPH}
Set Resistor for Preheat Time	R_{RTPH}	0	25	kΩ	
Mains Frequency	f_{Mains}	45	65	Hz	NOTCH Filter Operation

1) Limitation due to creeping distance between the HS&LS Pins
2) Limited by Maximum of Current Range at LVS
3) Limited by Minimum of Voltage Range at LVS

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5.3 Characteristics

5.3.1 Power Supply Section

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from –25 °C to +125 °C. Typical values represent the median values, which are related to 25 °C. Unless otherwise stated, a supply voltage of 15 V and V_{HSVCC} = 15 V is assumed and the IC operates in active mode. Furthermore, all voltages refer to GND if not otherwise stated.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
VCC Quiescent Current1	I_{VCCqu1}	–	90	130	µA	V_{VCC} = V_{VCCOff} – 0.5V
VCC Quiescent Current2	I_{VCCqu2}	–	120	160	µA	V_{VCC} = V_{VCCOn} – 0.5V
VCC Supply Current[1)]	$I_{VCCSupply}$	–	4.2	6.0	mA	V_{PFCVS} > 2.725V
VCC Supply Current in Latched Fault Mode	$I_{VCCLatch}$	–	110	170	µA	V_{RES} = 5V
LSVCC Turn-On Threshold LSVCC Turn-Off Threshold LSVCC Turn-On/Off Hyst.	V_{VCCOn} V_{VCCOff} V_{VCCHys}	13.5 10.0 3.2	14.0 10.6 3.6	14.5 11.0 4.0	V V V	Hysteresis
VCC Zener Clamp Voltage	$V_{VCCClamp}$	15.5	16.3	16.9	V	I_{VCC} = 2mA/V_{RES} = 5V
VCC Zener Clamp Current	$I_{VCCZener}$	2.5	–	5	mA	V_{VCC} = 17.5V/V_{RES} = 5V
High Side Leakage Current	$I_{HSGNDleak}$	–	0.01	2	µA	V_{HSGND} = 650V, V_{GND}=0V
HSVCC Quiescent Current	$I_{HSVCCqu1}$[2)]	–	190	280	µA	V_{HSVCC} = $V_{HSVCCOn}$ – 0.5V
HSVCC Quiescent Current[1)]	$I_{HSVCCqu2}$[2)]	0.3	0.65	1.2	mA	V_{HSVCC} > $V_{HSVCCOn}$
HSVCC Turn-On Threshold HSVCC Turn-Off Threshold HSVCC Turn-On/Off Hyst.	$V_{HSVCCOn}$[2)] $V_{HSVCCOff}$[2)] $V_{HSVCCHy}$[2)]	9.8 8.1 1.4	10.4 8.6 1.7	11.0 9.3 2.0	V V V	Hysteresis
Low Side Ground	GND					

1) With inactive gate

2) Referring to High Side Ground (HSGND)

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5.3.2 PFC Section

5.3.2.1 PFC Current Sense (PFCCS)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Turn – Off Threshold	$V_{PFCCSOff}$	0.95	1.0	1.05	V	
Over Current Blanking + Propagation Delay[1]	$t_{PFCCSOff}$	140	200	260	ns	
Leading Edge Blanking	$t_{Blanking}$	180	250	310	ns	Pulse width when V_{PFCCS} > 1.0 V
PFCCS Bias Current	$I_{PFCCSBias}$	–0.5	–	0.5	µA	V_{PFCCS} = 1.5V

1) Propagation delay = 50 ns

5.3.2.2 PFC Zero Current Detection (PFCZCD)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Zero Crossing upper Thr.[1]	$V_{PFCZCDUp}$	1.4	1.5	1.6	V	
Zero Crossing lower Thr.[2]	$V_{PFCZCDLow}$	0.4	0.5	0.6	V	
Zero Crossing Hysteresis	$V_{PFCZCDHys}$	–	1.0	–	V	
Clamping of pos. Voltages	$V_{PFCZCDpclp}$	4.1	4.6	5.1	V	$I_{PFCZCDSink}$ = 2mA
Clamping of neg. Voltages	$V_{PFCZCDnclp}$	–1.7	–1.4	–1.0	V	$I_{PFCZCDSource}$ = –2mA
PFCZCD Bias Current	$I_{PFCZCDBias}$	–0.5	–	5.0	µA	V_{PFCZCD} = 1.5V
PFCZCD Bias Current	$I_{PFCZCDBias}$	–0.5	–	0.5	µA	V_{PFCZCD} = 0.5V
PFCZCD Ringing Su.[3] Time	$t_{Ringsup}$	350	500	650	ns	
Limit Value for ON Time Extension	$\Delta t \times I_{ZCD}$	500	700	900	pAxs	

1) Turn OFF threshold
2) Turn ON threshold
3) Ringing Suppression Time

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5.3.2.3 PFC Bus Voltage Sense (PFCVS)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Trimmed Reference Voltage	$V_{PFCVSRef}$	2.47	2.50	2.53	V	± 1.2 %
Overvoltage turn Off (109%)	$V_{PFCVSRUp}$	2.68	2.73	2.78	V	
Overvoltage turn On (105%)	$V_{PFCVSLow}$	2.57	2.63	2.68	V	
Overvoltage Hysteresis	$V_{PFCVSHys}$	70	100	130	mV	4 % rated bus voltage
Under voltage (75%)	$V_{PFCVSUV}$	1.835	1.88	1.915	V	
Under voltage (12.5%)	$V_{PFCVSUV}$	0.237	0.31	0.387	V	
Rated Bus Voltage (95%)	$V_{PFCVS95}$	2.325	2.38	2.425	V	
PFCVS Bias Current	$I_{PFCVSBias}$	–1.0	–	1.0	µA	V_{PFCVS} = 2.5V

5.3.2.4 PFC PWM Generation

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Initial ON – Time[1)]	$t_{PFCON_initial}$	–	4.0	–	µs	V_{PFCZCD} = 0V
Max. ON – Time[2)]	t_{PFCON_max}	18.0	24.0	28.0	µs	0.45V < VPFCVS < 2.45V
Switch Threshold from CritCM into DCM	t_{PFCON_min}	160	270	370	ns	
Repetition Time[1)]	t_{PFCRep}	47	52	57	µs	V_{PFCZCD} = 0V
Off Time	t_{PFCOff}	42	47	52	µs	

1) When missing Zero Crossing Signal
2) At the maxima of the AC Line Input Voltage

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5.3.2.5 PFC gate Drive (PFCGD)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
PFCGD Low Voltage	$V_{PFCGDLow}$	0.4	0.7	0.9	V	I_{PFCGD} = 5mA
		0.4	0.75	1.1	V	I_{PFCGD} = 20mA
		–0.2	0.3	0.6	V	I_{PFCGD} = -20mA
PFCGD High Voltage	$V_{PFCGDHigh}$	10.0	11.0	11.6	V	I_{PFCGD} = -20mA
		9.0	–	–	V	I_{PFCGD} = -1mA / V_{VCC} [1]
		8.5	–	–	V	I_{PFCGD} = -5mA / V_{VCC} [1]
PFCGD active Shut Down	$V_{PFCGASD}$	0.4	0.75	1.1	V	I_{PFCGD} = 20mA V_{VCC}=5V
PFCGD UVLO Shut Down	$V_{PFCGDuvlo}$	0.3	1.0	1.5	V	I_{PFCGD} = 5mA V_{VCC}=2V
PFCGD Peak Source Current	$I_{PFCGDSouce}$	–	–100	–	mA	[2]+[3]
PFCGD Peak Sink Current	$I_{PFCGDSink}$	–	500	–	mA	[2]+[3]
PFCGD Voltage during sink Current	$V_{PFCGDHigh}$	11.0	11.7	12.3	V	$I_{PFCGDSinkH}$ = 3mA
PFC Rise Time	$t_{PFCGDRise}$	100	245	405	ns	2V > V_{LSGD} > 8V [2]
PFC Fall Time	$t_{PFCGDFall}$	20	45	70	ns	8V > V_{LSGD} > 2V [2]

1) $V_{VCC} = V_{VCCOff} + 0.3$ V
2) $R_{Load} = 4\Omega$ and $C_{Load} = 3.3$ nF
3) The parameter is not subject to a production test – verified by design / characterization

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5.3.3 Inverter Section

5.3.3.1 Low Side Current Sense (LSCS)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Overcurrent Shut Down Volt.	$V_{LSCSOvC1}$	1.5	1.6	1.7	V	1)
Overcurrent Shut Down Volt.	$V_{LSCSOvC2}$	0.75	0.8	0.85	V	2)
Duration of Overcurrent	$t_{LSCSOvC}$	450	600	700	ns	
Capacitive Mode Det. Level 1	$V_{LSCSCap1}$	30	50	73	mV	During Run Mode
Capacitive Mode Duration 1	$t_{LSCSCap1}$	–	280	–	ns	3)
Capacitive Mode Det. Level 2	$V_{LSCSCap2}$	1.8	2.0	2.2	V	During Run Mode
Capacitive Mode Duration 2	$t_{LSCSCap2}$	–	50	–	ns	4)
Capacitive Mode Det. Level 3	$V_{LSCSCap3}$	–70	-50	-27	mV	
Capacitive Mode Duration 3	$t_{LSCSCap3}$	–	280	–	ns	5)
LSCS Bias Current	$I_{LSCSBias}$	–1.0	–	1.0	µA	@ V_{LSCS} = 1.5V

1) Overcurrent Voltage Threshold active during: Start Up, Soft start, Ignition and pre-run Mode
2) Overcurrent Voltage Threshold active during: Preheating and Run Mode
3) During 2nd 50% Duty Cycle of LSGD in Run Mode
4) Active during Turn ON of the HSGD in Run Mode
5) Active before Turn ON of the HSGD in Run Mode

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5.3.3.2 Low Side Gate Drive (LSGD)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
LSGD Low Voltage	$V_{LSGDLow}$	0.4	0.7	1.0	V	I_{LSGD} = 5mA[1]
		0.4	0.8	1.2	V	I_{LSGD} = 20mA[1]
		–0.3	0.2	0.5	V	I_{LSGD} = - 20mA (Source)
LSGD High Voltage	$V_{LSGDHigh}$	10.0	10.8	11.6	V	[2]
		9.0	–	–	V	[3]
		8.5	–	–	V	[4]
LSGD active Shut Down	$V_{LSGDASD}$	0.4	0.75	1.1	V	V_{CC}=5V / I_{LSGD} = 20mA[1]
LSGD UVLO Shut Down	$V_{LSGDUVLO}$	0.3	1.0	1.5	V	V_{CC}=2V / I_{LSGD} = 5mA[1]
LSGD Peak Source Current	$I_{LSGDSource}$	–	–50	–	mA	[5]+[6]
LSGD Peak Sink Current	$I_{LSGDSink}$	–	300	–	mA	[5]+[6]
LSGD Voltage during [1]	$V_{LSGDHigh}$	–	11.7	–	V	$I_{LSGDsinkH}$ = 3mA
LSGD Rise Time	$t_{LSGDRise}$	100	245	405	ns	2V < V_{LSGD} < 8V[5]
LSGD Fall Time	$t_{LSGDFall}$	20	35	60	ns	8V > V_{LSGD} > 2V[5]

1) Sink Current
2) I_{LSGD} = - 20mA Source Current
3) V_{CCOFF} + 0.3V and ILSGD = - 1mA Source Current
4) V_{CCOFF} + 0.3V and ILSGD = - 5mA Source Current
5) Load: R_{Load} = 10Ω and C_{Load} = 1nF
6) The parameter is not subject to a production test – verified by design / characterization

5.3.3.3 Inverter Control Run (RFRUN)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Fixed Start – Up Frequency	$F_{StartUp}$	121.5	135	148.5	kHz	
Duration of Soft Start	$t_{SoftStart}$	9	11	13.5	ms	[1]
RFRUN Voltage in Run Mode	V_{RFRUN}	–	2.5	–	V	@ 100µA<I_{RFRUN}<600µA
Run Frequency	F_{RFRUN}	49	50	51	kHz	R_{RFRUN} = 10kΩ
Adjustable Run Frequency	F_{RFRUN1}	–	20	–	kHz	I_{RFRUN} = – 100 µA
	F_{RFRUN2}	–	40	–	kHz	I_{RFRUN} = – 200 µA
	F_{RFRUN3}	–	100	–	kHz	I_{RFRUN} = – 500 µA
RFRUN max. Current Range	$I_{RFRUNmax}$	–	–1000	– 650	µA	@ V_{RFRUN} = 0V

1) Shift Start Up Frequency to Preheating Frequency

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5.3.3.4 Inverter Control Preheating (RFPH, RTPH)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
RFPH Voltage Preheating	V_{RFPH}	–	2.5	–	V	V_{RFPH} = 0V in Run Mode
Preheating Frequency	F_{RFPH1}	97	100	103	kHz	R_{RFPH} = R_{RFRUN} = 10kΩ
RFPH max. Current Range	$I_{RFPHmax}$	–	–1000	– 550	µA	@ V_{RFPH} = 0V
Current for set Preh. Time	I_{RTPH}	–	–100	–	µA	
Preheating Time	t_{RTPH1}	950	1000	1050	ms	R_{RTPH1} = 10kΩ
	t_{RTPH2}	50	100	150	ms	R_{RTPH2} = 1kΩ
	t_{RTPH3}	–	500	–	ms	R_{RTPH3} = 5kΩ
	t_{RTPH4}	–	2000	–	ms	R_{RTPH4} = 20kΩ
	t_{RTPH5}	–	2500	–	ms	R_{RTPH5} = 25kΩ

5.3.3.5 Restart after Lamp Removal (RES)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
High Side Filament In Det.	V_{RES1}	1.55	1.60	1.65	V	U_{VLO}, V_{CC} < V_{CCON}
	V_{RES2}	1.25	1.30	1.35	V	
	V_{RES3}	–	3.2	–	V	Run Mode
RES Current Source	I_{RES1}	–53.2	–42.6	–32.0	µA	V_{RES} = 1V ;LVS = 5µA
	I_{RES2}	–44.2	–35.4	–26.6	µA	V_{RES} = 2V ;LVS = 5µA
	I_{RES3}	–26.6	–21.3	– 16.0	µA	V_{RES} = 1V ;LVS = 30µA
	I_{RES4}	–22.1	–17.7	–13.3	µA	V_{RES} = 2V ;LVS = 30µA

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5.3.3.6 Lamp Voltage Sense (LVS)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Source Current before Startup	$I_{LVSSource}$	–5.0	–3.0	–2.0	µA	V_{LVS} = 0V
Enable Lamp Monitoring	$V_{LVSEnable1}$	350	530	750	mV	1)
Sink Current for Lamp Det.	$I_{LVSSink}$	8.0	12.0	18.0	µA	$V_{LVS} > V_{LVSClamp}$
Positive Clamping Voltage	$V_{LVSClamp}$	–	6.5	–	V	@ I_{LVS} = 300µA
AC EOLCurrent Threshold	$I_{LVSSourceAC}$	190	210	230	µApp	$I_{LVS} > I_{LVSEOLpp}$ EOL 1
Positive EOL Current Thr.	$I_{LVSDCPos}$	34	42	50	µA	$I_{LVS} > I_{LVSDCPos}$ EOL 2
Negative EOL Current Thr.	$I_{LVSDCNeg}$	–50	–42	–34	µA	$I_{LVS} > I_{LVSDCNeg}$ EOL 2

1) If $V_{LVS} < V_{LVSEnable1}$ monitoring is disabled

5.3.3.7 High Side Gate Drive (HSGD)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
HSGD Low Voltage	$V_{HSGDLow}$	0.02	0.05	0.1	V	I_{HSGD} = 5mA (sink)
		0.5	1.1	2.5	V	I_{HSGD} = 100mA (sink)
		–0.4	–0.2	–0.05	V	I_{LSGD} = - 20mA (source)
HSGD High Voltage	$V_{HSGDHigh}$	9.7	10.5	11.2	V	V_{CCHS}=15V I_{HSGD} = - 20mA (source)
		7.8	–	–	V	$V_{CCHSOFF}$ + 0.3V I_{HSGD} = - 1mA (source)
HSGD active Shut Down	$V_{HSGDASD}$	0.05	0.22	0.5	V	V_{CCHS}=5V I_{HSGD} = 20mA (sink)
HSGD Peak Source Current	$I_{HSGDSource}$	–	–50	–	mA	R_{Load} = 10Ω+C_{Load} = 1nF 1)
HSGD Peak Sink Current	$I_{HSGDSink}$	–	300	–	mA	R_{Load} = 10Ω+C_{Load} = 1nF 1)
HSGD Rise Time	$t_{HSGDRise}$	120	220	300	ns	2V < V_{LSGD} < 8V R_{Load} = 10Ω+C_{Load} = 1nF
HSGD Fall Time	$t_{HSGDFall}$	20	35	70	ns	8V > V_{LSGD} > 2V R_{Load} = 10Ω+C_{Load} = 1nF

1) The parameter is not subject to a production test – verified by design / characterization

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5.3.3.8 Timer Section

Delay Timer 1	t_{TIMER1}	70	100	160	ms	For lamp detection
Delay Timer 2	t_{TIMER2}	74	84	94	ms	For V_{BUS} > 95%
Inverter Time	t_{Inv}	100	130	160	µs	
Inverter Dead Time Max	$t_{DeadMax}$	1.75	2.1	2.40	µs	
Inverter Dead Time Min	$t_{DeadMin}$	0.8	1.05	1.3	µs	
Δ Inverter Dead Time Max	$t_{DeadMax}$	–200	–	200	ns	
Δ Inverter Dead Time Min	$t_{DeadMin}$	–200	–	200	ns	
Min. Duration of Ignition	$t_{Ignition}$	34	40	48	ms	
Max. Duration of Ignition	$t_{NOIgnition}$	197	–	236	ms	
Duration of Pre – Run	t_{PRERUN}	565	625	685	ms	

5.3.3.9 Built-In Customer Test Mode

Voltage at RTPH Pin	V_{RTPH}	0	V	Preheating time = 0 ms (skipped preheating)
Voltage at RTPH Pin	V_{RTPH}	5.0	V[1)]	IC remains in Preheating
Voltage at LVS	V_{LVS}	0	V	Disables Lamp Voltage Sense
Voltage at RES Pin	V_{RES}	0	V	Disable the Filament Detection
Voltage at RFPH Pin	V_{RFPH}	5.0	V[1)]	Built-in Customer Test Mode - Clock Acceleration. Decreasing time for the following procedures: Preheating by factor 4 Timeout ignition by factor 2 Pre-run by factor 15; EOL by 60
Voltage at RFRUN Pin	V_{RFRUN}	5.0	V[1)]	
Voltage at VCC Pin	V_{CC}	> 14.0	V	
Voltage at RES Pin	V_{RES}	0	V	

1) Tolerance for this voltage is ± 5%

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5.3.4 Parameter limits for extended temperature range down to -40°C

For any other parameter which is not listed below, the -25°C limit is also valid for -40°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Junction Temperature	T_J	-40		150	°C	
LSVCC Turn-On Threshold	V_{VCCOn}	13.48	14.0	14.5	V	Hysteresis
VCC Zener Clamp Voltage	$I_{VCCZener}$	2.5	-	5.05	mA	V_{VCC} = 17.5V/V_{RES} = 5V
HSVCC Quiescent Current	$I_{HSVCCqu2}$	0.26	0.65	1.2	mA	V_{HSVCC} > $V_{HSVCCOn}$
HSVCC Turn-On Threshold HSVCC Turn-Off Threshold HSVCC Turn-On/Off Hyst.	$V_{HSVCCOn}$ $V_{HSVCCOff}$ $V_{HSVCCHy}$	9.8 8.08 1.4	10.4 8.6 1.7	11.0 9.3 2.03	V V V	Hysteresis
Over Current Blanking + Propagation Delay	$t_{PFCCSOff}$	140	200	262	ns	
Leading Edge Blanking	$t_{Blanking}$	180	250	315	ns	Pulse width when V_{PFCCS} > 1.0 V
Clamping of pos. Voltages	$V_{PFCZCDpclp}$	4.1	4.6	5.12	V	$I_{PFCZCDSink}$ = 2mA
Clamping of neg. Voltages	$V_{PFCZCDnclp}$	-1.69	-1.4	-1.0	V	$I_{PFCZCDSource}$ = -2mA
PFCZCD Ringing Suppress. Time	$t_{Ringsup}$	350	500	660	ns	
Limit Value for ON Time Extension	$\Delta t \times I_{ZCD}$	498	700	900	pAxs	
Trimmed Reference Voltage	$V_{PFCVSRef}$	2.468	2.50	2.53	V	± 1.2 %
Overvoltage turn Off (109%)	$V_{PFCVSRUp}$	2.677	2.73	2.78	V	
Overvoltage turn On (105%)	$V_{PFCVSLow}$	2.567	2.63	2.68	V	
Under voltage (75%)	$V_{PFCVSUV}$	1.832	1.88	1.915	V	
Rated Bus Voltage (95%)	$V_{PFCVS95}$	2.320	2.38	2.425	V	
Max. ON – Time	t_{PFCON_max}	18.0	24.0	28.6	µs	0.45V < VPFCVS < 2.45V
Off Time	t_{PFCOff}	42	47	52.5	µs	
PFCGD Low Voltage	$V_{PFCGDLow}$	0.4	0.7	0.92	V	I_{PFCGD} = 5mA
		0.4	0.75	1.12	V	I_{PFCGD} = 20mA
		-0.2	0.3	0.62	V	I_{PFCGD} = -20mA
PFCGD High Voltage	$V_{PFCGDHigh}$	10.0	11.0	11.6	V	I_{PFCGD} = -20mA
		8.98	–	–	V	I_{PFCGD} = -1mA / V_{VCC} [1]
		8.47	–	–	V	I_{PFCGD} = -5mA / V_{VCC} [1]
PFCGD active Shut Down	$V_{PFCGASD}$	0.4	0.75	1.12	V	I_{PFCGD} = 20mA V_{VCC}=5V
PFCGD UVLO Shut Down	$V_{PFCGDuvlo}$	0.3	1.0	1.56	V	I_{PFCGD} = 5mA V_{VCC}=2V
PFC Rise Time	$t_{PFCGDRise}$	100	245	450	ns	2V > V_{LSGD} > 8V [2]
PFC Fall Time	$t_{PFCGDFall}$	20	45	72	ns	8V > V_{LSGD} > 2V [2]
LSGD Low Voltage	$V_{LSGDLow}$	0.4	0.7	1.02	V	I_{LSGD} = 5mA (sink)
		0.4	0.8	1.22	V	I_{LSGD} = 20mA (sink)
		-0.3	0.2	0.53	V	I_{LSGD} = -20mA (source)

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Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
LSGD High Voltage	$V_{LSGDHigh}$	10.0	10.8	11.6	V	
		8.98	–	–	V	
		8.47	–	–	V	
LSGD active Shut Down	$V_{LSGDASD}$	0.4	0.75	1.12	V	V_{CC}=5V / I_{LSGD} = 20mA (sink)
LSGD UVLO Shut Down	$V_{LSGDUVLO}$	0.3	1.0	1.6	V	V_{CC}=2V / I_{LSGD} = 5mA (sink)
LSGD Rise Time	$t_{LSGDRise}$	100	245	460	ns	2V < V_{LSGD} < 8V[3]
LSGD Fall Time	$t_{LSGDFall}$	20	35	61	ns	8V > V_{LSGD} > 2V
Fixed Start – Up Frequency	$F_{StartUp}$	120	135	148.5	kHz	
Duration of Soft Start	$t_{SoftStart}$	9	11	13.56	ms	[4]
Run Frequency	F_{RFRUN}	49	50	51.07	kHz	R_{RFRUN} = 10kΩ
RFRUN max. Current Range	$I_{RFRUNmax}$	–	-1000	-612	µA	@ V_{RFRUN} = 0V
RFPH max. Current Range	$I_{RFPHmax}$	–	-1000	-512	µA	@ V_{RFPH} = 0V
Preheating Time	t_{RTPH1}	920	1000	1050	ms	R_{RTPH1} = 10kΩ
High Side Filament In Det.	V_{RES1}	1.546	1.60	1.65	V	U_{VLO}, V_{CC} < V_{CCON}
	V_{RES2}	1.247	1.30	1.35	V	
RES Current Source	I_{RES1}	-53.2	-42.6	-30.5	µA	V_{RES} = 1V ;LVS = 5µA
	I_{RES2}	-44.2	-35.4	-25.1	µA	V_{RES} = 2V ;LVS = 5µA
	I_{RES3}	-26.6	-21.3	-15	µA	V_{RES} = 1V ;LVS = 30µA
	I_{RES4}	-22.1	-17.7	-12.3	µA	V_{RES} = 2V ;LVS = 30µA
Source Current before Startup	$I_{LVSSource}$	-5.0	-3.0	-1.9	µA	V_{LVS} = 0V
Sink Current for Lamp Det.	$I_{LVSSink}$	7.0	12.0	18.0	µA	V_{LVS} > $V_{LVSClamp}$
AC EOLCurrent Threshold	$I_{LVSSourceAC}$	186	210	230	µApp	I_{LVS} > $I_{LVSEOLpp}$ EOL 1
HSGD Low Voltage	$V_{HSGDLow}$	0.018	0.05	0.1	V	I_{HSGD} = 5mA (sink)
		0.46	1.1	2.5	V	I_{HSGD} = 100mA (sink)
		-0.4	-0.2	-0.04	V	I_{LSGD} = - 20mA (source)
HSGD active Shut Down	$V_{HSGDASD}$	0.041	0.22	0.5	V	V_{CCHS}=5V I_{HSGD} = 20mA (sink)
HSGD Fall Time	$t_{HSGDFall}$	19	35	70	ns	8V > V_{LSGD} > 2V R_{Load} = 10Ω+C_{Load} = 1nF
Delay Timer 1	t_{TIMER1}	70	100	163.6	ms	For lamp detection
Inverter Time	t_{Inv}	100	130	163	µs	
Inverter Dead Time Max	$t_{DeadMax}$	1.75	2.1	2.50	µs	
Inverter Dead Time Min	$t_{DeadMin}$	0.8	1.05	1.33	µs	
Δ Inverter Dead Time Max	$t_{DeadMax}$	-240	–	200	ns	
Δ Inverter Dead Time Min	$t_{DeadMin}$	-230	–	200	ns	

1) V_{VCC} = V_{VCCOff} + 0.3 V
2) R_{Load} = 4Ω and C_{Load} = 3.3nF
3) Load: R_{Load} = 10Ω and C_{Load} = 1nF
4) Shift Start Up Frequency to Preheating Frequency

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6 Application Example

6.1 Schematic Ballast 54W T5 Single Lamp

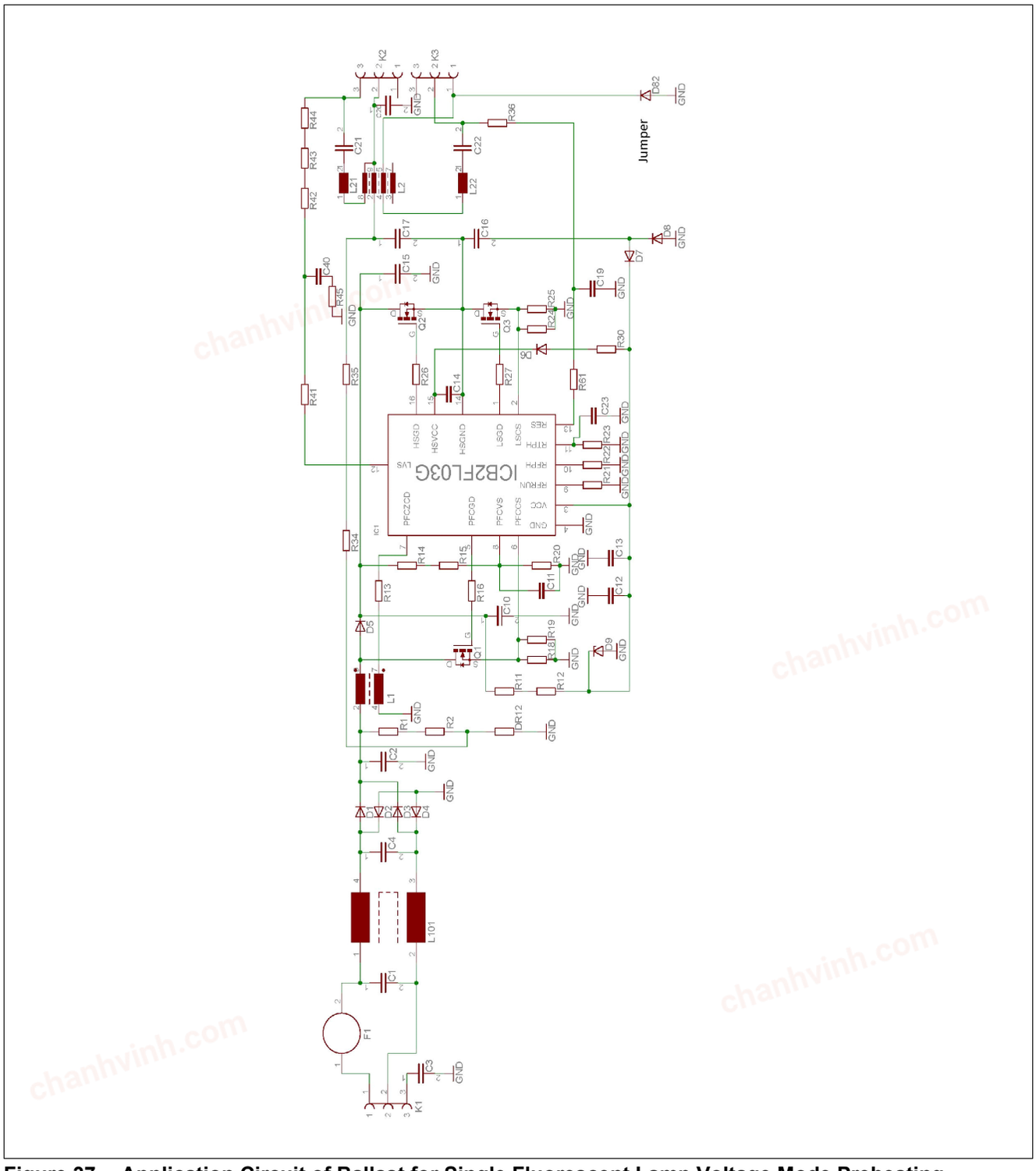


Figure 37 Application Circuit of Ballast for Single Fluorescent Lamp Voltage Mode Preheating

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6.2 Bill of Material

BOM: Demoboard 1x54W T5 - VM - 180VAC to 270VAC - ICB2FL03G

				ICB2FL03G			
	Input voltage = 180VAC to 270VAC			VBUS = 410 VRMS			
				Package			Package
F1	Fuse 1A fast	Wickmann	Typ 370		R1	470kΩ	.1206
					R2	470kΩ	.1206
K1/1	AC Input	WAGO 250-203			R11	470kΩ	.1206
K1/2	AC Input				R12	470kΩ	.1206
K1/3	PE				R13	33kΩ	.1206
K2/1	not connected	WAGO 250-203			R14	820kΩ	.1206
K2/2	High Side Filament				R15	820kΩ	.1206
K2/3	High Side Filament				R16	10Ω	.0805
K3/1	Low Side Filament	WAGO 250-203			R18	1Ω	.1206
K3/2	Low Side Filament				R19	not assembled	.1206
K3/3	not connected				R20	10kΩ	.0805
IC1	ICB2FL03G	Infineon		SO-16	R21	11kΩ	.0805
Q1	IPD60R1k4C6	Infineon		D-Pack	R22	8.2kΩ	.0805
Q2	IPD60R1k4C6	Infineon		D-Pack	R23	10kΩ	.0805
Q3	IPD60R1k4C6	Infineon		D-Pack	R24	0.68Ω	.1206
D1…4	S1M	Fairchild	(1000V/1A/2µs)	DO-214AC	R25	0.68Ω	.1206
D5	MURS160T3	ON Semi	(600V/1A/75ns)	SMB	R26	10Ω	.0805
D6	BYG20J	Philips	(600V/1,5A/75ns)	SOD124	R27	10Ω	.0805
D7	BYG22D	Philips	(200V/1A/25ns)	DO214	R30	33Ω	.1206
D8	BYG22D	Philips	(200V/1A/25ns)	DO214	R34	150kΩ	.1206
D9	BZV55-C16	NXP		SOD-80C	R35	150kΩ	.1206
DR12	110kΩ			.1206	R36	56kΩ	.1206
D82	0Ω			.2512	R41	68kΩ	.0805
					R42	68kΩ	.1206
L101	2x68mH/0.6A	Epcos	B82732F2601B001		R43	68kΩ	.1206
L1 PFC	1.58mH	Epcos	B78326P7373A005	EFD25/13/9	R44	68kΩ	.1206
L 2	1.46mH	Epcos	B78326P7374A005	EFD25/13/9	R45	6,8kΩ	.1206
L 21	100µH/760mA	Epcos	B82144B1104J000	RM5	R61	0Ω	.0805
L 22	100µH/760mA	Epcos	B82144B1104J000	RM5			
C1	220nF/X2/305V	Epcos	B32922C3224M000	RM15			
C2	33nF/630V/MKT	Epcos	B32521N8333K000	RM10			
C3	3,3nF/Y2/300V	Epcos	B32021A3332K000	RM10			
C4	220nF/X2/305V	Epcos	B32922C3224M000	RM15			
C10	10µF/450V	Epcos	B43888C5106M000	single ended			
C11	2,2nF/50V	X7R		.0805			
C12	100nF/50V	X7R		.0805			
C13	1µF/25V	X7R		.1206			
C14	68nF/50V	X7R		.0805			
C15	22nF/630V/MKT	Epcos	B32621A6223K000	RM10			
C16	1nF/630V/MKT	Epcos	B32529C8102K000	RM5			
C17	100nF/630V/MKP	Epcos	B32612A6104K008	RM15			
C19	22nF/50V	X7R		.0805			
C20	4,7nF/1600V/MKP	Epcos	B32612-J1472J008	RM15			
C21	22nF/400V/MKP	Epcos	B32620A4223J000	RM7,5			
C22	22nF/400V/MKP	Epcos	B32620A4223J000	RM7,5			
C23	10nF/50V	X7R		.0805			
C40	220nF/50V	X7R		.0805			

Figure 38 Bill of Material

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6.3 Multi Lamp Ballast Topologies (Series Connection)

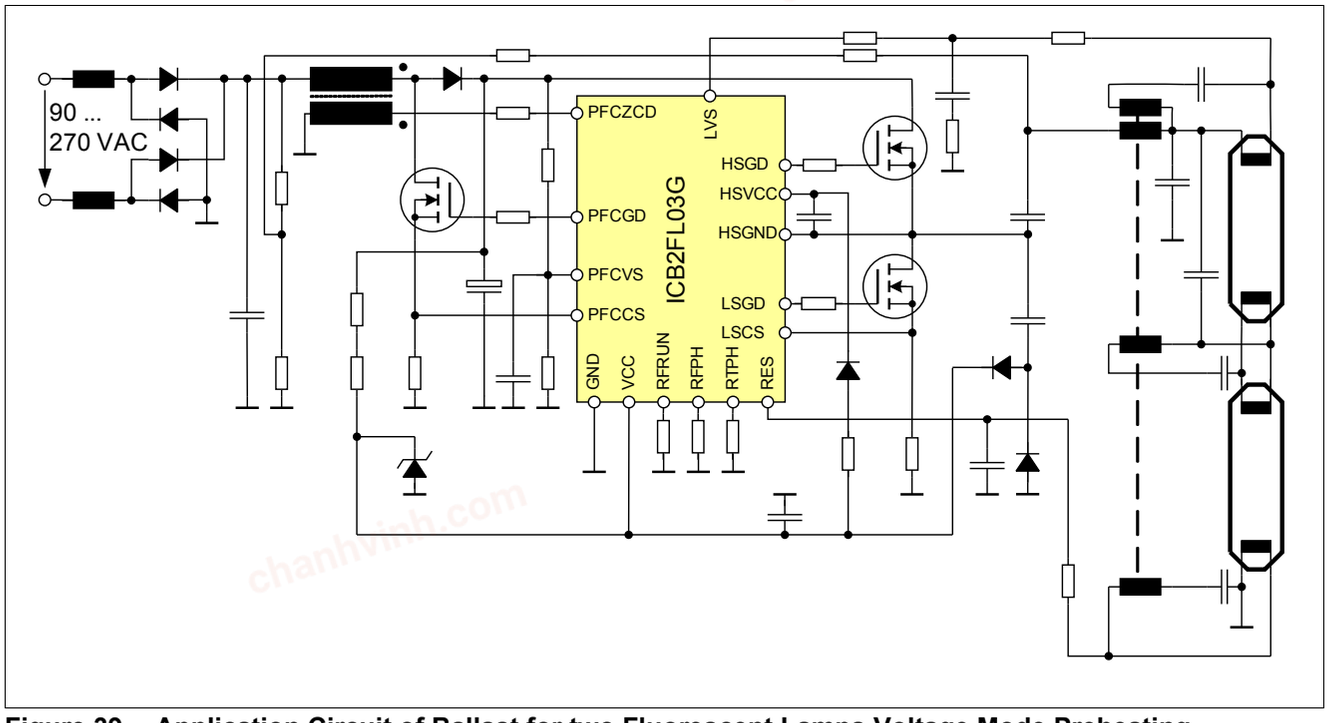
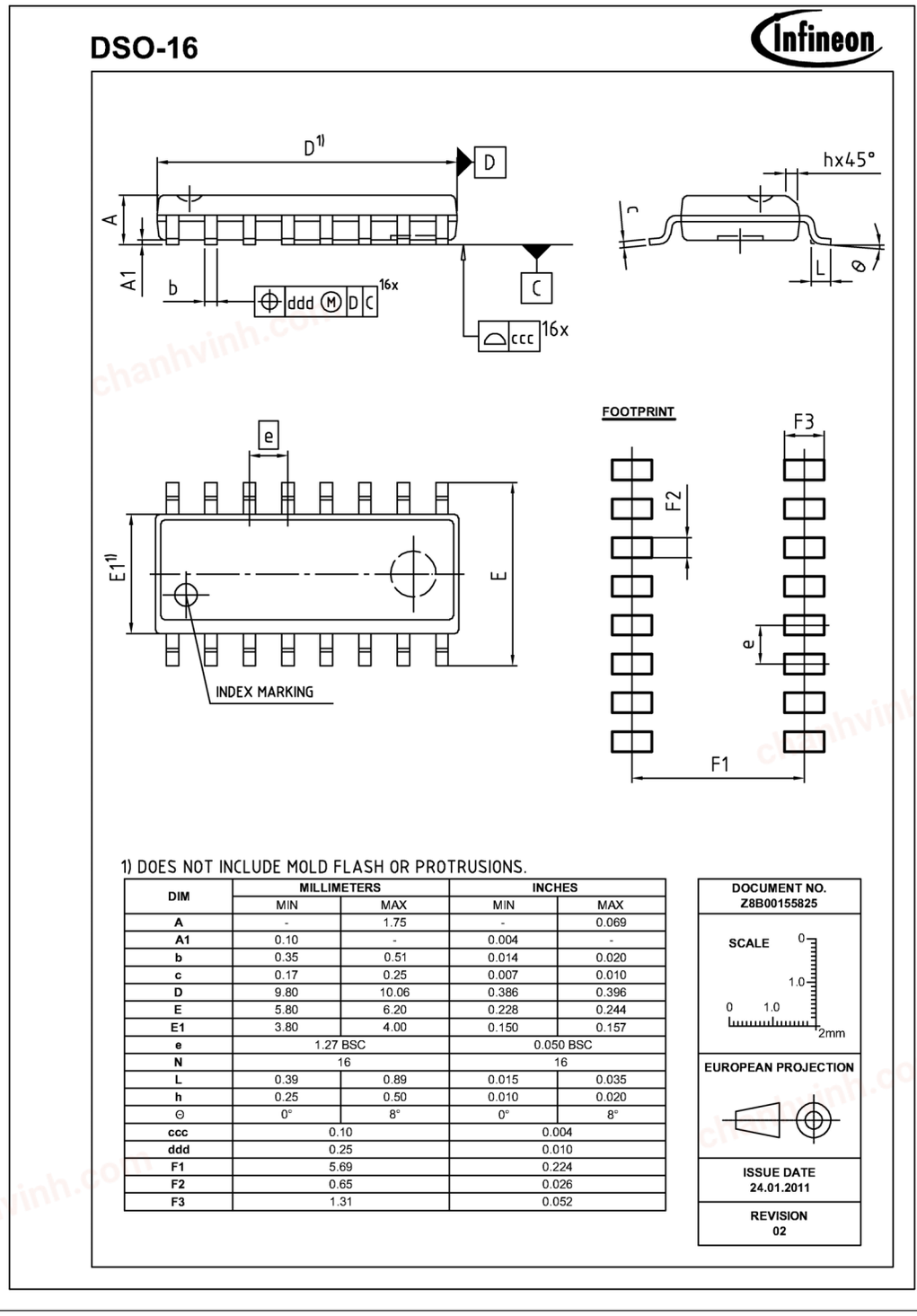


Figure 39 Application Circuit of Ballast for two Fluorescent Lamps Voltage Mode Preheating

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7 Package Outline

7.1 Outline Dimensions of PG-DSO-16



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	9.80	10.06	0.386	0.396
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
N	16		16	
L	0.39	0.89	0.015	0.035
h	0.25	0.50	0.010	0.020
Θ	0°	8°	0°	8°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.69		0.224	
F2	0.65		0.026	
F3	1.31		0.052	

Figure 40 Package Outline with Creepage Distance

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