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Infineon 1400 W DC-DC ZVS Full-bridge solution for server and industrial SMPS systems

EVAL_1K4W_ZVS_FB_CFD7

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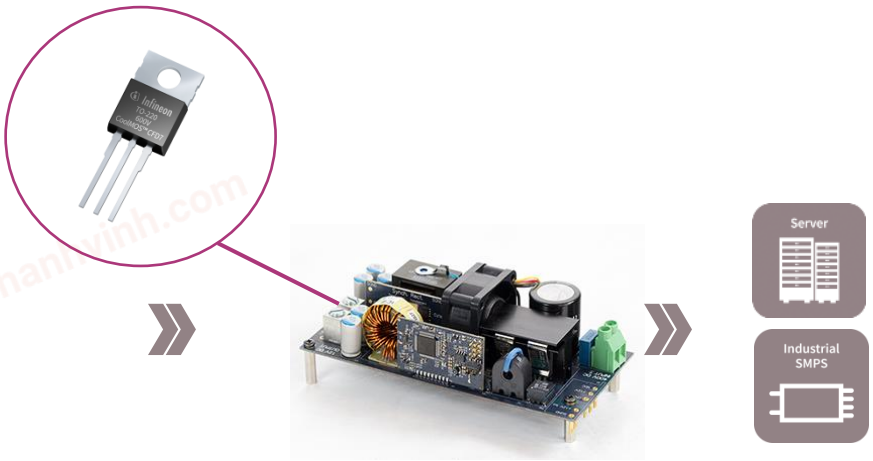
3 Design concept

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Evaluation board with 600 V CoolMOS™CFD7 superjunction MOSFET

EVAL_1K4W_ZVS_FB_CFD7



Technical & order details

Parameter	Value
Input voltage	350 V_{DC} ~ 410 V_{DC}
Output voltage	11.8 V_{DC} ~ 12.2 V_{DC}
Max output current Output Power	117 A 1400 W
Peak Efficiency @50% load	>96.5%

Learn more	
Sales name	EVAL_1K4W ZVS FB CFD7
SAP Mat number	SP001783674
Infineon Order Code	EVAL1K4WZVSFBCFD7TOBO1

Features

- Full digital control, with both peak current mode and voltage mode options implemented
- Fast body diode device for high reliability even in critical operations
- Innovative stacked planar transformer concept
- Graphical User Interface (GUI)

Benefits

- High Efficiency in the whole load range
- High Power density
- Safe operation in all conditions
- Easy interaction and fine tuning with GUI

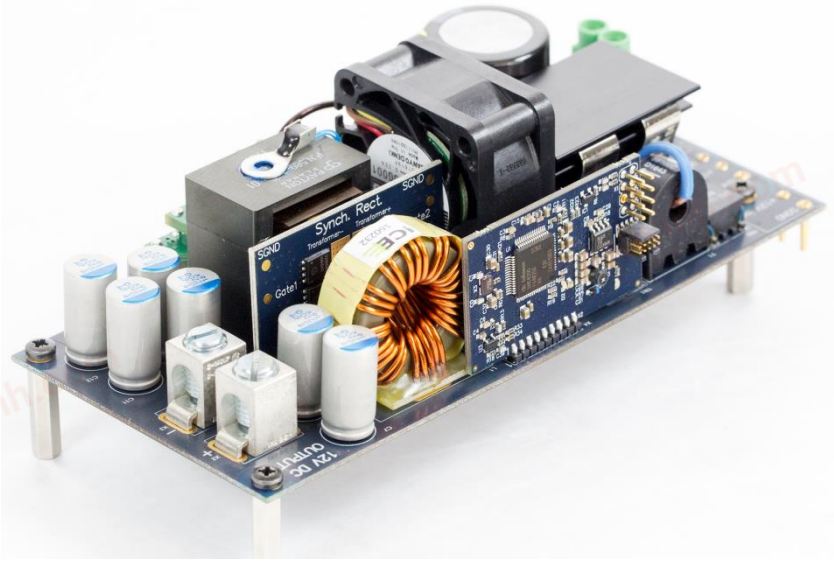
Following additional expert kits are available
- KIT_6W_12V_BIAS_ICE3 DC-DC Bias board
- KIT_6W_12V_BIAS_ICE5 DC-DC Bias board

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General

This is a high-performance evaluation board example with a complete Infineon solution, including high voltage and low voltage power MOSFETs, controllers and drivers. This board demonstrates a very effective way to design the high voltage DC-DC stage of a server or industrial SMPS fulfilling the highest standard of efficiency and reliability. The overall best-in-class performance is achieved because of a mix of proper control techniques and best-in-class power device selection. Key Infineon products used to achieve this performance level include, 600V CoolMOS™ CFD7 SJ MOSFET (IPP60R170CFD7), EiceDRIVER™ 2EDN advanced dual-channel gate driver IC (2EDN7524F), OptiMOS™ 5 80V synchronous rectification MOSFETs (BSC026N08NS5), XMC™ microcontroller (XMC4200-F64K256 BA) and an auxiliary supply solution featuring off-line SMPS current mode controller IC (ICE5QSAG) with an integrated 800 V CoolMOS™ device.



Summary of features:

- Input voltage: 350–410 V_{DC} (nom. 400 V_{DC})
- Output voltage: 12 V±4%
- Max. output current/power: 117 A/1400 W
- Switching Frequency: 100 KHz

The following variant is available:

- EVAL_1K4W_ZVS_FB_CFD7

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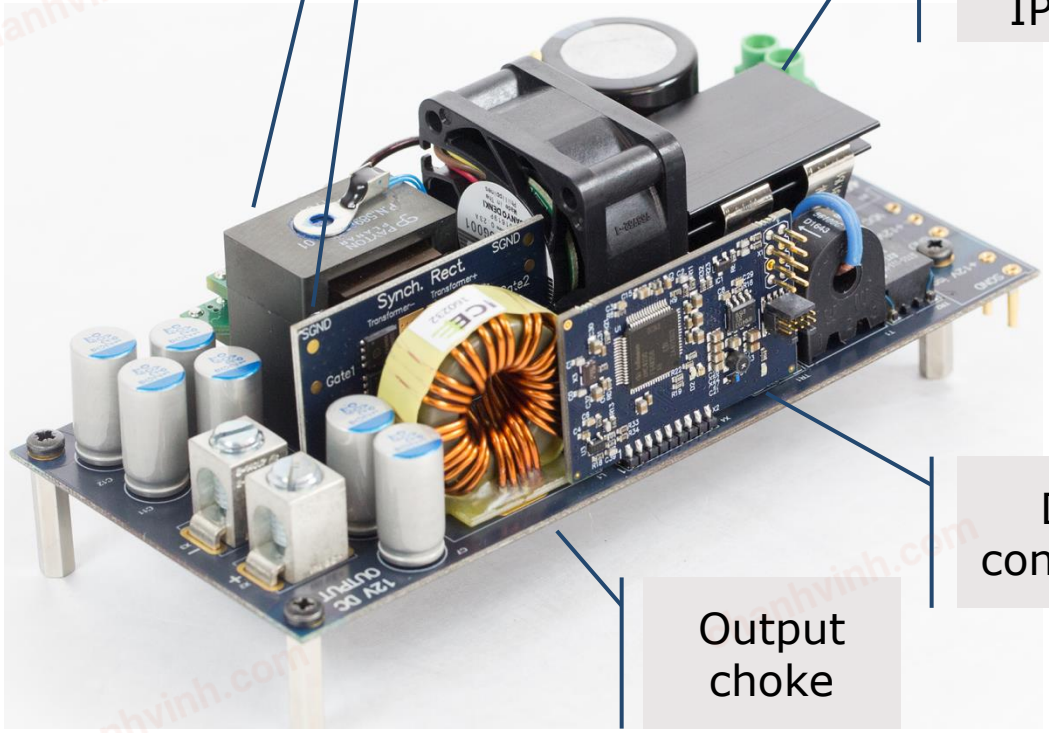
1400 W DC-DC ZVS full-bridge solution for server and industrial SMPS systems

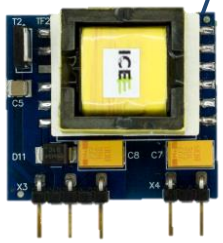
Main Transformer

Synchronous rectification BSC026N08NS5

Full-bridge 600 V CoolMOS™ CFD7 IPP60R170CFD7

Auxiliary bias supply KIT_6W_12V_ BIAS_ICE5





Digital control card

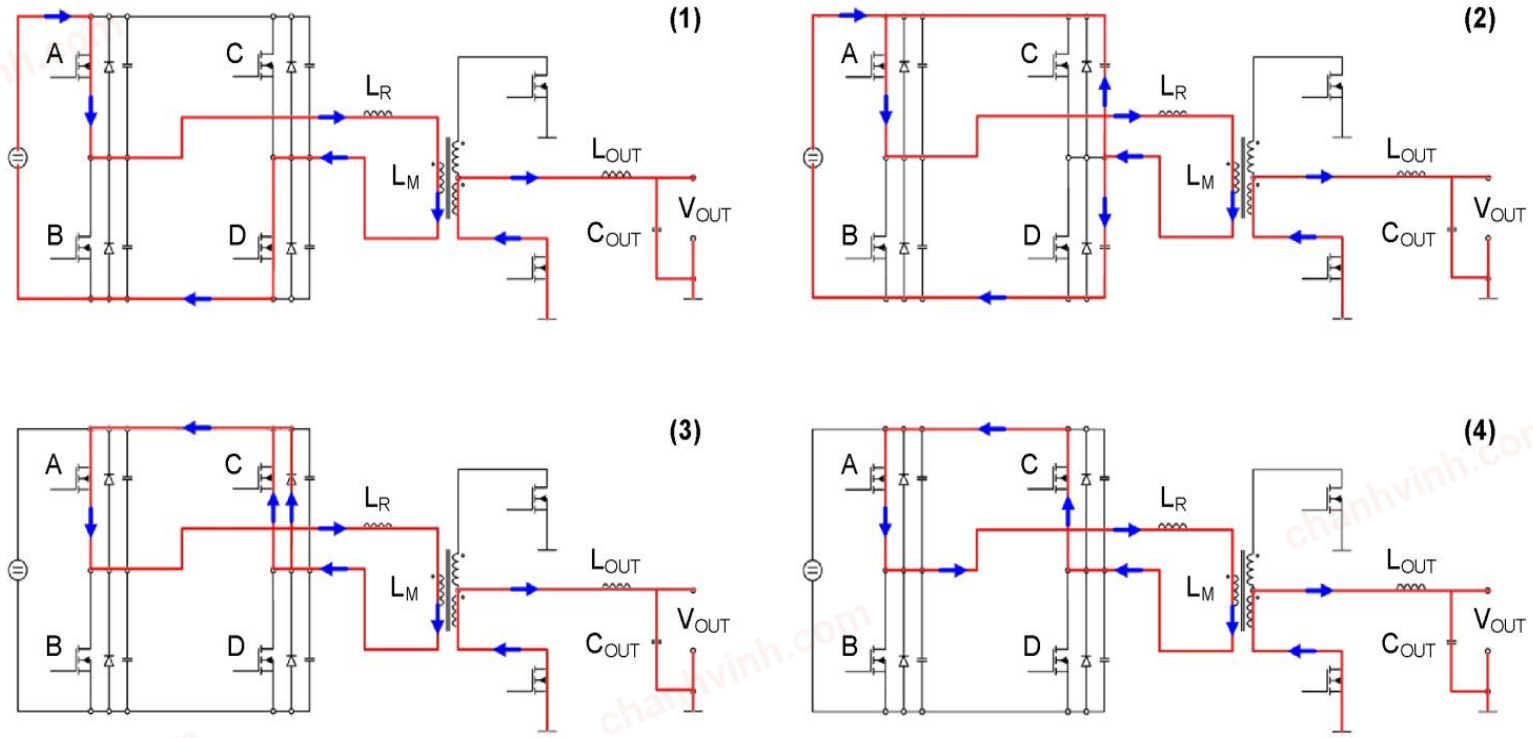
Output choke

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Principle of operation I

› The ZVS PSFB topology principle of operation is already described in [1]. For the reader's convenience, Figures 2 and 3 recap the fundamental steps.

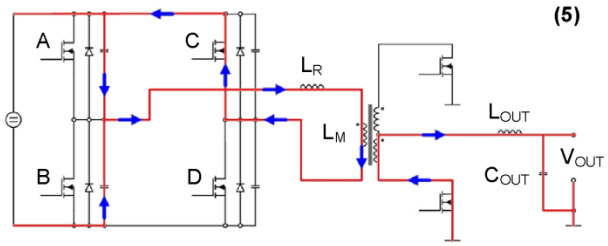


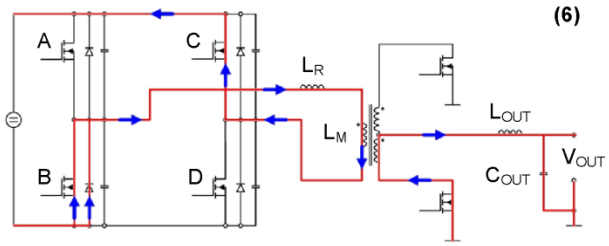
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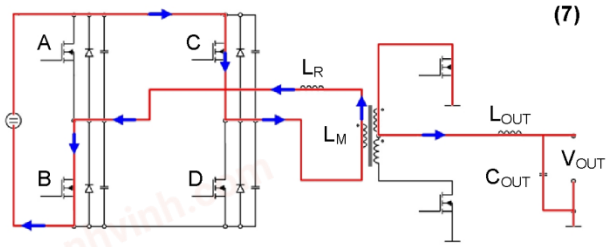
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Principle of operation II

- Power transfer phase: MOSFETs A and D are turned on and the current flows as shown in the diagram. During this phase the primary current is rising according to the value of the total primary inductance.
- The second phase is responsible for the zero-voltage switching of MOSFET C. In order to reach a zero-voltage turn-on, the energy stored in the resonant inductance is used to discharge the output capacitance of MOSFET C and charge the output capacitance of MOSFET D.
- After the output capacitance of MOSFET C is discharged, the current is commutating to the body-diode of MOSFET C.
- MOSFET C is actively turned on and the current is flowing through the channel and not through the body-diode anymore. This phase is also called the “freewheeling phase”.





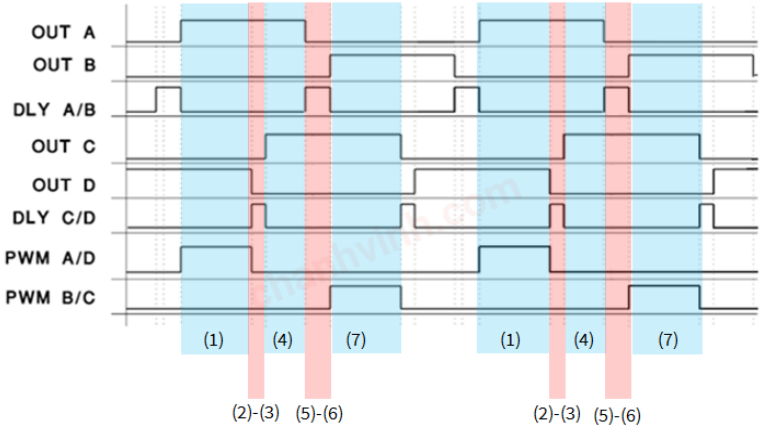


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Principle of operation III

- In order to start a new power transfer phase MOSFET B is turned on. This phase is achieved in the same way as phase 2 by turning off MOSFET A. The output capacitance of MOSFET A is charged and the output capacitance of MOSFET B is discharged before actively switching on the MOSFET.
- The body-diode conduction time of MOSFET B, which is visible in this phase, should also be reduced to a minimum as in phase 3.
- MOSFET B is actively turned on, the current changes its direction and the next power transfer phase starts.
- Figure 4 shows the control signals applied to the four MOSFETs of the bridge.
- (1) and (7) are power transfer phases, whose duration defines the total effective on-time (and thus the duty cycle), which is given by the overlapping conducting period of the MOSFET on the same diagonal (A–D and B–C). The time intervals (2)–(3) and (5)–(6) are also called dead times: they represent the time between the turn-off and turn-on of the MOSFETs on the same leg. They must be set long enough in order to achieve the Zero Voltage Switching (ZVS) turn-on.



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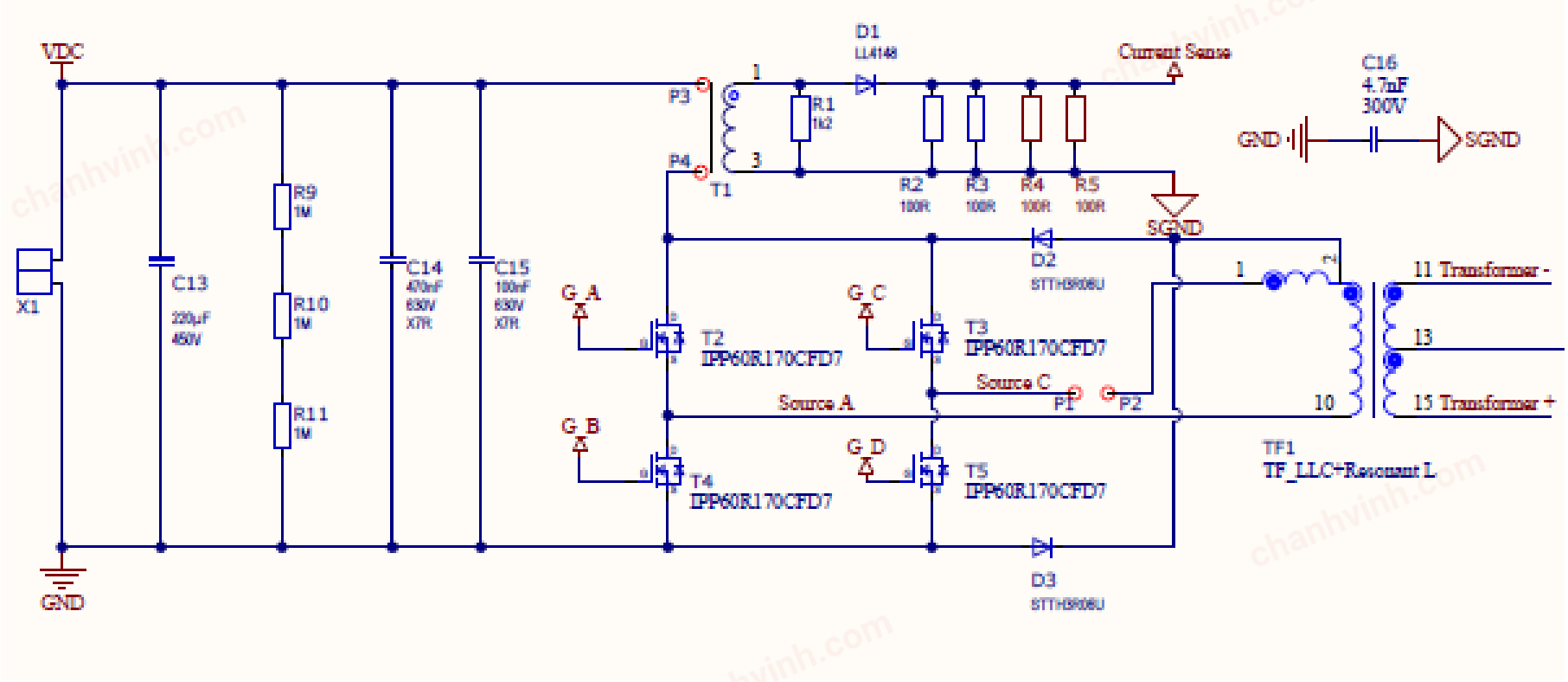
Principle of operation IV

- It can be observed that the duration of these two times is not equal: the one applied to the C–D leg is lower compared to the one applied to the A–B leg. This is because C–D starts a ZVS transition after a power transfer phase, so with more resonant energy available compared to A–B, which starts the transition before the power transfer.
- For this reason C–D is commonly called the “lagging leg” and A–B the “leading leg”.
- Thus, assuming the same MOSFETs (C_{oss}) are used in the two legs, the time needed to discharge the output capacitance is obviously lower for the lagging leg compared to the leading leg.
- Further and more detailed explanations of the ZVS PSFB topology operation and control, including the secondary synchronous rectification, are reported in section 4 of this document.

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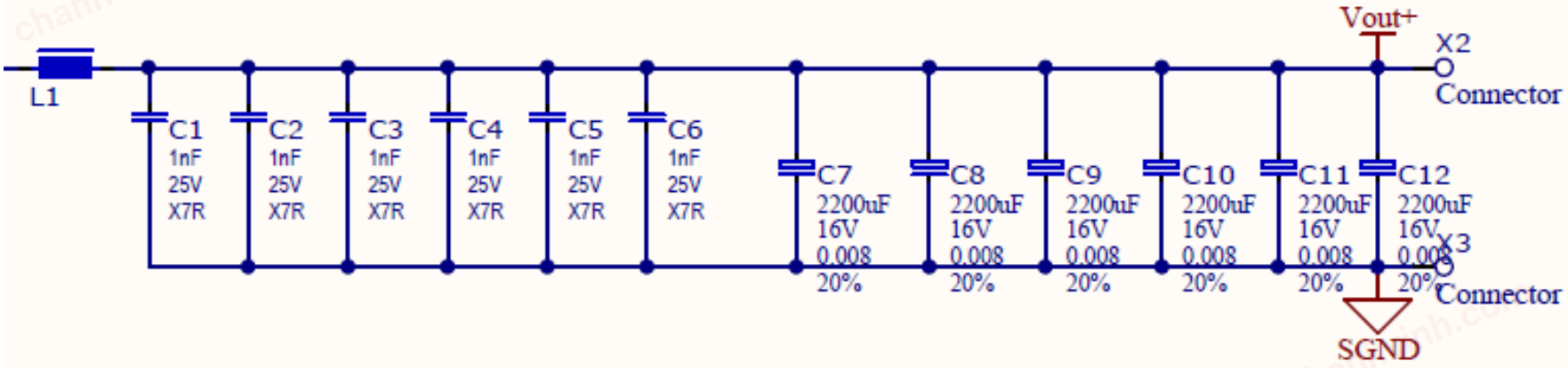
Board schematics
Main converter - Primary side



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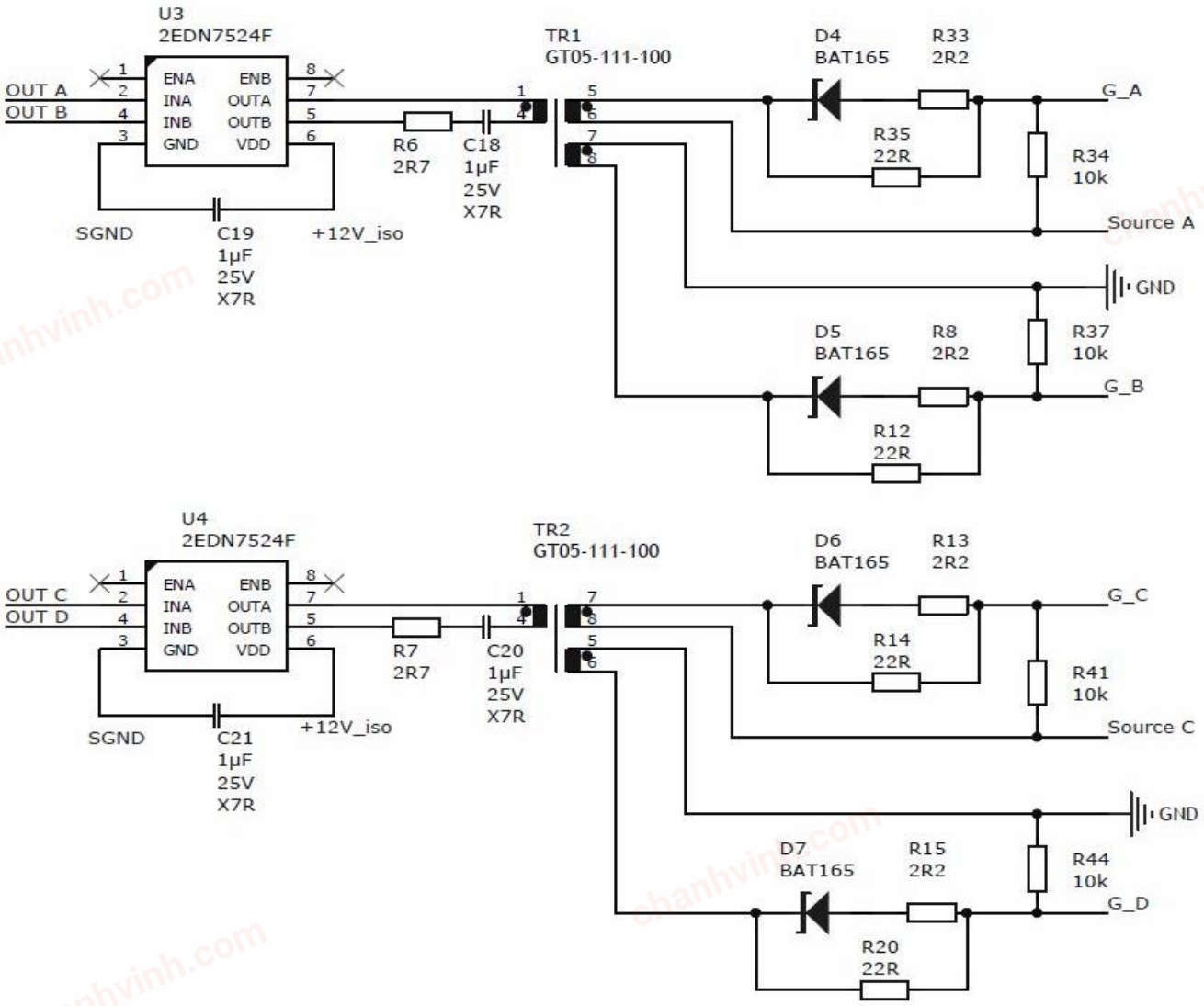
Board schematics
Main converter - Secondary side



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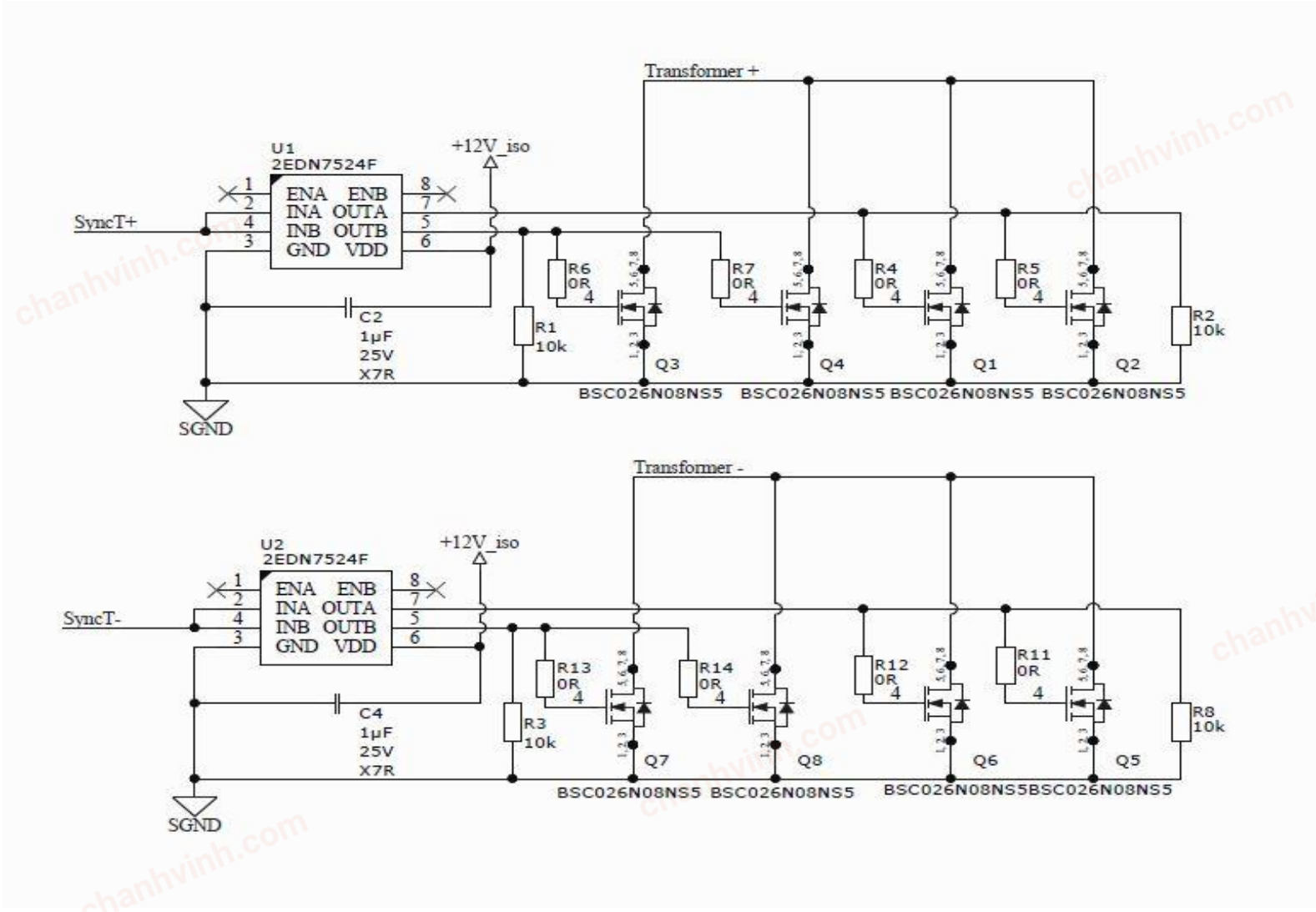
Board schematics
Main converter - Gate driver



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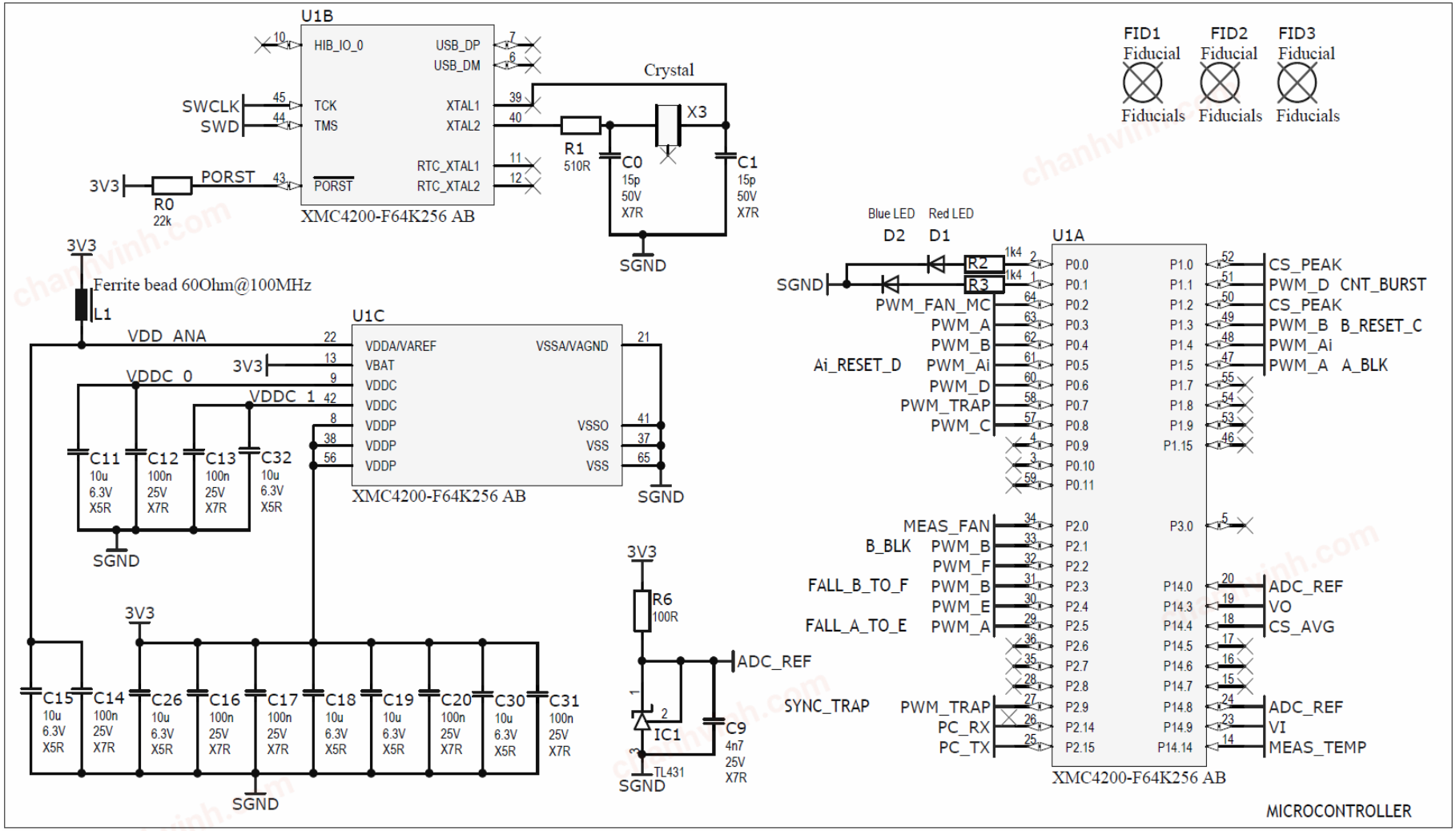
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Board schematics
Synchronous rectification daughter card



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Board schematics
Control board - Microcontroller pin-out



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Description
KIT_6W_12V_ICE5 (one bias board included)



Ordering code: KIT_6W_12V_ICE5

Auxiliary supply solution featuring off-line SMPS current mode controller IC with an 800 V CoolMOS™

Board components

- QR flyback PWM controller 5th generation (ICE5QSAG)
- 800 V CoolMOS™ P7 SJ MOSFET (IPU80R4K5P7)

Board specifications

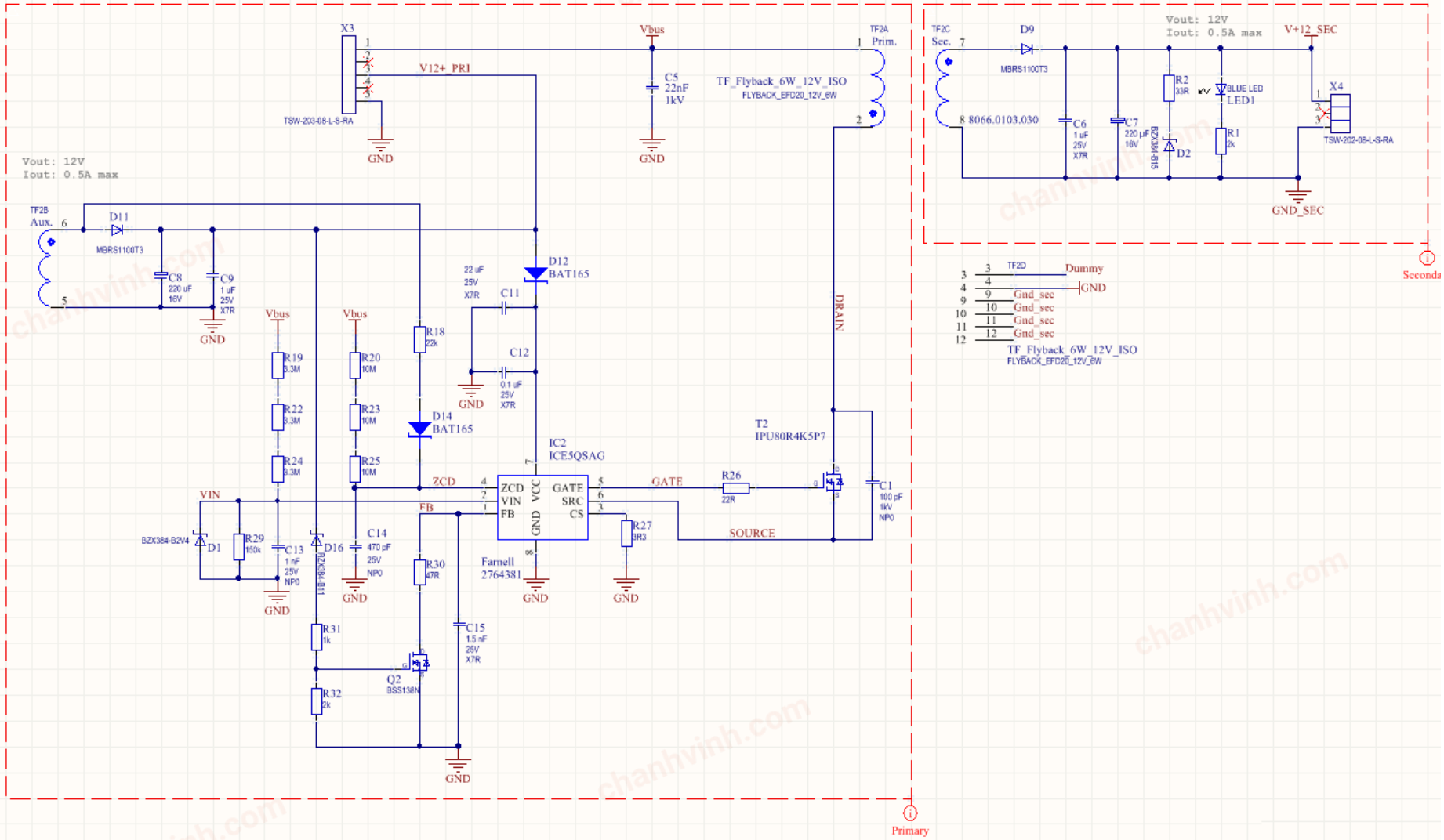
- Input voltage: 90 V_{DC} - 400 V_{DC}
- Output voltage: 12 V_{DC} (prim. and sec. side)
- Output power max.: 6 W (prim. + sec. side)

To be used with the following boards

- EVAL_800W_ZVS_FB_CFD7
- EVAL_1K4W_ZVS_FB_CFD7
- EVAL_2KW_ZVS_FB_CFD2
- EVAL_2KW_ZVS_FB_CFD7
- EVAL_2.5KW_CCM_4PIN
- EVAL_2K5W_CCM_4P

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Bias board
KIT_6W_12V_ICE5 (one bias board included)



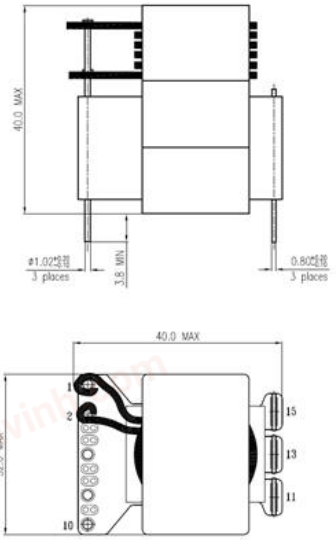
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Magnetic
Main transformer

Measurement	Terminal	Specification
Magnetizing inductance	2–10	2.1 mH +/- 20% @ 100 kHz, 0.5 Vrms
Leakage inductance	2–10 (11–15 shorted)	4.3 µH nominal @ 100 kHz, 0.5 Vrms
Inductor inductance	1–2	21 µH +/- 15% @ 100 kHz, 0.5 Vrms
DCR	1–10 11–15	280 mΩ max. 0.6 mΩ max.
TR	2–10:11–13 2–10:13–15	22 22
Hi-pot	Pri. to sec.	4.0 kV AC, 6 mm creepage
Hi-pot	Pri. to core	2.5 kV AC
Hi-pot	Sec. to core	0.5 kV DC

Electrical specifications at 25°C ±5°C:



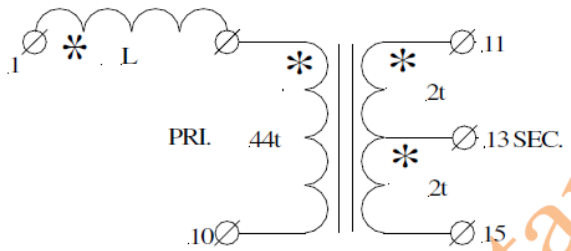


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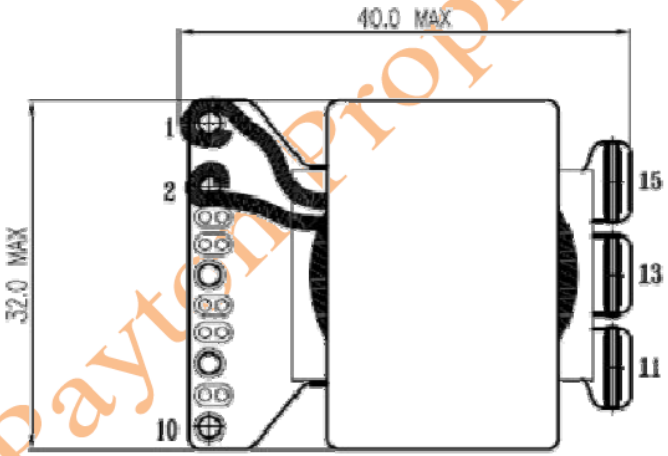
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Magnetic
Bias transformer

Electrical diagram.



Terminals layout sketch (preliminary; top view; not to scale)



Note Terminations made of through hole pins.

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Payton Proprietary

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Magnetic
Output choke

800W ZVS Phase Shift Full Bridge Output Choke Design_
F. Di Domenico

Core Part Number:	Magnetics 58930-A2 or CSC CH270125 or equivalent
Permeability:	125
Inductance Factor:	157 mH/1000 Turns
Core Area:	0.661 sq cm
Path Length:	6.54 cm
Turns:	6
Wire Size:	3 strands of #12 AWG or 5 strands diam. 1.25mm
DC Resistance:	0.001 Ohms
Header P/N:	TV-H4916-4A
Wound Core Dimensions:	TDB
Inductance (full load):	2.05 µH
Inductance (no load):	5.65 µH
Core Losses:	811.2 mW
Copper Losses:	4894.0 mW
Total Losses:	5705.2 mW
Temp. Rise:	63.0 degrees C





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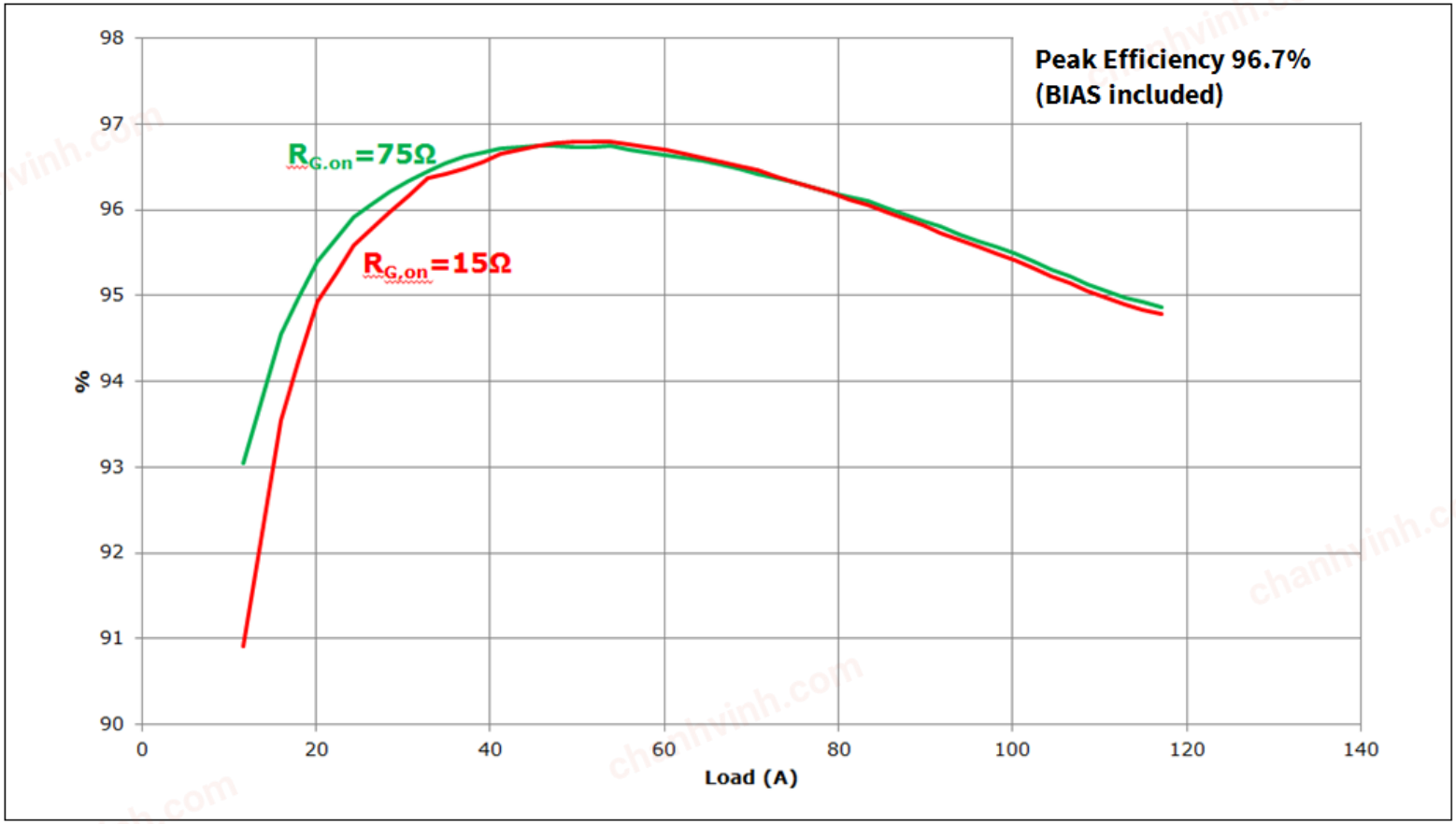
3 Design concept

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Efficiency plots

› The efficiency plots reported here are measured with a fully automated set-up and following the typical procedures prescribed by the 80+ standard.



Effect of different vales of $R_{G,on}$ on IPP60R170CFD7 efficiency plot in 1400W demo board

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Design concept

This general description provides an overview of the Infineon 1400 W ZVS PSFB demo board based on the new CoolMOS™ CFD7 technology, for extended information please refer to the related application note.

- The design concept and the performance evaluation are described in the Application Note with special focus on the key contribution of the CFD7 technology to enable high efficiency combined with reliable operation across the whole load range, including the typical critical modes of this topology. In fact the demo board design is optimized for the 170 mΩ 600 V CoolMOS™ CFD7 JS MOSFET device, namely IPP60R170CFD7.
- An important contribution to the final excellent results also comes out of the applied digital control by Infineon XMC4200. Two possible options, peak current mode and voltage mode, are offered to users for the converter control: these two are in fact the most popular in SMPS application of the PSFB topology. The applied control paths, on both the primary and secondary MOSFETs, with optimized delay time setting, enable an efficiency plot targeting the HV DC-DC stage of a 80+ Platinum level server power supply. A GUI has been designed to help the user interact with the demo board: it enables real-time reading of some key electrical parameters, along with the possibility of designing fine-tuning and protection monitoring.
- The planar main transformer with stacked resonant choke helps achieve the high power density of the demo board and minimizes AC and core losses, resulting in high efficiency across the entire load range, along with a perfect heat spread.
- The final result is a robust and high-performance design able to fulfill all the general requirements for the HV DC-DC isolated stage of a server or industrial SMPS.

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Design concept

- This paper demonstrates that the ZVS PSFB topology is a valuable alternative to the LLC topology in addressing the 80+ Platinum standard. A proper power devices selection, both in the primary and secondary side, and an appropriate control enable a good balance of performance, cost and reliability, avoiding all the pitfalls of a fully resonant approach, as in the LLC topology.
- Further developments of the present design are already planned at Infineon:
  - The gate-driving concept used for the HV MOSFETs on the primary side is going to be improved thanks to the upcoming Infineon 2EDS family of driver ICs with reinforced isolation: this will enable replacement of the gate drive transformers and will provide a reliable and efficient solution with even smaller form factor.

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Support

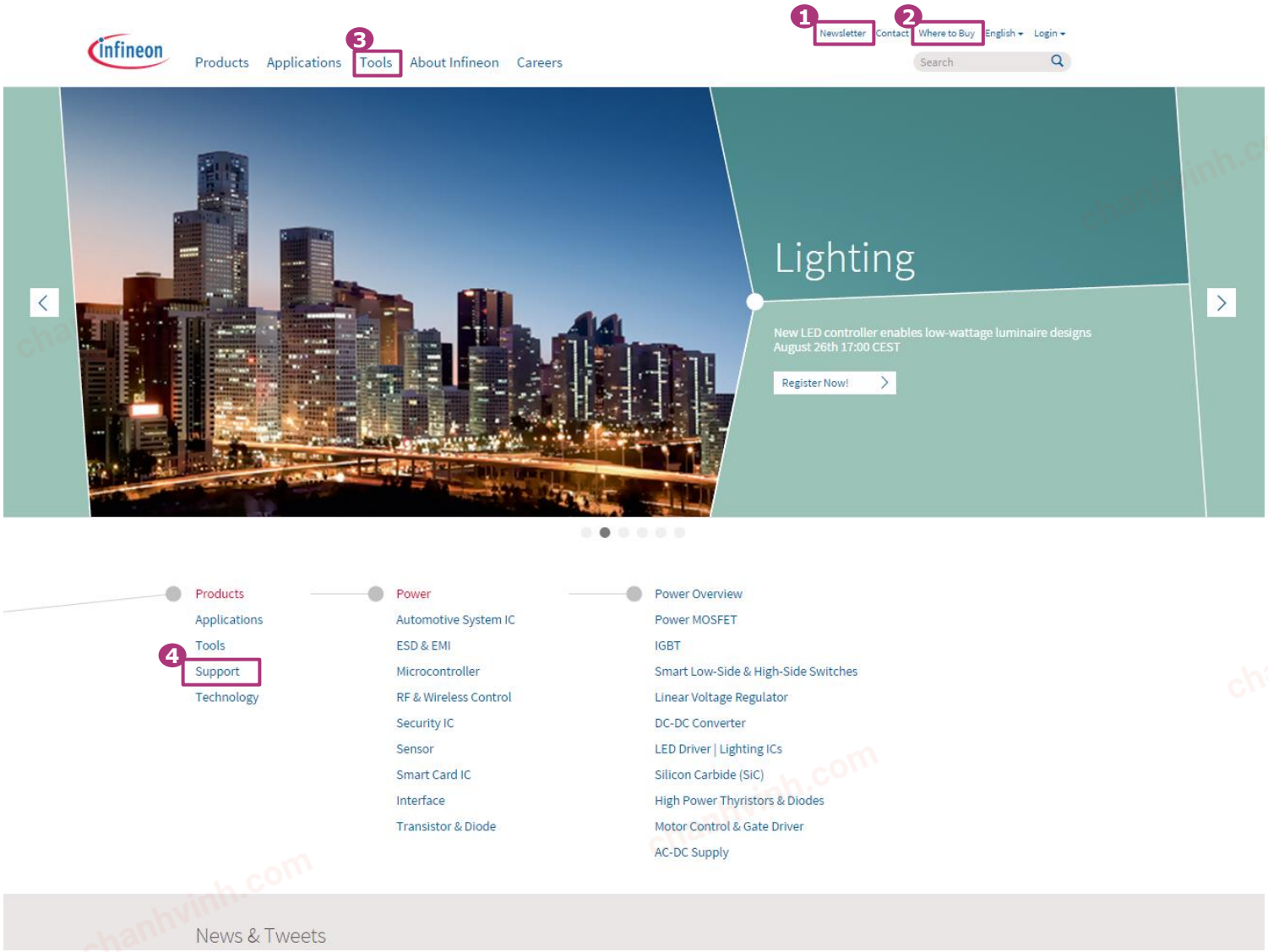


Technical Material	› Application Notes › Simulation Models › Datasheets › PCB Design Data	› EVAL_1K4W_ZVS_FB_CFD7 › EVAL_800W_ZVS_FB_CFD7 › EVAL_2KW_ZVS_FB_CFD2 › EVAL_2KW_ZVS_FB_CFD7 › EVAL_2K5W_CCM_4P
Evaluation Boards	› Evaluation Boards › Demoboards › Reference Designs	› www.infineon.com/evaluationboards
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