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EVAL-1ED3890Mx12M (X3-Digital) user guide

Evaluation board description and getting started guide

About this document

Scope and purpose

This user guide is intended to introduce and provide an overview of the gate driver evaluation board Eval-1ED3890Mx12M with the 1ED3890MC12M or 1ED3890MU12M gate driver ICs, including the functionality, adjustment possibilities and key features of the Infineon EiceDRIVER™ 1ED-X3 Digital gate driver IC family.

The Eval-1ED3890Mx12M board is designed to evaluate the functionalities and capabilities of 1ED3890MC12M or 1ED3890MU12M gate drivers ICs.

This user guide will only selectively present the key features of the gate driver, and the reference manual and the datasheet to observe the full functionality and flexibility of the 1ED3890MC12M or 1ED3890MU12M gate drivers and Eval-1ED3890Mx12M.

Intended audience

This document is intended for all technical specialists who want to evaluate the functionality, performance and features of 1ED3890MC12M or 1ED3890MU12M gate driver ICs. The evaluation board is intended to be used under laboratory conditions only by trained specialists.

It is a prerequisite to read the reference manual and the datasheet of the 1ED3890MC12M or 1ED3890MU12M in order to be familiar with the configurable parameters of the gate driver.

It is highly recommended to have an EiceDRIVER™ Eval-1ED38x0DCT driver configuration microcontroller board available for an easy configuration and evaluation of the Eval-1ED3890Mx12M evaluation board.

Evaluation Board

This board will be used during design in, for evaluation and measurement of characteristics, and proof of data sheet specifications.

Note: PCB and auxiliary circuits are NOT optimized for final customer design.

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Important notice

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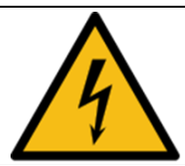
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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 1000 V_{DC}. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

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1 The board at a glance

The Eval-1ED3890Mx12M evaluation board was designed to be used by design engineers to evaluate the 1ED3890MC12M or 1ED3890MU12M EiceDRIVER™ isolated gate driver IC in a half-bridge configuration.

The board comes with unpopulated TO-247 transistor footprints, as seen in Figure 1. The desired power switch, such as Infineon IGBTs, CoolSiC™ or CoolMOS™, can be freely selected. as seen in Figure 1. After selecting the switch, the full functionality and flexibility of the of the 1ED3890MC12M or 1ED3890MU12M gate drivers can be evaluated.

Details about the EiceDRIVER™ Digital 1ED3890MC12M or 1ED3890MU12M can be found on our product pages at *https://www.infineon.com/gdisolated* or by the product search.

The board has a size of 85 × 85 × 15 mm^3 without any power switches assembled. As the board was designed for non-continuous operation, such as double-pulse testing, special consideration should be taken regarding the power tracks current capabilities and to ensure proper cooling of the power switches. It is also recommended to add additional high-voltage decoupling capacitors at the high-voltage input.

The board is designed to be used in conjunction with EiceDRIVER™ Eval-1ED38x0DCT microcontroller board, in order to be able to configure all the parameters in an easy and fast manner. **It is highly recommended to include an EiceDRIVER™ Eval-1ED38x0DCT in your initial order.**

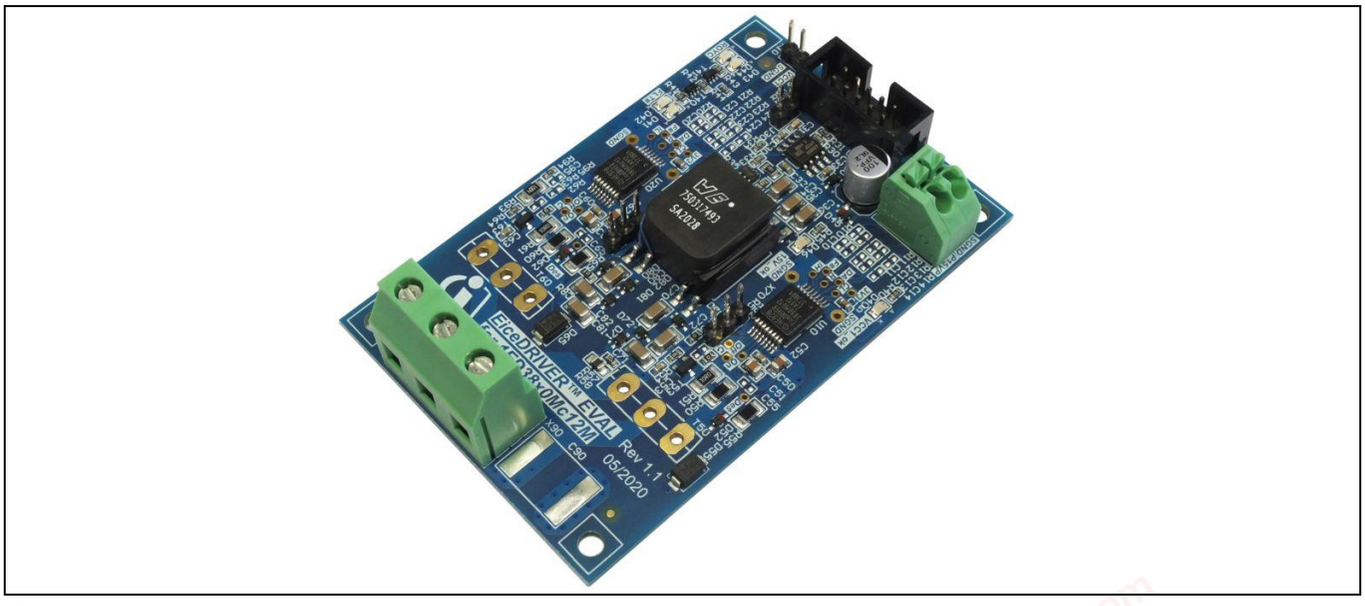


Figure 1 Eval-1ED3890Mx12M board

1.1 Delivery content

The delivery contains the evaluation board Eval-1ED3890Mx12M and a ribbon connection cable to connect to the EiceDRIVER™ Eval-1ED38x0DCT.

1.2 Block diagram

The board block diagram is shown in Figure 2. The IGBTs are not present on the board, and are only shown in the block diagram in order to exemplify the intended connections.

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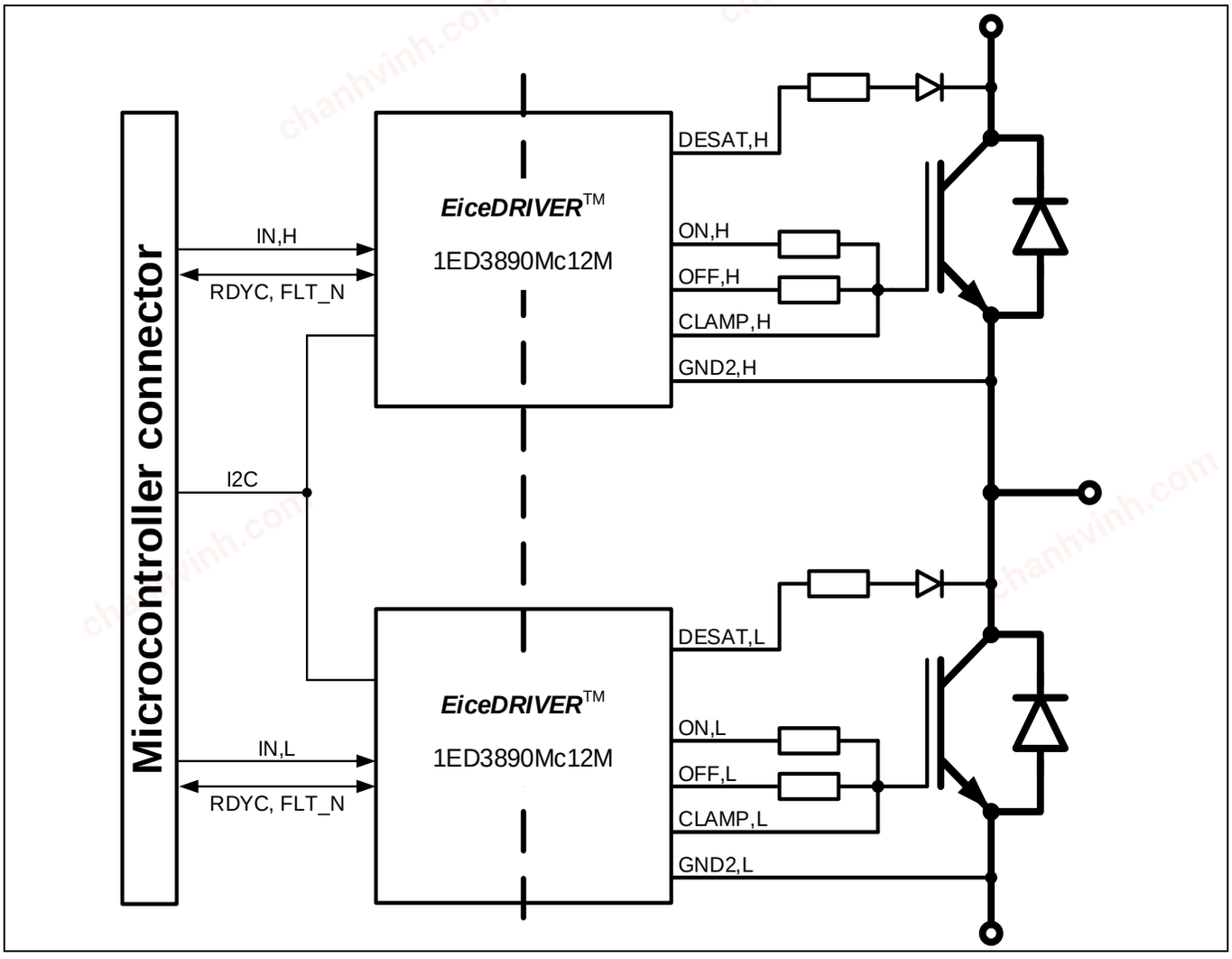


Figure 2 Block diagram of evaluation board

1.3 Main features

The Eval-1ED3890Mx12M is an evaluation board for the 1ED3890MC12M or 1ED3890MU12M gate drivers ICs. It was designed in a half-bridge configuration with a 900 V maximum blocking capability across the power terminals. The board is designed for easy measurement and configuration of the gate driver parameters, and the main features of the board and gate driver include:

- 40 V absolute maximum output supply voltage
- ± 9 A typical sourcing and sinking gate current capability
- Separate source and sink output for optimized gate driving
- Adjustable clamp/clamp driver/ADC pin
- I^2C bus for parameter adjustment, state and fault feedback, ADC measurements and condition monitoring
- Two precise $V_{CE(sat)}$ detection (DESAT[2]) circuits with fault output, adjustable leading-edge blanking time and individually adjustable trigger voltages, filter times
- Two-level turn-off (TLTO) with adjustable slopes, plateau time and plateau level
- Selectable turn-off: hard turn-off and two-level turn-off
- Adjustable soft turn-off after desaturation detection

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- Adjustable input filter
- Hardware undervoltage lockout (UVLO) protection with hysteresis for input side
- Adjustable hardware UVLO with hysteresis for IGBTs and MOSFETs on both VCC2 and VEE2 rails with active shutdown
- Adjustable software UVLO for accurate supply voltage monitoring on both VCC2 and VEE2 rails
- ADC measurement of internal parameters: supply voltages and internal temperature
- Pin state reporting via I^2C and fault
- Internal counters for DESAT or UVLO events
- Gate driver operation at high ambient temperature up to 125°C with over-temperature shutdown at 160°C (±10°C)
- Tight IC-to-IC propagation delay propagation delay matching ($t_{PDD,max}$ = 30 ns)
- Undervoltage lockout protection with hysteresis for input and output side with active shutdown
- High common-mode transient immunity CMTI = 200 kV/µs
- Small space-saving DSO-16 fine-pitch package with large creepage distance (>8 mm)
- Gate driver safety certification:
    - UL 1577 recognized (planned) with $V_{ISO,test}$ = 6840 V (rms) for 1 s, V_{ISO} = 5700 V (rms) for 60 s
    - IEC 60747-17/VDE 0884-11 approval (planned) with V_{IORM} = 1.767 kV (peak, reinforced)

1.4 Board parameters and technical data

The absolute maximum ratings are summarized in Table 2.

Table 2 Absolute maximum ratings

Parameter/Pin	Symbol	Conditions/Notes	Value	Unit
Board power supply input	P15VP	Referenced to signal ground (SGND)	-0.3 … 20	V
Primary side supply voltage	VCC1	Referenced to SGND. Not to be used with EiceDRIVER™ Eval-1ED38x0DCT	-0.3 … 6.5	V
I^2C Serial Clock Line	SCL	Referenced to SGND	-0.3 … 6.5	V
I^2C Serial Data Line	SDA	Referenced to SGND	-0.3 … 6.5	V
Ready state output/ fault-clear input and fault-off input	RDYC	Input/Output digital signal. Referenced to SGND	-0.3 … 6.5	V
Fault output/ fault-off input	FLT#	Input/Output Digital signal. Referenced to SGND	-0.3 … 6.5	V
PWM input for high-side gate driver	IN_HS	Referenced to SGND	-0.3 … 6.5	V
PWM input for low-side gate driver	IN_LS	Referenced to SGND	-0.3 … 6.5	V
Secondary side positive supply voltages	VCC2H/ VCC2L	Referenced to VEE2H/VEE2L. Not to be used with power supply circuit enabled	-0.3 … 40	V
Secondary side negative supply voltages	VEE2H/ VEE2L	Referenced to GND2H/GND2L. Not to be used with power supply circuit enabled	-40 … 0.3	V
DC-link voltage	P1000VP	Referenced to GND power terminal. Limited by component ratings and design clearances. For	-0.2 … 900	V

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Parameter/Pin	Symbol	Conditions/Notes	Value	Unit
		voltages above 42 V, special safety measures should be taken		
Phase peak current	I_{out}		30	A
	t_{pulse}	Maximum ON pulse length for double-pulse tests. Power dissipation should be considered	100	µs
	f_{sw}	Maximum switching frequency for continuous operation. Power dissipation should be considered	100	kHz

The recommended operating conditions are summarized in Table 3.

Table 3 Recommended operating conditions and supply for 3.3 V

Parameter/Pin	Symbol	Conditions/Notes	Value			Unit
			Min.	Typ.	Max	
Power supply input voltage	P15VP	Referenced to SGND	15.0	15.5	16	V
Primary side supply voltage	VCC1	Referenced to SGND. Not to be used with EiceDRIVER™ Eval-1ED38x0DCT	3.2	3.3	3.5	V
I²C serial clock line	SCL	Referenced to SGND	-0.1	*VCC1*	*VCC1*+0.1	V
I²C serial data line	SDA	Referenced to SGND	-0.1	*VCC1*	*VCC1*+0.1	V
Ready state output/ fault-clear input and fault-off input	RDYC	Referenced to SGND	-0.1	*VCC1*	*VCC1*+0.1	V
Fault output/ fault-off input	#FLT	Referenced to SGND	-0.1	*VCC1*	*VCC1*+0.1	V
PWM input for high-side gate driver	IN_HS	Referenced to SGND	-0.1	*VCC1*	*VCC1*+0.1	V
PWM input for low-side gate driver	IN_LS	Referenced to SGND	-0.1	*VCC1*	*VCC1*+0.1	V
Secondary-side positive supply voltages	VCC2H/ VCC2L	Referenced to VEE2H/VEE2L. Not to be used with power supply circuit enabled	12	22	30	V
Secondary-side ground reference supply voltages	GND2H/ GND2L	Referenced to VEE2H/VEE2L. Not to be used with power supply circuit enabled	0	7	15	V
DC-link voltage	P1000VP	Referenced to GND power terminal. For voltages above 42 V, special safety measures should be taken	25	-	800	V

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2 System and functional description

The board is designed to be used in conjunction with EiceDRIVER™ Eval-1ED38x0DCT microcontroller board in order to be able to configure all the parameters in an easy and fast manner. In the following chapter, it is assumed that the EiceDRIVER™ Eval-1ED38x0DCT will be used.

2.1 Getting started

The Eval-1ED3890Mx12M is optimized to be used with both 5 V and 3.3 V VCC1 primary side supply voltage. The threshold values for the primary-side input signals are always proportional to the VCC1 supply voltage.

It is recommended to use the board with the built-in power supply. For a nominal input voltage, P15VP, of 15.5 V, the power supply will provide a bipolar +15 V/-7.5 V supply voltage for the secondary sides for both high-side and low-side gate drivers.

In case separate power supplies will be used on the secondary side, the built-in power supply can be disabled by linking jumper J30.

2.1.1 Prerequisites

- PC with Windows 7 or higher with Infineon XMC USB driver installed
- EiceDRIVER™ 1ED38x0 DCT software installed
- USB A to micro-USB cable
- EiceDRIVER™ Eval-1ED38x0DCT microcontroller board
- Suitable power switches assembled in the sockets T50 and T60. E.g.: IKW50N120CS7 TRENCHSTOP™ IGBTs or IMW120R030M1H CoolSiC™ SiC MOSFETs
- Assembled external high-voltage decoupling capacitor (100 µF) across the high-voltage power terminals: X90-1 (P1000VP) and X90-3 (GND)
- Low-voltage power supply for supplying primary-side power supply circuit, capable of supplying 15 V, 100 mA (P15VP, SGND)
- High-voltage power supply for supplying the power stage between X90-1 (P1000VP) and X90-3 (GND)
- A suitable inductive load for double-pulse testing

2.1.2 Evaluation of Eval-1ED3890Mx12M board with another microcontroller

While not recommended to new users or for fast evaluation, the Eval-1ED3890Mx12M can be used with any microcontroller capable of communicating over I^2C and generating PWM signals. For this, it is important to read the documentation, especially the reference manual, of the gate drivers. Special care should be taken when reviewing the I^2C section, where the byte format, read/write operation and initial addressing are described. After the review, the EiceDRIVER™ 1ED38x0 DCT can be used to configure the registers settings and export them, as shown in Chapter 2.2.5.

2.1.3 Power-up sequence

1. Connect the EiceDRIVER™ Eval-1ED38x0DCT to the connector X1 of the EiceDRIVER™ Eval-1ED38x0DCT via the ribbon cable.
2. Connect the EiceDRIVER™ Eval-1ED38x0DCT via the USB cable to the computer used for configuration.
3. Ensure that jumper J30 is open in order to have the built-in power supply enabled.
4. Connect one end of the inductive load to terminal X90-2 (PHASE) and the other end, depending on the double-pulse test requirements, to either X90-1 (P1000VP) or X90-3 (GND) for low-side or high-side testing.

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5. Supply the input side power supply, P15VP, at connector X45 with +15.5 V and ground.
6. The green LED D46 (15V_ok) will turn on to signal the input supply is present.
7. The green LED D40 (VCCC1_ok) will turn on to signal the primary side supply of the gate driver is present
8. The green LED D41 (FLT#) will turn on, signaling there is no internal fault registered in the gate driver.
9. The red LED D44 (RDYC) will turn on, signaling the gate driver is not configured.
10. Start the EiceDRIVER™ 1ED38x0 DCT and configure the gate drivers (see Chapter 2.3)
11. Connect the high-voltage supply to connector X90-1(P1000VP) and X90-3 (GND).

The board is now ready for double-pulse evaluation.

2.2 Introduction to EiceDRIVER™ 1ED38x0 DCT

This chapter will only provide a short overview of the EiceDRIVER™ 1ED38x0 DCT, for a more in-depth explanation of the software, please read EiceDRIVER™ Eval-1ED38x0DCT user guide.

The 1ED3890MC12M or 1ED3890MU12M gate driver present on the evaluation board is highly configurable via I^2C. In order to familiarize yourself with it, and to easily evaluate its performance with no programming required, the EiceDRIVER™ Eval-1ED38x0DCT microcontroller board can be used with the EiceDRIVER™ 1ED38x0 DCT. It is recommended that first-time users select the guided mode (Chapter 2.2.2), as this also provides a detailed explanation of each configurable parameter.

2.2.1 Main window

When the software is started with the EiceDRIVER™ Eval-1ED38x0DCT board connected to the computer, the screen in Figure 3 appears.

The top of the windows, shown in Figure 3-a, allows for easy access to the file menu and the three main configuration modes: guided mode, advanced mode and hardware mode. This allows for easy changing from one mode to the other. If the user would like to go to the previous view, there is also a dedicated button for that.

In the middle part of the window, an easy-start mode is proposed in 3 steps, shown in Figure 3-c. Or if the software was previously used, a quick-start button appears that allows the last used configuration to be loaded, as shown in Figure 3-b. The software comes with a few pre-settings for the board, which are a good starting point, and which can be altered afterwards.

At the bottom of the windows, the status of the USB connection, I^2C and the FLT_N and RDYC pins is shown as seen in Figure 3-d. To the right, there is a short log message that presents the status of the activities.

Once a gate driver is configured as desired, all settings can be saved as a preset using the **File → Save user preset**. This can then be transferred to another system and loaded using the **File → Load user saved preset option**.

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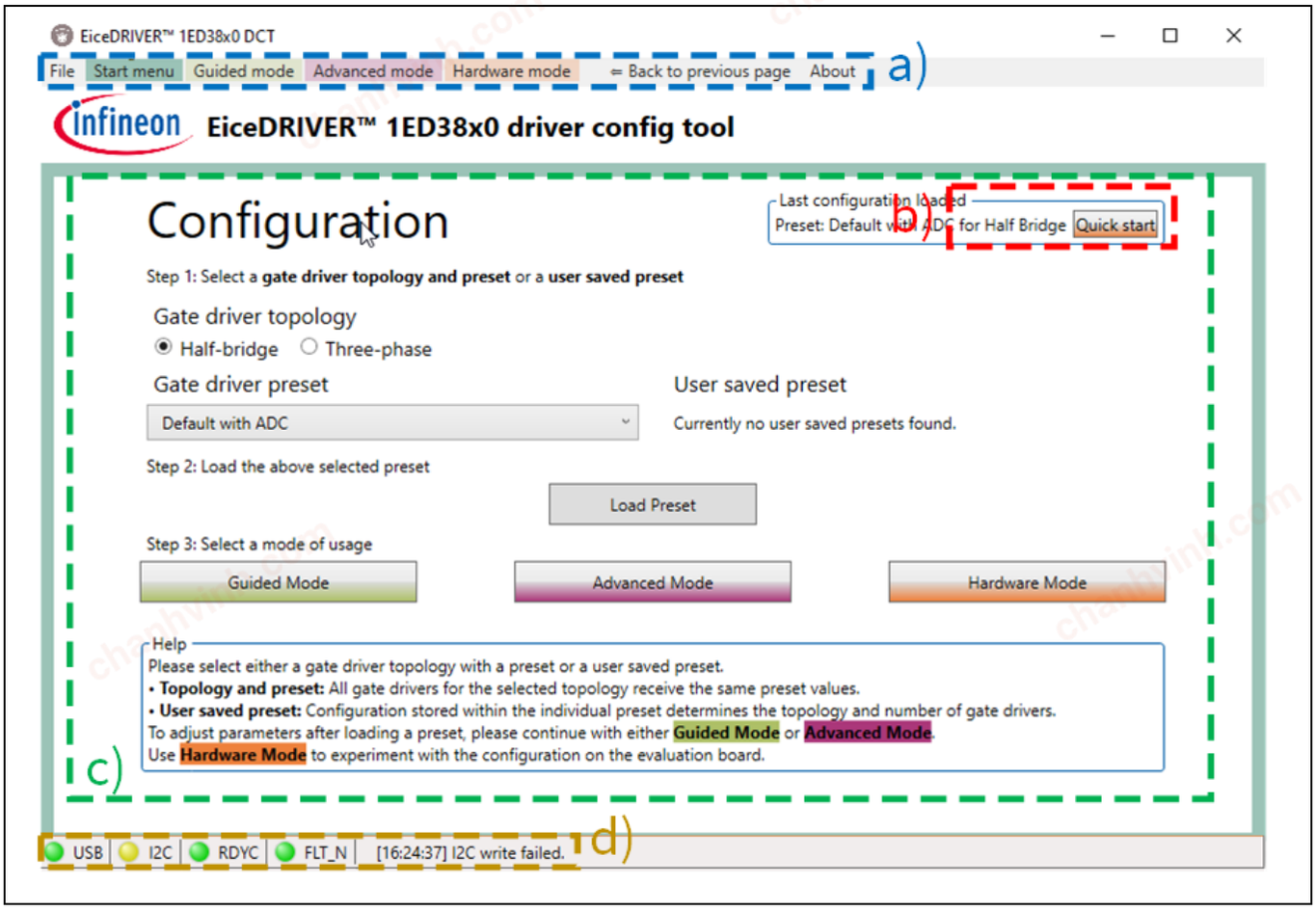


Figure 3 Main window of EiceDRIVER™ 1ED38x0 DCT: a) top menu; b) reload last session configuration; c) main window; d) State signaling and log information

2.2.2 Introduction to guided mode

The guided configuration mode is entered by clicking on the green button in Figure 3, and will provide a detailed explanation of each configurable parameter. Afterwards, each of the 49 setting windows can be navigated through, either by using the drop-down menu as shown in Figure 4-a or by using the navigation buttons in Figure 4-c. On page 49, there is an option to copy the settings also to the high-side gate driver. On each page, the parameters can be adjusted in the area shown in Figure 4-b, and a full explanation of each parameter with the associated register configuration is provided in Figure 4-d.

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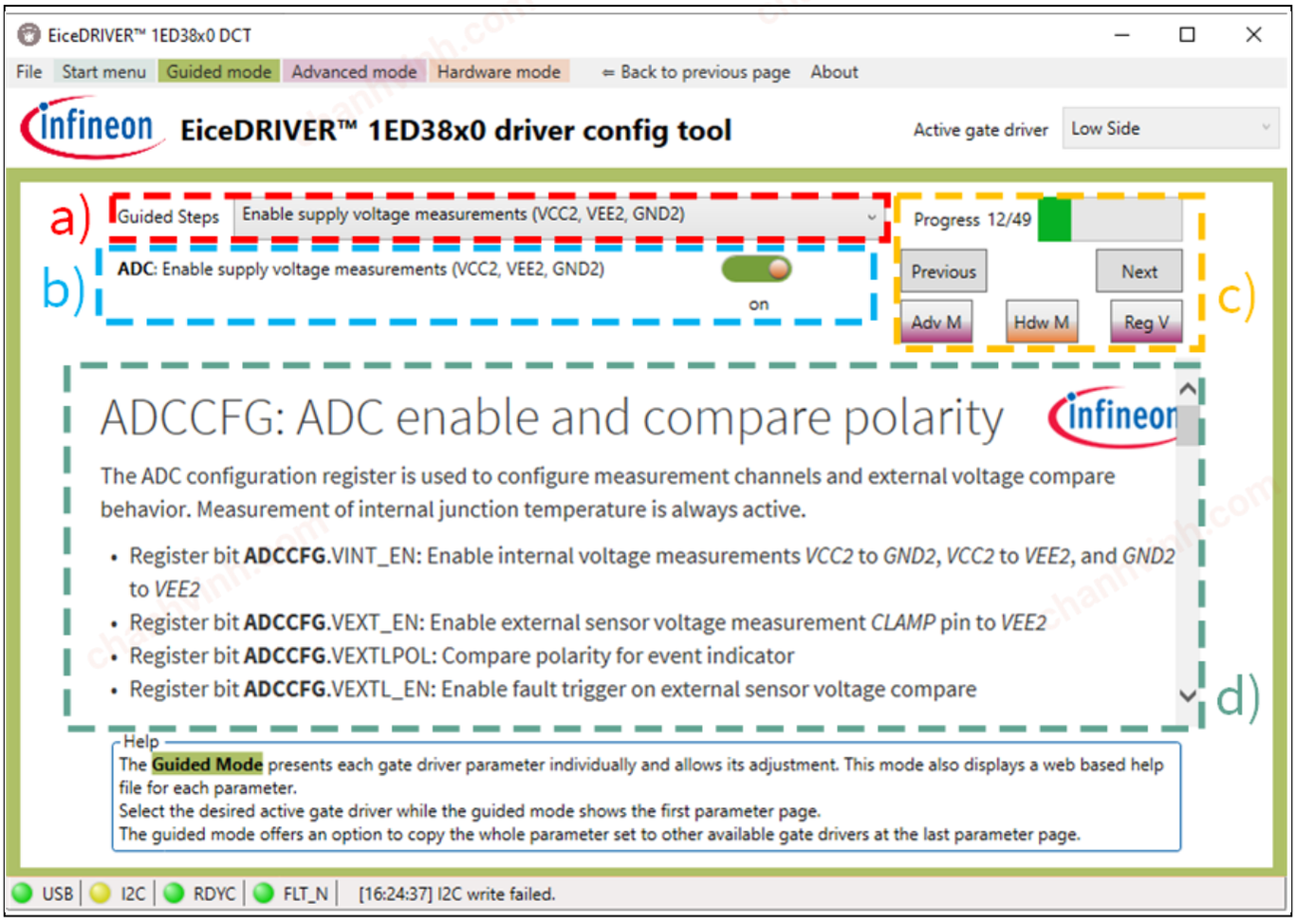


Figure 4 Guided mode view of EiceDRIVER™ 1ED38x0 DCT: a) step/setting selection; b) parameter adjustment; c) navigation panel; d) parameter explanation window

2.2.3 Introduction to advanced mode

The advanced configuration mode is entered by clicking on the magenta button in Figure 3. Figure 5 shows the window of the advanced configuration mode. Using the button in Figure 5-a, the active gate driver for which the settings are made can be easily selected between the low-side one and the high-side one.

Each of the adjustable parameters are grouped into eight tabs based on their main function, as shown in Figure 5-b.

The last tab, Register View, can be used to observe the registers' hexadecimal values for the high-side and low-side gate drivers. The register view can also be used to save the current registers' configuration as an XML file, load a previously saved configuration, transfer the configuration to the gate driver, or read the current registers' configuration in the gate drivers.

After adjusting the settings on each of the settings tabs, in the area marked in Figure 5-c, the impacted registers are shown with their new value. By using the DT button or GT button, the settings can be pushed to the active gate driver, or to all the connected gate drivers, respectively. Before moving to another section, all the changed settings have to be pushed to the gate driver, by using one of the two buttons.

In the section marked in Figure 5-d, the setting for that specific group can be changed. In case any of the parameters are unclear or a refresh is needed, clicking on the parameter name will switch to the guided mode

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for a more detailed description about that specific parameter. In order to return back to the same place in the guided mode, the “back to previous page” button at the top can be used.

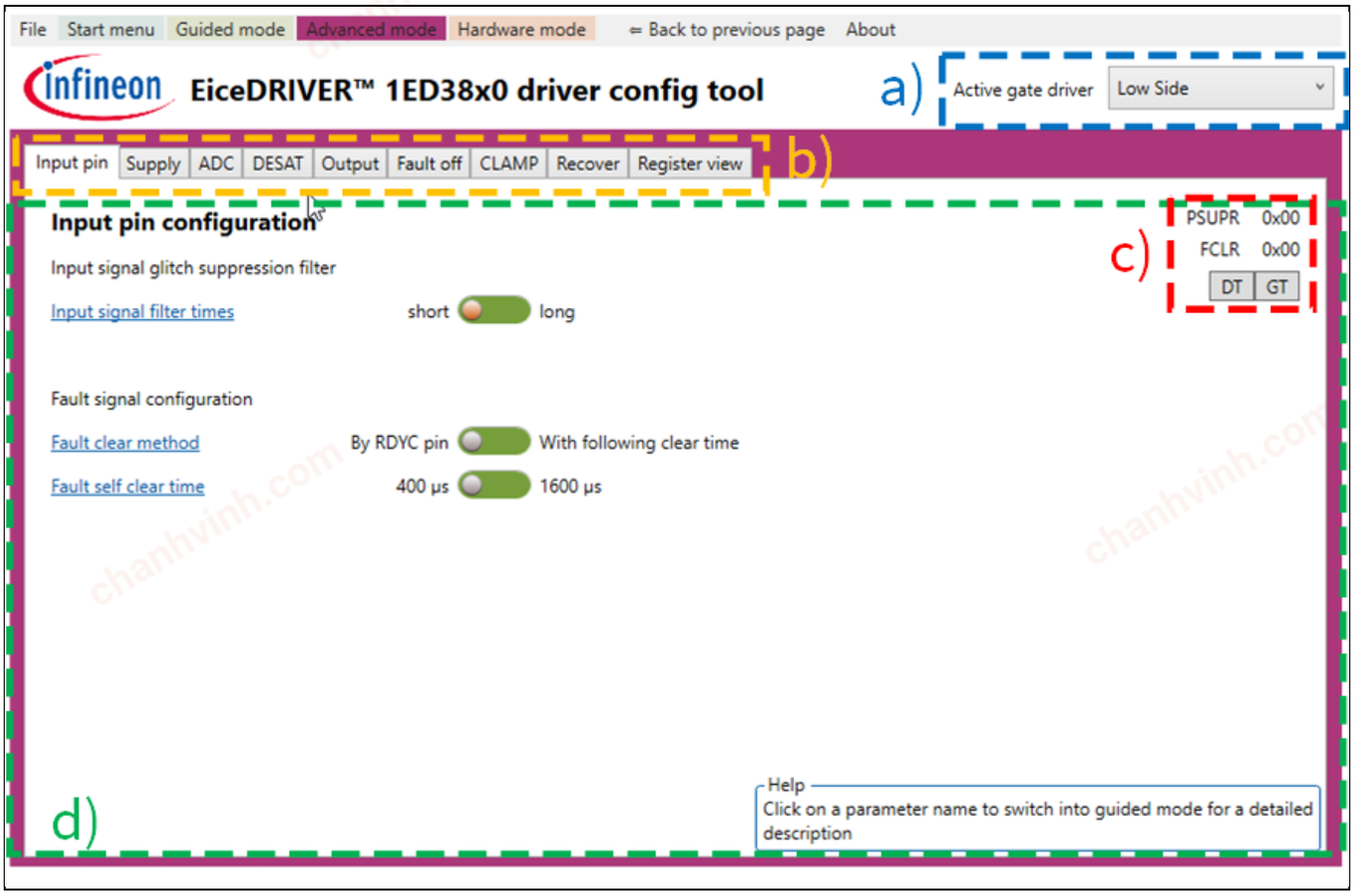


Figure 5 Advanced mode view of the EiceDRIVER™ 1ED38x0 DCT: a) active gate driver selection; b) tabs for grouped settings; c) single gate driver/group update buttons; d) main settings window

2.2.4 Introduction to hardware mode

The hardware mode is entered by clicking on the orange button in Figure 3. On the top, as shown in Figure 6-a, there are two tabs for switching between the connection interface and the status tab. The I^2C connection settings and addresses can be adjusted, as shown in Figure 6-b. The default settings should not be changed unless you understand what the impact is, or have been instructed to do so by Infineon customer support. In Figure 6-c, the connection settings can be adjusted, such as connecting and disconnecting to the EiceDRIVER™ Eval-1ED38x0DCT board, load presets, setting the address and currently configured registers, and resetting the XMC microcontroller.

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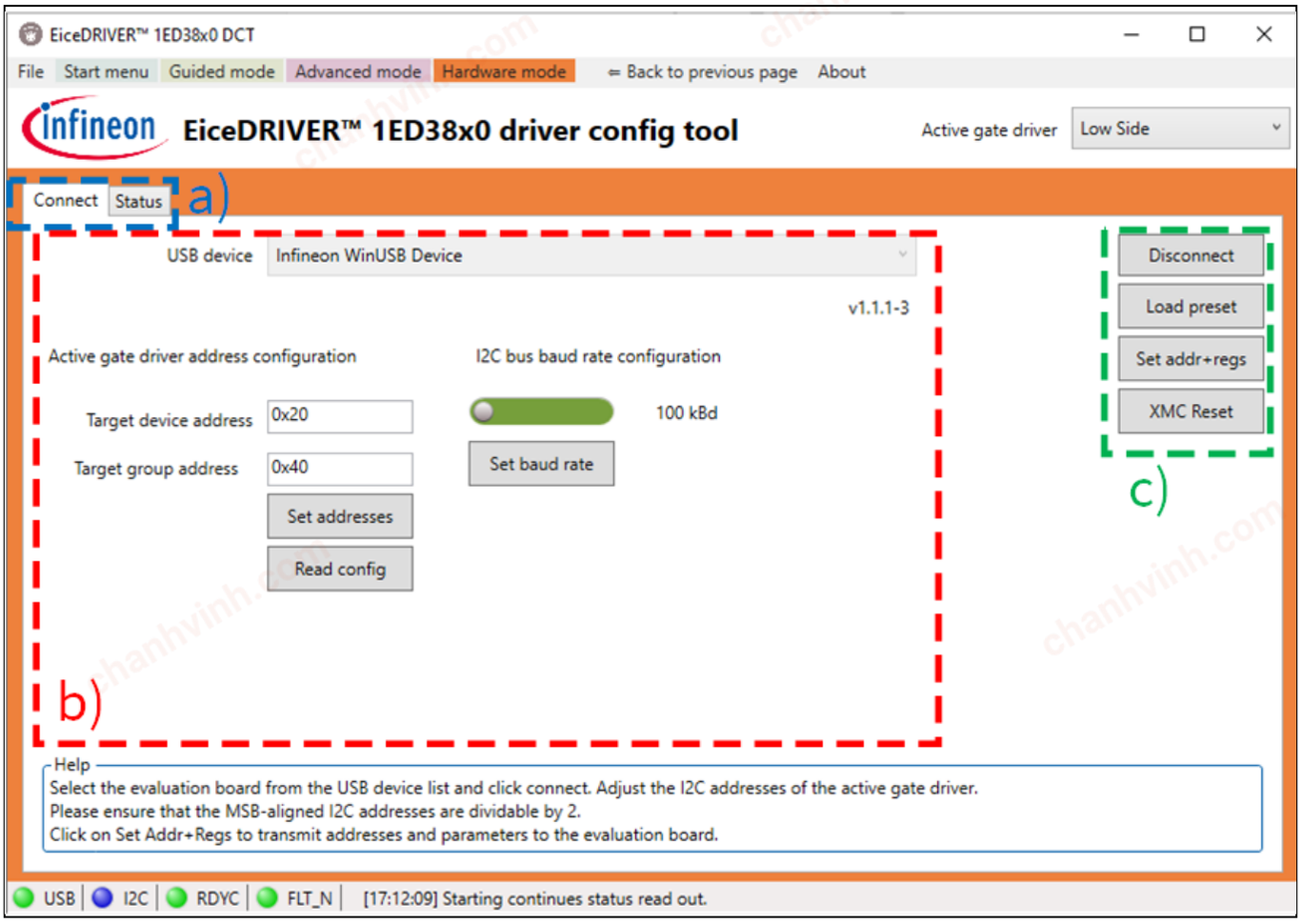


Figure 6 Hardware mode of the EiceDRIVER™ 1ED38x0 DCT: a) connection/status tabs; b) I²C window settings; c) XMC connection and gate driver configuration buttons

Figure 7 shows the status tab of the hardware menu. Using the selector shown in Figure 7-a, it is possible to select the gate driver for which the state and register values will be monitored. In the area highlighted by Figure 7-c, the state registers are shown by color coding in an easy-to-read manner. These are read by the microcontroller and passed on to the EiceDRIVER™ 1ED38x0 DCT. Hovering the pointer over any of the state registers names will bring up a short description of their meaning in the area shown in Figure 7-b. Hovering the pointer over the colored indicator will give a short explanation of the event that triggered the state.

In the area shown in Figure 7-d, the counter registers values and the ADC registers values are displayed in an easy-to-read way together with their hexadecimal values. These are read by the microcontroller and passed on to the EiceDRIVER™ 1ED38x0 DCT.

In order to aid the evaluation, a simple-pulse generator is configured into the microcontroller EiceDRIVER™ Eval-1ED38x0DCT as seen in Figure 7-e. Here, 4 different states are available: 1) PWM off; 2) static on/off for low-side/high-side 3) pulse generator for double-pulse testing for low or high-side, and lastly 4) PWM generator with dead time for the half-bridge.

Note: During the evaluation, if a fault event occurs and FLT_N goes low, it can be cleared by clicking on the FLT_N in Figure 7-c or in the status bar in the lower part of the EiceDRIVER™ 1ED38x0 DCT.

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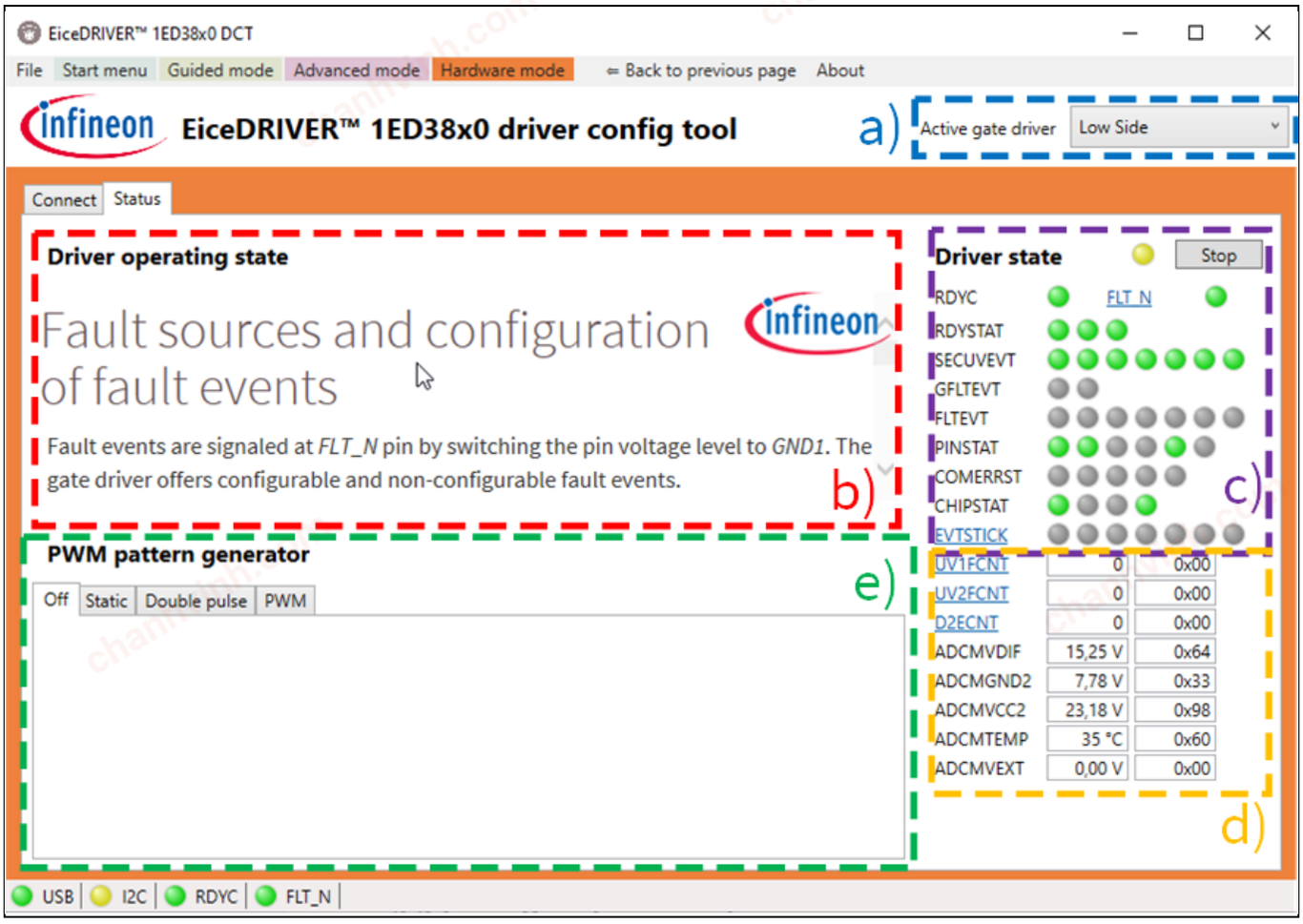


Figure 7 **Status view of the EiceDRIVER™ 1ED38x0 DCT: a) active gate driver selection; b) explanation of driver-state registers; c) feedback state of status registers; d) counters and ADC registers values; e) PWM generator interface**

2.2.5 Registers exporting

The EiceDRIVER™ 1ED38x0 DCT can also be used as a stand-alone tool to set the 1ED38x0Mx12M registers in an easy-to-follow manner. Using the register view, the settings for the high-side and low-side gate drivers can be seen in hexadecimal value, as shown in Figure 8. After following the flow in the guided mode or advanced mode flow, the registers settings can be exported in an easy-to-read XML format for later review, using the buttons in Figure 8-a. As an alternative, the file menu can also be used to save the configuration. This would allow for simple export of the gate-driver settings, and integration at a later time in any microcontroller code.

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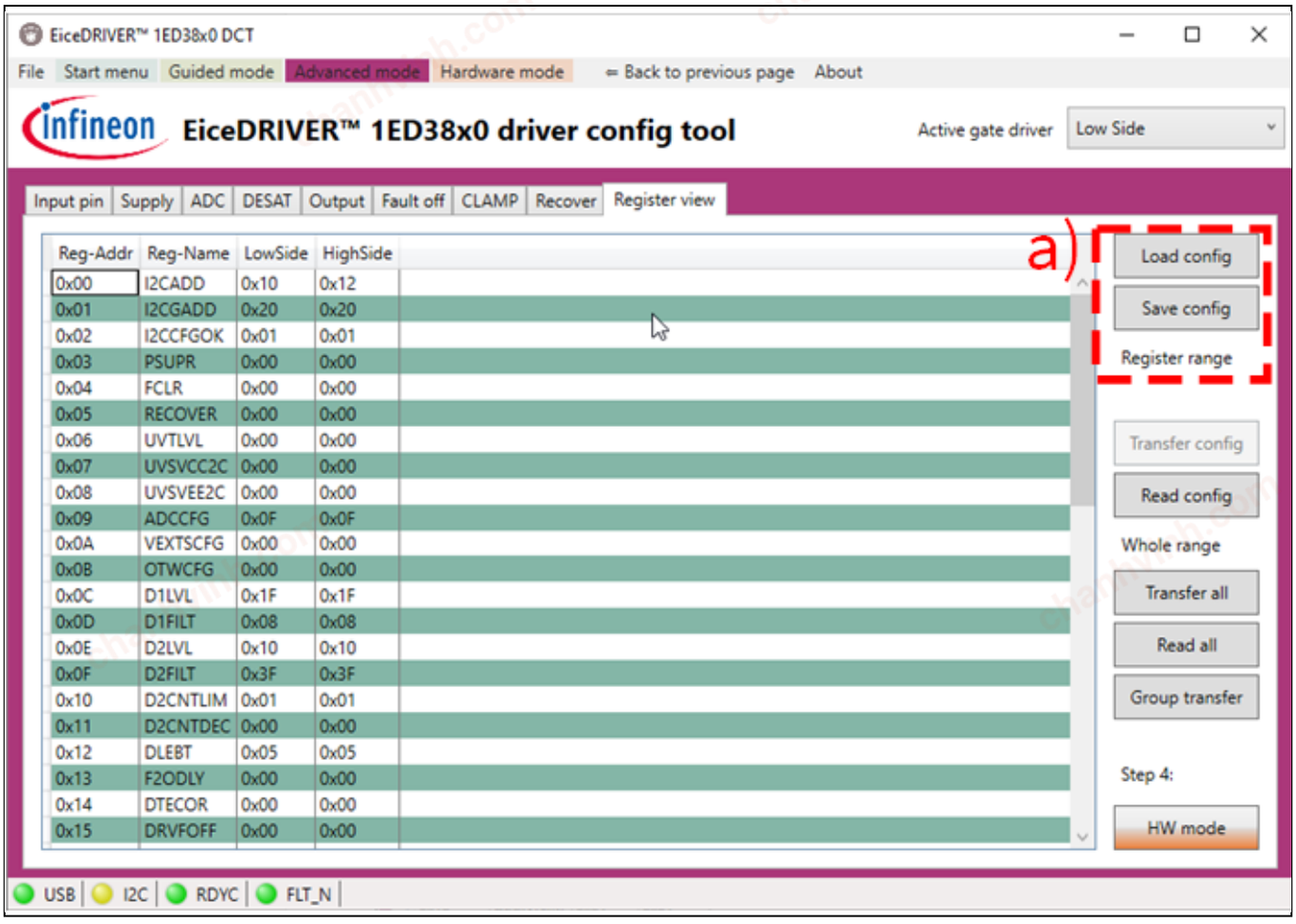


Figure 8 Register view of the EiceDRIVER™ 1ED38x0 DCT: a) register configuration saving/loading

2.3 Gate driver configuration

The gate driver has an extensive range of configurable settings. In the following chapters, these will be briefly presented to support the user in getting started. The parameter selection will be based on the advanced mode (chapter 2.2.3) in the EiceDRIVER™ 1ED38x0 DCT. It is always recommended to read the reference manual for a complete understanding of the gate driver IC registers settings. After adjusting the settings, and before navigating away from the window, remember to select the DT or GT button in order to send the settings to the gate driver board.

2.3.1 Input settings

Two input filter times can be selected based on application requirements by adjusting the register *PSUPR* value. This setting impacts both the PWM input as well as the I^2C communcation pins, and allows for a better filtering of the input signals in noise-prone applications. The input settings are shown in Figure 9. Here the input filter times can be controlled together with the gate-driver fault-signal clearing mode.

For the PWM input, *IN*, the input filter can be selected between short, 100 ns, or long 200 ns. This is shown in Figure 10, where the input pulse width is varied from 90 ns to 101 ns and to 201 ns. In one case, the input filter is set to 100 ns, resulting in the gate driver ignoring any pulse shorter than 100 ns. In the second case, the 200 ns filter rejects any signal under this value.

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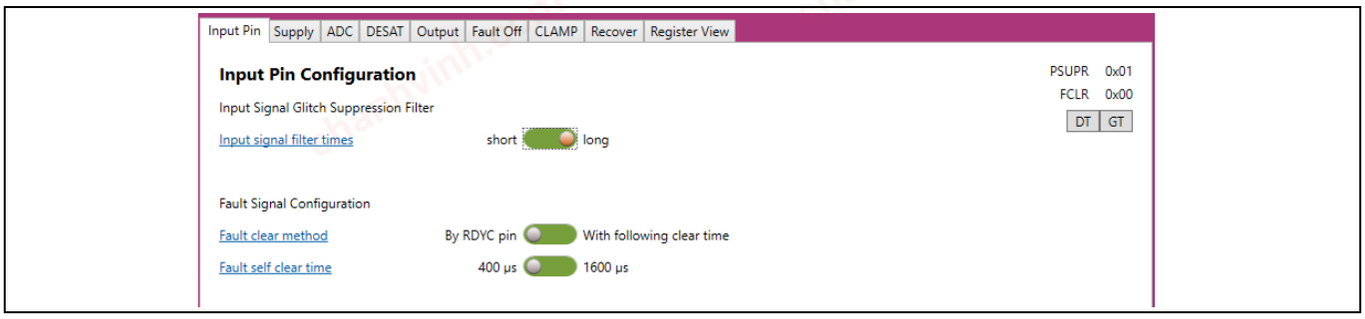


Figure 9 Input settings window

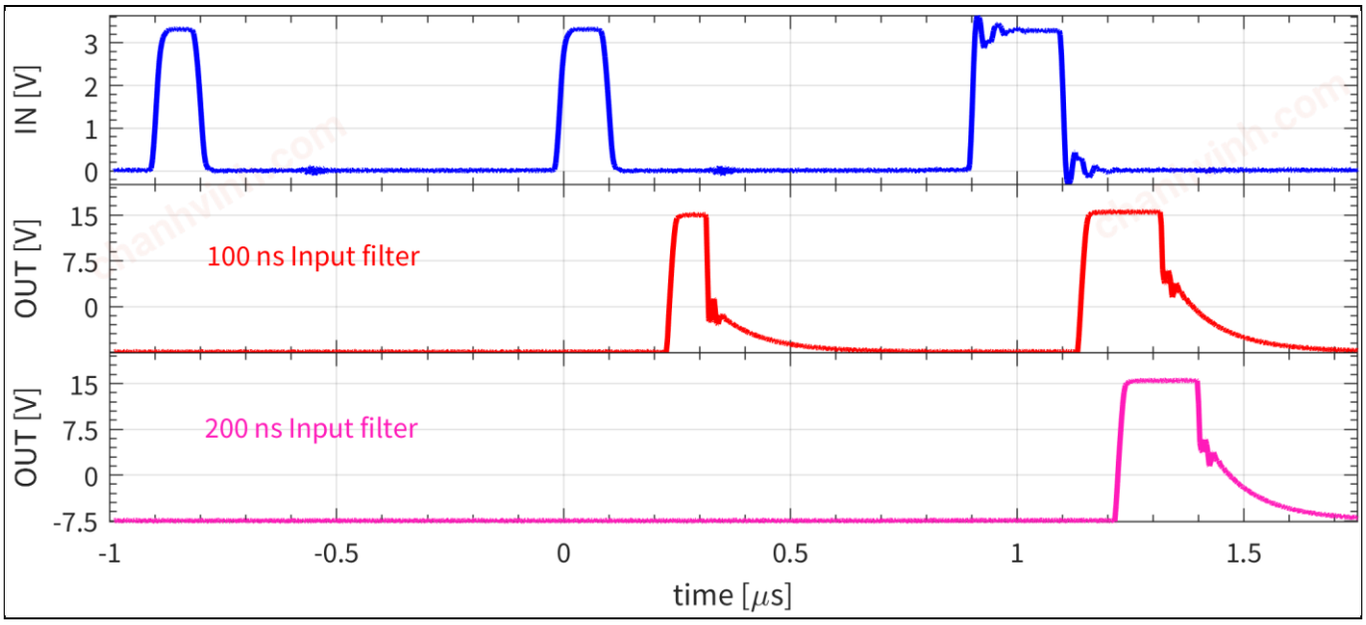


Figure 10 Input filter waveform

Clearing of the fault signal can be also configured to be performed by either the RDYC pin, or to be self-cleared based on an adjustable timer, with settings of 400 µs or 1600 µs.

2.3.2 Supply configuration

As shown in Figure 11, the gate driver has substantial undervoltage lockout (UVLO) settings for the secondary-side power supply. As seen in Figure 11-a, the gate driver secondary side allows two positive settings: IGBT and MOSFET, VCC2-GND2. These are designed to fit most applications on the market. Independently, a negative UVLO setting, VEE2-GND2, can also be adjusted in three discrete values for applications that require negative gate voltages for correct operation.

For fine-tuning, of more demanding applications or enhanced protection, the gate driver comes with a software-based UVLO function, as shown in Figure 11-b. This feature allows the use of finely adjusted UVLO filters for the positive, VCC2, and negative, VEE2 rails. For the positive power rail, the threshold can be adjusted in 15 discrete values of 0.5 V up to 17 V. For the negative power rail, the resolution is 1 V and can be set between -2 V and -17 V as required. This is a heavily filtered ADC measurement, which disables the output if the supply voltage goes below the set threshold, for VCC2, or the threshold, for VEE2. Operation is automatically resumed once the supply voltage returns above the threshold.

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Figure 12 shows the software UVLO function operation with a set VCC2 threshold voltage of 14.5 V, with the fault-off behavior shown in Figure 12-a, and resuming operation in Figure 12-b.

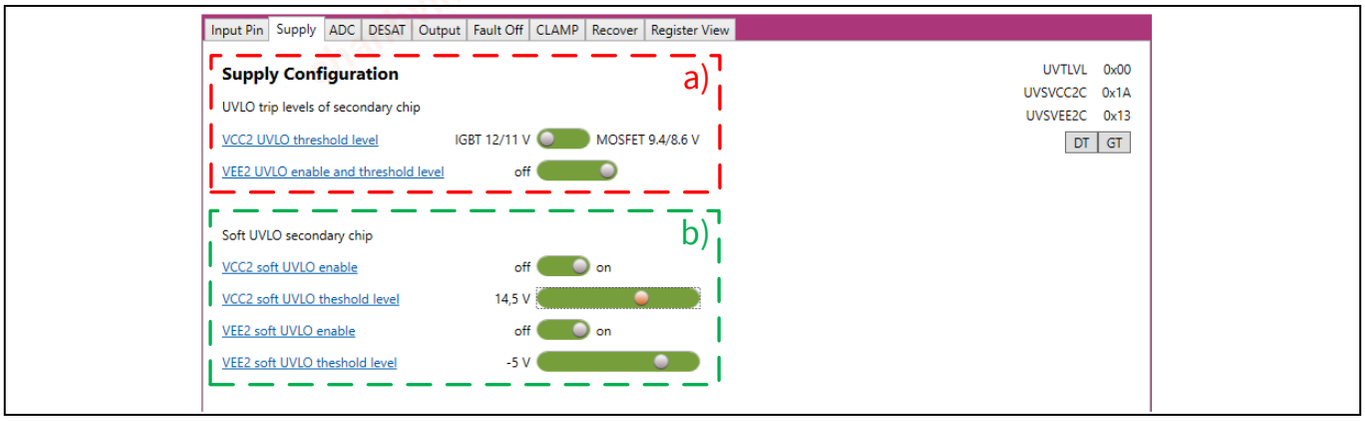


Figure 11 Supply configuration window: a) hardware UVLO settings; b) software UVLO settings

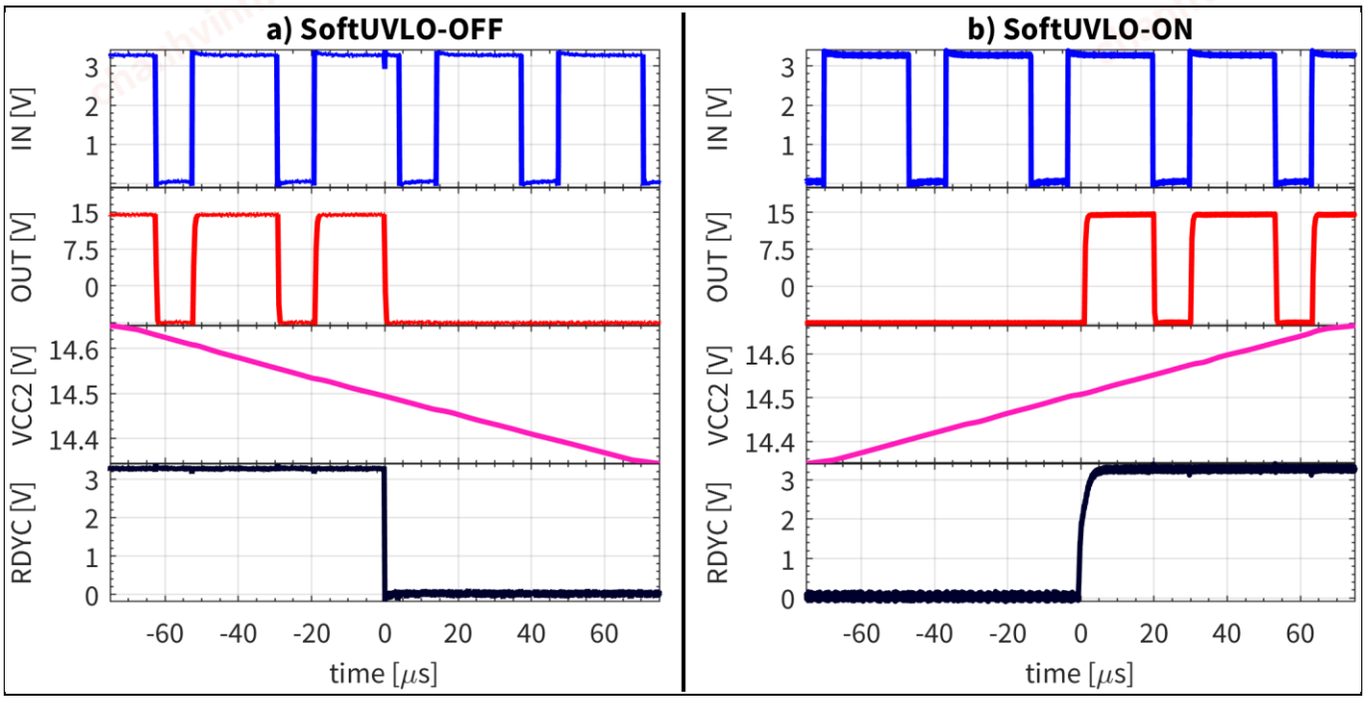


Figure 12 Software UVLO with VCC2 threshold at 14.5 V: a) VCC2 dipping under threshold; b) VCC2 returning above threshold

2.3.3 ADC configuration

Figure 13 shows the extensive ADC measurement and monitoring capabilities of the gate driver. This makes it possible to enable the internal ADC measurement of the secondary side power supply voltages, VCC2 and GND2, referenced to VEE2, as observed in Figure 13-a. Afterwards this can be read in the status window, as shown in Figure 7-d, under the hardware tab of the EiceDRIVER™ 1ED38x0 DCT. Using the options shown in Figure 13-b, the CLAMP pin can be enabled as an input for ADC measurements. As the CLAMP pin can also be used as a clamp or clamp driver, as shown in Chapter 2.3.7, it is recommended to disable that functionality when used as an ADC measurement.

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The gate driver gives the possibility to compare if the ADC measured voltage is above or below an adjustable threshold value, and can even trigger a fault event in such a case.

The threshold reference voltage is an 8-bit adjustable reference between 0 V and 2.88 V. The internal comparator can be configured to trigger an event if the measurement is above or below the reference value, and if desired, this set flag can also trigger a fault even in the gate driver.

The internal ADC also samples the internal IC temperature. This can be configured to trigger a warning once an adjustable threshold value is reached. This threshold can be configured in eight discrete values from 95°C to 140°C. If desired, the over-temperature can also be enabled to trigger a fault event.

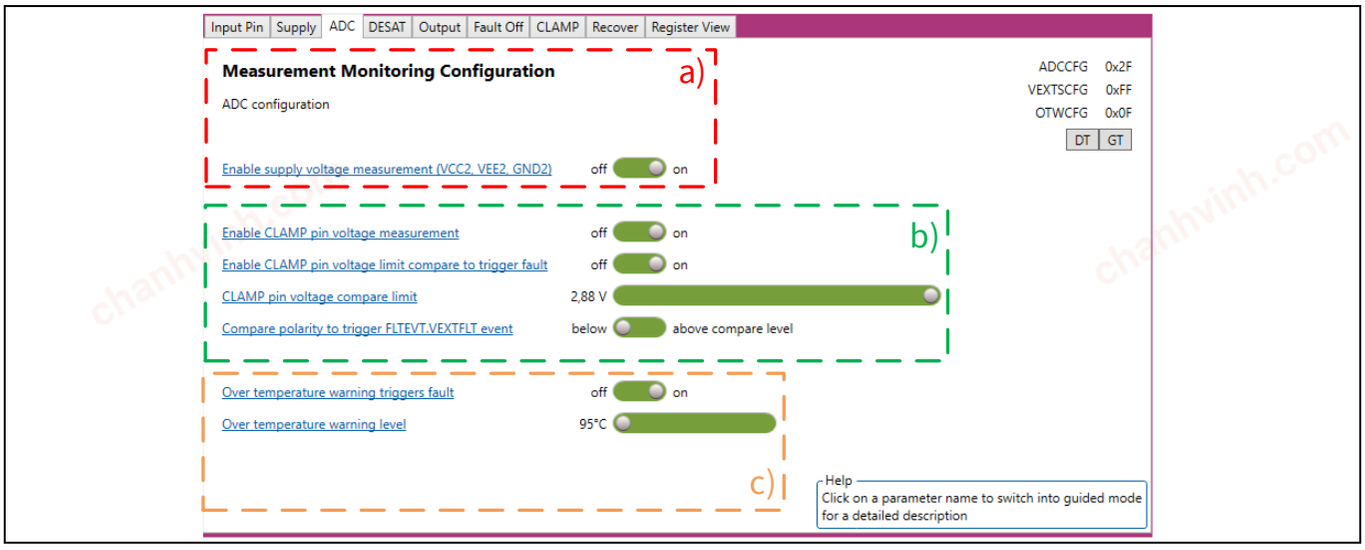


Figure 13 ADC setting of the gate driver: a) supply voltage measurement; b) CLAMP pin measurement options; c) internal temperature measurement options

In this evaluation board, if the clamp or clamp driver functionality is not needed, the CLAMP ADC can be used to measure a thermistor on the PCB for the high-side gate driver, or to sample the DC-link voltage through a voltage divider for the low-side gate driver. By default, the evaluation board comes with the circuitry configured for the CLAMP pin to be used as a clamp pre-driver, and is designed to be easily reconfigured. The hardware changes required to adjust the CLAMP pin as a clamp, clamp driver and ADC for NTC or DC-link measurements are shown in Chapter 2.5.

2.3.4 DESAT configuration

Figure 14 shows the extensive options of the DESAT function of the gate driver. As this gate driver contains two DESAT detection circuits which, when enabled, can be independently adjusted, it provides great flexibility in standard applications. Both DESAT circuits use the same DESAT pin and leading-edge blanking (LEB) transistor, and are completely digital. This translates into more complex internal functionality and simplified external circuitry, with no need for a DESAT capacitor and the associated variations that come with component tolerances.

The main DESAT function, DESAT1, can be used as the classic DESAT protection to detect when the power switch is short-circuited or goes into soft saturation, and to trigger a fault-off event. This will result in the power transistor being turned off, the gate driver output will be turned off and the FLT_N pin will be pulled low.

The second DESAT function, DESAT2, can be disabled independently of DESAT1, and can be used with a completely different set of trigger values and filter timings. The DESAT2 comes with an increased number of

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features aimed at conditional monitoring. If desired, the DESAT2 can be set to only count the occurrence events, or to trigger after a certain number of DESAT2 events, making it ideal for conditional monitoring. Or it can enable another detection point for desaturation, such as soft desaturation in drives when the short circuit is at the end of a long cable.

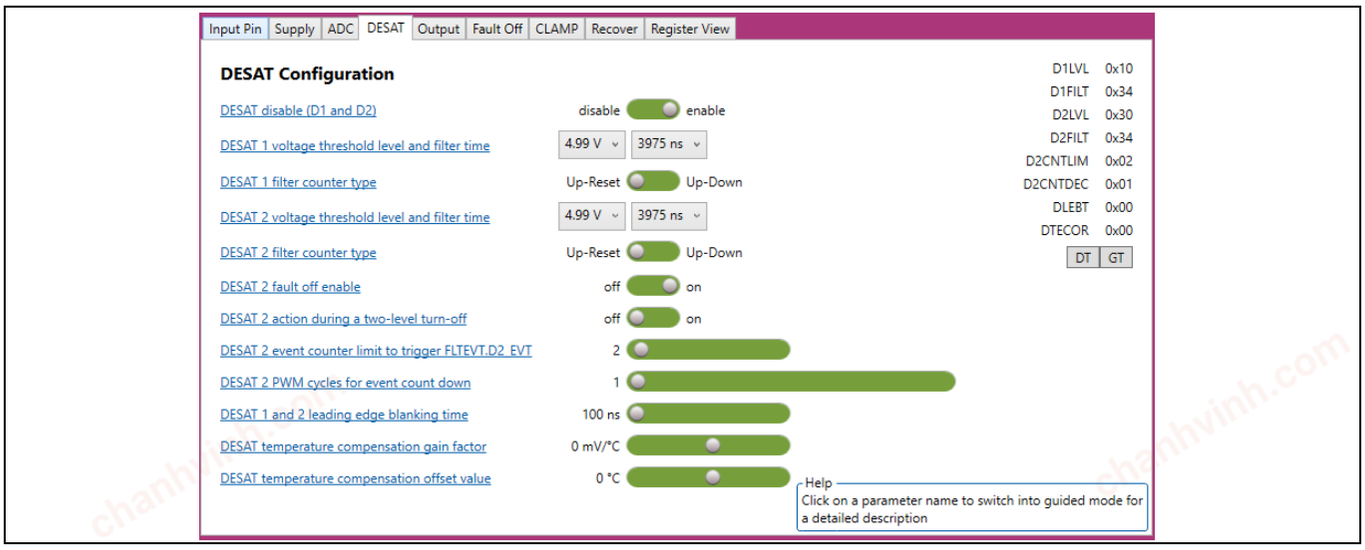


Figure 14 Extensive DESAT settings of the gate driver

2.3.4.1 Leading-edge blanking time configuration

Both DESAT functions share the same LEB filter time, which can be adjusted in 64 discrete values, from 100 ns up to 3.3 µs. Figure 15 shows an example of six different LEB filters referenced to the gate signal. The LEB will allow filtering of false triggering events, where the voltage across the transistor could still be above the threshold value at turn-on, or when excessive noise is present at the DESAT pin during turn-on.

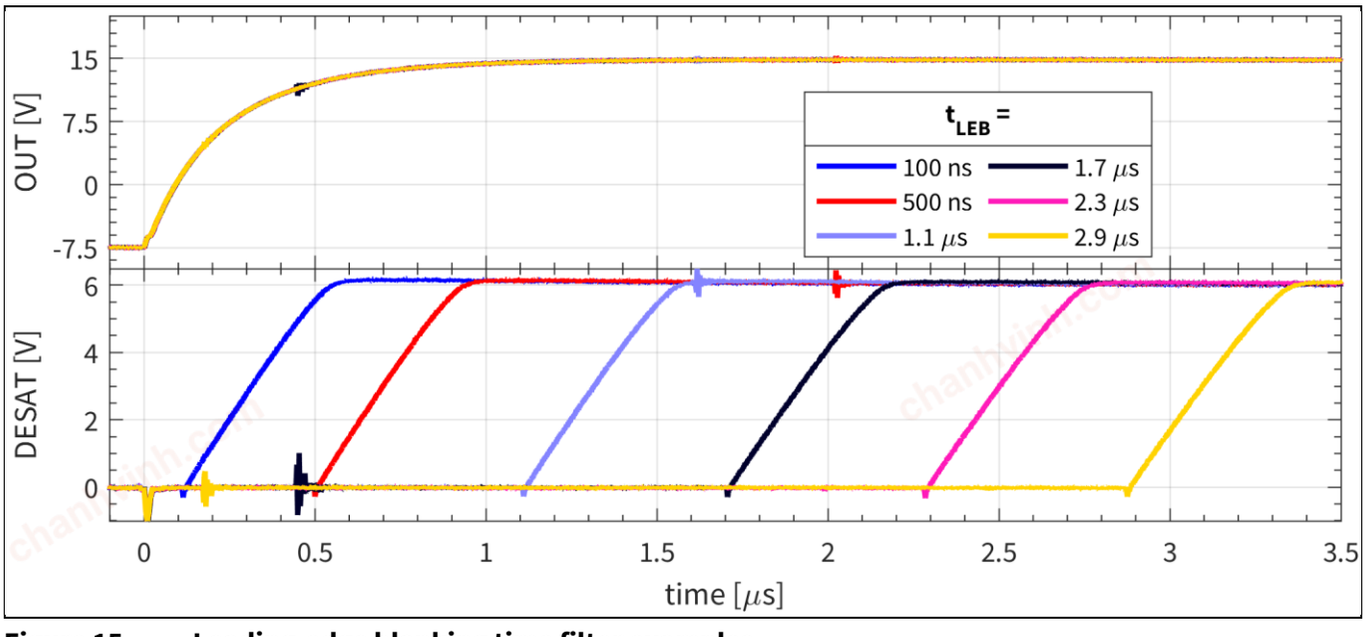


Figure 15 Leading-edge blanking time filter examples

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2.3.4.2 DESAT filter time configuration

Both DESAT1 and DESAT2 circuitry have adjustable filter-time configurations for the DESAT event triggering. This can be done in 32 discrete values to best fit the application. In Figure 16, a few examples of these are shown. For all the measurements, the LEB filter was adjusted to 100 ns, and the DESAT threshold voltage to 4.99 V. By adjusting the filter timing, the gate-driver reaction time to DESAT events can be adjusted. This can be decreased for fast detection of short circuits, or increased for cases where a fast reaction time might not be desired, such as noise-prone applications. The DESAT1 filter counter type was set to UP-RESET. This means that after the voltage at DESAT1 passes the set threshold, the counter will start increasing. However, if it drops under the threshold, it will be reset, and a new filter interval will have to elapse. If the filter counter type is set to UP-DOWN, the counter will start increasing once the voltage at the DESAT pin goes above the threshold voltage, and if it drops below the threshold voltage, it will decrease.

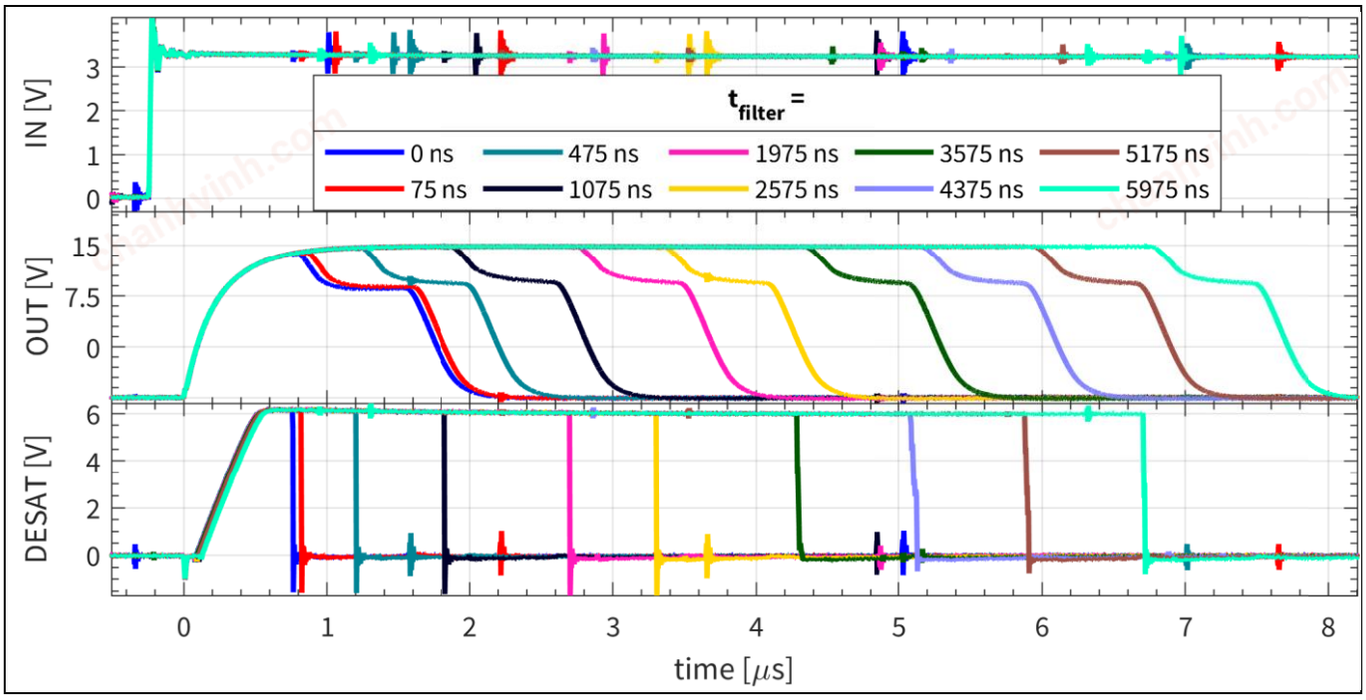


Figure 16 DESAT filter time examples with LEB = 100 ns and $V_{DESAT,th}$ = 4.99 V

2.3.4.3 DESAT threshold voltage configuration

Both DESAT1 and DESAT2 circuitry have adjustable threshold voltage configuration for the DESAT event triggering. This can be adjusted in 32 discrete values to best fit the applications. Figure 17 shows a few examples of the setting. For all the measurements, the leading-edge blanking filter was set to 100 ns, and the DESAT filter was adjusted to 1575 ns. The adjustable threshold voltage for the DESAT functions allows for a great customization of the DESAT protection. This enables a faster detection of the desaturation event in order to improve short-circuit detection. At the same time, the DESAT2 function can be used with a lower threshold voltage, and detect abnormal increases in the forward voltage drop across the power transistor. It will also store the number of events in the register D2ECNT without necessarily triggering a fault-off event. This can then be read by the microcontroller and assessed for future use in applications such as predictive maintenance.

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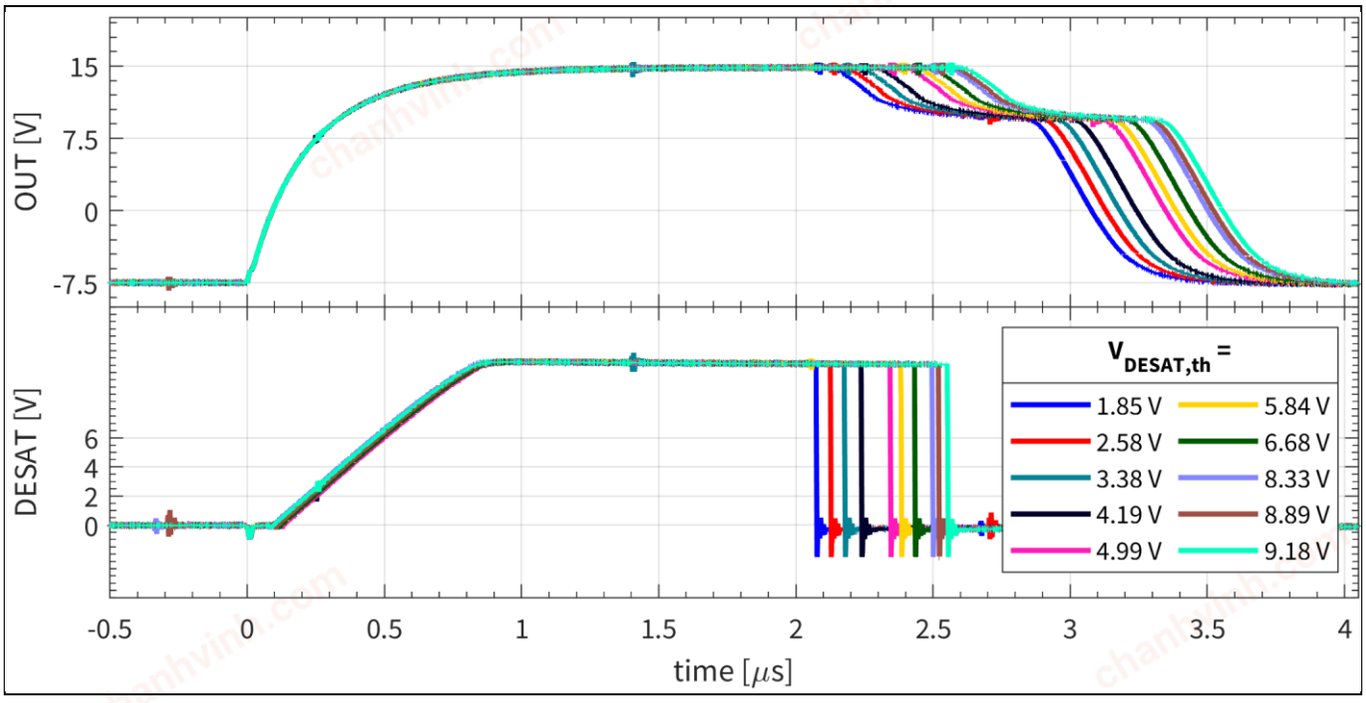


Figure 17 DESAT threshold voltage examples with LEB = 100 ns and t_{DESAT} = 1575 ns

2.3.4.4 DESAT2 event counters

The DESAT2 function can be disabled independently of DESAT1, and at the same time can be enabled to trigger a fault-off event, or to count the number of desaturation events in the D2ECNT register based on the DESAT2 settings. This expands the DESAT2 usability for other preemptive functions, such as condition monitoring and preventive maintenance.

If the DESAT2 function is turned on and enabled to trigger a fault-off event, it can be used in combination with the counter, D2ECNT, and the registers D2CNTLIM and D2CNTDEC. This makes it possible to trigger a fault-off event only after a certain number of desaturation events have been detected. D2ECNT is a six-bit counter without overflow. The gate driver register, D2CNTLIM, a six-bit register, adjusts the limit at which the fault-off event will be triggered. At the same time, the DESAT2 function has another eight-bit counter for PWM cycles without events, D2CNTDEC, which can be used to count down, or substract, the DESAT2 events in D2ECNT. In order to make this clearer, Figure 18 can be used as an example. Table 4 summarizes the DESAT2 settings for the example measurements. During the first switching event, the DESAT2 function is triggered, and the D2ECNT is increased to one. During the second switching the voltage at the DESAT pin is under $V_{DESAT2,th}$. As D2CNTDEC is one, the D2ECNT counter will decrease by one. Afterwards, for the 3 and 4 PWM cycle on the input, the D2ECNT is increased by one each time. As the limit set in D2CNTLIM is two, this would trigger a fault-off event. This can be observed in the *OUT* and *FLTN* waveforms. After the gate driver output is disabled, the following input PWM signals on the input are ignored.

Table 4 DESAT2 settings for the example

$V_{DESAT2,th}$	LEB	t_{DESAT2}	DESAT2 fault-off enabled	D2CNTLIM	D2CNTDEC
4.99 V	100 ns	3975 ns	ON	2	1

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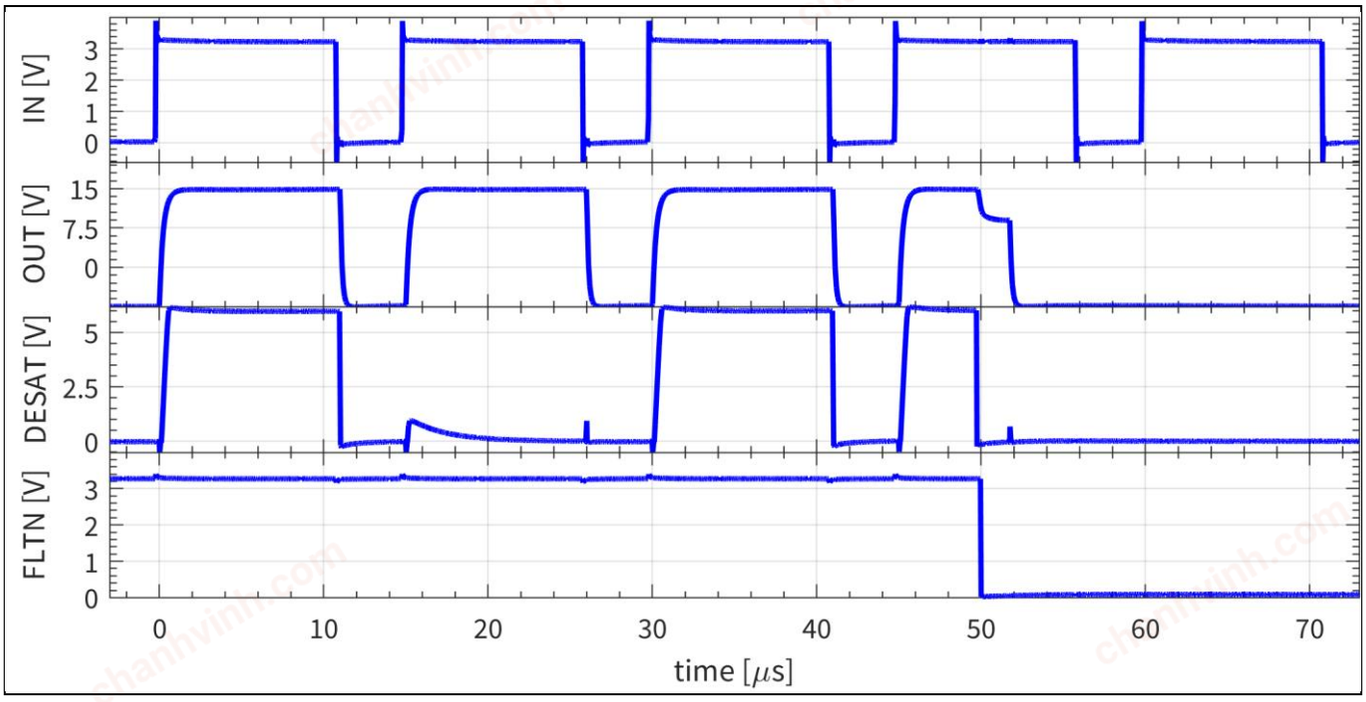


Figure 18 **DESAT2 event counter examples: $V_{DESAT2,th}$ = 4.99 V, LEB = 100 ns, t_{DESAT2} = 3975 ns, DESAT2 fault-off enabled, D2CNTLIM = 2, D2CNTDEC = 1**

2.3.5 Two-level turn-off configuration

The gate driver output can be configured to have two types of turn-offs during normal operation. One of them is the classic turn-off, while the other is the two-level turn-off (TLTOff).

Figure 19 shows the extensive configuration options for the standard turn-off, mainly related to the TLTOff. The settings allows to adjust the intermediate level of the TLTOff, the slopes of the two transitions and the duration of the intermediate voltage level.

In order to aid the internal control loop of the slopes, the field TLTO_GCH in the register DRVCFG can be adjusted in 4 discrete values depending on the gate charge of the power transistor. Once one of the four ranges of gate charges is chosen, the gains and limits of the gate-signal slope control loop are adjusted. If selected properly, this will decrease the over-/undershoot of the gate voltage when transitioning between the levels of the gate driver. If the ratio between the selected gate-charge range and the power-transistor gate charge is too large, the slope control loop can be too aggressive, and overcompensate. This would result in undershoots of the intermediate voltage. If on the other hand the power-transistor gate charge is much larger than the selected range, the internal gate-voltage control loop could become slow and take longer to settle, and might not be able to povide the desired gate voltage slope.

The intermediate voltage level of the TLTOff, TLTO_V can also be adjusted between 12 V and 4.25 V in 32 discrete values. This allows the turn-off to be tuned for high-current transistors in order to minimize voltage overshoot.

Slopes can be adjusted for both transition ramps, ramp A and rampB. For ramp A, the slope TLTO_RA can have 4 discrete values from 7.5 V/µs to 60 V/µs. For the ramp B slope, TLTO_RB, an extra discrete value, Max, is added, which will try to achieve as high a slope as possible.

Lastly, the duration from the start of the turn-off until the end of the intermediate level, TLTO_T can also be adjusted between 0 µs and 7.75 µs in 32 discrete values, with 0 µs only enabling ramp B.

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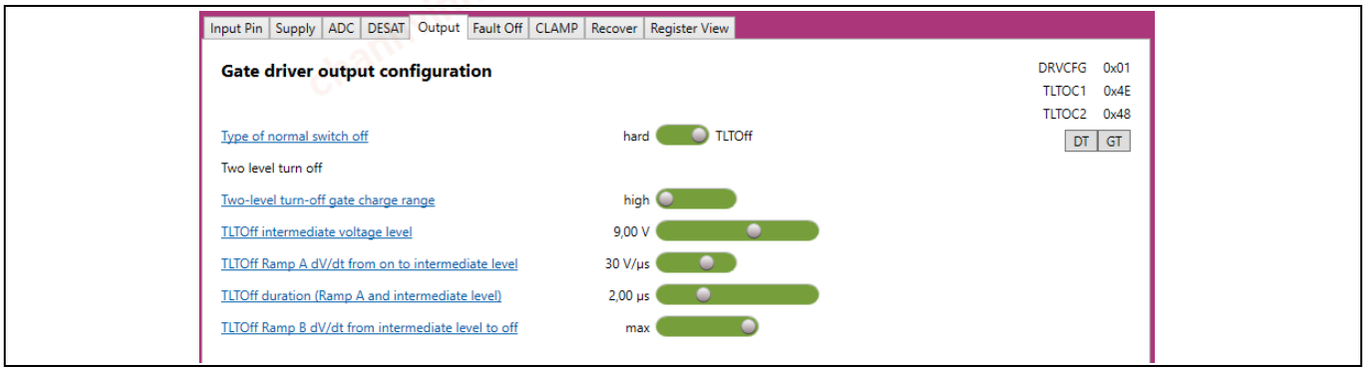


Figure 19 Output settings of the gate driver

In order to show the functionality, twelve measurements have been performed with the parameter variations as detailed in Table 5, and shown in Figure 20. The gate driver was discharging a 10 nF capacitor, emulating a MOSFET gate, through a 10 Ω gate resistor.

For measurement 1 and 2, shown in Figure 20-a, the gate charge range was varied. As the setting “high” is generally designed for larger gate capacitances, the internal control loop generated more aggressive gate voltage swings.

For measurements 2 and 3, shown in Figure 20-b, the intermediate voltage level was adjusted.

In Figure 20-c, the slope of Ramp A was varied. This can limit undershoots during transitions and also ensure that the power transistor is turned off slower, if needed.

In Figure 20-d, the slop of ramp b was changed, giving the same flexibility as in the case of ramp A.

Lastly, in Figure 20-e, the TLTOff duration was adjusted. This provides great flexibility in case of overcurrent switching events, such as short circuit, to hold the gate voltage at the intermediate level for a specific time in order for the current to decrease to a safer value before fully turning off the power transistor.

Table 5 Parameter variation for the measurements

Parameter	Measurement											
	1	2	3	4	5	6	7	8	9	10	11	12
Gate Charge Range	High	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
Intermediate voltage level [V]	7.5	7.5	4.25	12	7.5	7.5	7.5	7.5	7.5	7.5	7.5	7.5
Ramp A [V/µs]	60	60	60	60	7.5	15	60	60	60	60	60	60
TLTOff duration [µs]	3	3	3	3	3	3	3	3	3	1	6	7.75
Ramp B [V/µs]	60	60	60	60	60	60	7.5	15	Max	60	60	60

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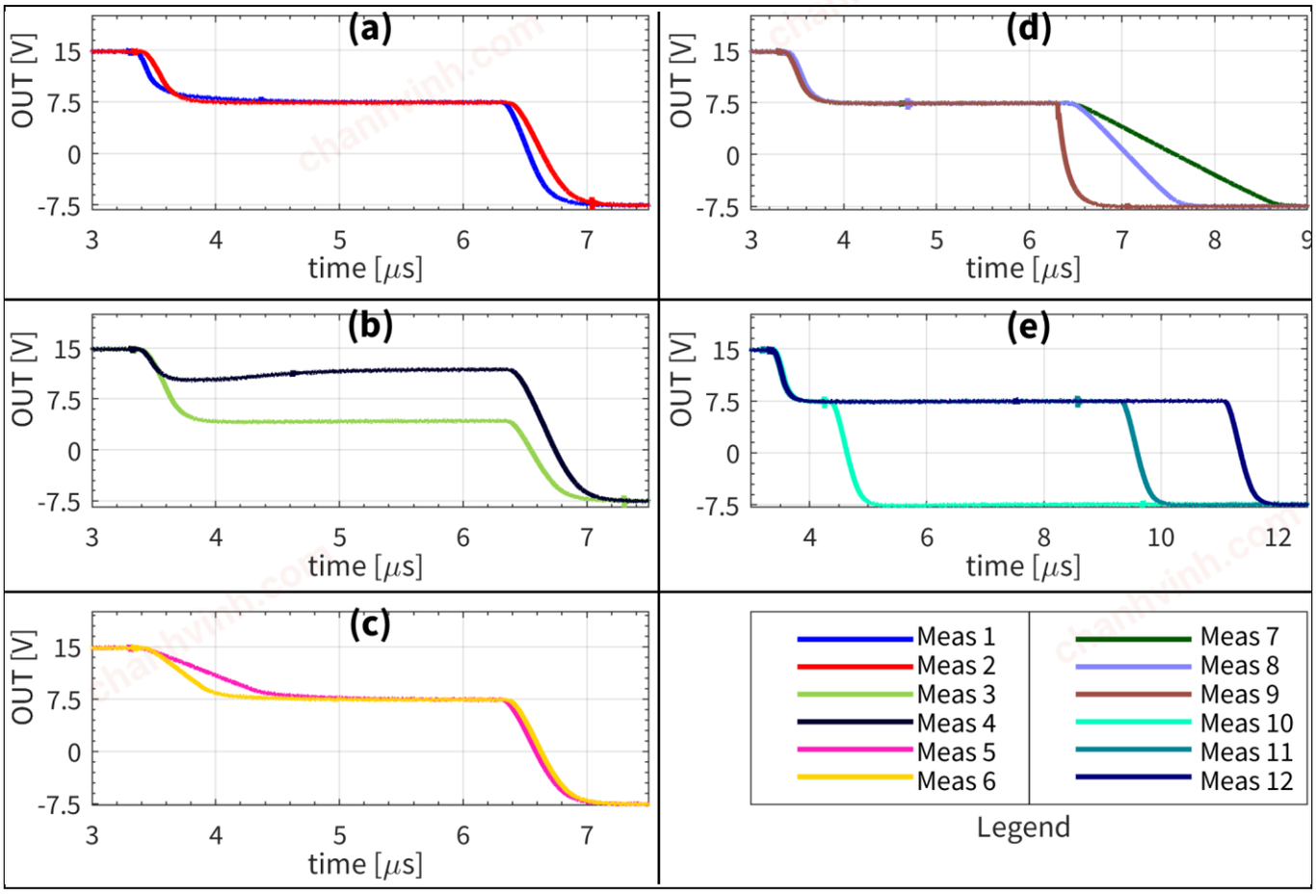


Figure 20 **Two-level turn-off functionality examples: a) charge range variation; b) intermediate voltage level adjustment; c) ramp A adjustment; d) ramp B adjustment; e) intermediate voltage level duration**

2.3.5.1 Pulse-width matching

The gate driver is designed to match the pulse width of the input signal to the output signal. This pulse width matching functionality is also enabled when the two-level turn-off is used for standard turn-off. If the two-level turn-off is enabled as a standard turn-off, the gate drive will introduce a turn-on delay equal to the TLTOff duration, as shown in Figure 21. This will ensure that the gate driver output signal will be equal in length to the PWM input, simplifying the PWM generation in the application.

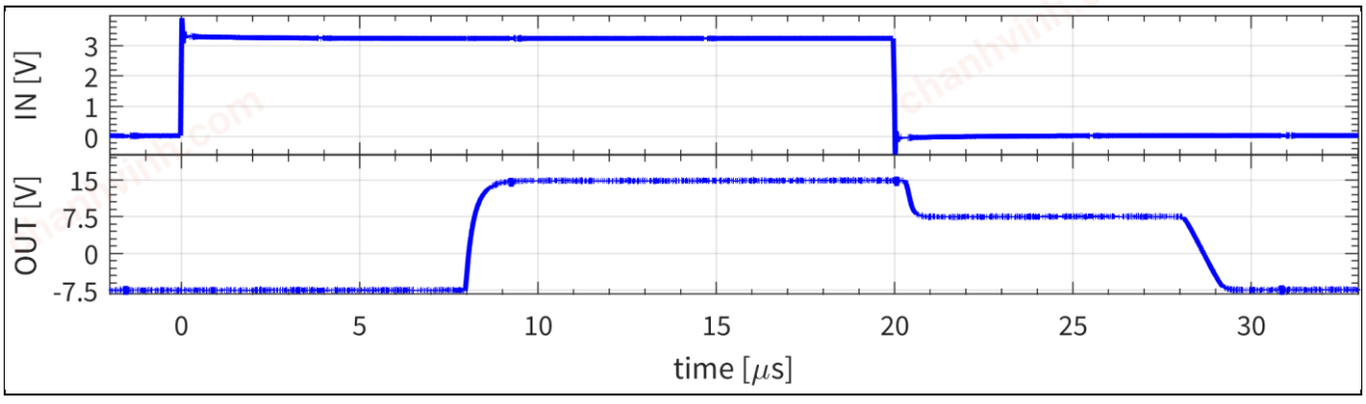


Figure 21 **Pulse-width matching example when TLTOff is used as standard turn-off: TLTO_V = 7.5 V**

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2.3.5.2 Short-pulse behavior

If the standard turn-off is set to TLTOff, the gate driver will ensure that the power transistor is turned on properly by monitoring the gate voltage, and checking that it goes above the intermediate voltage level set for the TLTOff for at least the TLTOff duration time, t_{TLTOFF} plus the CLAMP pin monitoring filter time, $t_{CLAMPfilter,x}$, as will be explained in Chapter 2.3.7.1. If the gate voltage does not rise above the intermediate voltage level for at least the set amount, the TLTOff will be aborted, and the gate driver will turn off with a hard turn-off. If the pulse fulfills both the peak and length requirements, then a TLTOff will be used. The aim of this functionality is to ensure that the power transistor is turned on and off properly, and to avoid situations where, due to short pulses, the transistor will stay in saturation and generate losses without carrying any relevant current.

An example of short-pulse behavior is shown in Figure 22. Here, for the same input pulse, the TLTOff duration time, t_{TLTOFF}, is adjusted between 0.5 µs and 0.75 µs. The TLTOff intermediate voltage is set to 9 V and the $t_{CLAMPfilter,x}$ is adjusted to 370 ns. As observed for the shorter t_{TLTOFF}, the normal TLTOff is used when the gate voltage rises above 9 V for a sufficient period of time. In the case of the t_{TLTOFF} = 0.75 µs, a hard turn-off is triggered, as the pulse has not risen above the intermediate value for a long enough time.

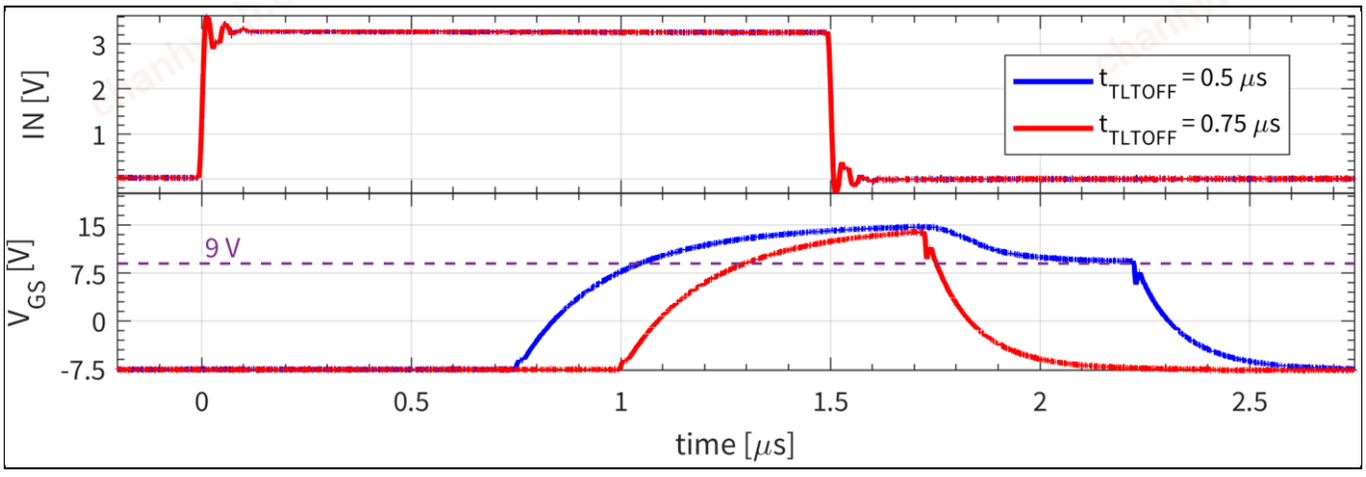


Figure 22 Two-level turn-off short on-pulse behavior; intermediate TLTOff voltage = 9 V, $t_{CLAMPfilter,x}$ = 370 ns

2.3.6 Fault-off configuration

The gate driver has a complex fault-off configuration, as shown in Figure 23. In case a fault event is triggered, e.g. a DESAT event, the gate driver will initiate a fault-off turn-off. Three types of turn-off can be assigned to this: a hard switch-off, which is the standard turn-off; TLTOff, which was explained in Chapter 2.3.5; and a soft turn-off, which will be explained below.

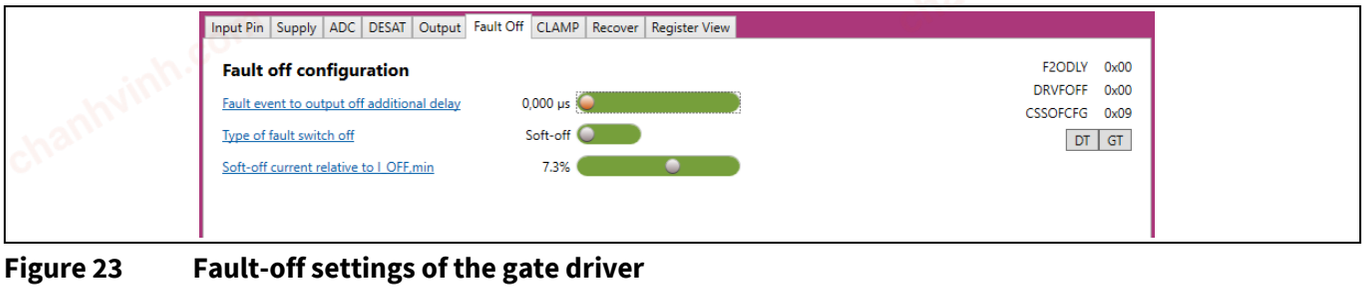


Figure 23 Fault-off settings of the gate driver

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Beside this, a delay from fault event to the start of the turn-off, t_{FAULTn}, can be added. This is aimed to support topologies which require additional delays for individual switch positions. The delay can be adjusted in 32 discrete values from 0 µs up to 7.763 µs. Some examples of this are shown in Figure 24. Here a DESAT1 was triggered. All the measurements were performed with the same DESAT1 settings and only t_{FAULTn} was varied with a 10 nF capacitor acting as the load. The DESAT1 settings are as following: $V_{DESAT1,th}$ = 9.18 V, LEB = 100 ns, t_{DESAT1} = 2375 ns, the fault switch-off type was set to soft-off with I_{OFF} = 0.7 %.

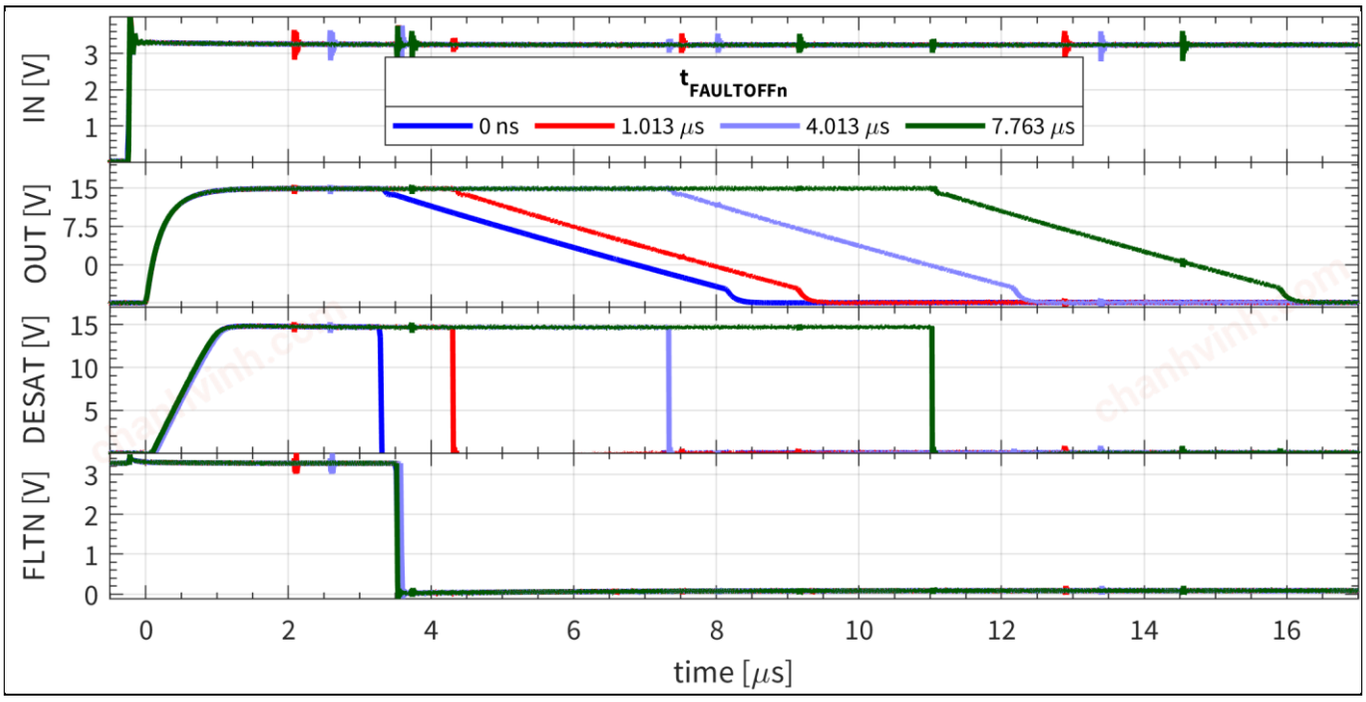


Figure 24 Examples of $t_{FAULTOFFn}$ settings: DESAT settings: $V_{DESAT1,th}$ = 9.18 V, LEB = 100 ns, t_{DESAT1} = 2375 ns, soft-off fault-off, I_{OFF} = 0.7%.

2.3.6.1 Soft-off configuration

During a fault turn-off, such as short circuit, the soft-off function allows the gate driver to slowly turn-off the power transistor using a constant current source. This ensures that the power transistor will gradually reduce the excess current flow to prevent voltage overshoots due to inductance in the current path that could cause an overvoltage failure of the power transistor.

The soft-off turn-off current can be adjusted in 16 discrete values from 0.7% up to 11.7% of the gate driver sink current capability. Figure 25 shows a few examples of the I_{OFF} functionality. Here a DESAT1 was triggered. All the measurements were performed with the same DESAT1 settings, and only t_{FAULTn} was varied with a 10 nF capacitor acting as the load. The DESAT1 settings are as follows: $V_{DESAT1,th}$ = 9.18 V, LEB = 100 ns, t_{DESAT1} = 2375 ns, and the fault switch-off type was set to soft-off with $t_{FAULTOFFn}$ = 0 ns.

The soft-off function will timeout in 2.4 µs, and in case the voltage does not reach *VEE* + 2 V, all sink-capable pins will be turned on to discharge the gate of the power transistor. This should be taken into consideration when selecting the soft-off current. An extra time-out filter, switch-off timeout time, can be used to extend this period, as shown in the CLAMP configuration, Chapter 2.3.7.2.

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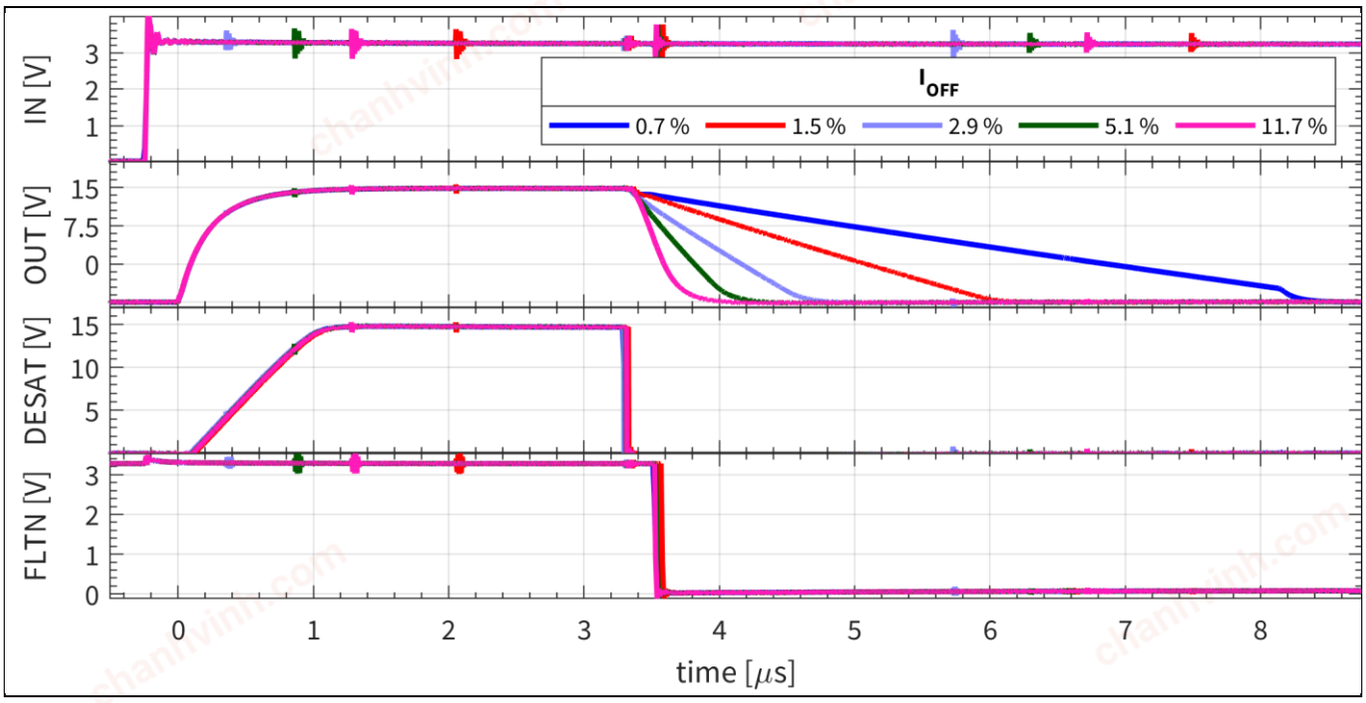


Figure 25 **Examples of I_{OFF} settings: DESAT settings: $V_{DESAT1,th}$ = 9.18 V, LEB = 100 ns, t_{DESAT1} = 2375 ns, soft-off fault-off, $t_{FAULTOFFn}$ = 0 ns.**

A very useful application for this soft-off function is to ensure similar turn-off for different power transistors. Figure 26 shows the soft-off turn-off for two different capacitive loads, C_{load1} = 22 nF and C_{load2} = 47 nF, associated with two different power transistor gate capacitances. The soft turn-off is performed using the same gate resistor. By selecting two different current percentages values in the soft-off function, the threshold voltage of both switches can be reached in the same time. This allows a similar behavior of the circuit, despite different power switches being used. In this case the typical threshold voltage range is reached for both loads at the same time. Thus, by simply adjusting the gate driver settings, different power switches can be used in similar applications while maintaining similar operational behavior.

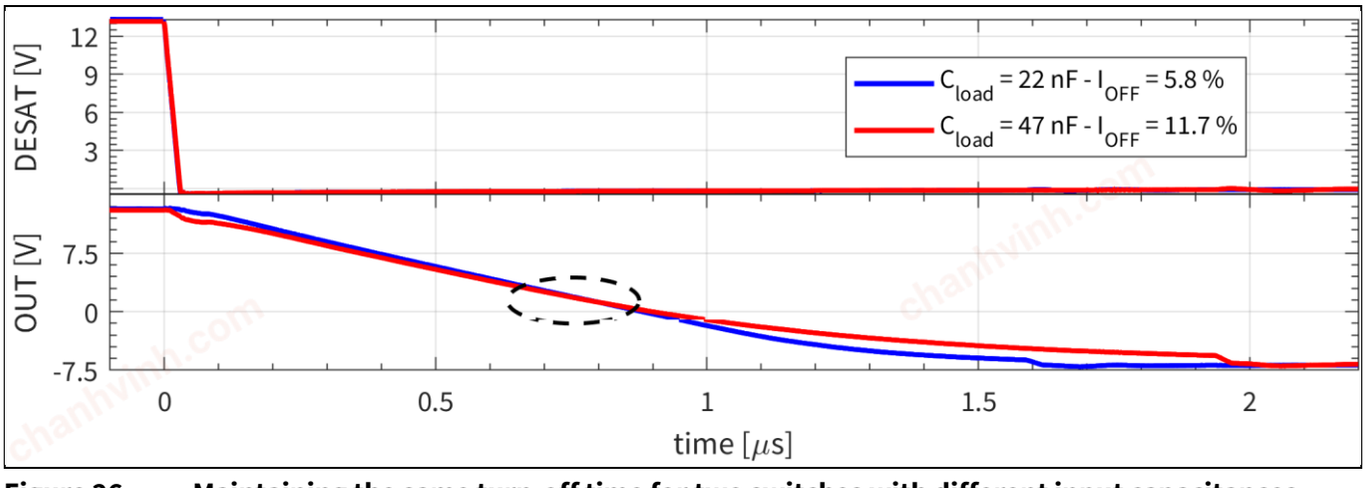


Figure 26 **Maintaining the same turn-off time for two switches with different input capacitances**

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2.3.7 CLAMP configuration

The gate driver comes with a large range of options for the clamp function, as shown in Figure 27. First, the clamp functionality can be turned on or off. As explained in Chapter 2.3.3, the CLAMP pin can be used as an ADC input if desired. However, the clamping functionality has to be turned off for this to be usable, so as to not influence the measurement.

If the CLAMP pin is enabled for gate clamping, there are two different options, an internal or a clamp pre-driver. If internal is chosen, an internal transistor is used for the clamping function, e.g. to clamp the gate of an IGBT during fast switching events in order to avoid parasitic pull-up through the Miller capacitance.

In cases where there is a long distance between the power transistors to the gate driver, such as for power modules, a clamp transistor can be used, and placed close to the gate and source kelvin pins. In this case the gate driver can be configured as a clamp pre-driver, providing the correct signals to drive an external clamp transistor.
The evaluation board is designed to allow the evaluation of all possible functionalities attached to the CLAMP pin: clamp, clamp pre-driver, and ADC measurement with minimal effort. The hardware changes required to adjust the CLAMP pin as a clamp, clamp driver and ADC for NTC or DC-link measurements are shown in Chapter 2.5. By default, the board comes configured with the CLAMP pin as a clamp pre-driver.

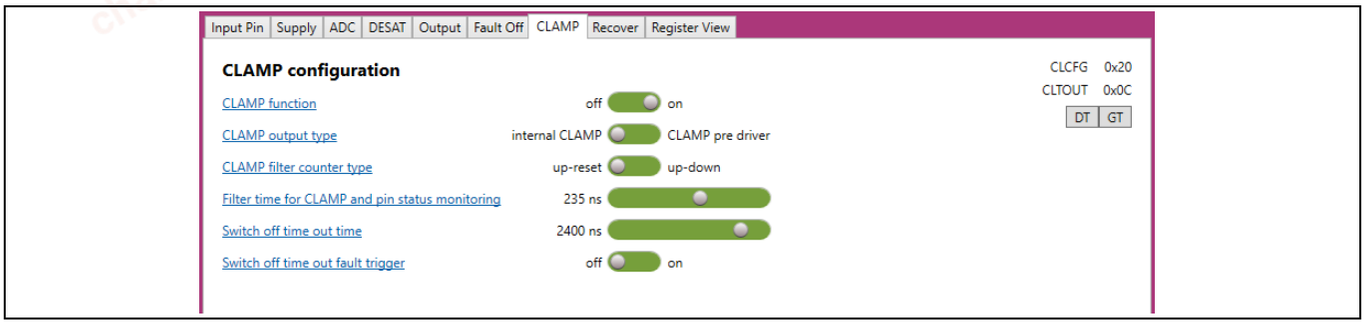


Figure 27 CLAMP configuration of the gate driver

2.3.7.1 Filter time for CLAMP and pin-status monitoring

The filter time for CLAMP and pin-status monitoring, $t_{CLAMPfilter,x}$, is used to adjust the sensitivity of a pin-status change during operation. This filter time is then added as a delay between the actual value of the pin crossing its threshold and the reaction time of the gate driver. This can provide extra noise immunity in applications, by sampling the signal during this period. In the case of the clamp function, after the gate voltage of the power transistor passes the threshold, VEE + 2 V, an additional time, equal to $t_{CLAMPfilter,x}$, will need to elapse before the CLAMP function is activated.

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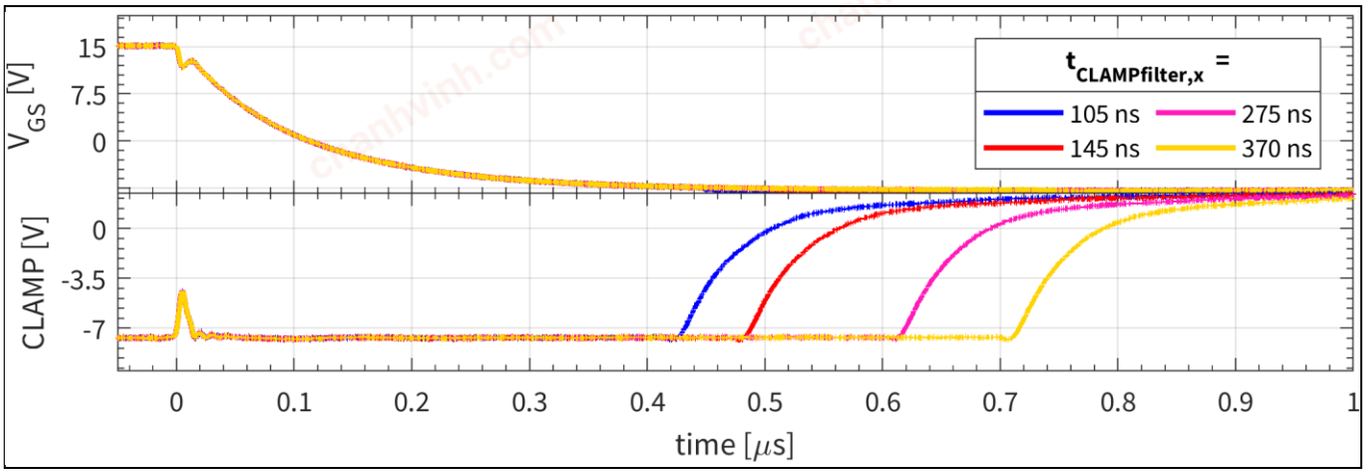


Figure 28 Examples of filter time for CLAMP and pin status monitoring influence on the clamp

The same filter time is used also for pin-status monitoring, in which a pin-state change is recorded only after this filter time is reached and the pin voltage has not re-crossed its specific threshold voltage. For example, if TLTOff is selected as standard turn-off, and a short pulse event takes place, as described in Chapter 2.3.5.2, the gate voltage is recorded only after the extra $t_{CLAMPfilter,x}$ filter time has elapsed. An example of this is shown in Figure 29, where for the same TLTOff settings, t_{TLTOFF} = 0.5 µs, V_{TLTOFF} = 9 V, the input pulse can be recorded as too short, depending on the $t_{CLAMPfilter,x}$ value.

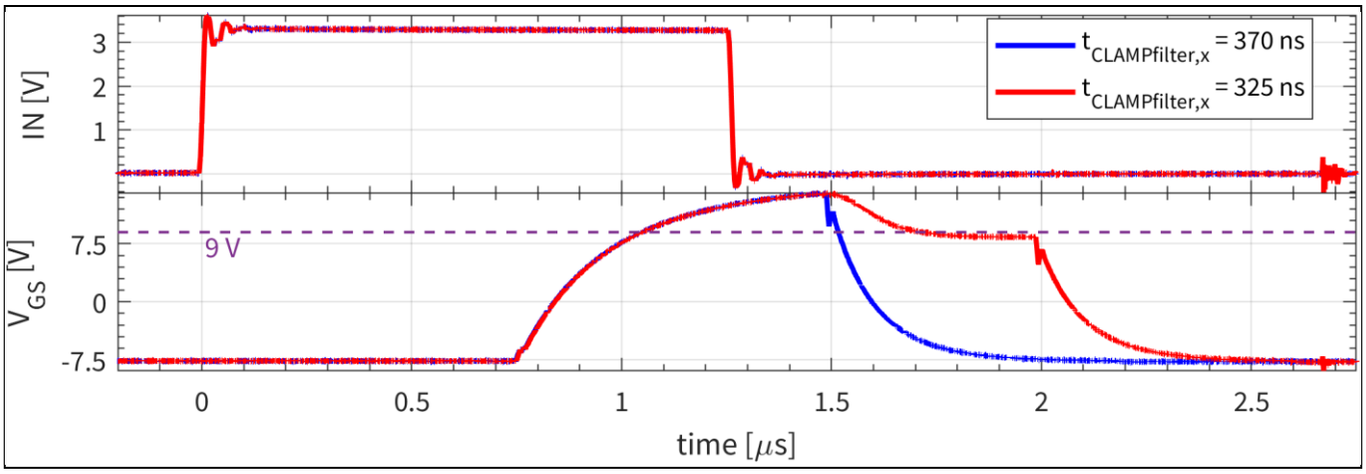


Figure 29 Impact of filter time for CLAMP and pin-status monitoring on the short on-pulse behavior during normal TLTOff usage; intermediate TLTOff voltage = 9 V, t_{TLTOFF} = 0.5 µs

2.3.7.2 Switch-off timeout time

The adjustable switch-off timeout time t_{SOTOUT} is an extra adjustable filter time that can be inserted in the turn-off procedure in order to adjust the turn-off behavior of the gate driver. This has a three-bit value and can be selected from eight discrete time values. Each of the three turn-off options of the gate driver can have a different total turn-off time, as below:

- Soft-off: After the typical 2.4 µs soft-off timeout, the adjustable switch-off timeout time t_{SOTOUT} is added
- TLTOff: After the adjustable TLTOff time, the adjustable switch-off timeout time t_{SOTOUT} is added
- Hard switch-off: Only the adjustable switch-off timeout time t_{SOTOUT} is applied

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Figure 30 shows the adjustable switch-off timeout time t_{SOTOUT} used with a soft-off function turn-off. The value of the time was varied in order to show its impact on the turn-off behavior. For this measurement, the gate capacitance was 10 nF and the soft-off current I_{OFF} was set to 0.7%. It can be observed that for the first three measurements, the CLAMP is triggered before gate voltage is fully discharged.

The switch-off timeout event always sets a register bit on detection. Optionally, a fault event can also be triggered from the switch-off if desired.

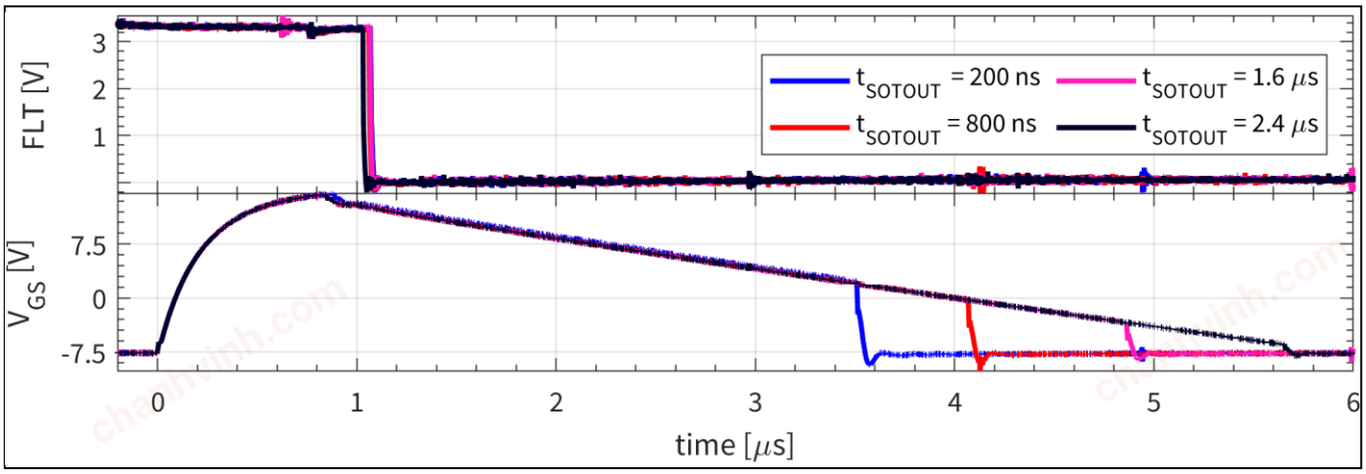


Figure 30 Settings of the adjustable switch-off timeout time, t_{SOTOUT}; I_{OFF} = 0.7%, C_{load} = 10 nF

2.3.8 Recovery modes configuration

The gate driver IC is equipped with an advanced configuration-restore function for the input and output side in case of configuration reset, such as in UVLO events. This is shown in Figure 31. If enabled, the output side configuration is restored from the input side, once the output side supply is above its UVLO settings. Similarly, if enabled, the input-side configuration will be recovered from the output side, once the input-side supply voltage is above its UVLO settings. If any of the two options is disabled, that specific side will be reset in case of UVLO events, and will need to be reconfigured before operation can be resumed.

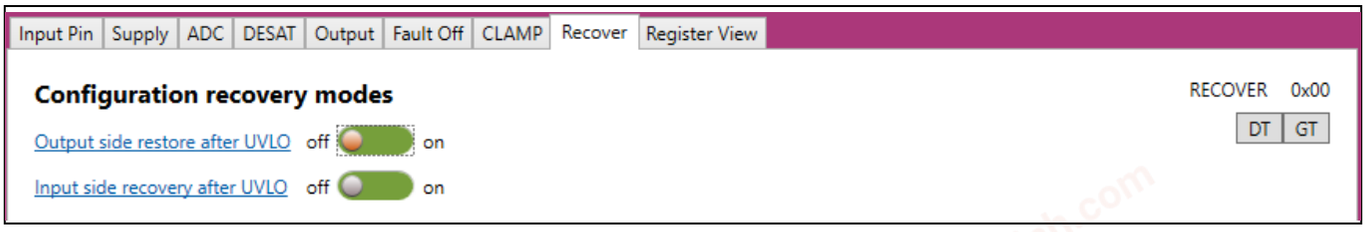


Figure 31 Recovery configuration of the gate driver

2.4 Switching investigation

As mentioned earlier, the hardware mode comes with a simple PWM generator for evaluation of the Eval-1ED3890Mx12M evaluation board.

By default, the PWM pattern generator will start in the OFF state, as show in Figure 32. In case a fault event is registered, the software will switch from any other mode back to the OFF state.

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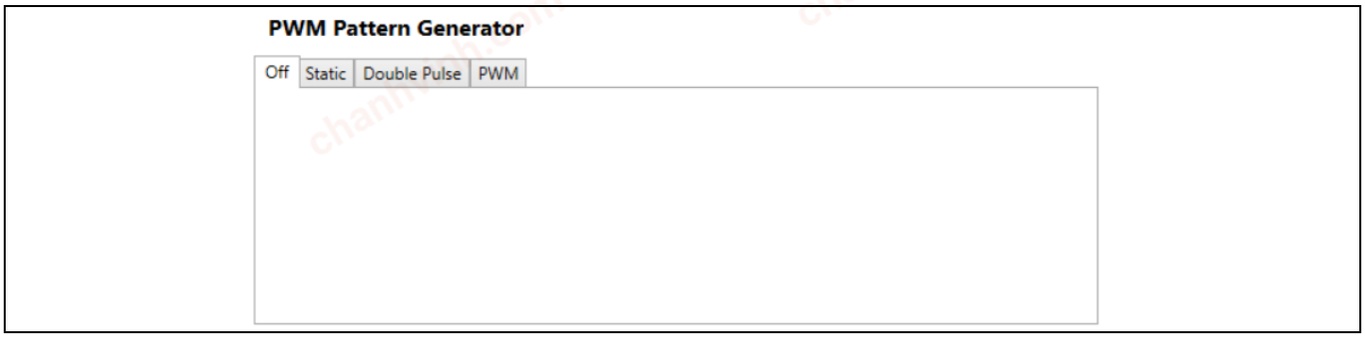


Figure 32 OFF (default) mode of PWM Pattern Generator

If a static high for the low-side gate driver or for the high-side gate driver needs to be generated, the static option can be used, as shown in Figure 33. By clicking on any of the two buttons the state of the low/high-side can be changed, with red showing the output being off (LOW) and green being ON (HIGH).

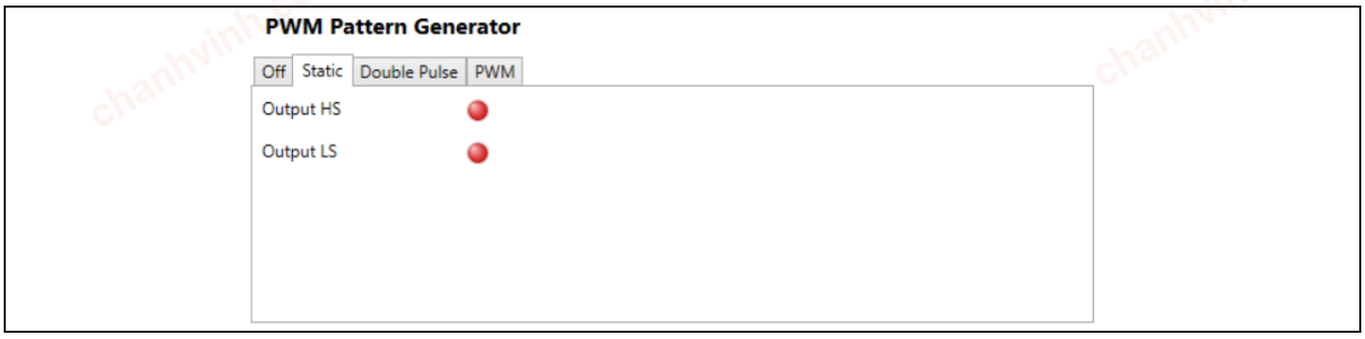


Figure 33 Static mode of PWM pattern generator

If the evaluation board is to be used as part of a double-pulse test setup, the double-pulse mode can be used as shown in Figure 34. The generator allows switching between the low-side and high-side testing. By use of sliders, the charging pulse, A, the diode free-wheeling time between pulse A and B, and length of second pulse, B, can be adjusted. Afterwards, the trigger button can be used to trigger a double-pulse pattern.

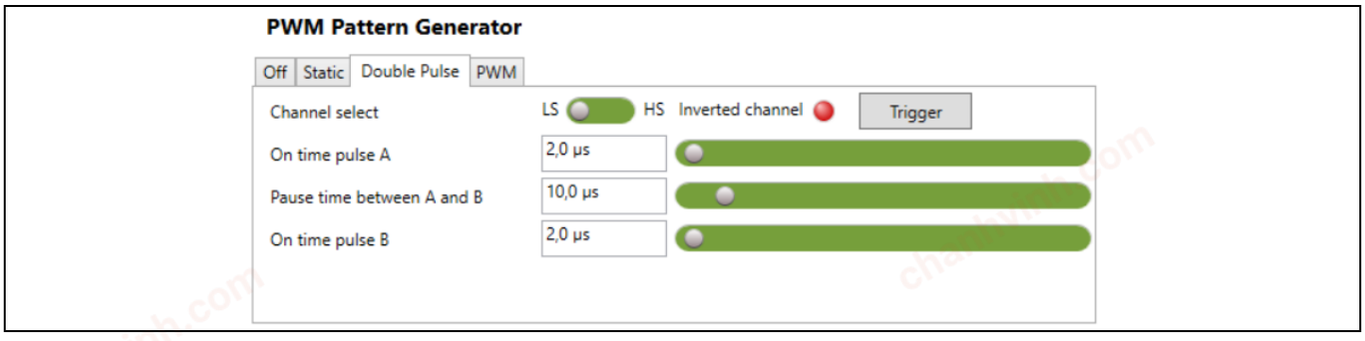


Figure 34 Double-pulse test mode of PWM pattern generator

Lastly, the PWM mode can be used to generate a PWM pattern. Here the switching frequency, duty cycle, and dead-time between low and high-sides can be adjusted using the sliders, as shown in Figure 35. The PWM generator can be turned on and off using the RUN/STOP button.

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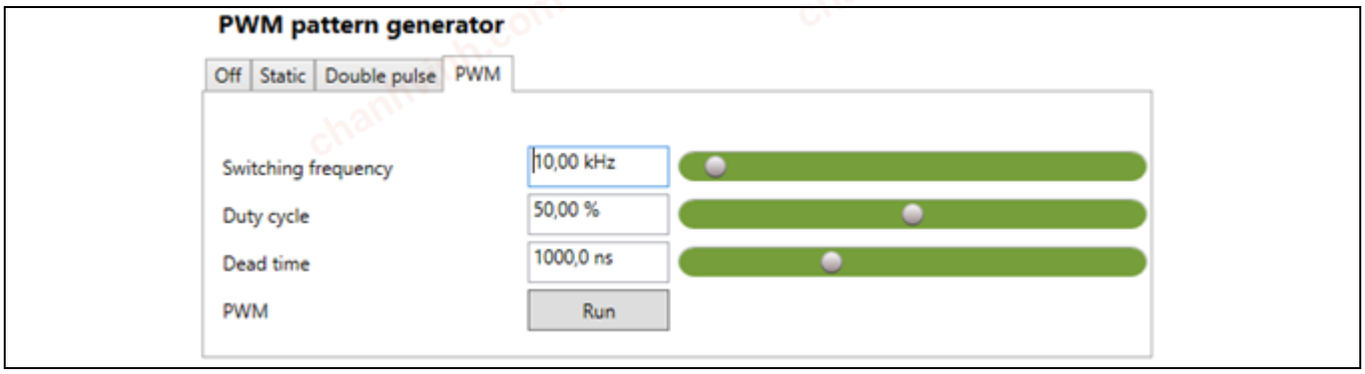


Figure 35 PWM mode of PWM pattern generator

2.5 Hardware adjustment of clamp pin

As mentioned earlier, the evaluation board offers the possibility to evaluate all the CLAMP pin functions. For this, a small hardware modification has to be made, depending on the desired function, as shown in this chapter. By default, the board comes configured for use with the CLAMP pin as a clamp pre-driver, with an external clamp transistor.

For the high-side gate driver, the adjustment is done via R52, R53 and R56, marked in Figure 36. In Figure 37, a detail of the top-side layout is shown with R52 and R53 marked in red. R56 is placed on the bottom side of the PCB.

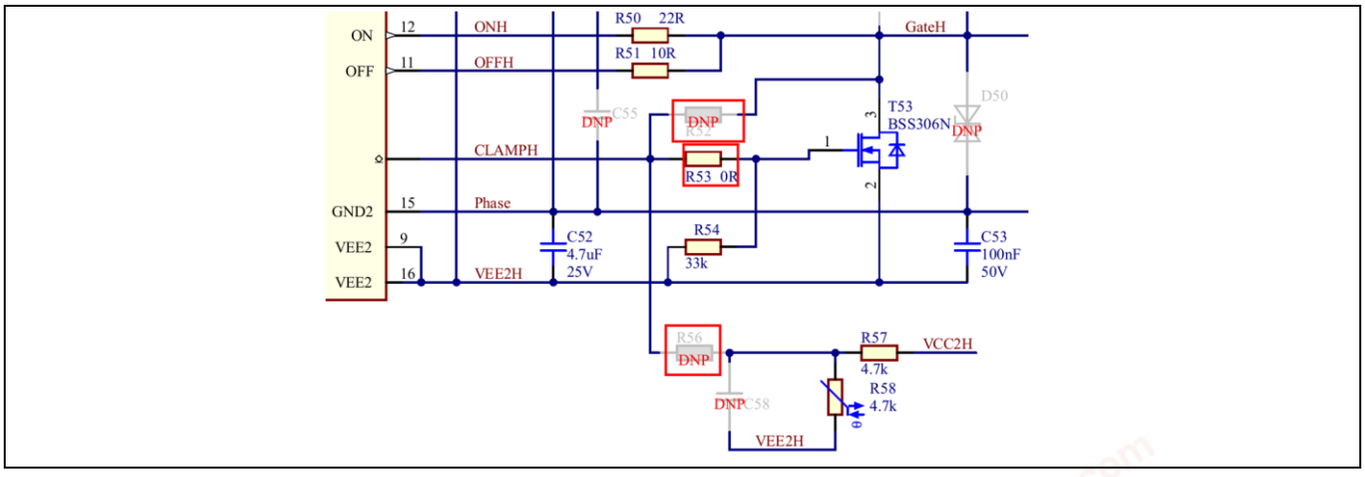


Figure 36 Schematic detail of CLAMP pin hardware configuration for the high-side gate driver

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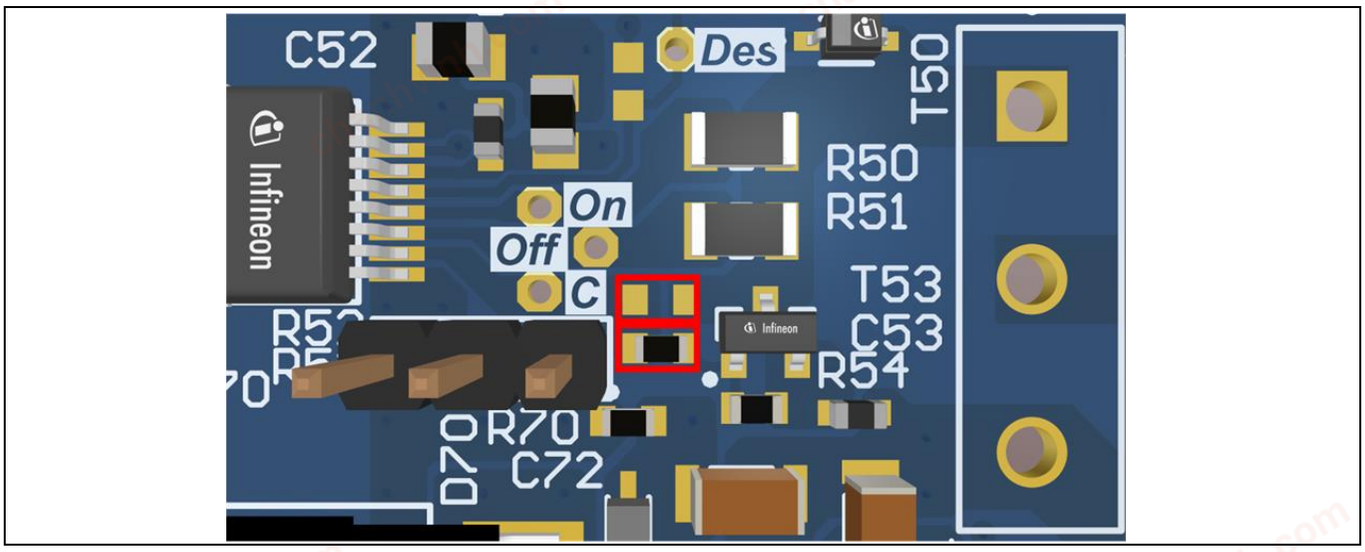


Figure 37 Top-side layout detail with CLAMP configuration resistors marked for high-side gate driver

For the low-side gate driver, the adjustment is done via R62, R63 and R95, marked in Figure 38. These are also shown in the detail of the top PCB layout in Figure 39, with all three resistors marked in red.

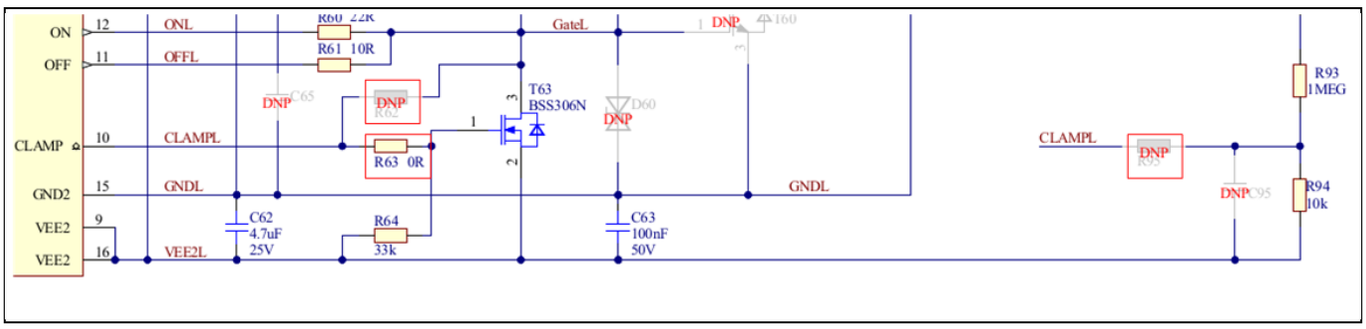


Figure 38 Schematic detail of CLAMP pin hardware configuration for the low-side gate driver

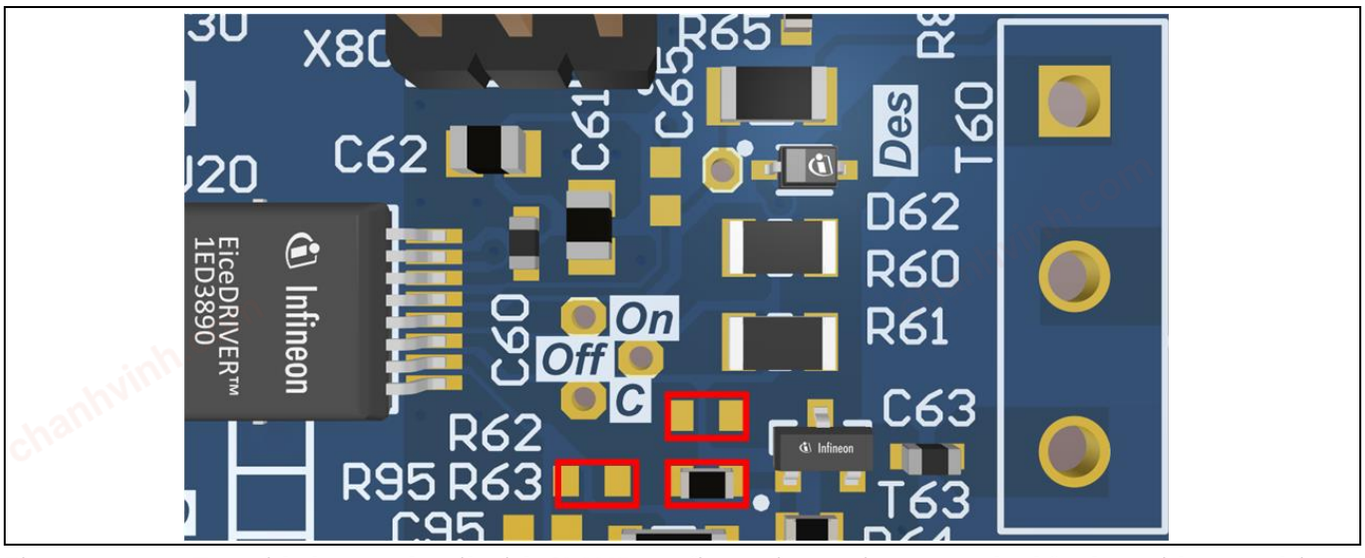


Figure 39 Top-side layout detail with CLAMP configuration resistors marked for low-side gate driver

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2.5.1 Clamp-driver configuration

By default, the board comes pre-configured for use with the CLAMP pin function as a clamp transistor driver, having resistors R53 and R63 populated with a 0 Ω resistor for the high-side and low-side, repectively. R52, R62, R56 and R95 must be left unpopulated.

2.6 Clamp configuration

If the clamp function is to be evaluated, the board requires minimal modification. For the high-side gate driver, the 0 Ω resistor from R53 has to be desoldered, and moved to R52. For the low-side, similarly, the 0 Ω resistor should be moved from R63 to R62.

2.7 ADC input configuration

If the ADC function is to be evaluated, the 0 Ω should be moved to a new position. For the high-side gate driver, the 0 Ω resistor should be moved to R56. In order to improve noise immunity, C58 can be populated. For the low-side, similarly, the 0 Ω resistor should be moved to R95. To improve noise immunity for the DC-link measurement, capacitor C95 can be used in combination with a higer resistor value to create an RC filter.

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3 System design

The Eval-1ED3890Mx12M evaluation board is designed to evaluate the Infineon EiceDRIVER™ 1ED-X3 Digital gate driver IC family. To support the customer in getting started with the design, the schematics, Gerber data and Altium project files can be found on the Infineon homepage.

3.1 Schematics

The schematics of the evaluation board are separated into the following parts:

- Gate driver ICs with surrounding circuit
- Power supply section for primary and secondary sides
- Status interface LEDs
- Interface with connectors

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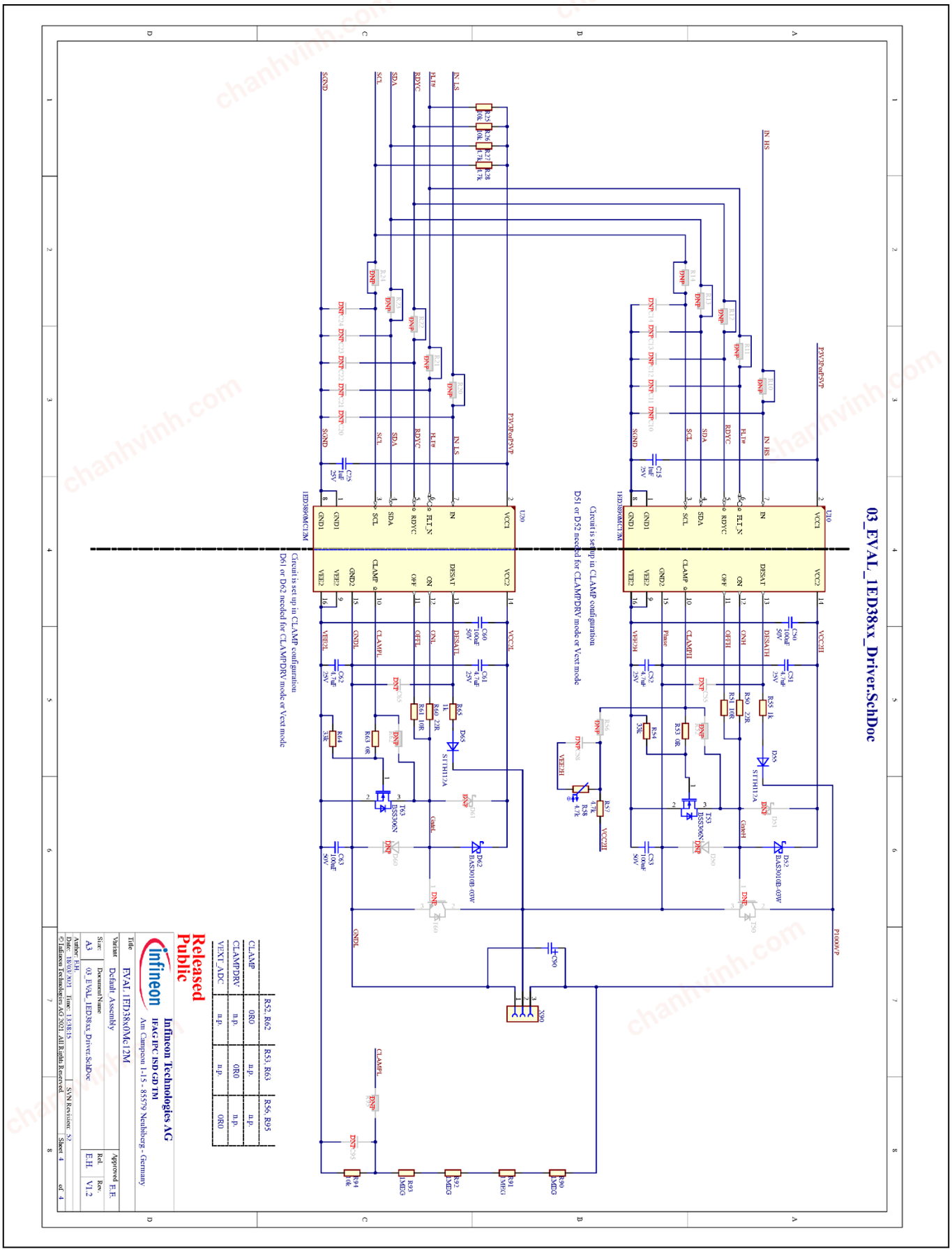


Figure 40 Schematic of gate driver ICs and surrounding circuit

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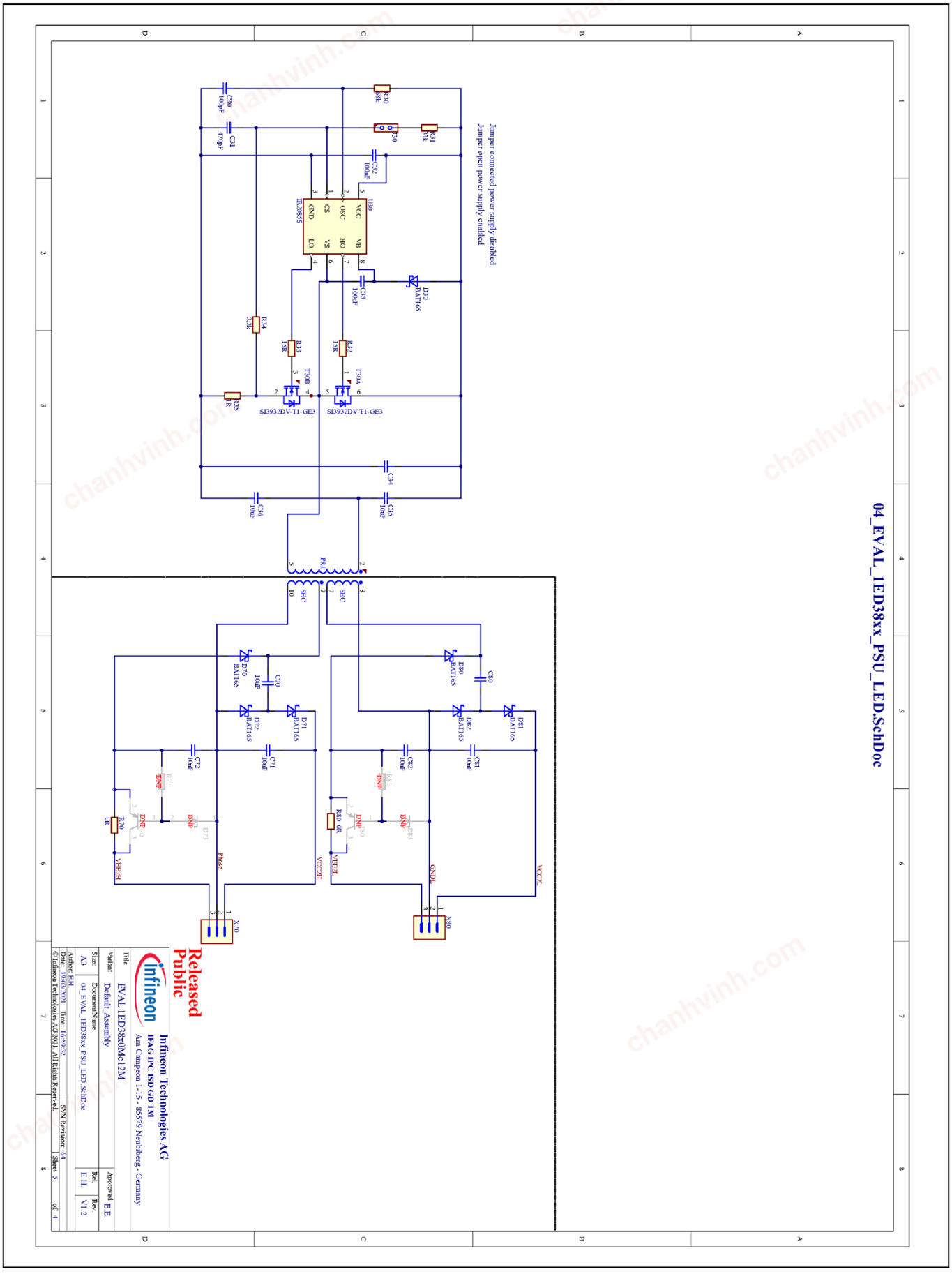


Figure 41 Schematic of power supply and voltage regulators

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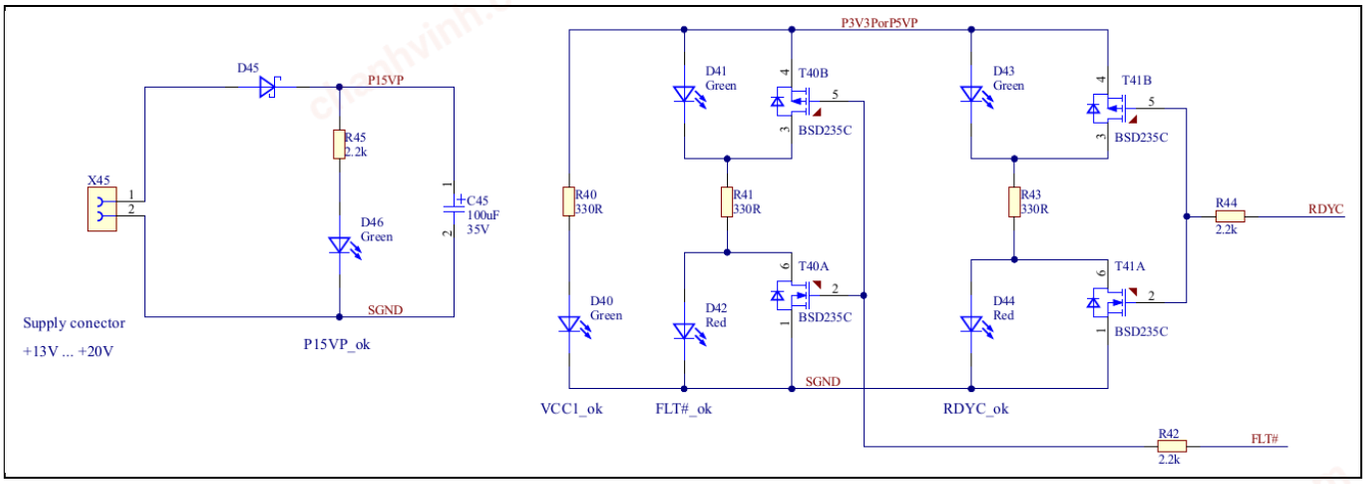


Figure 42 Schematic of status LEDs

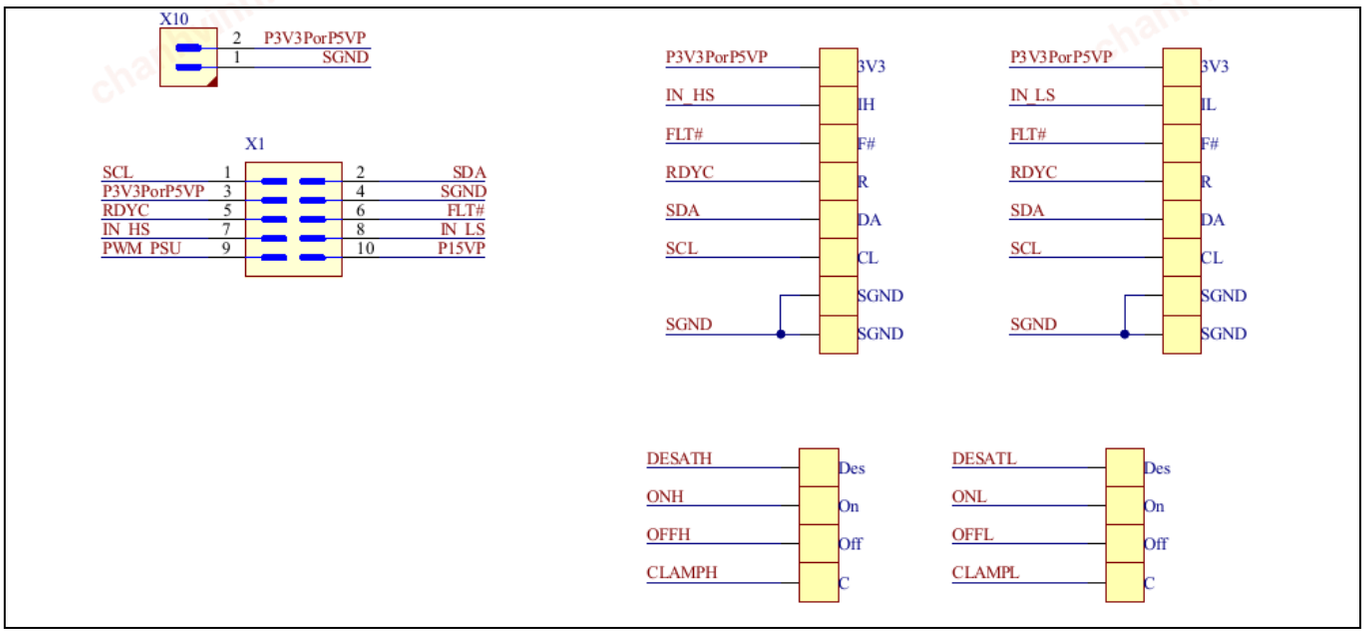


Figure 43 Schematic of input connectors and test points

3.2 Layout

The layout from this basic schematic is intended as a starting point for developing more complex application circuits. The evaluation board has a four-layer PCB. For orientation, only the assembly diagram and the top and bottom layer are shown.

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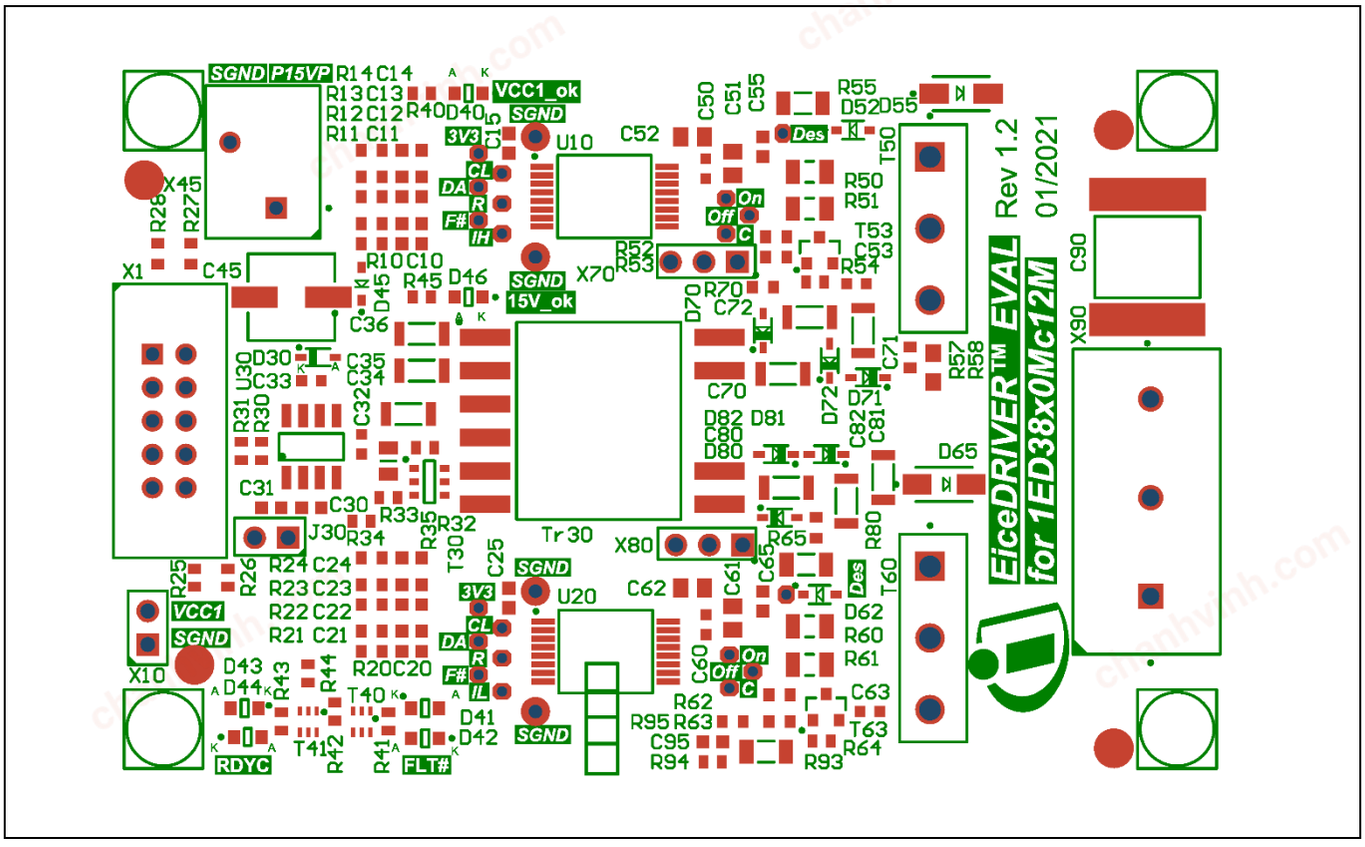


Figure 44 Assembly drawing top side

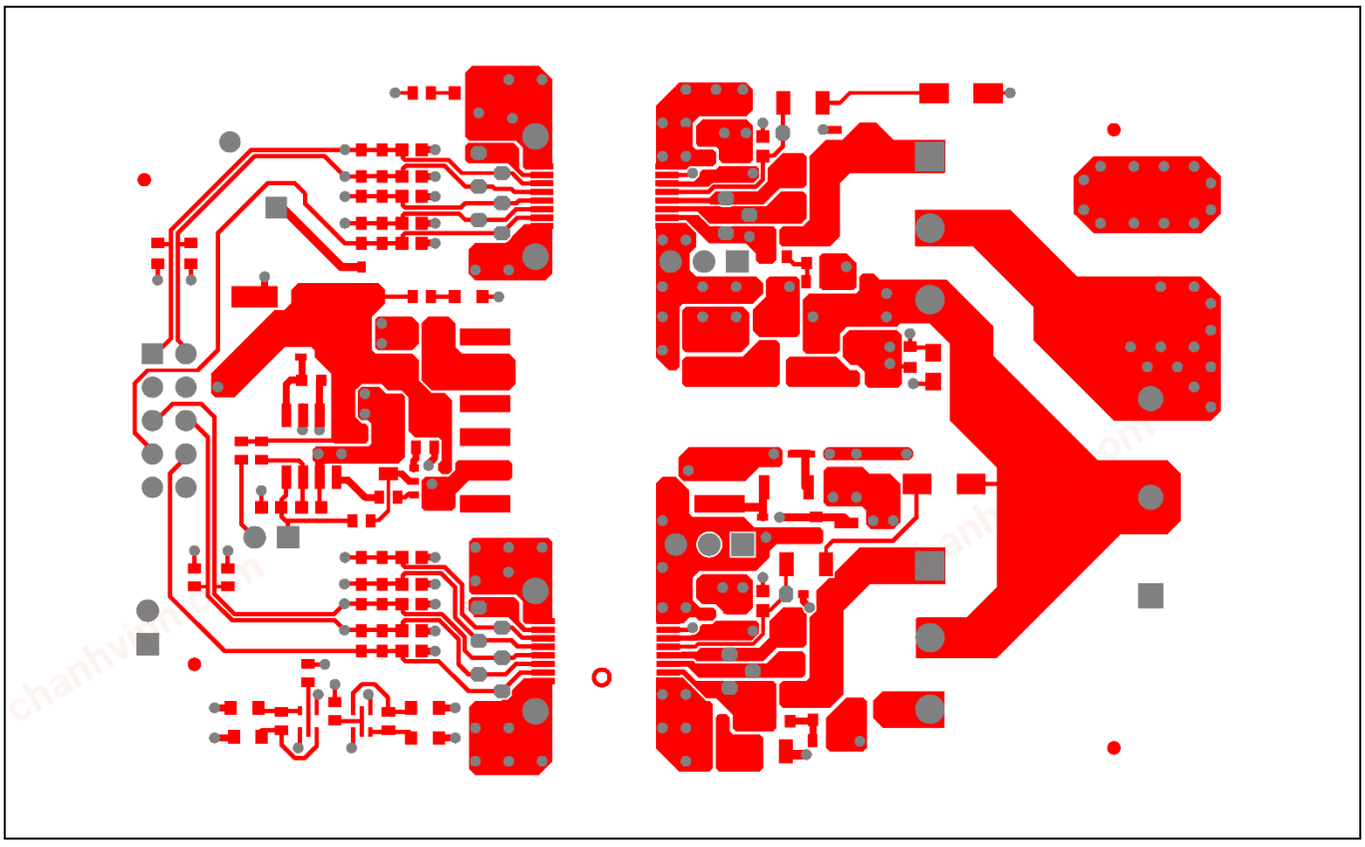


Figure 45 PCB top layer

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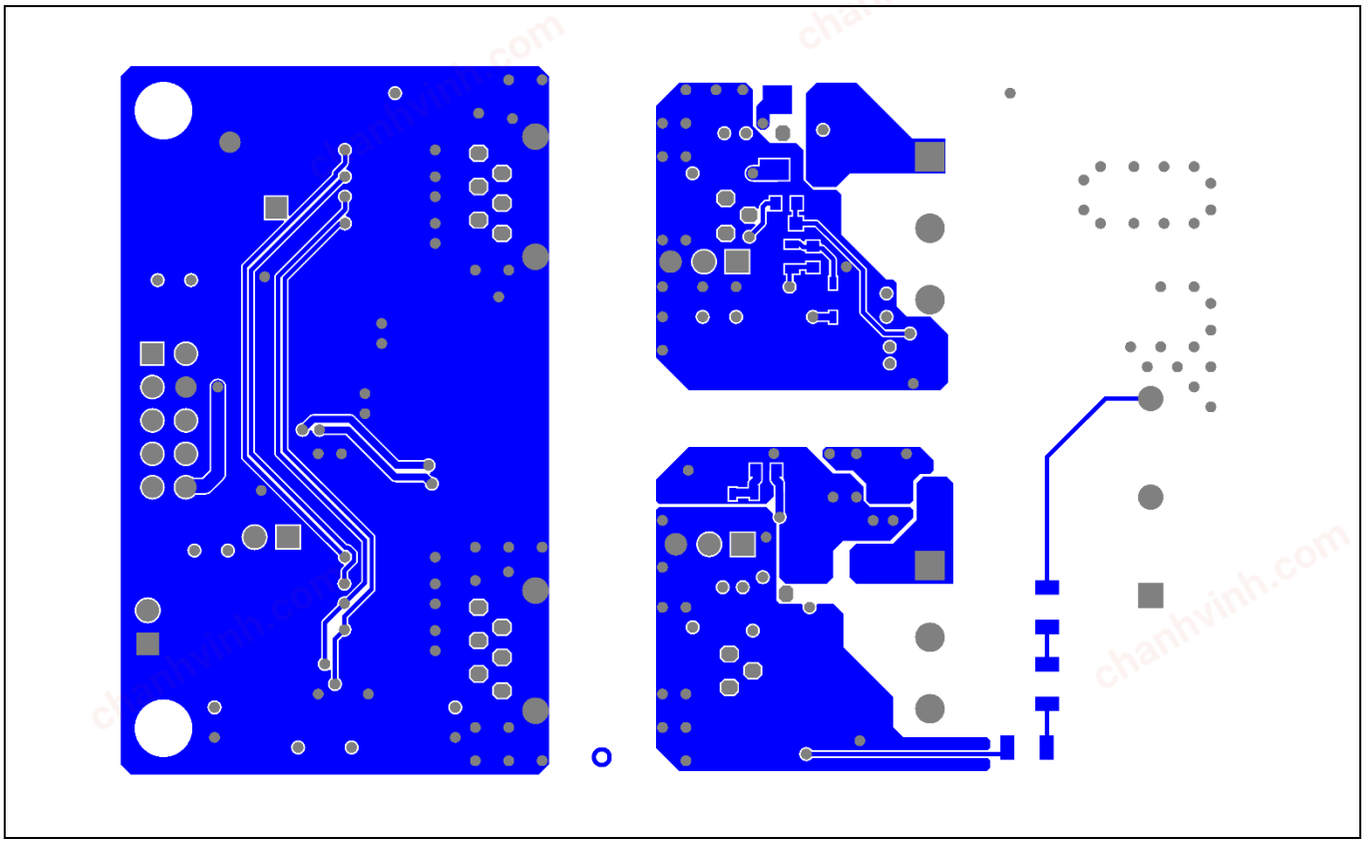


Figure 46 PCB bottom layer

3.3 Bill of material

The complete bill of material is available on the download section of the Infineon homepage. A log-in is required to download this material.

Table 6 Bill of materials

Designator	Quantity	Description	Manufacturer	Manufacturer P/N
C34, C35, C36, C70, C71, C72, C80, C81, C82	9	10uF	Wurth Elektronik	885012208069
C45	1	100uF	Wurth Elektronik	865080545012
C51, C52, C61, C62	4	4.7uF	Wurth Elektronik	885012107018
C90	1	250nF	TDK Corporation	B58031I9254M062
D30, D70, D71, D72, D80, D81, D82	7	BAT165	Infineon Technologies	BAT165
D40, D41, D43, D46	4	Green	Wurth Elektronik	150080VS75000
D42, D44	2	Red	Wurth Elektronik	150080RS75000
D45, D52, D62	3	BAS3010B-03W	Infineon Technologies	BAS3010B-03W
D55, D65	2	STTH112A	STMicroelectronics	STTH112A
J30	1	61300211121	Wurth Elektronik	61300211121
MP1, MP2, MP3, MP4	4	970150365	Wurth Elektronik	970150365
MP5, MP6, MP7, MP8	4	97790503211	Wurth Elektronik	97790503211
R25, R26, R94	3	10k	Vishay	CRCW060310K0FK
R27, R28, R57	3	4.7k	Yageo	RC0603FR-074K7L
R30	1	68k	Vishay	CRCW060368K0FK
R31, R54, R64	3	33k	Vishay	CRCW060333K0FK
R32, R33	2	15R	Vishay	CRCW060315R0FK
R34, R42, R44, R45	4	2.2k	Vishay	CRCW06032K20FK

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Designator	Quantity	Description	Manufacturer	Manufacturer P/N
R35	1	1R	Vishay	CRCW08051R00FK
R40, R41, R43	3	330R	Vishay	CRCW0603330RFK
R50, R60	2	22R	Vishay	RCS120622R0FKEA
R51, R61	2	10R	Vishay	RCS120610R0FKEA
R53, R63, R70, R80	4	0R	Yageo	RC0603JR-070RL
R55, R65	2	1k	Vishay	CRCW12061K00FK
R58	1	4.7k	TDK Corporation	B57401V2472J062
R90, R91, R92, R93	4	1MEG	Vishay	CRCW12061M00FK
T30	1	SI3932DV-T1-GE3	Vishay	SI3932DV-T1-GE3
T40, T41	2	BSD235C	Infineon Technologies	BSD235C
T53, T63	2	BSS306N	Infineon Technologies	BSS306N
Tr30	1	750317493 or 750318016	Wurth Elektronik	750317493 or 750318016
U10, U20	2	1ED3890MC12M	Infineon Technologies	1ED3890MC12M
U30	1	IR2085S	Infineon Technologies	IR2085S
X1	1	T821110A1S100CEU	Amphenol	T821110A1S100CEU
X10	1	61300211121	Wurth Elektronik	61300211121
X45	1	1985195	Phoenix Contact	1985195
X70, X80	2	61300311121	Wurth Elektronik	61300311121
X90	1	1731035	Phoenix Contact	1731035

3.4 Connector details

General information about the connectors of the Eval-1ED3890Mx12M evaluation board is provided in this section.

Table 7 shows the connection of the high-voltage connector X90.

Table 7 High-voltage connector

PIN	Label	Function
X90 (1)	P1000VP	DC-link high-side connection
X90 (2)	PHASE	Half-bridge midpoint connection
X90 (3)	GNDL	DC-link ground side connection

Table 8 shows the connections of the primary side connectors. This includes all 3 connectors, X45, X1 and X10.

Table 8 Input side connectors pinout

PIN	Label	Function
X45 (1)	SGND	Ground for primary side
X45 (2)	P15VP	Supply voltage for the isolated power supply
X1 (1)	SCL	I^2C clock line
X1 (2)	SDA	I^2C data line
X1 (3)	P3VP	Supply voltage for gate driver ICs primary side supply (shorted to VCC1)
X1 (4)	SGND	Ground for primary side
X1 (5)	RDYC	Connection to both RDYC pins of the gate driver ICs
X1 (6)	FLT#	Connection to both FLT# pins of the gate driver ICs

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X1 (7)	res.	Not used
X1 (8)	P15VP	Supply voltage for the isolated power supply
X10 (1)	VCC1	Supply voltage for gate driver ICs primary side supply (shorted to P3VP)
X10 (2)	SGND	Ground for primary side

Table 9 shows the connection of the high-voltage connector X70. This is used to supply the high-side gate drive secondary side. If the onboard power supply is not to be used and dissabled, VCC2, GND2, and VEE2 voltage can be supplied here by means of an isolated power supply that allows floating operation of the gate driver as per application.

Table 9 High-side gate driver IC -isolated secondary power supply

PIN	Label	Function
X70 (1)	-	High-side gate driver positive supply (VCC2) connection
X70 (2)	-	High-side gate driver supply ground reference (GND2) connection
X70 (3)	-	High-side gate driver negative supply (VEE2) connection

Error! Reference source not found.shows the connection of the high-voltage connector X70. This is used to supply the high-side gate drive secondary side. If the onboard power supply is not to be used and dissabled, VCC2, GND2, and VEE2 voltage can be supplied here by means of an isolated power supply that allows floating operation of the gate driver as per application.

Table 10 Low-side gate driver IC -isolated secondary power supply

PIN	Label	Function
X80 (1)	-	Low-side gate driver positive supply (VCC2) connection
X80 (2)	-	Low-side gate driver supply ground reference (GND2) connection
X80 (3)	-	Low-side gate driver negative supply (VEE2) connection

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4 System performance

4.1 Test points

The board uses the same test point names for the high-side and low-side gate driver. This allows the test point names to be more compact. As the board is separated horizontally, there should be no problems identifying which test points belong to which gate driver. The test point names are summarized in Table 11.

Table 11 Test points

Test point name	Signal measured	Ground reference test point
3V3	VCC1	SGND
CL	I²C clock line	SGND
DA	I²C data line	SGND
R	RDYC	SGND
F#	Fault_N	SGND
Des	DESAT pin	GND2
ON	ON pin	GND2
OFF	ON pin	GND2
C	Clamp pin	GND2

4.2 Example of switching with with CoolSiC™ IMW120R030M1

Figure 47 shows a typical waveform of the gate driver switching a CoolSiC™ IMW120R030M1 with a resistive load.

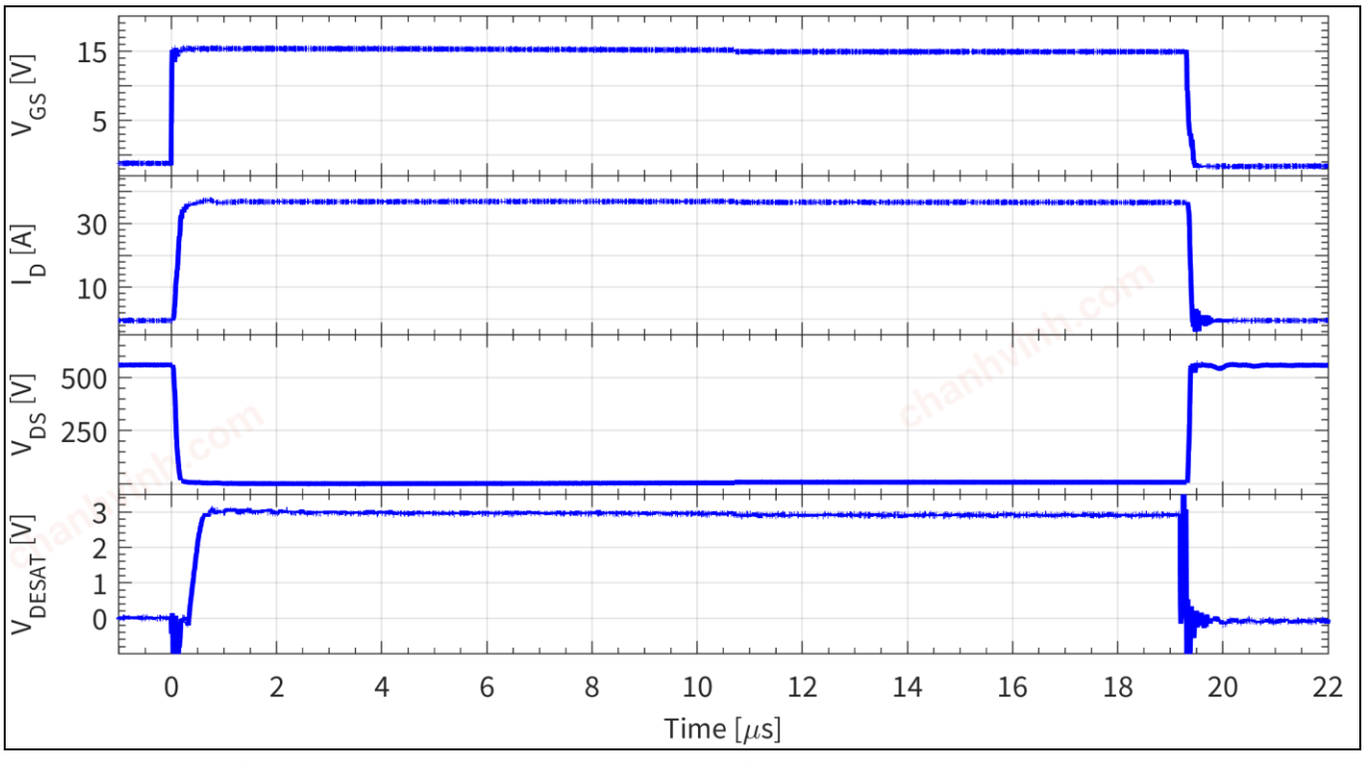


Figure 47 CoolSiC™ IMW120R030M1 switching example

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4.3 Examples of DESAT1 short-circuit protection with CoolSiC™ IMW120R030M1

Figure 48 shows two examples of DESAT1 protection when switching a CoolSiC™ IMW120R030M1 to short circuit. The t_{LEB} filter can be adjusted to allow for more or less blaking time to better suit the application, and accommodate the different turn-on transitions. The t_{DESAT} can also be adjusted to prevent false triggering due to noise coupling. At the same time, it offers fast protection and prevents degradation of the switch.

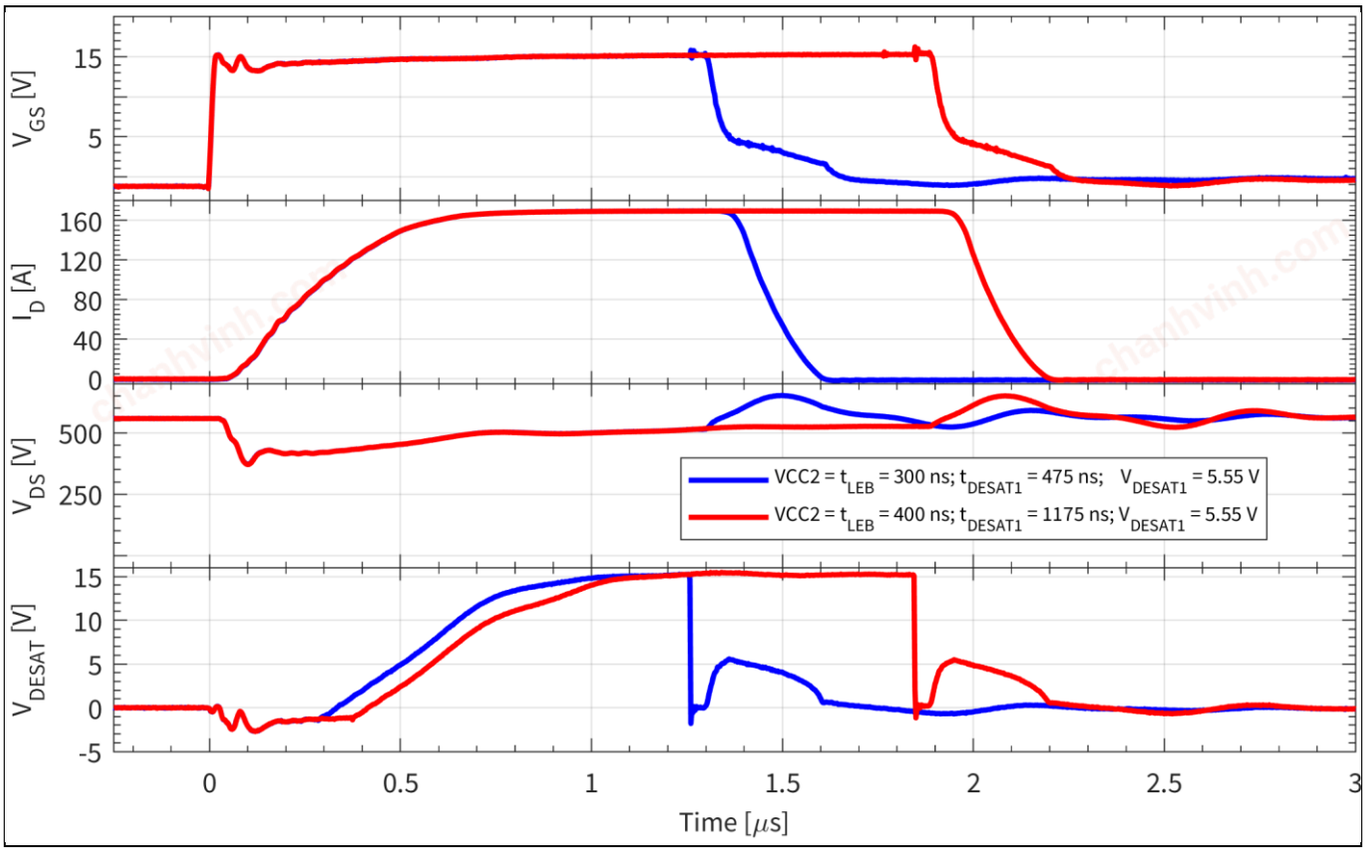


Figure 48 Example waveforms of DESAT1 settings when driving CoolSiC™ IMW120R030M1

4.4 Examples of DESAT2 soft desaturation protection with CoolSiC™ IMW120R030M1

As mentioned earlier, the DESAT2 can be used to monitor for soft-degradation of the gate driver power supply. When such a soft-degradation of the power supply occurs, the gate voltage of the driven switch will be lower. In the case of SiC transistors, such as CoolSiC™, this will have a significant impact on the transistor forward voltage drop during conduction, resulting in higher conduction losses. The increase conduction losses can be significant and negatively affect the SiC MOSFET operation.

The DESAT2 function can be used to detect such small increases in the transistor forward voltage drop. Figure 49 shows an example of using the DESAT2 function as a protection for soft-desaturation. The DESAT2 settings are as follows: V_{DESAT2} = 2.98 V, t_{leb} = 300 ns, $t_{DESATfilter}$ = 4775 ns and fault-off enabled. Here the DESAT2 was adjusted to detect when the CoolSiC™ MOSFET is driven with a gate voltage lower than 14.5 V. When the transistor is driven with a V_{GS} = 15 V, the transistor operation is unaffected. As seen on the blue curve, but as the voltage drops to 14.2 V, as shown by the red curve, the DESAT2 function is triggered, in this case, after approximately 4.5 µs.

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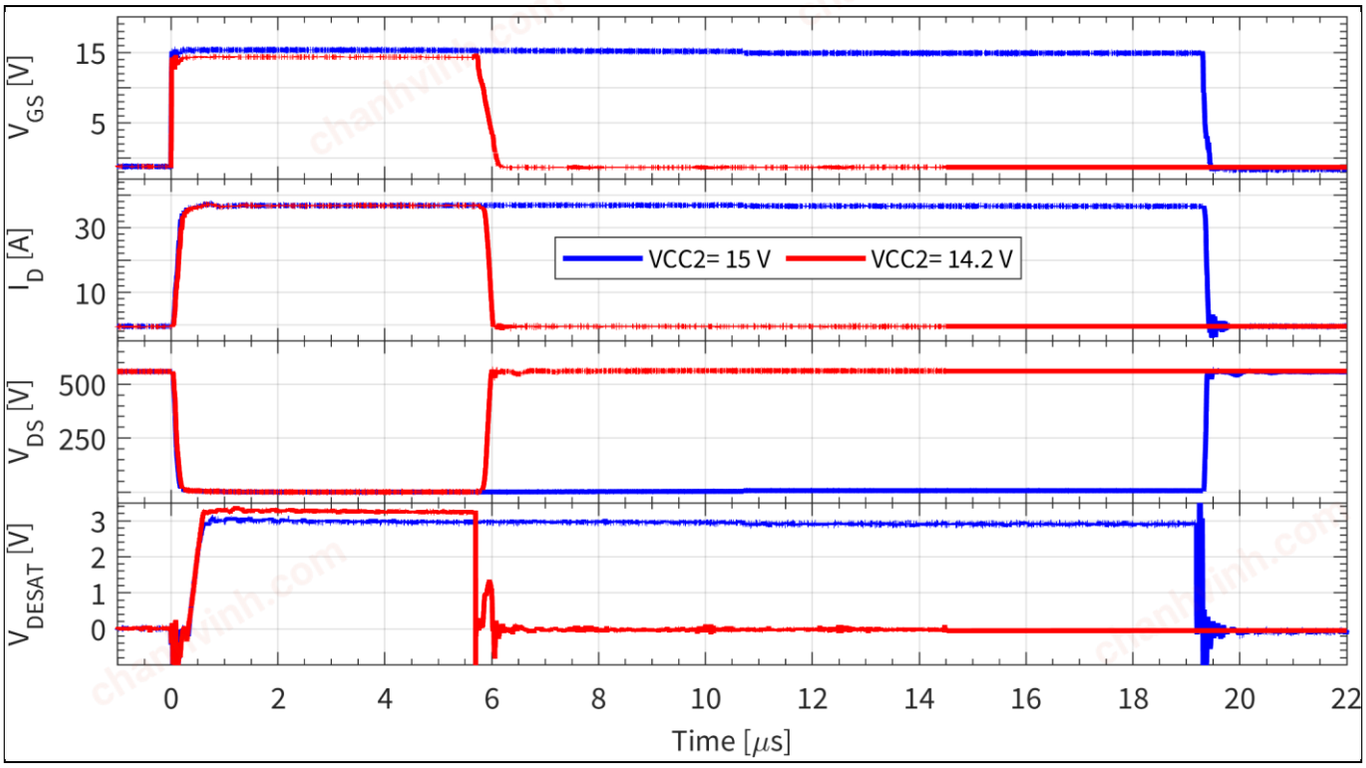


Figure 49 **Example waveform of DESAT2 being used for soft desaturation protection, V_{DESAT2} = 2.98 V, t_{leb} = 300 ns, $t_{DESATfilter}$ = 4775 ns and fault-off enable: blue – VCC2 = 15 V; red – VCC2 = 14.2 V**

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5 References and appendices

5.1 References

[1] Datasheet of Infineon 1ED3890MC12M

[2] Datasheet of Infineon 1ED3890MU12M

[3] Reference manual of Infineon 1ED3890MC12M

[4] User guide of EiceDRIVER™ EVAL-1ED38x0DCT

[5] 1ED38xx X3 Digital configuration software

[6] Datasheet of Infineon IKW50N120CS7

[7] Datasheet of Infineon IMW120R030M1H

5.2 Ordering information

Base Part Number	Package	Standard Pack		Orderable Part Number
		Form	Quantity	
Eval-1ED3890Mx12M	-	Boxed	1	EVAL1ED3890MX12MTOBO1
1ED3890MC12M	PG-DSO-16	TAPE & REEL	1000	1ED3890MC12MXUMA1
1ED3890MU12M	PG-DSO-16	TAPE & REEL	1000	1ED3890MU12MXUMA1

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Revision history

Document version	Date of release	Description of changes
V1.0	19/03/2021	Initial creation
V1.1	29/03/2021	Updated styling
V1.2	30/03/2021	Added version number
V1.3	31/05/2021	Updated board names
V1.4	07/06/2021	Updates software references

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