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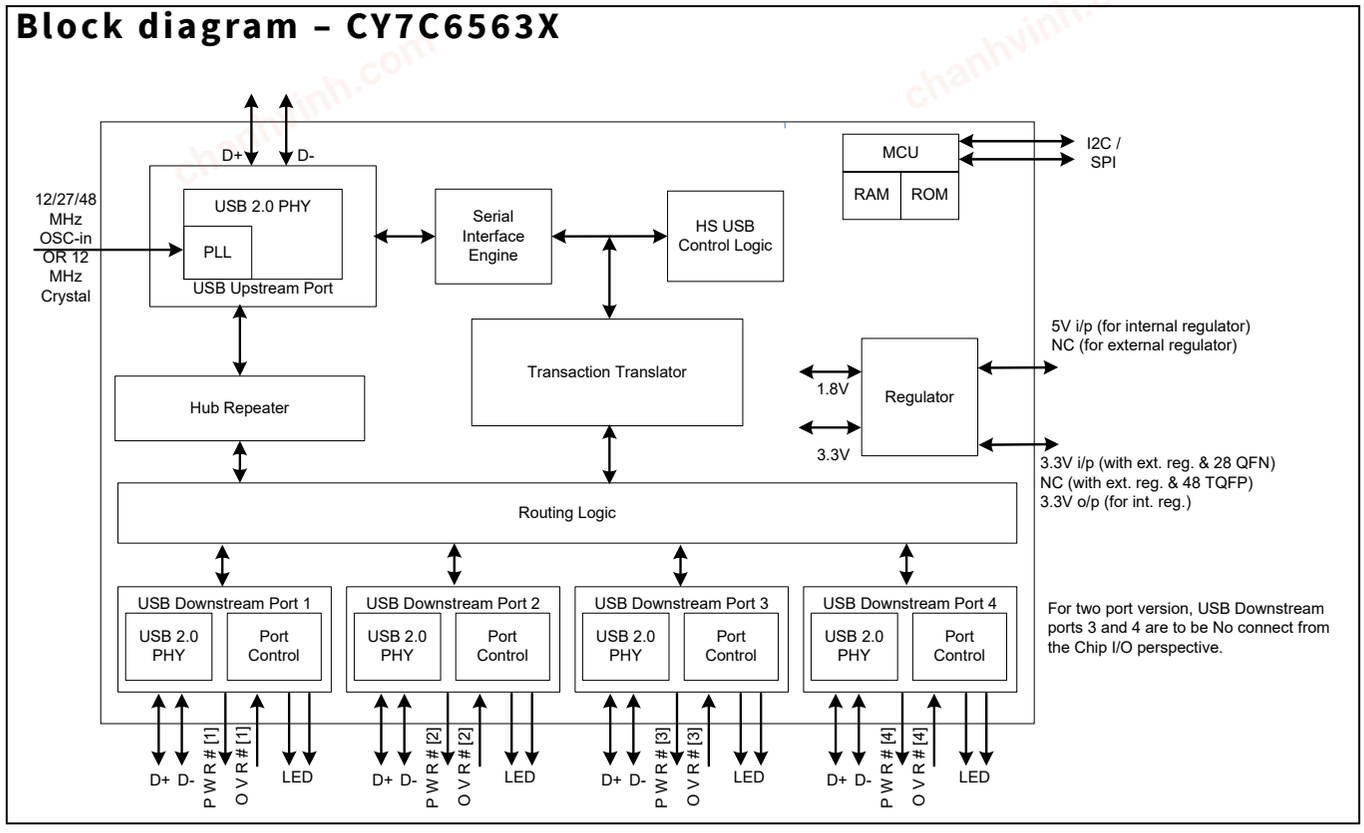
HX2VL - Very Low-Power USB 2.0 Hub Controller

Features

- High performance, low-power USB 2.0 Hub, optimized for low cost designs with minimum bill-of-material
- USB 2.0 hub controller
  - Compliant with USB 2.0 specification, TID# 30000060
  - Up to four downstream ports support
  - Downstream ports are backward compatible with FS, LS
  - Single transaction translator (TT) for low cost
- Very low power consumption
  - Supports bus-powered and self-powered modes
  - Auto switching between bus-powered and self-powered
  - Single MCU with 2K ROM and 64 byte RAM
  - Lowest power consumption
- Highly integrated solution for reduced BOM cost
  - Internal regulator – single power supply 5 V required
  - Provision of connecting 3.3 V with external regulator
  - Integrated upstream pull-up resistor
  - Integrated pull-down resistors for all downstream ports
  - Integrated upstream/downstream termination resistors
  - Integrated port status indicator control
  - 12 MHz +/– 500 ppm external crystal with drive level 600 µW (integrated PLL) clock input with optional 27/48 MHz oscillator clock input
  - Internal power failure detection for ESD recovery
- Downstream port management
  - Support individual and ganged mode power management
  - Overcurrent detection
  - Two port status indicators per downstream port
- Maximum configurability
  - VID and PID are configurable through external EEPROM
  - Number of ports, removable/non-removable ports are configurable through EEPROM and I/O pin configuration
  - I/O pins can configure gang/individual mode power switching, reference clock source and polarity of power switch enable pin
  - Configuration options also available through mask ROM
- Available in space saving 48-pin (7 × 7 mm) TQFP and 28-pin (5 × 5 mm) QFN packages
- Supports 0°C to 70°C temperature range

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Block diagram – CY7C6563X



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1 More information

Infineon provides a wealth of data at **www.infineon.com** to help you to select the right HX2VL device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the **HX2VL product page**.

- Overview: **USB portfolio**
- USB 2.0 Hub Controller selectors: **HX2LP**, **HX2VL**
- Application notes: Infineon offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with HX2VL are:
  - **AN72332 - Guidelines on System Design using Infineon's USB 2.0 Hub (HX2VL)**
  - **AN69235 - Migrating from HX2/HX2LP to HX2VL**
- Reference designs:
  - **CY4608 HX2VL Very Low-Power USB 2.0 Compliant 4-Port Hub Development Kit**
  - **CY4607 HX2VL Very Low-Power USB 2.0 Compliant 4-Port Hub Development Kit**
- Models: **HX2VL (CY7C65632/34/42) - IBIS**

1.1 HX2VL Development Kit

HX2VL Development Kit board is a tool to demonstrate the features of HX2VL devices (CY7C65632, CY7C65634). In the initial phase of the design, this board helps developers to understand the chip features and limitations before proceeding with a complete design. The Development kit includes support documents related to board hardware, PC application software, and EEPROM configuration data (.iic) files.

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2 Introduction

HX2VL™ is Infineon's next generation family of high performance, very low power USB 2.0 hub controllers. HX2VL has integrated upstream and downstream transceivers; a USB Serial Interface Engine (SIE); USB Hub Control and Repeater logic; and Transaction Translator (TT) logic. Infineon has also integrated external components such as voltage regulator and pull-up/pull-down resistors, reducing the overall bill of materials required to implement a USB hub system.

The CY7C6563X is a part of the HX2VL portfolio. This device option is for ultra low power but high performance applications that require up to four downstream ports. All downstream ports share a single transaction translator. The CY7C6563X is available in 48-pin TQFP and 28-pin QFN package options.

All device options are supported by Infineon's world class reference design kits, which include board schematics, bill of materials, Gerber files, Orcad files, and thorough design documentation.

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3 HX2VL architecture

The **“Block diagram – CY7C6563X”** on page 2 shows the HX2VL single TT hub architecture.

3.1 USB serial interface engine

The serial interface engine (SIE) allows HX2VL to communicate with the USB host. The SIE handles the following USB activities independently of the Hub Control Block.

- Bit stuffing and unstuffing
- Checksum generation and checking
- TOKEN type identification
- Address checking

3.2 HS USB control logic

‘Hub Control’ block co-ordinates enumeration, suspend and resume. It generates status and control signals for host access to the hub. It also includes the frame timer that synchronizes the hub to the host. It has status/control registers which function as the interface to the firmware in the MCU.

3.3 Hub Repeater

The Hub Repeater manages the connectivity between upstream and downstream facing ports that are operating at the same speed. It supports full and high speed connectivity. According to the USB 2.0 specification, the Hub Repeater provides the following functions:

- Sets up and tears down connectivity on packet boundaries
- Ensures orderly entry into and out of ‘Suspend’ state, including proper handling of remote wakeups.

3.4 MCU

HX2VL has MCU with 2K ROM and 64 byte RAM. The MCU operates with a 12 MHz clock to decode USB commands from host and respond to the host. It can also handle GPIO settings to provide higher flexibility to the customers and control the read interface to the EEPROM which has extended configuration options. The MCU is programmable while manufacturing in the factory as per customer needs.

3.5 Transaction translator

The transaction translator translates data from one speed to another. A TT takes high speed split transactions and translates them to full or low speed transactions when the hub is operating at high speed (the upstream port is connected to a high speed host controller) and has full or low speed devices attached. The operating speed of a device attached on a downstream port determines whether the routing logic connects a port to the TT or to hub repeater. When the upstream host and downstream device are functioning at different speeds, the data is routed through the TT. In all other cases, the data is routed through the repeater. For example, If a full or low speed device is connected to the high speed host upstream through the hub, then the data transfer route includes TT. If a high speed device is connected to the high speed host upstream through the hub, the transfer route includes the repeater. When the hub is connected to a full speed host controller upstream, then high speed peripheral does not operate at its full capability. These devices only work at full speed. Full and low speed devices connected to this hub operate at their normal speed.

3.6 Port Control

The downstream ‘Port Control’ block handles the connect/disconnect and over current detection as well as the power enable and LED control. It also generates the control signals for the downstream transceivers.

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4 Applications

Typical applications for the HX2VL device family are:

- Docking stations
- Standalone hubs
- Monitor hubs
- Multi-function printers
- Digital televisions
- Advanced port replicators
- Keyboard hubs
- Gaming consoles

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5 Functional overview

The Infineon CY7C6563X USB 2.0 Hubs are low power hub solutions for USB which provide maximum transfer efficiency. The CY7C6563X USB 2.0 Hubs integrate 1.5 kohm upstream pull-up resistors for full speed operation and all downstream 15 kohm pull-down resistors and series termination resistors on all upstream and downstream D+ and D– pins. This results in optimization of system costs by providing built-in support for the USB 2.0 specification.

5.1 System initialization

On power up, CY7C6563X has an option to enumerate from the default settings in the mask ROM or from reading an external EEPROM for configuration information. At the most basic level, this EEPROM has the Vendor ID (VID) and the Product ID (PID), for the customer's application. For more specialized applications, other configuration options can be specified. See **"EEPROM Configuration options"** on page 20 for more details. CY7C6563X verifies the checksum before loading the EEPROM contents as the descriptors.

5.2 Enumeration

CY7C6563X enables the pull-up resistor on D+ to indicate its presence to the upstream hub, after which a USB Bus Reset is expected. After a USB Bus Reset, CY7C6563X is in an unaddressed, unconfigured state (configuration value set to '0'). During the enumeration process, the host sets the hub's address and configuration. After the hub is configured, the full hub functionality is available.

5.3 Upstream port

The upstream port includes the transmitter and the receiver state machine. The transmitter and receiver operate in high speed and full speed depending on the current hub configuration. The transmitter state machine monitors the upstream facing port while the Hub Repeater has connectivity in the upstream direction. This machine prevents babble and disconnect events on the downstream facing ports of this hub from propagating and causing the hub to be disabled or disconnected by the hub to which it is attached.

5.4 Downstream ports

The CY7C6563X supports a maximum of four downstream ports, each of which may be marked as usable or removable in the EEPROM configuration, see **"EEPROM Configuration options"** on page 20. Additionally it can also be configured by pin strapping, see **"Pin configuration options"** on page 23.

Downstream D+ and D– pull-down resistors are incorporated in CY7C6563X for each port. Before the hubs are configured, the ports are driven SE0 (Single Ended Zero, where both D+ and D– are driven low) and are set to the unpowered state. When the hub is configured, the ports are not driven and the host may power the ports by sending a SetPortPower command for each port. After a port is powered, any connect or disconnect event is detected by the hub. Any change in the port state is reported by the hubs back to the host through the Status Change Endpoint (endpoint 1).

On receipt of SetPortReset request for a port with a device connected, the hub does as follows:

- Performs a USB Reset on the corresponding port
- Puts the port in an enabled state
- Enables babble detection after the port is enabled.

Babble consists of a non idle condition on the port after EOF2. If babble is detected on an enabled port, that port is disabled. A ClearPortEnable request from the host also disables the specified port.

Downstream ports can be individually suspended by the host with the SetPortSuspend request. If the hub is not suspended, a remote wakeup event on that port is reflected to the host through a port change indication in the Hub Status Change Endpoint. If the hub is suspended, a remote wakeup event on this port is forwarded to the host. The host may resume the port by sending a ClearPortSuspend command.

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5.5 Power switching

The CY7C6563X includes interface signals for external port power switches. Both ganged and individual (per-port) configurations are supported by pin strapping, see **“Pin configuration options”** on page 23.

After enumerating, the host may power each port by sending a SetPortPower request for that port. Power switching and overcurrent detection are managed using respective control signals (PWR#[n] and OVR#[n]) which are connected to an external power switch device. Both High/Low enabled power switches are supported and the polarity is configured through GPIO setting, see **“Pin configuration options”** on page 23.

5.6 Overcurrent detection

The OVR#[n] pins of the CY7C6563X series are connected to the respective external power switch’s port overcurrent indication (output) signals. After detecting an overcurrent condition, hub reports overcurrent condition to the host and disables the PWR#[n] output to the external power device. OVR#[n] has a setup time of 20 ns. It takes 3 to 4 ms from overcurrent detection to de-assertion of PWR#[n]

5.7 Port indicators

The USB 2.0 port indicators are also supported directly by CY7C6563X. According to the specification, each downstream port of the hub optionally supports a status indicator. The presence of indicators for downstream facing ports is specified by bit 7 of the wHub Characteristics field of the hub class descriptor. The default CY7C6563X descriptor specifies that the port indicators are supported. The CY7C6563X port indicators has two modes of operation: automatic and manual.

On power up the CY7C6563X defaults to automatic mode, where the color of the Port Indicator (green, amber, off) indicates the functional status of the CY7C6563X port. The LEDs are turned off when the device is suspended.

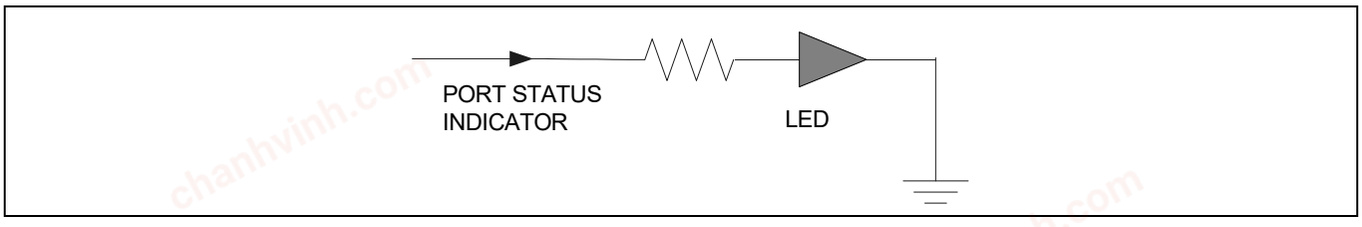


Figure 1 Port status indicator LED

5.8 Power regulator

CY7C6563X requires 3.3 V source power for normal operation of internal core logic and USB physical layer (PHY). The integrated low-drop power regulator converts 5 V power input from USB cable (Vbus) to 3.3 V source power. The 3.3 V power output is guaranteed by an internal voltage reference circuit when the input voltage is within the 4.75 V to 5.25 V range. The regulator’s maximum current loading is 150 mA, which provides tolerance margin over CY7C6563X’s normal power consumption of below 100 mA. The on chip regulator has a quiescent current of 28 µA.

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5.9 External regulation scheme

CY7C6563X supports both external regulation and internal regulation schemes. When an external regulation is chosen, then for the 48 pin package, VCC and VREG are to be left open with no connection. The external regulator output 3.3 V has to be connected to VCC_A and VCC_D pins. This connection has to be done externally, on board. For the 28-pin package, the 3.3 V output from the external regulator has to be connected to VREG, VCC_A and VCC_D. The VCC pin has to be left open with no connection. From the external input 3.3 V, 1.8 V is internally generated for the chip's internal usage.

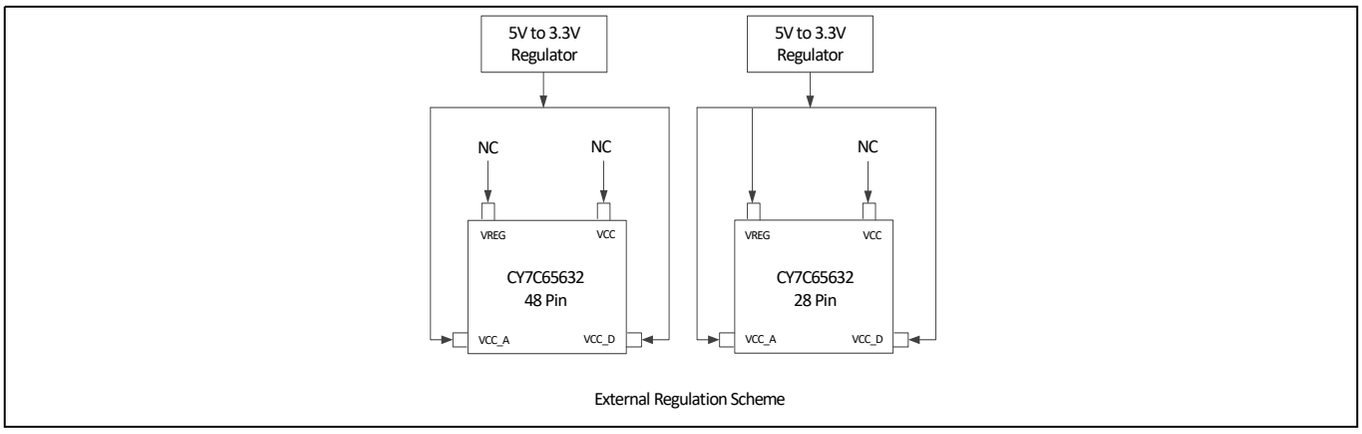


Figure 2 External regulation scheme

5.10 Internal regulation scheme

When the built-in internal regulator is chosen, then the VCC pin has to be connected to a 5 V, in both 48-pin and 28-pin packages. Internally, the built-in regulator generates a 3.3 V and 1.8 V for the chip's internal usage. Also a 3.3 V output is available at VREG pin, that has to be connected externally to VCC_A and VCC_D.

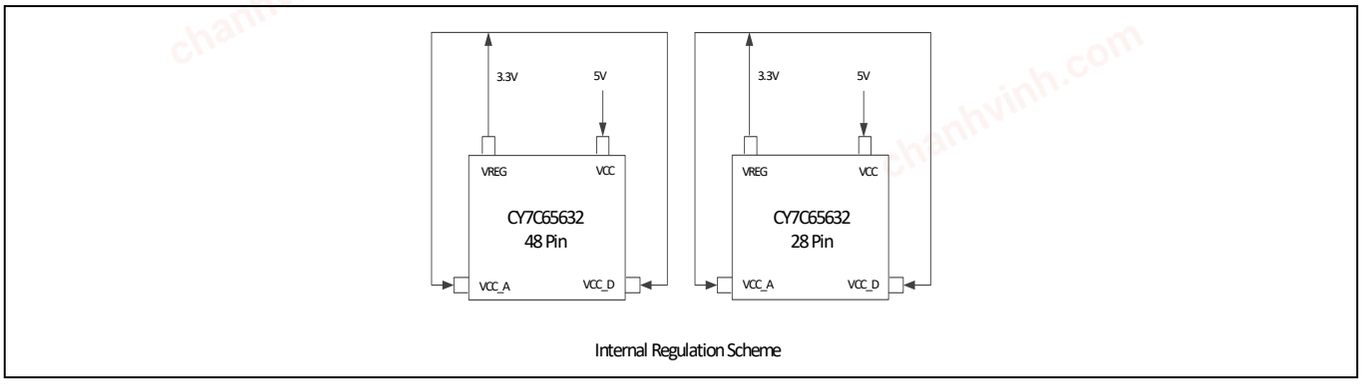


Figure 3 Internal regulation scheme

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6 Pin configurations

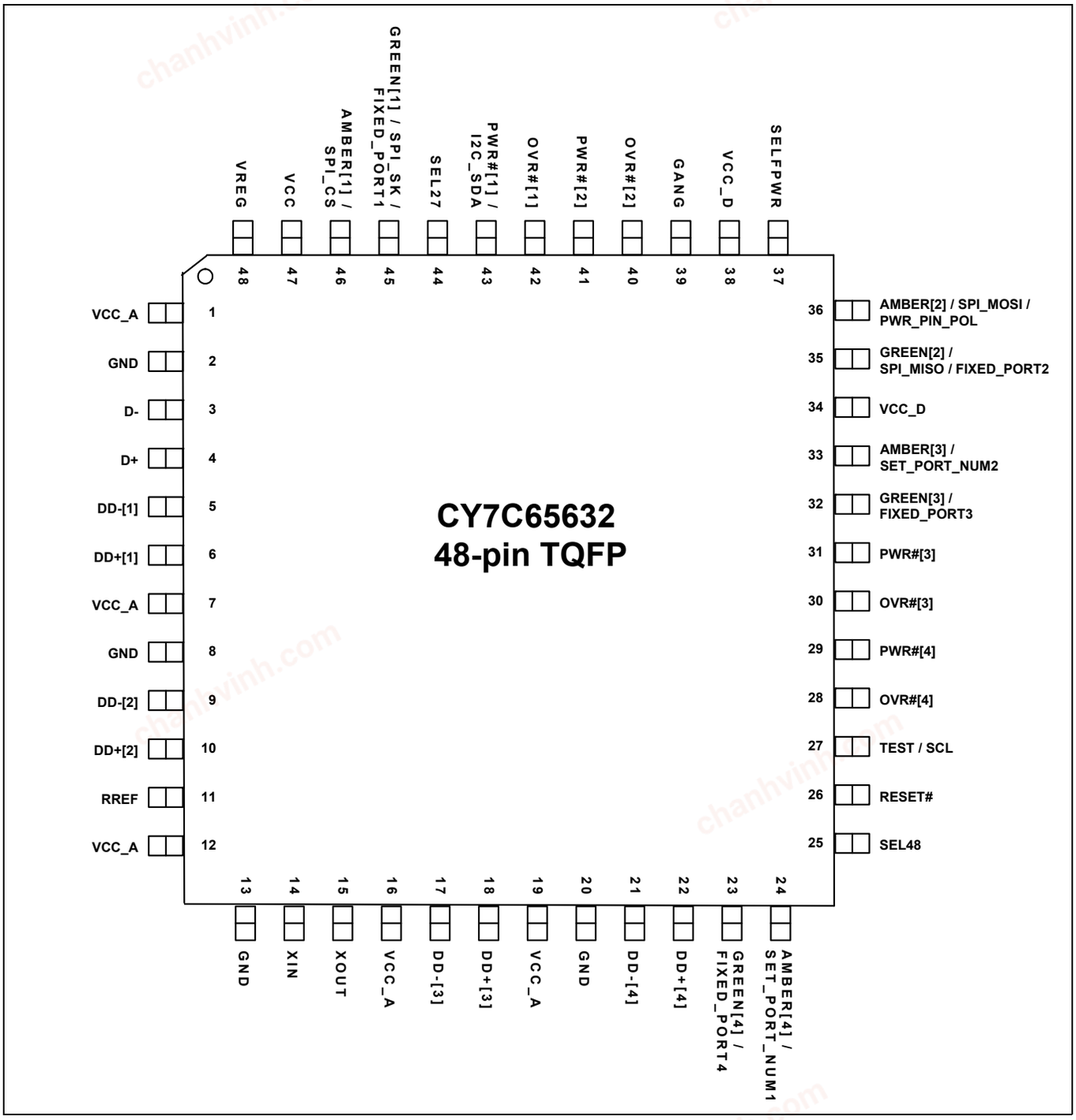


Figure 4 48-pin TQFP (7 × 7 × 1.4 mm) pinout

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Pin configurations

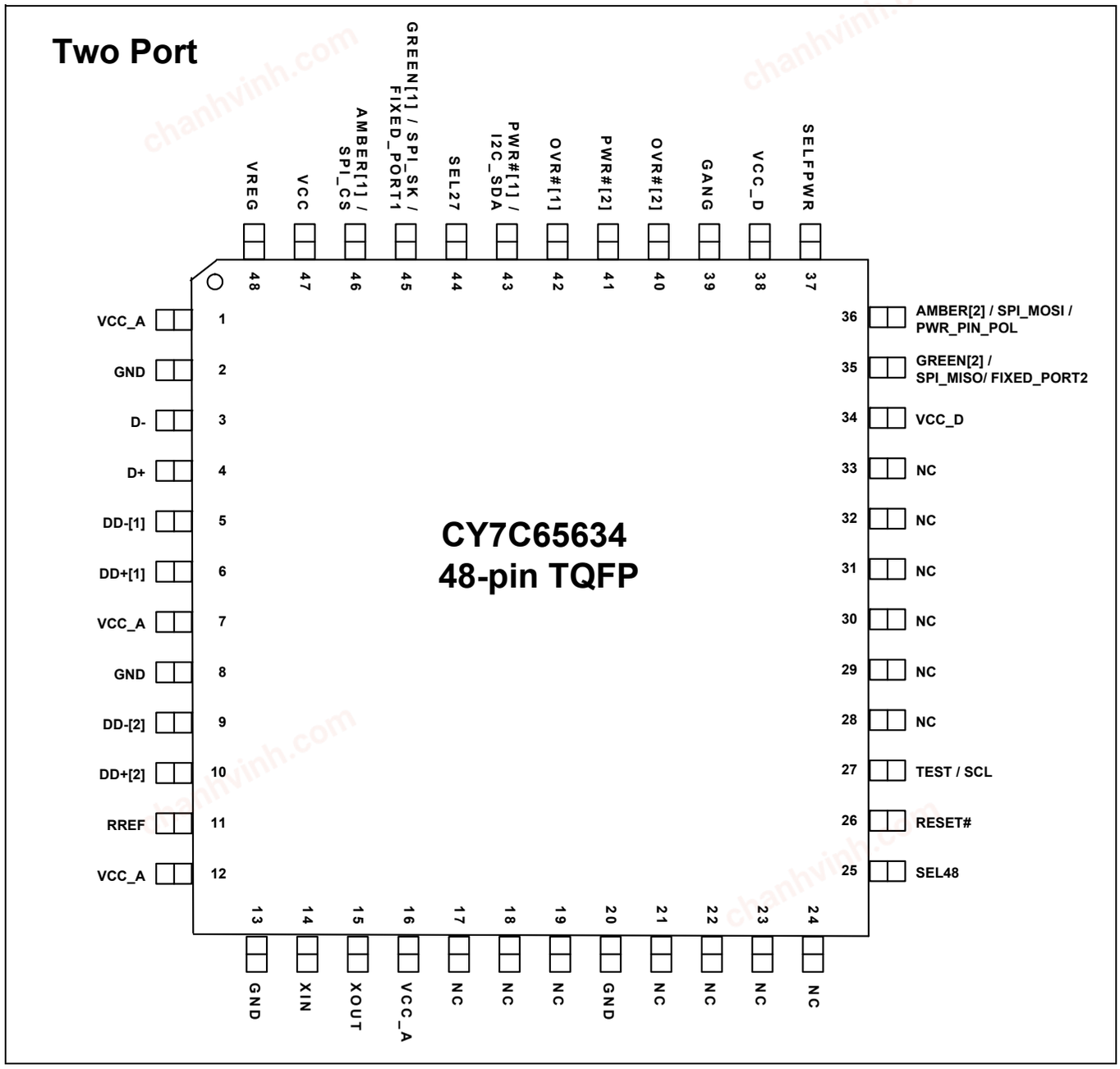


Figure 5 48-pin TQFP (7 × 7 × 1.4 mm) pinout

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Pin configurations

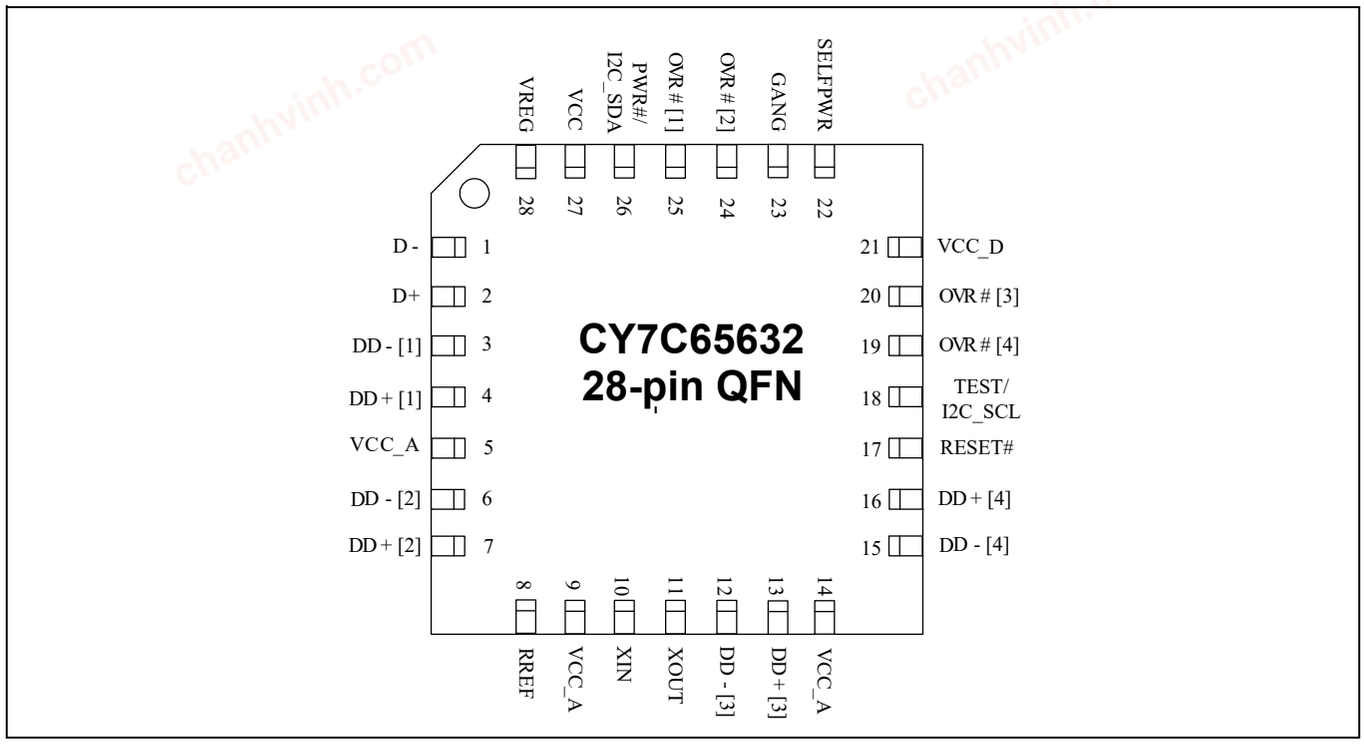


Figure 6 28-pin QFN (5 × 5 × 0.8 mm) pinout

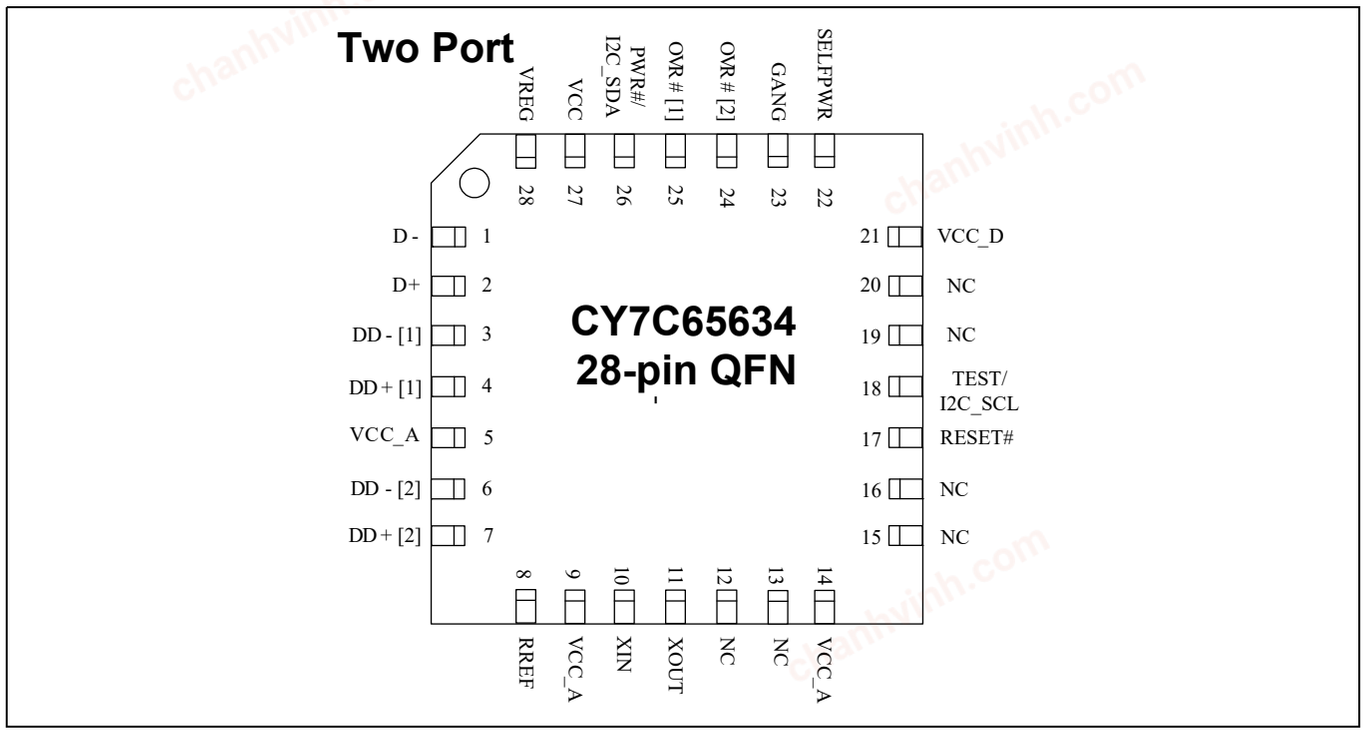


Figure 7 28-pin QFN (5 × 5 × 0.8 mm) pinout

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7 Pin definitions

Table 1 Pin definitions

48-pin TQFP package

Name	Pin No.	Type [1]	Description
Power and Clock			
VCC_A	1	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	7	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	12	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	16	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	19	P	**V_{CC_A}**. 3.3 V analog power to the chip. NC in CY7C65634.
VCC_D	34	P	**V_{CC_D}**. 3.3 V digital power to the chip.
VCC_D	38	P	**V_{CC_D}**. 3.3 V digital power to the chip.
VCC	47	P	**V_{CC}**. 5 V input to the internal regulator; NC if using external regulator.
VREG	48	P	**V_{REG}**. 5 V–3.3 V regulator o/p during internal regulation; NC if using external regulator.
GND	2	P	**GND**. Connect to Ground with as short a path as possible.
GND	8	P	**GND**. Connect to Ground with as short a path as possible.
GND	13	P	**GND**. Connect to Ground with as short a path as possible.
GND	20	P	**GND**. Connect to Ground with as short a path as possible.
XIN	14	I	12 MHz crystal clock input, or 12/27/48 MHz clock input.
XOUT	15	O	12 MHz Crystal OUT.
SEL48/SEL27	25 / 44	I	**Clock source selection inputs**. 00: Reserved 01: 48 MHz OSC-in 10: 27 MHz OSC-in 11: 12 MHz Crystal or OSC-in
RESET#	26	I	**Active LOW Reset**. External reset input, default pull high 10 kΩ; When RESET = low, whole chip is reset to the initial state.
SELFPWR	37	I	**Self Power**. Input for selecting self/bus power. 0 is bus powered, 1 is self powered.
GANG	39	I/O	**GANG**. Default is input mode after power-on-reset. Gang Mode: Input:1 -> Output is 0 for Normal Operation and 1 for Suspend. Individual Mode: Input:0 -> Output is 1 for Normal Operation and 0 for Suspend. Refer to Gang/Individual Power Switching Modes in Pin Configuration Options section for details.
RREF	11	I/O	649 ohm resistor must be connected between RREF and Ground.

Notes

1. Pin Types: I = Input, O = Output, P = Power/Ground.;
   Z = High Impedance, R_{DN} = Pad internal Pull Down Resistor, R_{UP} = Pad internal Pull Up Resistor.
2. The alternate function of these pins as LED indicator is not available if the pins are strapped to logic high, unless a separate circuit is designed to support logic high disconnect after 60 ms of power-on reset (POR), when these pins are reconfigured as outputs.

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Pin definitions

Table 1 Pin definitions *(continued)*

48-pin TQFP package

Name	Pin No.	Type [1]	Description
System Interface			
Test I2C_SCL	27	I(R_{DN}) I/O(R_{DN})	**Test**: 0: Normal Operation & 1: Chip will be put in test mode. **I2C_SCL**: Can be used as I2C clock pin to access I2C EEPROM.
Upstream Port			
D–	3	I/O/Z	**Upstream D– Signal**.
D+	4	I/O/Z	**Upstream D+ Signal**.
Downstream Port 1			
DD–[1]	5	I/O/Z	**Downstream D– Signal**. Downstream D– signal of port 1.
DD+[1]	6	I/O/Z	**Downstream D+ Signal**. Downstream D+ signal of port 1.
AMBER[1][1, 2] SPI_CS	46	O(R_{DN}) O(R_{DN})	**LED**. Driver output for Amber LED. Port Indicator Support. Default is Active HIGH. **SPI_CS**. Can be used as chip select to access external SPI EEPROM.
GREEN[1, 2] SPI_SK FIXED_PORT1	45	O(R_{DN}) O(R_{DN}) I(R_{DN})	**LED**. Driver output for Green LED. Port Indicator Support. Default is Active HIGH. **SPI_SK**. Can be used as SPI Clock to access external SPI EEPROM. **FIXED_PORT1**. At POR used to set Port1 as non removable port. Refer pin configuration Section.
OVR#[1]	42	I(R_{UP})	**Active LOW Overcurrent Condition Detection Input**. Overcurrent condition detection input for Port 1.
PWR#[1] I2C_SDA	43	O/Z I/O	**Power Switch Driver Output**. Default is Active LOW. **I2C_SDA**. Can be used as I2C Data pin, connected with I2C EEPROM.
Downstream Port 2			
DD–[2]	9	I/O/Z	**Downstream D– Signal**. Downstream D– signal of port 2.
DD+[2]	10	I/O/Z	**Downstream D+ Signal**. Downstream D+ signal of port 2.
AMBER[2][2] SPI_MOSI PWR_PIN_POL	36	O(R_{DN}) O(R_{DN}) I(R_{DN})	**LED**. Driver output for Amber LED. Port Indicator Support. Default is Active HIGH. **SPI_MOSI**. Can be used as Data Out to access external SPI EEPROM. **PWR_PIN_POL**. Used for power switch enable pin polarity setting. Refer Configuration section.
GREEN[2][2] SPI_MISO FIXED_PORT2	35	O(R_{DN}) I(R_{DN}) I(R_{DN})	**LED**. Driver output for Green LED. Port Indicator Support. Default is Active HIGH. **SPI_MISO**. Can be used as Data In to access external SPI EEPROM. **FIXED_PORT2**. At POR used to set Port2 as non removable port. Refer Configuration section.
OVR#[2]	40	I(R_{UP})	**Active LOW Overcurrent Condition Detection Input**. Overcurrent condition detection input for Port 2.
PWR#[2]	41	O/Z	**Power Switch Driver Output**. Default is Active LOW.

Notes

1. Pin Types: I = Input, O = Output, P = Power/Ground.;
   Z = High Impedance, R_{DN} = Pad internal Pull Down Resistor, R_{UP} = Pad internal Pull Up Resistor.
2. The alternate function of these pins as LED indicator is not available if the pins are strapped to logic high, unless a separate circuit is designed to support logic high disconnect after 60 ms of power-on reset (POR), when these pins are reconfigured as outputs.

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Pin definitions

Table 1 Pin definitions *(continued)*

48-pin TQFP package

Name	Pin No.	Type [1]	Description
Downstream Port 3			
DD–[3]	17	I/O/Z	**Downstream D– Signal**. NC in CY7C65634.
DD+[3]	18	I/O/Z	**Downstream D+ Signal**. NC in CY7C65634.
AMBER[3][2] SET_PORT_NUM2	33	O(R_{DN}) I(R_{DN})	**LED**. Driver output for Amber LED. Port Indicator Support. Default is Active HIGH. **SET_PORT_NUM2**. Used to set port numbering along with SET_PORT_NUM1. Refer pin configuration section. NC in CY7C65634.
GREEN[3][2] FIXED_PORT3	32	O(R_{DN}) I(R_{DN})	**LED**. Driver output for Green LED. Port Indicator Support. Default is Active HIGH. **FIXED_PORT3**. At POR used to set Port3 as non removable port. Refer pin configuration section. NC in CY7C65634.
OVR#[3]	30	I(R_{UP})	**Active LOW Overcurrent Condition Detection Input**. Overcurrent condition detection input for Port 3. NC in CY7C65634.
PWR#[3]	31	O/Z	**Power Switch Driver Output**. Default is Active LOW. NC in CY7C65634.
Downstream Port 4			
DD–[4]	21	I/O/Z	**Downstream D– Signal**. NC in CY7C65634.
DD+[4]	22	I/O/Z	**Downstream D+ Signal**. NC in CY7C65634.
AMBER[4][2] SET_PORT_NUM1	24	O(R_{DN}) I(R_{DN})	**LED**. Driver output for Amber LED. Port Indicator Support. Default is Active HIGH. **SET_PORT_NUM1**. Used to set port numbering along with SET_PORT_NUM2. Refer configuration section. NC in CY7C65634.
GREEN[4][2] FIXED_PORT4	23	O(R_{DN}) I(R_{DN})	**LED**. Driver output for Green LED. Port Indicator Support. Default is Active HIGH. **FIXED_PORT4**. At POR used to set Port4 as non removable port. Refer configuration section. NC in CY7C65634.
OVR#[4]	28	I(R_{UP})	**Active LOW Overcurrent Condition Detection Input**. Overcurrent condition detection input for Port 4. NC in CY7C65634.
PWR#[4]	29	O/Z	**Power Switch Driver Output**. Default is Active LOW. NC in CY7C65634.

Notes

1. Pin Types: I = Input, O = Output, P = Power/Ground.;
   Z = High Impedance, R_{DN} = Pad internal Pull Down Resistor, R_{UP} = Pad internal Pull Up Resistor.
2. The alternate function of these pins as LED indicator is not available if the pins are strapped to logic high, unless a separate circuit is designed to support logic high disconnect after 60 ms of power-on reset (POR), when these pins are reconfigured as outputs.

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8 Pin definitions

Table 2 Pin definitions

28-pin QFN package

Name	Pin No.	Type[3]	Description
Power and Clock			
VCC_A	5	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	9	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	14	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_D	21	P	**V_{CC_D}**. 3.3 V digital power to the chip.
VCC	27	P	**V_{CC}**. 5 V input to the internal regulator; NC if using external regulator
VREG	28	P	**V_{CC}**. 5 V–3.3 V regulator o/p during internal regulation; 3.3 V I/P if using external regulator.
XIN	10	I	12 MHz crystal clock input, or 12 MHz clock input.
XOUT	11	O	12 MHz Crystal OUT.
RESET#	17	I	**Active LOW Reset**. External reset input, default pull high 10 kΩ; When RESET = low, whole chip is reset to the initial state.
SELFPWR	22	I	**Self Power**. Input for selecting self/bus power. 0 is bus powered, 1 is self powered.
GANG[4]	23	I/O	**GANG**. Default is input mode after power-on-reset. Gang Mode: Input:1 -> Output is 0 for Normal Operation and 1 for Suspend. Individual Mode: Input:0 -> Output is 1 for Normal Operation and 0 for Suspend. Refer to Gang/Individual Power Switching Modes in Pin Configuration Options section for details.
RREF	8	I/O	649 ohm resistor must be connected between RREF and Ground.
System Interface			
Test I2C_SCL	18	I(R_{DN}) I/O(R_{DN})	**Test**: 0: Normal Operation & 1: Chip will be put in test mode. **I2C_SCL**: I2C Clock pin.
PWR# [5] I2C_SDA	26	I/O	**Power Switch Driver Output**. Default is Active LOW. **I2C_SDA**: I2C Data pin.
Upstream Port			
D–	1	I/O/Z	**Upstream D– Signal**.
D+	2	I/O/Z	**Upstream D+ Signal**.

Notes

3. Pin Types: I = Input, O = Output, P = Power/Ground.;
   Z = High Impedance, R_{DN} = Pad internal Pull Down Resistor, R_{UP} = Pad internal Pull Up Resistor.
4. In Gang mode, only OVR#1 (pin 25) is enabled.
5. PWR#/I2C_SDA can be used as either PWR# or I2C_SDA but not as both. If EEPROM is connected then the pin will act as I2C_SDA, it will not switch to PWR# mode (as it does in 48-pin TQFP package).

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Pin definitions

Table 2 Pin definitions *(continued)*

28-pin QFN package

Name	Pin No.	Type[3]	Description
Downstream Port 1			
DD–[1]	3	I/O/Z	**Downstream D– Signal**.
DD+[1]	4	I/O/Z	**Downstream D+ Signal**.
OVR#[1]	25	I(R_{UP})	**Active LOW Overcurrent Condition Detection Input**. Overcurrent condition detection input for Port 1. Only OVR#[1](pin 25) is enabled in Gang mode. OVR#[2](pin 24), OVR#[3](pin 20) and OVR#[4](pin 19) are disabled in Gang mode.
Downstream Port 2			
DD–[2]	6	I/O/Z	**Downstream D– Signal.**
DD+[2]	7	I/O/Z	**Downstream D+ Signal.**
OVR#[2]	24	I(R_{UP})	**Active LOW Overcurrent Condition Detection Input.** Overcurrent condition detection input for Port 2. Only OVR#[1](pin 25) is enabled in Gang mode. This (OVR#[2]) pin is disabled in Gang mode.
Downstream Port 3			
DD–[3]	12	I/O/Z	**Downstream D– Signal.** NC in CY7C65634.
DD+[3]	13	I/O/Z	**Downstream D+ Signal.** NC in CY7C65634.
OVR#[3]	20	I(R_{UP})	**Overcurrent Condition Detection Input.** Default is Active LOW. NC in CY7C65634. Only OVR#[1](pin 25) is enabled in Gang mode. This (OVR#[3]) pin is disabled in Gang mode.
Downstream Port 4			
DD–[4]	15	I/O/Z	**Downstream D– Signal.** NC in CY7C65634.
DD+[4]	16	I/O/Z	**Downstream D+ Signal.** NC in CY7C65634.
OVR#[4]	19	I(R_{UP})	**Overcurrent Condition Detection Input.** Default is Active LOW. NC in CY7C65634. Only OVR#[1](pin 25) is enabled in Gang mode. This (OVR#[4]) pin is disabled in Gang mode.
GND	PAD	P	Ground pin for the chip. It is the solderable exposed pad beneath the chip. Refer **Figure 12**.

Notes

3. Pin Types: I = Input, O = Output, P = Power/Ground.;
   Z = High Impedance, R_{DN} = Pad internal Pull Down Resistor, R_{UP} = Pad internal Pull Up Resistor.
4. In Gang mode, only OVR#1 (pin 25) is enabled.
5. PWR#/I2C_SDA can be used as either PWR# or I2C_SDA but not as both. If EEPROM is connected then the pin will act as I2C_SDA, it will not switch to PWR# mode (as it does in 48-pin TQFP package).

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9 EEPROM Configuration options

Systems using CY7C6563X have the option of using the default descriptors to configure the hub. Otherwise, it must have an external EEPROM for the device to have a unique VID, and PID. The CY7C6563X can communicate with an SPI (microwire) EEPROM like 93C46 or I2C EEPROM like 24C02. Example EEPROM connections are as shown in the following figure.

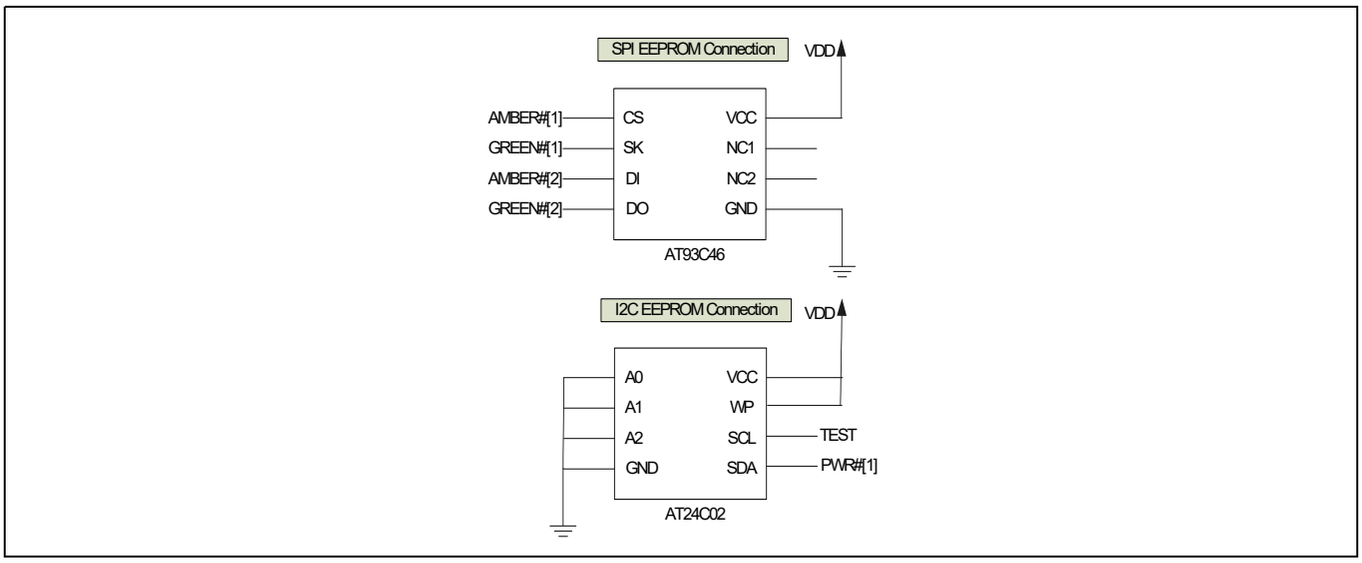


Figure 8 EEPROM connections

Note The 28-pin QFN package includes only support for I2C EEPROM like ATMEL/24C02N_SU27 D, MICROCHIP/4LC028 SN0509, SEIKO/S24CS02AVH9. The 48-pin TQFP package includes both I2C and SPI EEPROM connectivity options. In this case, user can use either SPI or I2C connectivity at a time for communicating to EEPROM. The 48-pin package supports ATMEL/AT93C46DN-SH-T, in addition to the above mentioned families. HX2VL can only read from SPI EEPROM. So, field programming of EEPROM is supported only for I2C EEPROM.

CY7C6563X verifies the check sum after power on reset and if validated loads the configuration from the EEPROM. To prevent this configuration from being overwritten, AMBER[1] is disabled when SPI EEPROM is present.

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EEPROM Configuration options

Table 3 EEPROM configuration options

Byte	Value
00h	VID_LSB
01h	VID_MSB
02h	PID_LSB
03h	PID_MSB
04h	ChkSum
05h	Reserved - FEh
06h	Removable Ports
07h	Port Number
08h	Maximum Power
09h–0Fh	Reserved - FFh
10h	Vendor String Length
11h–3Fh	Vendor String (ASCII code)
40h	Product String Length
41h–6Fh	Product String (ASCII Code)
70h	Serial Number Length
71h to 80h onwards	Serial Number String

Default VID is 0x4B4, PID is 0x6570.

Byte 0: VID (LSB)

Least Significant Byte of Vendor ID

Byte 1: VID (MSB)

Most Significant Byte of Vendor ID

Byte2: PID (LSB)

Least Significant Byte of Product ID

Byte 3: PID (MSB)

Most Significant Byte of Product ID

Byte 4: ChkSum

CY7C6563X will ignore the EEPROM settings if ChkSum is not equal to VID_LSB + VID_MSB + PID_LSB + PID_MSB +1

Byte 5: Reserved

Set to FEh

Byte 6: RemovablePorts

RemovablePorts[4:1] are the bits that indicates whether the device attached to the corresponding downstream port is removable (set to 0) or non-removable (set to 1). Bit 1 corresponds to Port 1, Bit 2 to Port 2 and so on. Default value is 0 (removable). These bit values are reported appropriately in the HubDescriptor:DeviceRemovable field.

Bits 0, 5, 6, 7 are set to 0.

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Byte 7: Port Number

Port Number indicates the number of downstream ports. The values must be 1 to 4. Default value is 4.

Byte 8: Maximum Power

This value is reported in the Configuration Descriptor: bMax-Power field and is the current in 2 mA increments that is required from the upstream hubs. The allowed range is 00h (0 mA) to FAh(500 mA). Default value is 32h (100mA).

Byte 9–15: Reserved

Set to FFh

Byte 16: Vendor String Length

Length of the Vendor String

Byte 17–63: Vendor String

Value of Vendor String.

Byte 64: Product String Length

Length of the Product String

Byte 65–111: Product String

Value of Product String.

Byte 112: Serial Number Length

Length of the Serial Number

Byte 113 onwards: Serial Number String

Serial Number String.

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10 Pin configuration options

10.1 Power on reset

The power on reset can be triggered by external reset or internal circuitry. The internal reset is initiated, when there is an unstable power event for silicon's internal core power (3.3 V ± 10%). The internal reset is released 2.7 µs± 1.2% after supply reaches power good voltage (2.5 V to 2.8 V). The external reset pin, continuously senses the voltage level (5 V) on the upstream VBUS as shown in the figure. In the event of USB plug/unplug or drop in voltage, the external reset is triggered. This reset trigger can be configured using the resistors R1 and R2. Infineon recommends that the reset time applied in external reset circuit should be longer than that of the internal reset time.

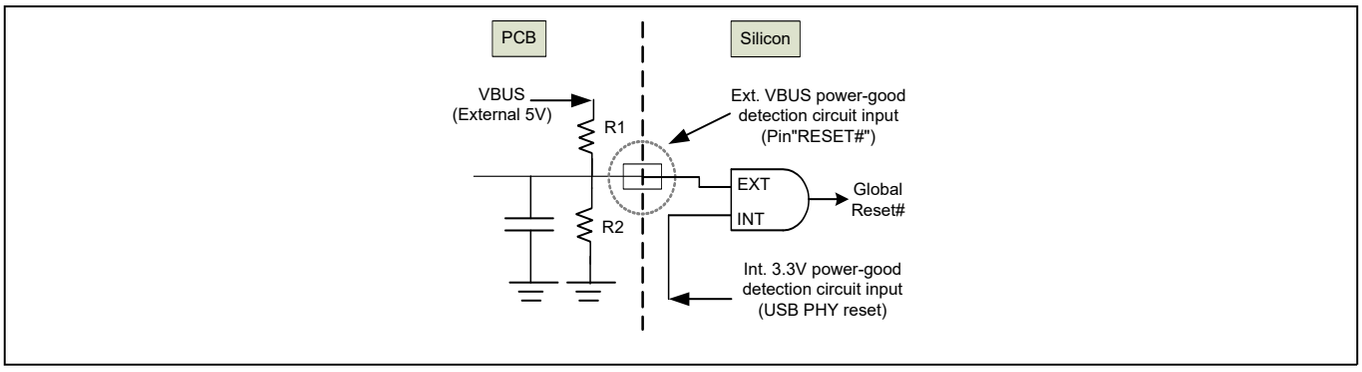


Figure 9 Power on reset circuit

10.2 Gang/individual power switching mode

A single pin is used to set individual / gang mode as well as output the suspend flag. This is done to reduce the pin count. The individual or gang mode is decided within 20 µs after power on reset. It has a setup time of 1 ns. 50 ms to 60 ms after reset, this pin is changed to output mode. CY7C6563X outputs the suspend flag, after it is globally suspended. Pull-down resistor of greater than 100K is needed for Individual mode and a pull-up resistor greater than 100K is needed for Gang mode. Figure below shows the suspend LED indicator schematics. The polarity of LED must be followed, otherwise the suspend current will be over the spec limitation (2.5 mA).

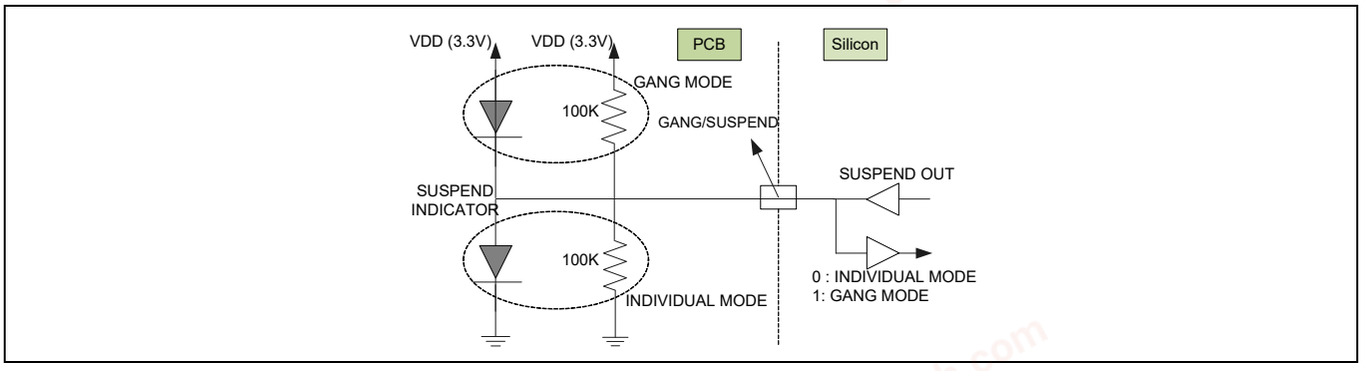


Figure 10 Power switching mode

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Pin configuration options

Table 4 Features supported in 48-pin and 28-pin packages

Supported features	48-pin	28-pin
Port number configuration	Yes	No
Non-Removable port configuration	Yes	No
Reference clock configuration	Yes	No
Power switch enable polarity	Yes	No
LED Indicator	Yes	No

10.3 Power switch enable pin polarity

The pin polarity is set Active-High by pin-strapping the PWR_PIN_POL pin to 1 and Active-Low by pin-strapping the PWR_PIN_POL pin to 0. Thus, both kinds of power switches are supported. This feature is not supported in 28-pin QFN package.

10.4 Port number configuration

In addition to the EEPROM configuration, as described above, configuring the hub for 2/3/4 ports is also supported using pin-strapping SET_PORT_NUM1 and SET_PORT_NUM2, as shown in following table. Pin strapping option is not supported in the 28-pin QFN package.

Table 5 Port number configuration using pinstrap

SET_PORT_NUM2	SET_PORT_NUM1	# Ports
1	1	1 (Port 1)
1	0	2 (Port 1/2)
0	1	3 (Port 1/2/3)
0	0	4 (All ports)

10.5 Non removable ports configuration

In embedded systems, downstream ports that are always connected inside the system, can be set as non-removable (always connected) ports, by pin-strapping the corresponding FIXED_PORT# pins 1~4 to High, before power on reset. At POR, if the pin is pull high, the corresponding port is set to non-removable. This is not supported in the 28-pin QFN package.

10.6 Reference clock configuration

This hub can support, optional 27/48 MHz clock source. When on-board 27/48 MHz clock is present, then using this feature, system integrator can further reduce the BOM cost by eliminating the external crystal. This is available through GPIO pin configuration shown as follows. This is not supported in the 28-pin QFN package.

Table 6 Reference clock options

SEL48	SEL27	Clock source
0	1	48 MHz OSC-in
1	0	27 MHz OSC-in
1	1	12 MHz X’tal/OSC-in

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11 Absolute maximum ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7 Absolute maximum ratings

Parameter	Ratings
Storage temperature	–55°C to +100°C
Ambient temperature	0°C to +70°C
5 V supply voltage to ground potential	–0.5 V to +6.0 V
3.3 V supply voltage to ground potential	–0.5 V to +3.6 V
Voltage at open drain input pins (OVR#1–4, SELFPWR, RESET#)	–0.5 V to +5.5 V
3.3 V input voltage for digital I/O	–0.5 V to +3.6 V
FOSC (oscillator or crystal frequency)	12 MHz ± 0.05%

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12 Operating conditions

Table 8 Operating conditions

Parameter	Conditions
Ambient temperature	0°C to +70°C
Ambient max junction temperature	0°C to +125°C
5 V supply voltage to ground potential	4.75 V to +5.25 V
3.3 V supply voltage to ground potential	3.15 V to +3.6 V
Input voltage for USB signal pins	0.5 V to +3.6 V
Voltage at open drain input pins	–0.5 V to +5.0 V
Thermal characteristics 48-pin TQFP	78.7 °C/W
Thermal characteristics 28-pin QFN	33.3 °C/W

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13 Electrical characteristics

13.1 DC electrical characteristics

Table 9 DC electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max		Unit
					External regulator	Internal regulator	
P_D	Power dissipation	Excluding USB signals	366.5	–	426.5		mW
V_{IH}	Input high voltage	–	2	–	–		V
V_{IL}	Input low voltage	–	–	–	0.8		
I_I	Input leakage current	Full speed / Low speed ($0 < V_{IN} < V_{CC}$)	–10	–	+10		µA
		High speed mode ($0 < V_{IN} < V_{CC}$)	–5	0	+5		
V_{OH}	Output voltage high	I_{OH} = 8 mA	2.4	–	–		V
V_{OL}	Output low voltage	I_{OL} = 8 mA	–	–	0.4		
R_{DN}	Pad internal pull-down resistor	–	29	59	135		KΩ
R_{UP}	Pad internal pull-up resistor	–	80	108	140		
C_{IN}	Input pin capacitance	Full speed / Low speed mode	–	–	20		pF
		High speed mode	4	4.5	5		
I_{SUSP}	Suspend current	–	–	0.786	1.043	1.3	mA

Notes
6. Current measurement is with device attached and enumerated.
7. No devices attached.

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Electrical characteristics

Table 9 DC electrical characteristics *(continued)*

Parameter	Description	Conditions	Min	Typ	Max		Unit
					External regulator	Internal regulator	
I_{CC}	Supply current						
	4 Active ports[6]	Full speed host, full speed devices	–	88.7	103.9	105.4	mA
		High speed host, high speed devices	–	81.9	88.2	89.3	
		High speed host, full speed devices	–	88.2	101.2	102.3	
	3 Active ports	Full speed host, full speed devices	–	79.1	91.6	93	
		High speed host, high speed devices	–	72.9	78.5	78.6	
		High speed host, full speed devices	–	75.9	88.7	88.8	
	2 Active ports	Full speed host, full speed devices	–	68.1	78.4	78.6	
		High speed host, high speed devices	–	61.9	67.6	69.6	
		High speed host, full speed devices	–	64.9	75.4	76.1	
	1 Active port	Full speed host, full speed devices	–	57.1	66.3	66.7	
		High speed host, high speed devices	–	51.9	57.6	59.3	
		High speed host, full speed devices	–	54.7	61.1	62.5	
	No Active Ports[7]	Full speed host	–	42.8	48.9	50.3	
		High speed host	–	44.2	49.1	50.6	

Notes
6. Current measurement is with device attached and enumerated.
7. No devices attached.

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13.2 AC electrical characteristics

USB Transceiver is USB 2.0 certified in low, full and high speed modes.

Both the upstream USB transceiver and all four downstream transceivers have passed the USB-IF USB 2.0 Electrical Certification Testing.

The 48-pin TQFP package can support communication to EEPROM using either I^2C or SPI. The 28-pin QFN package can support only I^2C communication to EEPROM.

AC Characteristics of these two interfaces to EEPROM are summarized in tables below:

Table 10 AC characteristics of SPI EEPROM interface

Parameter	Parameter	Min	Typ	Max	Units
t_{CSS}	CS setup time	3.0	–	–	µs
t_{CSH}	CS hold time	3.0	–	–	
t_{SKH}	SK high time	1.0	–	–	
t_{SKL}	SK low time	2.2	–	–	
t_{DIS}	DI setup time	1.8	–	–	
t_{DIH}	DI hold time	2.4	–	–	
t_{PD1}	Output delay to ‘1’	–	–	1.8	
t_{PD0}	Output delay to ‘0’	–	–	1.8	

Table 11 AC characteristics of I^2C EEPROM interface

Parameter	Parameter	1.8 V–5.5 V		2.5 V–5.5 V		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0.0	100	0.0	400	kHz
t_{LOW}	Clock LOW Period	4.7	–	1.2	–	µs
t_{HIGH}	Clock HIGH Period	4.0	–	0.6	–	
$t_{SU:STA}$	Start condition setup time	4.7	–	0.6	–	
$t_{SU:STO}$	Stop condition setup time	4.7	–	0.6	–	
$t_{HD:STA}$	Start condition hold time	4.0	–	0.6	–	
$t_{HD:STO}$	Stop condition hold time	4.0	–	0.6	–	
$t_{SU:DAT}$	Data in setup time	200.0	–	100.0	–	ns
$t_{HD:DAT}$	Data in hold time	0	–	0	–	
t_{DH}	Data out hold time	100	–	50	–	
t_{AA}	Clock to output	0.1	4.5	0.1	–	µs
t_{WR}	Write cycle time	–	10	–	5	ns

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14 Thermal resistance

Table 12 Thermal resistance

Parameter	Description	48-pin TQFP package	28-pin QFN package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	78.7	33.3	°C/W
Θ_{JC}	Thermal resistance (junction to case)	35.3	18.4	

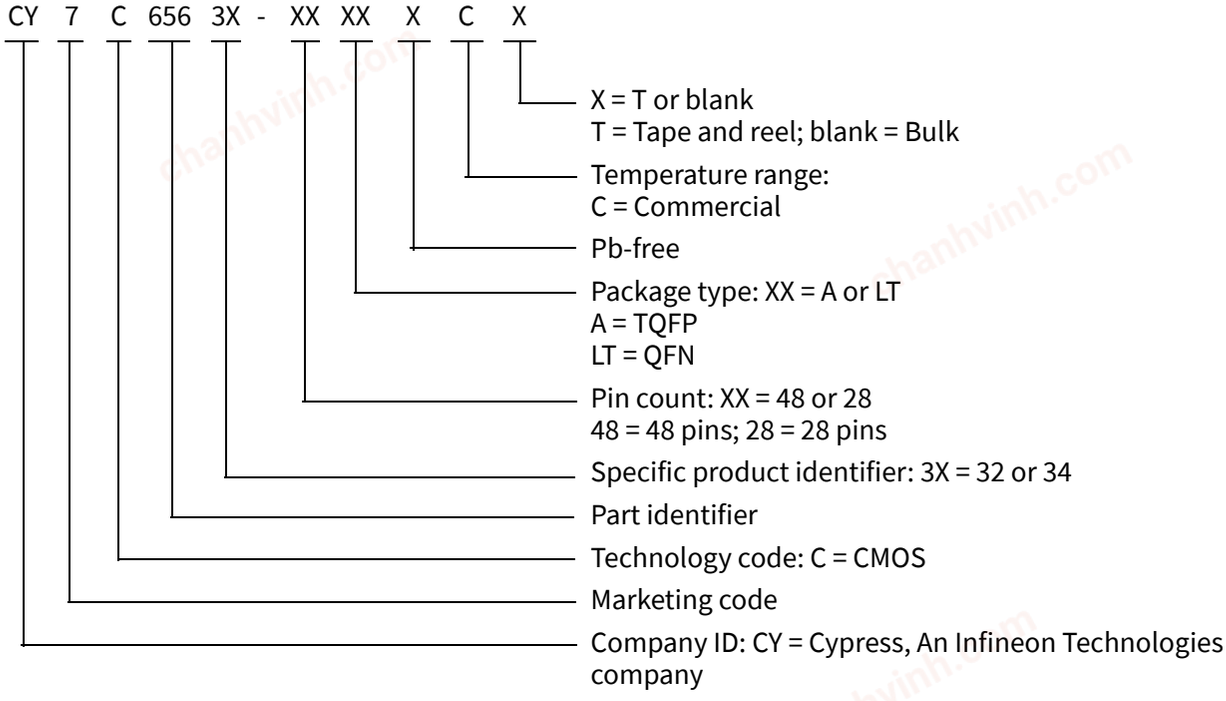
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15 Ordering information

Table 13 Ordering information

Ordering code	Device	Package type
CY7C65632, CY7C65634-48AXC	4 port Single-TT hub (configurable with GPIOs and EEPROM)	48-pin TQFP Bulk
CY7C65632, CY7C65634-28LTXC	4 port Single-TT hub (configurable with GPIOs and EEPROM)	28-pin QFN Bulk
CY7C65632, CY7C65634-48AXCT	4 port Single-TT hub (configurable with GPIOs and EEPROM)	48-pin TQFP - Tape and reel
CY7C65632, CY7C65634-28LTXCT	4 port Single-TT hub (configurable with GPIOs and EEPROM)	28-pin QFN - Tape and reel
CY7C65634-48AXC	2 port Single-TT hub (configurable with GPIOs and EEPROM)	48-pin TQFP Bulk
CY7C65634-28LTXC	2 port Single-TT hub (configurable with GPIOs and EEPROM)	28-pin QFN Bulk
CY7C65634-48AXCT	2 port Single-TT hub (configurable with GPIOs and EEPROM)	48-pin TQFP - Tape and reel
CY7C65634-28LTXCT	2 port Single-TT hub (configurable with GPIOs and EEPROM)	28-pin QFN - Tape and reel

15.1 Ordering code definitions



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16 Package diagrams

The CY7C65632, CY7C65634 is available in following packages:

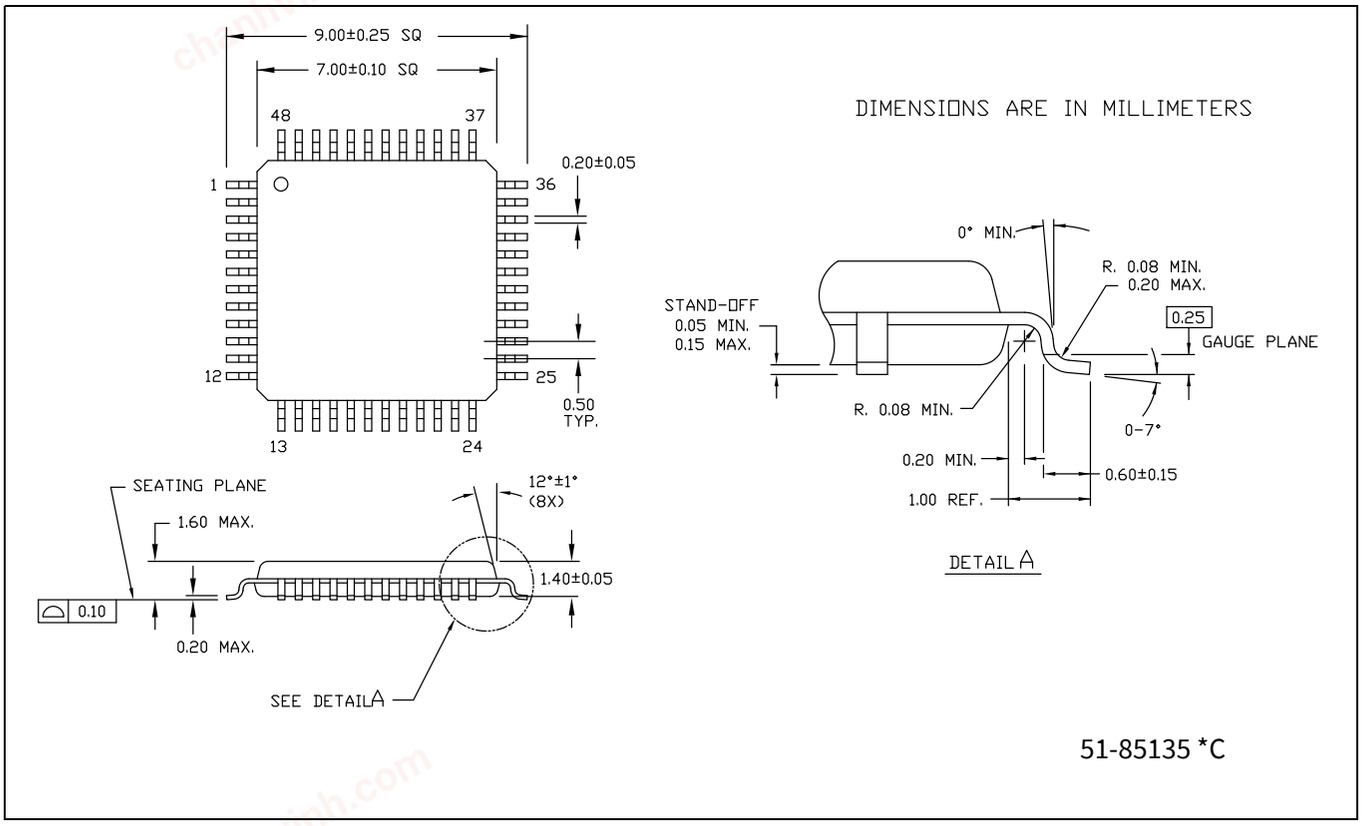


Figure 11 48-pin TQFP (7 × 7 × 1.4 mm) package outline, 51-85135

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Package diagrams

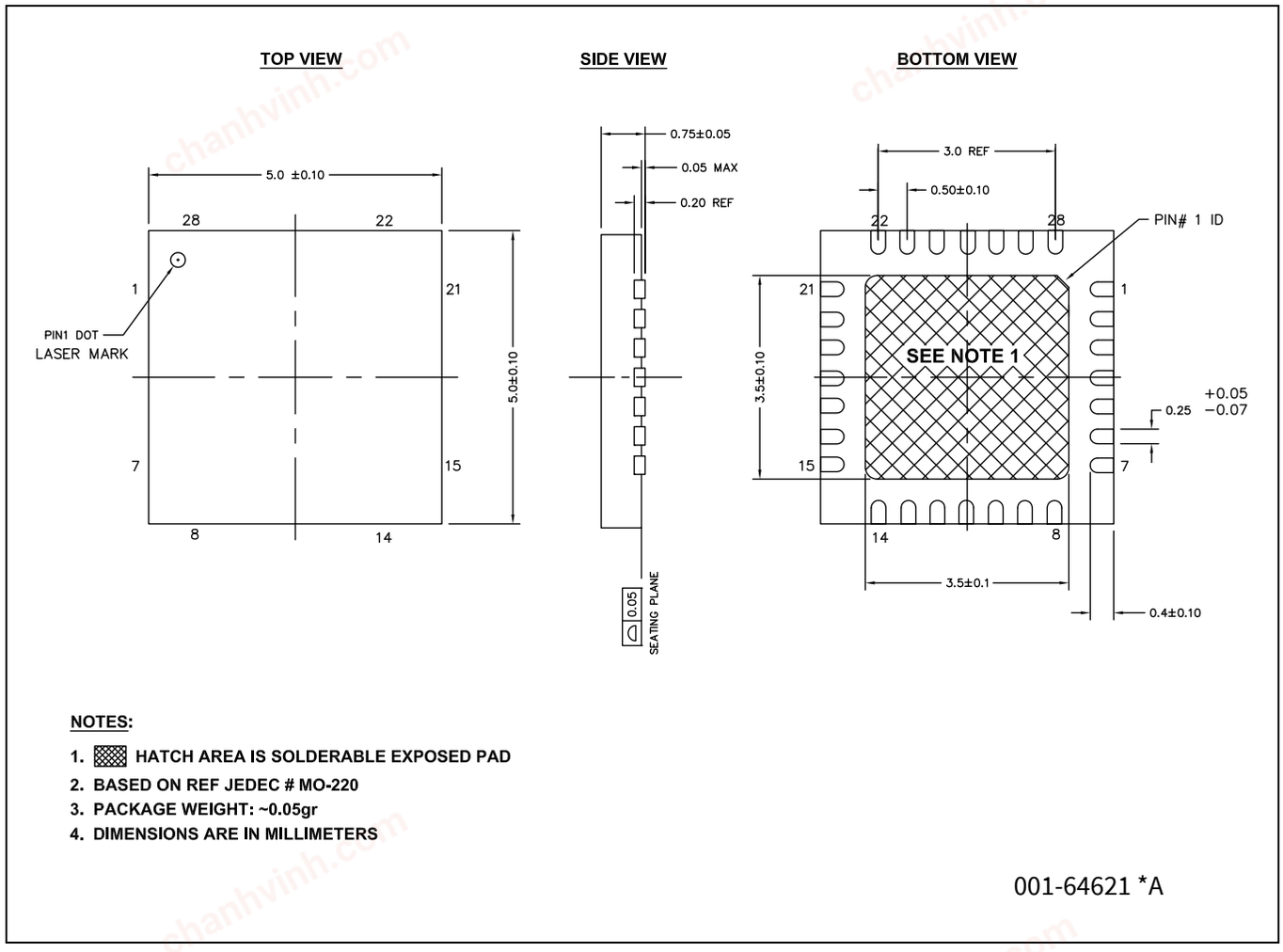


Figure 12 28-pin QFN ((5 × 5 × 0.8 mm) 3.5 × 3.5 E-Pad (Sawn)) package outline, 001-64621

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17 Acronyms

Table 14 Acronyms

Acronym	Description
AC	alternating current
ASCII	american standard code for information interchange
EEPROM	electrically erasable programmable read only memory
EMI	electromagnetic interference
ESD	electrostatic discharge
GPIO	general purpose input/output
I/O	input/output
LED	light emitting diode
LSB	least significant bit
MSB	most significant bit
PCB	printed circuit board
PLL	phase-locked loop
POR	power on reset
PSoC™	Programmable System-on-Chip™
QFN	quad flat no leads
RAM	random access memory
ROM	read only memory
SIE	serial interface engine
TQFP	thin quad flat pack
TT	transaction translator
USB	universal serial bus

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18 Document conventions

18.1 Units of measure

Table 15 Units of measure

Symbol	Unit of measure
°C	degree Celsius
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
µA	microampere
µs	microsecond
µW	microwatt
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ppm	parts per million
V	volt
W	watt

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19 Silicon Errata for the HX2VL, CY7C65632 product family

This section describes the errata for the HX2VL, CY7C65632. The details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Infineon Sales Representative, if you have any questions.

19.1 Part numbers affected

Part number	Device characteristics
CY7C65632	USB 2.0 Single TT Hub

19.2 HX2VL Qualification status

Product Status: In production

19.3 HX2VL Errata summary

This table defines the errata applicability to available HX2VL family devices.

Items	Part numbers	Silicon Revision	Workaround	Fix status
1. **USB device is not recognized properly if a disconnect followed by a connect event happen during hub suspend**	CY7C65632	Rev. **	Issue a Port-Reset from host USB application or driver if the USB device commands STALLed	No fix planned.

1. USB device is not recognized properly if a disconnect followed by a connect event happen during hub suspend

- **Problem definition**
  HX2VL sometimes does not recognize Downstream (DS) USB device after coming out of suspend if the connected DS device is disconnected and connected back to the same DS port during hub suspend state.
- **Parameters affected**
  N/A.
- **Trigger condition(s)**
  Disconnect followed by a Connect event of DS device from the hub during suspend state.
- **Scope of impact**
  The issue is not observed with standard Microsoft driver/class devices such as mouse, keyboard, mass storage, etc. as the standard class drivers recover the device using Port-Reset command when there is a STALL from the DS devices.
- **Workaround**
  Issue a Port-Reset from host USB application or driver to recover the DS device when it STALLS.
- **Fix status**
  No fix planned.

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Revision history

Document revision	Date	Description of changes
**	2011-03-02	New data sheet.
*A	2011-05-06	Updated **Functional overview**: Updated **Port indicators**: Added a Note “Pin-strapping GREEN#[1] and GREEN#[2] enables proprietary function that may affect the normal functionality of HX2VL. Configuring Port #1 and #2 as non-removable by pin-strapping should be avoided.”. Updated **Pin configurations**: Updated **Figure 4** (Pin 37 of the 48-pin TQFP package was named SELF_PWR. It is changed to SELFPWR.). Updated **Figure 5** (Pin 37 of the 48-pin TQFP package was named SELF_PWR. It is changed to SELFPWR.). Updated **Pin definitions** (for 48-pin TQFP package): Changed value from 680 Ω to 650 Ω in description of RREF pin. Updated **Functional overview**: Updated **Power regulator**: Changed regulator’s maximum current loading from 200 mA to 150 mA. Updated **Pin configuration options**: Updated **Power switch enable pin polarity**: Replaced first two occurrences of the word “setting” with “pin-strapping”. Updated **Electrical characteristics**: Updated **DC electrical characteristics**: Changed typical value of I_{SUSP} parameter from 693.3 µA to 786 µA. Changed maximum value of I_{SUSP} parameter 693.7 µA to 903 µA. Updated typical and maximum values of I_{CC} parameter.
*B	2011-07-25	Changed status from Preliminary to Final. Updated **Pin configurations**: Included CY7C65634 related information. Updated **Pin definitions** (for 48-pin TQFP package): Changed description of OVR# pins from “Default is Active LOW” to “Active LOW Overcurrent Condition Detection Input” (since the polarity is not configurable). Updated **Pin definitions** (for 28-pin QFN package): Changed description of OVR# pins from “Default is Active LOW” to “Active LOW Overcurrent Condition Detection Input” (since the polarity is not configurable). Updated **Electrical characteristics**: Updated **DC electrical characteristics**: Updated minimum, typical, and maximum values of R_{DN} and R_{UP} parameters to 81 kΩ, 103 kΩ, and 181 kΩ.
*C	2011-08-04	No technical updates.

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Revision history

Document revision	Date	Description of changes
*D	2011-10-18	Updated **Pin configurations**: Updated **Figure 4** (Renamed SPI_DI to SPI_MOSI, renamed SPI_DO to SPI_MISO respectively for clarity). Updated **Figure 5** (Renamed SPI_DI to SPI_MOSI, renamed SPI_DO to SPI_MISO respectively for clarity). Updated **Figure 6** (Updated pin 26 to describe the alternate function I2C_SDA.). Updated **Figure 7** (Updated to reflect pin 20 as NC). Updated **Pin definitions** (for 48-pin TQFP package): Renamed SPI_DI to SPI_MOSI, renamed SPI_DO to SPI_MISO respectively for clarity. Updated **Pin definitions** (for 28-pin QFN package): Added Note **5** and referred the same note in PWR#. Minor text edits to add clarity.
*E	2011-01-25	Updated **EEPROM Configuration options**: Removed text “Strings must comply with the USB specification. The first byte (Byte 16) must be the length of the string in bytes, the second must be 0x03, and the string must be in ASCII code.” below “Vendor string”, “Product string” and “Serial Number string”. Updated **Functional overview**: Updated **Overcurrent detection**: Included text “OVR#[n] has a setup time of 20 ns. It takes 3 to 4 ms from overcurrent detection to de-assertion of PWR#[n].”. Completing Sunset Review.
*F	2012-07-02	Updated **EEPROM Configuration options**: Changed the value of Byte 5 to FEh to match with the tabular column. Updated **Electrical characteristics**: Updated **DC electrical characteristics**: Splitted the Max column into two columns namely External regulator and Internal regulator for I_{SUSP} and I_{CC} parameters and updated the corresponding values. Added **Thermal resistance**. Updated to new template.
*G	2013-05-09	Added **Silicon Errata for the HX2VL, CY7C65632 product family**.

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Revision history

Document revision	Date	Description of changes
*H	2015-02-17	Added **More information**. Updated **Functional overview**: Updated **Port indicators**: Updated description. Updated **Pin definitions** (for 48-pin TQFP package): Replaced “Active LOW” with “Active HIGH” in “Description” column corresponding to pin numbers 46, 45, 36, 35, 33, 32, 24, 23 (as LEDs are active HIGH by default). Added Note **2** and referred the same note in “Name” column corresponding to pin numbers 46, 45, 36, 35, 33, 32, 24, 23. Updated **Pin definitions** (for 28-pin QFN package): Added Note **4** and referred the same note in “Name” column corresponding to pin number 23. Updated **Electrical characteristics**: Updated **DC electrical characteristics**: Updated all values corresponding to R_{DN} and R_{DUP} parameters. Added Note **6** and **7** and referred the same notes in “Description” column corresponding to I_{CC} parameter (for Active ports and No active ports). Updated **Package diagrams**: spec 51-85135 – Changed revision from *B to *C. spec 001-64621 – Changed revision from ** to *A. Updated **Silicon Errata for the HX2VL, CY7C65632 product family**: Updated **HX2VL Qualification status**: Changed Product Status from “Sampling” to “In production”. Completing Sunset Review.
*I	2016-07-21	Updated **Features**: Updated description. Updated **Pin definitions** (for 28-pin QFN package): Updated details in “Description” column corresponding to OVR#[1], OVR#[2], OVR#[3], and OVR#[4] pins. Updated to new template.
*J	2016-12-07	Updated **More information**: Updated description. Updated to new template.
*K	2017-05-05	Updated Cypress Logo and Copyright.
*L	2018-04-13	Updated **Pin configurations**: Updated **Figure 4** (Removed old Cypress Logo). Updated **Figure 5** (Removed old Cypress Logo). Updated **Figure 6** (Removed old Cypress Logo). Updated **Figure 7** (Removed old Cypress Logo). Updated **Silicon Errata for the HX2VL, CY7C65632 product family**: Updated **HX2VL Errata summary**: Updated description. Updated to new template.
*M	2021-05-20	Added watermark “Not Recommended for New Designs” across the document. Updated to new template.
*N	2023-02-13	Removed watermark “Not Recommended for New Designs” across the document. Updated hyperlinks across the document. Migrated to Infineon template. Completing Sunset Review.

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