chanhvinh.com

Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

chanhvinh.com

CYPRESS
EMBEDDED IN TOMORROW™

CY22150

One-PLL General-Purpose Flash-Programmable and I²C Programmable Clock Generator

Features

- Integrated phase-locked loop (PLL)
- Commercial and industrial operation
- Flash programmable
- Field programmable
- Two-wire I²C interface
- Low skew, low jitter, high accuracy outputs
- 3.3 V operation with 2.5 V output option
- 16-pin TSSOP

Benefits

- Internal PLL to generate six outputs up to 200 MHz. Able to generate custom frequencies from an external crystal or a driven source.
- Performance guaranteed for applications that require an extended temperature range.
- Nonvolatile reprogrammable technology allows easy customization, quick turnaround on design changes and product performance enhancements, and better inventory control. Parts can be reprogrammed up to 100 times, reducing inventory of custom parts and providing an easy method for upgrading existing designs.
- The CY22150 can be programmed at the package level. In-house programming of samples and prototype quantities is available using the CY3672 Development Kit. Production quantities are available through Cypress's value added distribution partners or by using third party programmers from BP Microsystems™, HiLo Systems™, and others.
- The CY22150 provides an industry standard interface for volatile, system level customization of unique frequencies and options. Serial programming and reprogramming allows quick design changes and product enhancements, eliminates inventory of old design parts, and simplifies manufacturing.
- High performance suited for commercial, industrial, networking, telecom, and other general purpose applications.
- Application compatibility in standard and low power systems.
- Industry standard packaging saves on board space.

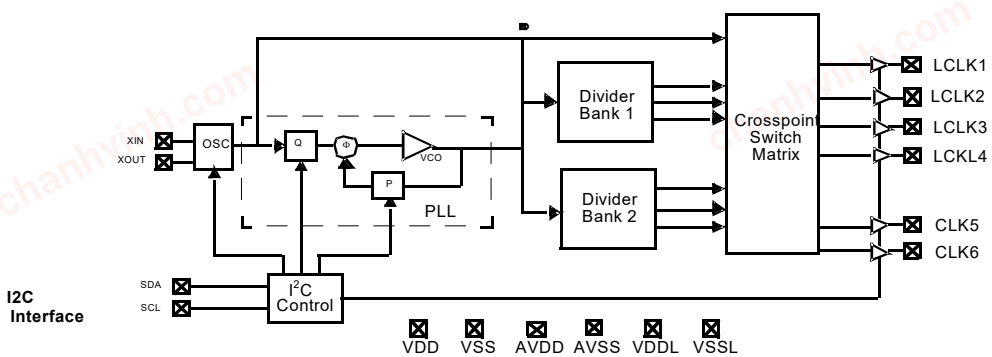
Functional Description

For a complete list of related documentation, click here.

Selection Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifications
CY22150KFZXC	6	8 MHz to 30 MHz (external crystal) 1 MHz to 133 MHz (driven clock)	80 kHz to 200 MHz (3.3 V) 80 kHz to 166.6 MHz (2.5 V)	Field programmable Serially programmable Commercial temperature
CY22150KFZXI	6	8 MHz to 30 MHz (external crystal) 1 MHz to 133 MHz (driven clock)	80 kHz to 166.6 MHz (3.3 V) 80 kHz to 150 MHz (2.5 V)	Field programmable Serially programmable Industrial temperature

Logic Block Diagram



chanhvinh.com

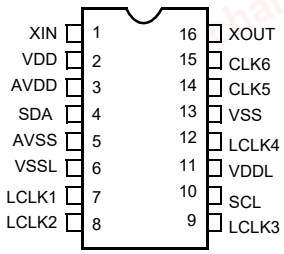
Contents

Pin Configuration **3**
Pin Definitions **3**
Functional Overview **4**
Frequency Calculation and Register Definitions 4
Default Startup Condition for the CY22150 5
Frequency Calculations and Register Definitions using the I2C Interface 5
I2C Interface Timing 9
Serial Bus specifications **11**
Applications **12**
Controlling Jitter 12
Test Circuit **12**
Absolute Maximum Conditions **13**
Recommended Operating Conditions **13**
DC Electrical Characteristics **14**
Device Characteristics **14**
AC Electrical Characteristics **15**
Ordering Information **17**
Possible Configurations 17
Ordering Code Definitions 17
Package Diagram **18**
Acronyms **19**
Document Conventions **19**
Units of Measure 19
Document History Page **20**
Sales, Solutions, and Legal Information **23**
Worldwide Sales and Design Support 23
Products 23
PSoC® Solutions 23
Cypress Developer Community 23
Technical Support 23

chanhvinh.com

Pin Configuration

Figure 1. 16-pin TSSOP pinout



Pin Definitions

Pin Name	Pin Number	Description
XIN	1	Reference Input. Driven by a crystal (8 MHz to 30 MHz) or external clock (1 MHz to 133 MHz). Programmable input load capacitors allow for maximum flexibility in selecting a crystal, regardless of manufacturer, process, performance, or quality
VDD	2	3.3 V Voltage Supply
AVDD	3	3.3 V Analog Voltage Supply
SDA	4	I^2C Serial Data Input/Output
AVSS	5	Analog Ground
VSSL	6	LCLK Ground
LCLK1	7	Configurable Clock Output 1 at V_{DDL} level (3.3 V or 2.5 V)
LCLK2	8	Configurable Clock Output 2 at V_{DDL} level (3.3 V or 2.5 V)
LCLK3	9	Configurable Clock Output 3 at V_{DDL} level (3.3 V or 2.5 V)
SCL	10	I^2C Serial Clock Input
VDDL	11	LCLK Voltage Supply (2.5 V or 3.3 V)
LCLK4	12	Configurable Clock Output 4 at V_{DDL} level (3.3 V or 2.5 V)
VSS	13	Ground
CLK5	14	Configurable Clock Output 5 (3.3 V)
CLK6	15	Configurable Clock Output 6 (3.3 V)
XOUT [1]	16	Reference Output

Note
1. Float XOUT if XIN is driven by an external clock source.

chanhvinh.com

Functional Overview

Frequency Calculation and Register Definitions

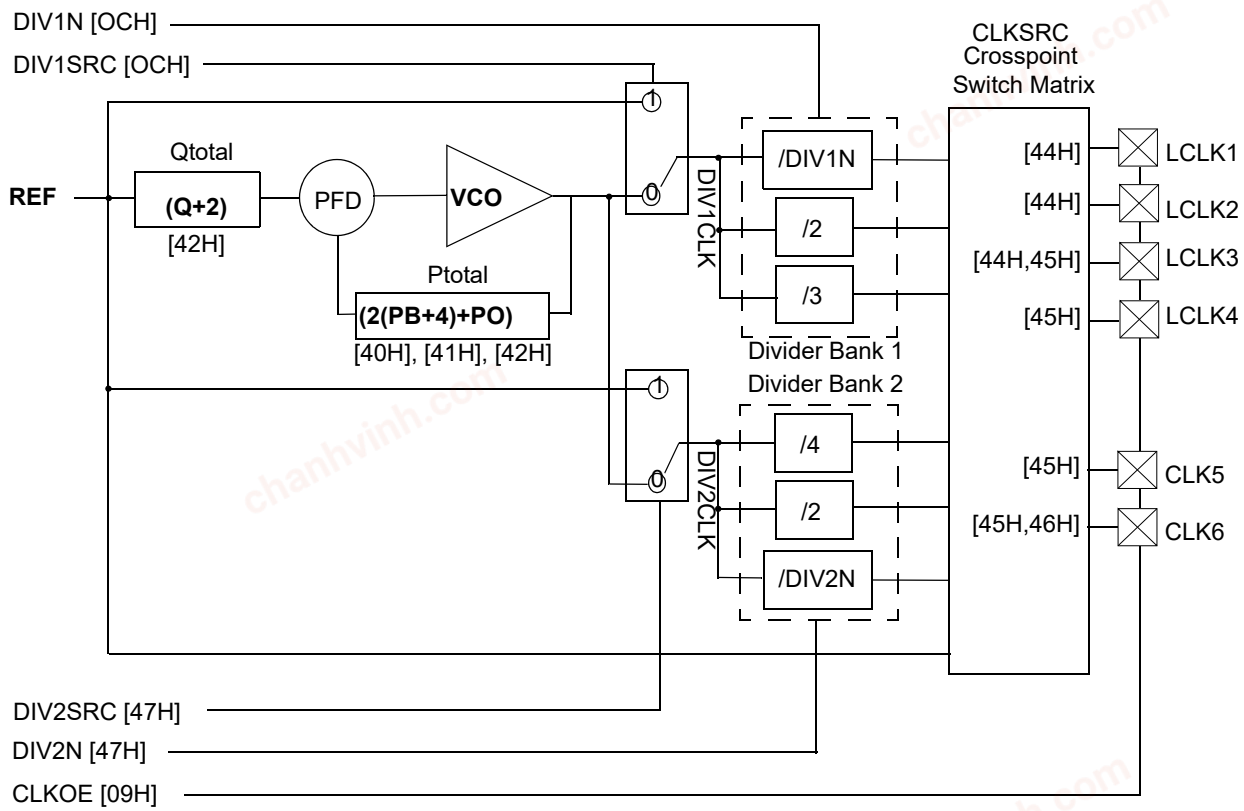
The CY22150 is an extremely flexible clock generator with four basic variables that are used to determine the final output frequency. They are the input reference frequency (REF), the internally calculated P and Q dividers, and the post divider, which can be a fixed or calculated value. There are three formulas to determine the final output frequency of a CY22150 based design:

- CLK = ((REF * P)/Q)/Post Divider
- CLK = REF/Post Divider
- CLK = REF.

The basic PLL block diagram is shown in Figure 2. Each of the six clock outputs on the CY22150 has a total of seven output options available to it. There are six post divider options available: /2 (two of these), /3, /4, /DIV1N and /DIV2N. DIV1N and DIV2N are independently calculated and are applied to individual output groups. The post divider options can be applied to the calculated VCO frequency ((REF*P)/Q) or to the REF directly.

In addition to the six post divider output options, the seventh option bypasses the PLL and passes the REF directly to the crosspoint switch matrix.

Figure 2. Basic Block Diagram of CY22150 PLL



chanhvinh.com

Default Startup Condition for the CY22150

The default (programmed) condition of the device is generally set by the distributor who programs the device using a customer specific JEDEC file produced by CyClocksRT™. Parts shipped from the factory are blank and unprogrammed. In this condition, all bits are set as default settings, all outputs are three-stated, and the crystal oscillator circuit is active.

While you can develop your own subroutine to program any or all of the individual registers described in the following pages, it may be easier to use CyClocksRT to produce the required register setting file.

The serial interface address of the CY22150 is 69H. If there is a conflict with any other devices in your system, then this can also be changed using CyClocksRT.

Frequency Calculations and Register Definitions using the I²C Interface

The CY22150 provides an industry standard serial interface for volatile, in-system programming of unique frequencies and options. Serial programming and re-programming allows for quick design changes and product enhancements, eliminates inventory of old design parts, and simplifies manufacturing.

The I²C Interface provides volatile programming. This means when the target system is powered down, the CY22150 reverts to its pre-I²C state, as defined above (programmed or unprogrammed). When the system is powered back up again, the I²C registers must be reconfigured again.

All programmable registers in the CY22150 are addressed with eight bits and contain eight bits of data. The CY22150 is a slave device with an address of 1101001 (69H).

Table 1 lists the I²C registers and their definitions. Specific register definitions and their allowable values are listed below.

Table 1. Summary Table – CY22150 Programmable Registers

Register	Description	D7	D6	D5	D4	D3	D2	D1	D0
09H	CLKOE control	0	0	CLK6	CLK5	LCLK4	LCLK3	LCLK2	LCLK1
OCH	DIV1SRC mux and DIV1N divider	DIV1SRC	DIV1N(6)	DIV1N(5)	DIV1N(4)	DIV1N(3)	DIV1N(2)	DIV1N(1)	DIV1N(0)
12H	Input crystal oscillator drive control	0	0	1	XDRV(1)	XDRV(0)	0	0	0
13H	Input load capacitor control	CapLoad (7)	CapLoad (6)	CapLoad (5)	CapLoad (4)	CapLoad (3)	CapLoad (2)	CapLoad (1)	CapLoad (0)
40H	Charge pump and PB counter	1	1	0	Pump(2)	Pump(1)	Pump(0)	PB(9)	PB(8)
41H		PB(7)	PB(6)	PB(5)	PB(4)	PB(3)	PB(2)	PB(1)	PB(0)
42H	PO counter, Q counter	PO	Q(6)	Q(5)	Q(4)	Q(3)	Q(2)	Q(1)	Q(0)
44H	Crosspoint switch matrix control	CLKSRC2 for LCLK1	CLKSRC1 for LCLK1	CLKSRC0 for LCLK1	CLKSRC2 for LCLK2	CLKSRC1 for LCLK2	CLKSRC0 for LCLK2	CLKSRC2 for LCLK3	CLKSRC1 for LCLK3
45H		CLKSRC0 for LCLK3	CLKSRC2 for LCLK4	CLKSRC1 for LCLK4	CLKSRC0 for LCLK4	CLKSRC2 for CLK5	CLKSRC1 for CLK5	CLKSRC0 for CLK5	CLKSRC2 for CLK6
46H		CLKSRC1 for CLK6	CLKSRC0 for CLK6	1	1	1	1	1	1
47H	DIV2SRC mux and DIV2N divider	DIV2SRC	DIV2N(6)	DIV2N(5)	DIV2N(4)	DIV2N(3)	DIV2N(2)	DIV2N(1)	DIV2N(0)

Reference Frequency

The REF can be a crystal or a driven frequency. For crystals, the frequency range must be between 8 MHz and 30 MHz. For a driven frequency, the frequency range must be between 1 MHz and 133 MHz.

Using a Crystal as the Reference Input:

The input crystal oscillator of the CY22150 is an important feature because of the flexibility it allows the user in selecting a crystal as a REF source. The input oscillator has programmable gain, allowing maximum compatibility with a reference crystal, regardless of manufacturer, process, performance, and quality.

Programmable Crystal Input Oscillator Gain Settings:

The Input crystal oscillator gain (XDRV) is controlled by two bits in register 12H and are set according to Table 2 on page 6. The parameters controlling the gain are the crystal frequency, the internal crystal parasitic resistance (ESR, available from the manufacturer), and the CapLoad setting during crystal startup.

Bits 3 and 4 of register 12H control the input crystal oscillator gain setting. Bit 4 is the MSB of the setting, and bit 3 is the LSB. The setting is programmed according to Table 2 on page 6. All other bits in the register are reserved and should be programmed as shown in Table 3 on page 6.

Using an External Clock as the Reference Input:

The CY22150 also accepts an external clock as reference, with speeds up to 133 MHz. With an external clock, the XDRV (register 12H) bits must be set according to Table 4 on page 6.

chanhvinh.com

Table 2. Programmable Crystal Input Oscillator Gain Settings

	Cap Register Settings	00H–80H		80H–C0H		C0H–FFH	
	Effective Load Capacitance (CapLoad)	6 pF to 12 pF		12 pF to 18 pF		18 pF to 30 pF	
	Crystal ESR	30 Ω	60 Ω	30 Ω	60 Ω	30 Ω	60 Ω
Crystal Input Frequency	8 to 15 MHz	00	01	01	10	01	10
	15 to 20 MHz	01	10	01	10	10	10
	20 to 25 MHz	01	10	10	10	10	11
	25 to 30 MHz	10	10	10	11	11	N/A

Table 3. Crystal Oscillator Gain Bit Locations and Values

Address	D7	D6	D5	D4	D3	D2	D1	D0
12H	0	0	1	XDRV(1)	XDRV(0)	0	0	0

Table 4. Programmable External Reference Input Oscillator Drive Settings

Reference Frequency	1 to 25 MHz	25 to 50 MHz	50 to 90 MHz	90 to 133 MHz
Drive Setting	00	01	10	11

Input Load Capacitors:

Input load capacitors allow the user to set the load capacitance of the CY22150 to match the input load capacitance from a crystal. The value of the input load capacitors is determined by 8 bits in a programmable register [13H]. Total load capacitance is determined by the formula:

$CapLoad = (C_L - C_{BRD} - C_{CHIP})/0.09375\ pF$

where:

- C_L = specified load capacitance of your crystal.
- C_{BRD} = the total board capacitance, due to external capacitors and board trace capacitance. In CyClocksRT, this value defaults to 2 pF.
- C_{CHIP} = 6 pF.
- 0.09375 pF = the step resolution available due to the 8-bit register.

In CyclocksRT, only the crystal capacitance (C_L) is specified. C_{CHIP} is set to 6 pF and C_{BRD} defaults to 2 pF. If your board capacitance is higher or lower than 2 pF, the formula given earlier is used to calculate a new CapLoad value and programmed into register 13H.

In CyClocksRT, enter the crystal capacitance (C_L). The value of CapLoad is determined automatically and programmed into the CY22150. Through the SDA and SCL pins, the value can be adjusted up or down if your board capacitance is greater or less than 2 pF. For an external clock source, CapLoad defaults to 0. See Table 5 for CapLoad bit locations and values.

The input load capacitors are placed on the CY22150 die to reduce external component cost. These capacitors are true parallel-plate capacitors, designed to reduce the frequency shift that occurs when nonlinear load capacitance is affected by load, bias, supply, and temperature changes.

Table 5. Input Load Capacitor Register Bit Settings

Address	D7	D6	D5	D4	D3	D2	D1	D0
13H	CapLoad(7)	CapLoad(6)	CapLoad(5)	CapLoad(4)	CapLoad(3)	CapLoad(2)	CapLoad(1)	CapLoad(0)

chanhvinh.com

PLL Frequency, Q Counter [42H(6..0)]

The first counter is known as the Q counter. The Q counter divides REF by its calculated value. Q is a 7 bit divider with a maximum value of 127 and minimum value of 0. The primary value of Q is determined by 7 bits in register 42H (6..0), but 2 is added to this register value to achieve the total Q, or Q_{total}. Q_{total} is defined by the formula:

$Q_{total} = Q + 2$

The minimum value of Q_{total} is 2. The maximum value of Q_{total} is 129. Register 42H is defined in the table.

Stable operation of the CY22150 cannot be guaranteed if REF/Q_{total} falls below 250 kHz. Q_{total} bit locations and values are defined in Table 6.

Table 6. P Counter and Q Counter Register Definition

Address	D7	D6	D5	D4	D3	D2	D1	D0
40H	1	1	0	Pump(2)	Pump(1)	Pump(0)	**PB(9)**	**PB(8)**
41H	**PB(7)**	**PB(6)**	**PB(5)**	**PB(4)**	**PB(3)**	**PB(2)**	**PB(1)**	**PB(0)**
42H	**PO**	Q(6)	Q(5)	Q(4)	Q(3)	Q(2)	Q(1)	Q(0)

PLL Frequency, P Counter [40H(1..0)], [41H(7..0)], [42H(7)

The next counter definition is the P (product) counter. The P counter is multiplied with the (REF/Q_{total}) value to achieve the VCO frequency. The product counter, defined as P_{total}, is made up of two internal variables, PB and PO. The formula for calculating P_{total} is:

$P_{total} = (2(PB + 4) + PO)$

PB is a 10-bit variable, defined by registers 40H(1:0) and 41H(7:0). The 2 LSBs of register 40H are the two MSBs of variable PB. Bits 4..2 of register 40H are used to determine the charge pump settings. The 3 MSBs of register 40H are preset and reserved and cannot be changed. PO is a single bit variable, defined in register 42H(7). This allows for odd numbers in P_{total}.

The remaining seven bits of 42H are used to define the Q counter, as shown in Table 6.

The minimum value of P_{total} is 8. The maximum value of P_{total} is 2055. To achieve the minimum value of P_{total}, PB and PO should both be programmed to 0. To achieve the maximum value of P_{total}, PB should be programmed to 1023, and PO should be programmed to 1.

Stable operation of the CY22150 cannot be guaranteed if the value of (P_{total}*(REF/Q_{total})) is above 400 MHz or below 100 MHz.

PLL Post Divider Options [0CH(7..0)], [47H(7..0)]

The output of the VCO is routed through two independent muxes, then to two divider banks to determine the final clock output frequency. The mux determines if the clock signal feeding into the divider banks is the calculated VCO frequency or REF. There are two select muxes (DIV1SRC and DIV2SRC) and two divider banks (Divider Bank 1 and Divider Bank 2) used to determine this clock signal. The clock signal passing through DIV1SRC and DIV2SRC is referred to as DIV1CLK and DIV2CLK, respectively.

The divider banks have four unique divider options available: /2, /3, /4, and /DIVxN. DIVxN is a variable that can be independently programmed (DIV1N and DIV2N) for each of the two divider banks. The minimum value of DIVxN is 4. The maximum value of DIVxN is 127. A value of DIVxN below 4 is not guaranteed to work properly.

DIV1SRC is a single bit variable, controlled by register 0CH. The remaining seven bits of register 0CH determine the value of post divider DIV1N.

DIV2SRC is a single bit variable, controlled by register 47H. The remaining seven bits of register 47H determine the value of post divider DIV2N.

Register 0CH and 47H are defined in Table 7.

Table 7. PLL Post Divider Options

Address	D7	D6	D5	D4	D3	D2	D1	D0
0CH	DIV1SRC	DIV1N(6)	DIV1N(5)	DIV1N(4)	DIV1N(3)	DIV1N(2)	DIV1N(1)	DIV1N(0)
47H	DIV2SRC	DIV2N(6)	DIV2N(5)	DIV2N(4)	DIV2N(3)	DIV2N(2)	DIV2N(1)	DIV2N(0)

chanhvinh.com

Charge Pump Settings [40H(2..0)]

The correct pump setting is important for PLL stability. Charge pump settings are controlled by bits (4..2) of register 40H, and are dependent on internal variable PB (see "*PLL Frequency, P Counter[40H(1..0)], [41H(7..0)], [42H(7)]*"). Table 8 summarizes the proper charge pump settings, based on Ptotal.

See Table 9 for register 40H bit locations and values.

Table 8. Charge Pump Settings

Charge Pump Setting – Pump(2..0)	Calculated P_{total}
000	16–44
001	45–479
010	480–639
011	640–799
100	800–1023
101, 110, 111	Do not use – device will be unstable

Table 9. Register 40H Change Pump Bit Settings

Address	D7	D6	D5	D4	D3	D2	D1	D0
40H	1	1	0	Pump(2)	Pump(1)	Pump(0)	PB(9)	PB(8)

Although using the above table guarantees stability, it is recommended to use the Print Preview function in CyClocksRT to determine the correct charge pump settings for optimal jitter performance.

PLL stability cannot be guaranteed for values below 16 and above 1023. If values above 1023 are needed, use CyClocksRT to determine the best charge pump setting.

Clock Output Settings: CLKSRC – Clock Output Crosspoint Switch Matrix [44H(7..0)], [45H(7..0)], [46H(7..6)]

Every clock output can be defined to come from one of seven unique frequency sources. The CLKSRC(2..0) crosspoint switch matrix defines which source is attached to each individual clock output. CLKSRC(2..0) is set in Registers 44H, 45H, and 46H. The remainder of register 46H(5:0) must be written with the values stated in the register table when writing register values 46H(7:6).

When DIV1N is divisible by four, then CLKSRC(0,1,0) is guaranteed to be rising edge phase-aligned with CLKSRC(0,0,1). When DIV1N is six, then CLKSRC(0,1,1) is guaranteed to be rising edge phase-aligned with CLKSRC(0,0,1).

When DIV2N is divisible by four, then CLKSRC(1,0,1) is guaranteed to be rising edge phase-aligned with CLKSRC(1,0,0). When DIV2N is divisible by eight, then CLKSRC(1,1,0) is guaranteed to be rising edge phase-aligned with CLKSRC(1,0,0).

Table 10. Clock Output Setting

CLKSRC2	CLKSRC1	CLKSRC0	Definition and Notes
0	0	0	Reference input.
0	0	1	DIV1CLK/DIV1N. DIV1N is defined by register [OCH]. Allowable values for DIV1N are 4 to 127. If Divider Bank 1 is not being used, set DIV1N to 8.
0	1	0	DIV1CLK/2. Fixed /2 divider option. If this option is used, DIV1N must be divisible by 4.
0	1	1	DIV1CLK/3. Fixed /3 divider option. If this option is used, set DIV1N to 6.
1	0	0	DIV2CLK/DIV2N. DIV2N is defined by Register [47H]. Allowable values for DIV2N are 4 to 127. If Divider Bank 2 is not being used, set DIV2N to 8.
1	0	1	DIV2CLK/2. Fixed /2 divider option. If this option is used, DIV2N must be divisible by 4.
1	1	0	DIV2CLK/4. Fixed /4 divider option. If this option is used, DIV2N must be divisible by 8.
1	1	1	Reserved – do not use.

chanhvinh.com

CLKOE – Clock Output Enable Control [09H(5..0)]

Each clock output has its own output enable, controlled by register 09H(5..0). To enable an output, set the corresponding CLKOE bit to 1. CLKOE settings are in Table 11.

The output swing of LCLK1 through LCLK4 is set by V_{DDL}. The output swing of CLK5 and CLK6 is set by V_{DD}.

Table 11. CLKOE Bit Setting

Address	D7	D6	D5	D4	D3	D2	D1	D0
09H	0	0	CLK6	CLK5	LCLK4	LCLK3	LCLK2	LCLK1

Test, Reserved, and Blank Registers

Writing to any of the following registers causes the part to exhibit abnormal behavior, as follows.

[00H to 08H] – Reserved
[0AH to 0BH] – Reserved
[0DH to 11H] – Reserved
[14H to 3FH] – Reserved
[43H] – Reserved
[48H to FFH] – Reserved.

Table 12. Clock Output Register Setting

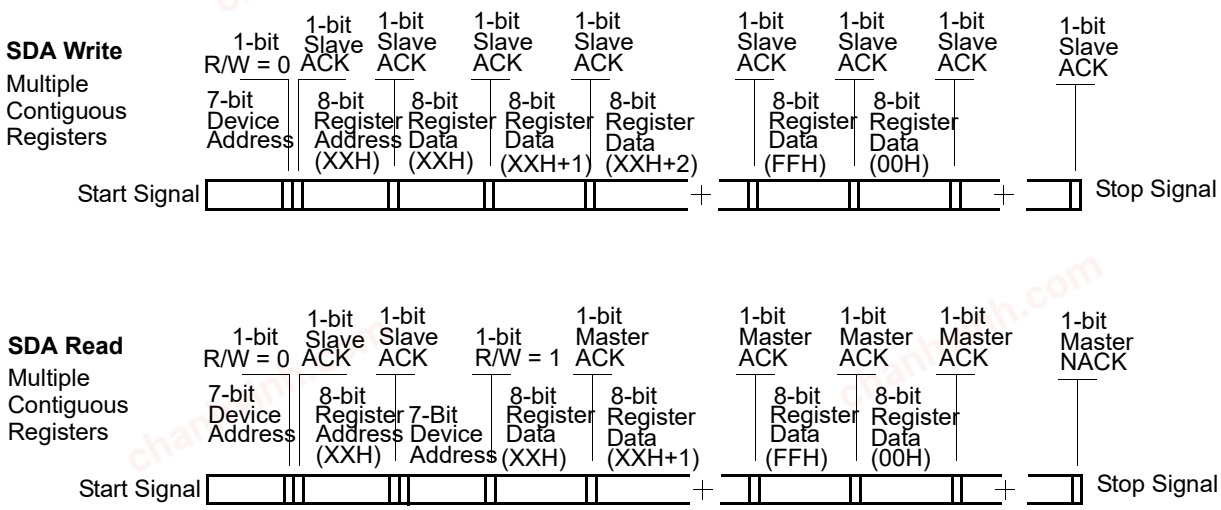
Address	D7	D6	D5	D4	D3	D2	D1	D0
44H	CLKSRC2 for LCLK1	CLKSRC1 for LCLK1	CLKSRC0 for LCLK1	CLKSRC2 for LCLK2	CLKSRC1 for LCLK2	CLKSRC0 for LCLK2	CLKSRC2 for LCLK3	CLKSRC1 for LCLK3
45H	CLKSRC0 for LCLK3	CLKSRC2 for LCLK4	CLKSRC1 for LCLK4	CLKSRC0 for LCLK4	CLKSRC2 for CLK5	CLKSRC1 for CLK5	CLKSRC0 for CLK5	CLKSRC2 for CLK6
46H	CLKSRC1 for CLK6	CLKSRC0 for CLK6	1	1	1	1	1	1

I²C Interface Timing

The CY22150 uses a two-wire I²C-interface that operates up to 400 kbits/second in Read or Write mode. The basic Write serial format is as follows.

Start Bit; seven-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); eight-bit Memory Address (MA); ACK; eight-bit data; ACK; eight-bit data in MA + 1 if desired; ACK; eight-bit data in MA+2; ACK; and so on until STOP bit.The basic serial format is illustrated in Figure 3.

Figure 3. Data Frame Architecture

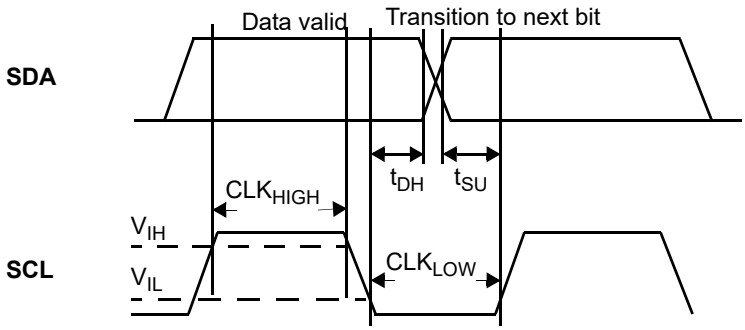


chanhvinh.com

Data Valid

Data is valid when the Clock is HIGH, and may only be transitioned when the clock is LOW, as illustrated in Figure 4.

Figure 4. Data Valid and Data Transition Periods



Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 5 on page 10.

Start Sequence – Start frame is indicated by SDA going LOW when SCL is HIGH. Every time a Start signal is given, the next eight-bit data must be the device address (seven bits) and a R/W bit, followed by register address (eight bits) and register data (eight bits).

Stop Sequence – Stop frame is indicated by SDA going HIGH when SCL is HIGH. A Stop frame frees the bus for writing to another part on the same bus or writing to another random register address.

Figure 5. Start and Stop Frame

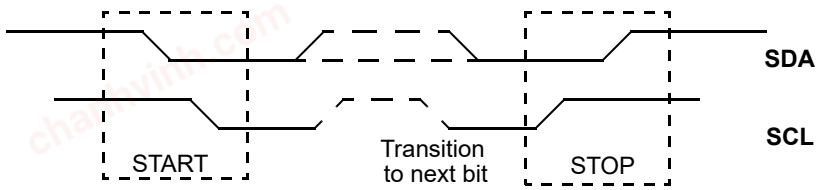
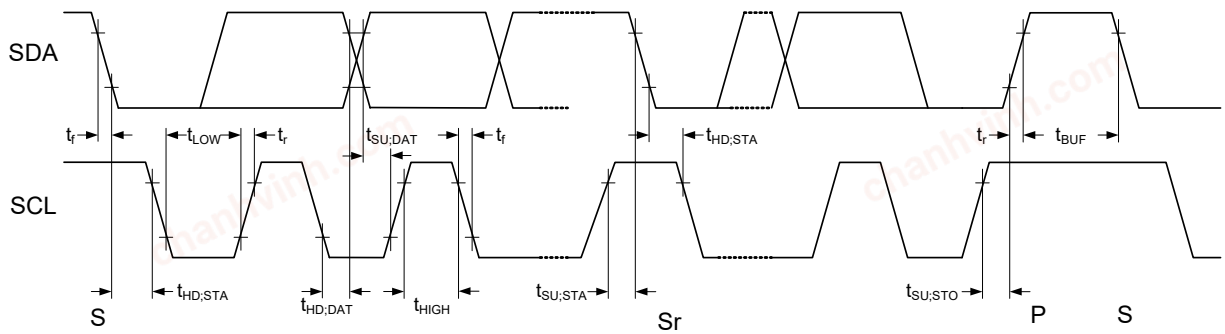


Figure 6. Definition for Timing on the Serial BUS

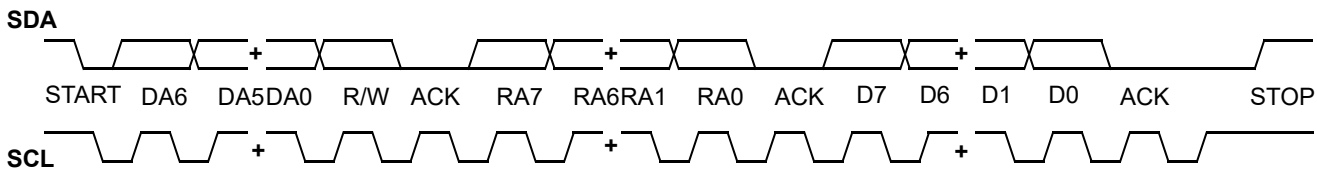


chanhvinh.com

Acknowledge Pulse

During Write mode, the CY22150 responds with an ACK pulse after every eight bits. This is accomplished by pulling the SDA line LOW during the N*9th clock cycle, as illustrated in Figure 7 on page 11. (N = the number of eight-bit segments transmitted.) During Read mode, the ACK pulse after the data packet is sent is generated by the master.

Figure 7. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Serial Bus specifications

Parameter	Description	Min	Max	Unit
f_{SCL}	Frequency of SCL	–	400	kHz
$t_{HD:STA}$	Hold time START condition	0.6	–	µs
t_{LOW}	Low period of the SCK clock	1.3	–	µs
t_{HIGH}	High period of the SCK clock	0.6	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition	0.6	–	µs
t_{DH}	Data hold (SCL LOW to data transition)	100	–	ns
$t_{HD:DAT}$	Data hold time	100	–	ns
$t_{SU:DAT}$	Data setup time	100	–	ns
t_R	Rise time	–	300	ns
t_F	Fall time	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition	0.6	–	µs
t_{BUF}	Bus-free time between STOP and START conditions	1.3	–	µs

chanhvinh.com

Applications

Controlling Jitter

Jitter is defined in many ways including: phase noise, long term jitter, cycle to cycle jitter, period jitter, absolute jitter, and deterministic. These jitter terms are usually given in terms of rms, peak to peak, or in the case of phase noise dBC/Hz with respect to the fundamental frequency.

Power supply noise and clock output loading are two major system sources of clock jitter. Power supply noise is mitigated by proper power supply decoupling (0.1 µF ceramic cap 0.25”) of the clock and ensuring a low impedance ground to the chip. Reducing capacitive clock output loading to a minimum lowers current spikes on the clock edges and thus reduces jitter.

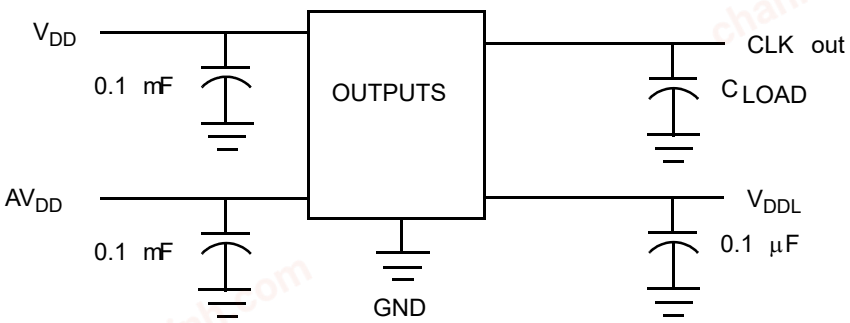
Reducing the total number of active outputs also reduce jitter in a linear fashion. However, it is better to use two outputs to drive two loads than one output to drive two loads.

The rate and magnitude that the PLL corrects the VCO frequency is directly related to jitter performance. If the rate is too slow, then long term jitter and phase noise is poor. Therefore, to improve long term jitter and phase noise, reducing Q to a minimum is advisable. This technique increases the speed of the Phase Frequency Detector which in turn drive the input voltage of the VCO. In a similar manner increasing P till the VCO is near its maximum rated speed also decreases long term jitter and phase noise. For example: Input Reference of 12 MHz; desired output frequency of 33.3 MHz. The following solution is possible: Set Q = 3, P = 25, Post Div = 3. However, the best jitter results is Q = 2, P = 50, Post Div = 9.

For more information, contact your local Cypress field applications engineer.

Test Circuit

Figure 8. Test Circuit



chanhvinh.com

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
V_{DDL}	I/O Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature [2]	–65	125	°C
T_J	Junction Temperature	–	125	°C
	Package Power Dissipation – Commercial Temperature	–	450	mW
	Package Power Dissipation – Industrial Temperature	–	380	mW
	Digital Inputs	AV_{SS} – 0.3	AV_{DD} + 0.3	V
	Digital Outputs Referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs Referred to V_{DDL}	V_{SS} – 0.3	V_{DDL} +0.3	V
ESD	Static Discharge Voltage per MIL-STD-833, Method 3015	–	2000	V

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
$VDDL_{HI}$[3]	Operating Voltage	3.135	3.3	3.465	V
$VDDL_{LO}$[3]	Operating Voltage	2.375	2.5	2.625	V
T_{AC}	Ambient Commercial Temp	0	–	70	°C
T_{AI}	Ambient Industrial Temp	–40	–	85	°C
C_{LOAD}	Max. Load Capacitance, V_{DD}/V_{DDL} = 3.3 V	–	–	15	pF
C_{LOAD}	Max. Load Capacitance, V_{DDL} = 2.5 V	–	–	15	pF
f_{REFD}	Driven REF	1	–	133	MHz
f_{REFC}	Crystal REF	8	–	30	MHz
t_{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Notes
2. Rated for 10 years.
3. V_{DDL} is only specified and characterized at 3.3 V ± 5% and 2.5 V ± 5%. V_{DDL} may be powered at any value between 3.465 V and 2.375 V.

chanhvinh.com

DC Electrical Characteristics

Parameter [4]	Description	Conditions	Min	Typ	Max	Unit
$I_{OH3.3}$	Output High Current	$V_{OH} = V_{DD} – 0.5$ V, $V_{DD}/V_{DDL} = 3.3$ V (sink)	12	24	–	mA
$I_{OL3.3}$	Output Low Current	$V_{OL} = 0.5$ V, $V_{DD}/V_{DDL} = 3.3$ V (source)	12	24	–	mA
$I_{OH2.5}$	Output High Current	$V_{OH} = V_{DDL} – 0.5$ V, $V_{DDL} = 2.5$ V (source)	8	16	–	mA
$I_{OL2.5}$	Output Low Current	$V_{OL} = 0.5$, $V_{DDL} = 2.5$ V (sink)	8	16	–	mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	–	–	V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–	–	0.3	V_{DD}
C_{IN}	Input Capacitance	SCL and SDA Pins	–	–	7	pF
I_{IZ}	Input Leakage Current	SCL and SDA Pins	–	5	–	µA
V_{HYS}	Hysteresis of Schmitt triggered inputs	SCL and SDA Pins	0.05	–	–	V_{DD}
I_{VDD} [5, 6]	Supply Current	AV_{DD}/V_{DD} Current	–	45	–	mA
$I_{VDDL3.3}$ [5, 6]	Supply Current	V_{DDL} Current ($V_{DDL} = 3.465$ V)	–	25	–	mA
$I_{VDDL2.5}$ [5, 6]	Supply Current	V_{DDL} Current ($V_{DDL} = 2.625$ V)	–	17	–	mA

Device Characteristics

Parameter	Description	Value	Unit
θ_{JA}	Theta JA	115	°C/W
Complexity	Transistor Count	74,600	Transistors

Notes
4. Not 100% tested.
5. I_{VDD} currents specified for two CLK outputs running at 125 MHz, two LCLK outputs running at 80 MHz, and two LCLK outputs running at 66.6 MHz.
6. Use CyClocksRT to calculate actual I_{VDD} and I_{VDDL} for specific output frequency configurations.

chanhvinh.com

AC Electrical Characteristics

Parameter [7]	Description	Conditions	Min	Typ	Max	Unit
t1	Output Frequency, Commercial Temperature	Clock output limit, 3.3 V	0.08 (80 kHz)	–	200	MHz
		Clock output limit, 2.5 V	0.08 (80 kHz)	–	166.6	MHz
	Output Frequency, Industrial Temperature	Clock output limit, 3.3 V	0.08 (80 kHz)	–	166.6	MHz
		Clock output limit, 2.5 V	0.08 (80 kHz)	–	150	MHz
$t2_{LO}$	Output Duty Cycle	Duty cycle is defined in Figure 9 on page 16; t1/t2, fOUT < 166 MHz, 50% of V_{DD}	45	50	55	%
$t2_{HI}$	Output Duty Cycle	Duty cycle is defined in Figure 9; t1/t2, fOUT > 166 MHz, 50% of V_{DD}	40	50	60	%
$t3_{LO}$	Rising Edge Slew Rate (V_{DDL} = 2.5 V)	Output clock rise time, 20% to 80% of V_{DDL}. Defined in Figure 10	0.6	1.2	–	V/ns
$t4_{LO}$	Falling Edge Slew Rate (V_{DDL} = 2.5 V)	Output dlock fall time, 80% to 20% of V_{DDL}. Defined in Figure 10	0.6	1.2	–	V/ns
$t3_{HI}$	Rising Edge Slew Rate (V_{DDL} = 3.3 V)	Output dlock rise time, 20% to 80% of V_{DD}/V_{DDL}. Defined in Figure 10	0.8	1.4	–	V/ns
$t4_{HI}$	Falling Edge Slew Rate (V_{DDL} = 3.3 V)	Output dlock fall time, 80% to 20% of V_{DD}/V_{DDL}. Defined in Figure 10	0.8	1.4	–	V/ns
t5[8]	Skew	Output-output skew between related outputs	–	–	250	ps
t6[9]	Clock Jitter	Peak-to-peak period jitter	–	250	–	ps
t10	PLL Lock Time		–	0.30	3	ms

Notes
7. Not 100% tested, guaranteed by design.
8. Skew value guaranteed when outputs are generated from the same divider bank. See Logic Block Diagram on page 1 for more information.
9. Jitter measurements vary. Actual jitter is dependent on XIN jitter and edge rate, number of active outputs, output frequencies, V_{DDL}, (2.5 V or 3.3 V jitter).

chanhvinh.com

Figure 9. Duty Cycle Definition; DC = t2/t1

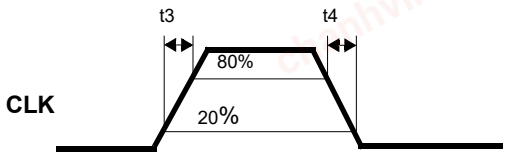


Figure 10. Rise and Fall Time Definitions

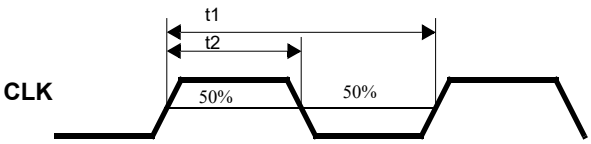
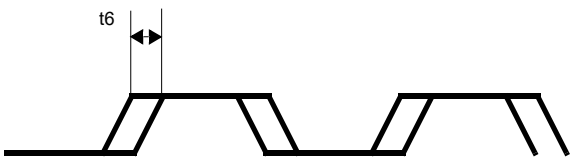


Figure 11. Peak-to-Peak Jitter



chanhvinh.com

Ordering Information

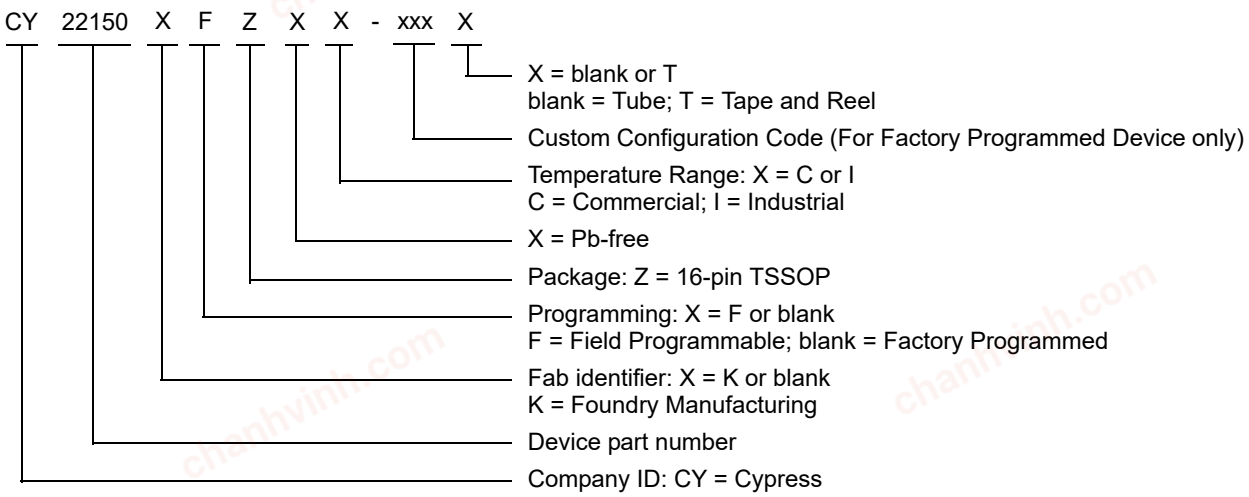
Ordering Code	Package Type	Operating Range	Operating Voltage
Pb-free			
CY22150KFZXC	16-pin TSSOP	Commercial (0 °C to 70 °C)	3.3 V
CY22150KFZXCT	16-pin TSSOP – Tape and Reel	Commercial (0 °C to 70 °C)	3.3 V
CY22150FZXC	16-pin TSSOP	Commercial (0 °C to 70 °C)	3.3 V
CY22150FZXCT	16-pin TSSOP – Tape and Reel	Commercial (0 °C to 70 °C)	3.3 V
CY22150FZXI	16-pin TSSOP	Industrial (–40 °C to 85 °C)	3.3 V
CY22150FZXIT	16-pin TSSOP – Tape and Reel	Industrial (–40 °C to 85 °C)	3.3 V
Programmer			
CY3672-USB	Programmer with USB interface		
CY3695	CY22150 Adapter Socket for CY3672-USB		

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

Possible Configurations

Ordering Code	Package Type	Operating Range	Operating Voltage
CY22150ZXC-xxx[10]	16-pin TSSOP	Commercial (0 °C to 70 °C)	3.3 V
CY22150ZXC-xxxT[10]	16-pin TSSOP – Tape and Reel	Commercial (0 °C to 70 °C)	3.3 V
CY22150ZXI-xxx[10]	16-pin TSSOP	Industrial (–40 °C to 85 °C)	3.3 V
CY22150ZXI-xxxT[10]	16-pin TSSOP – Tape and Reel	Industrial (–40 °C to 85 °C)	3.3 V

Ordering Code Definitions



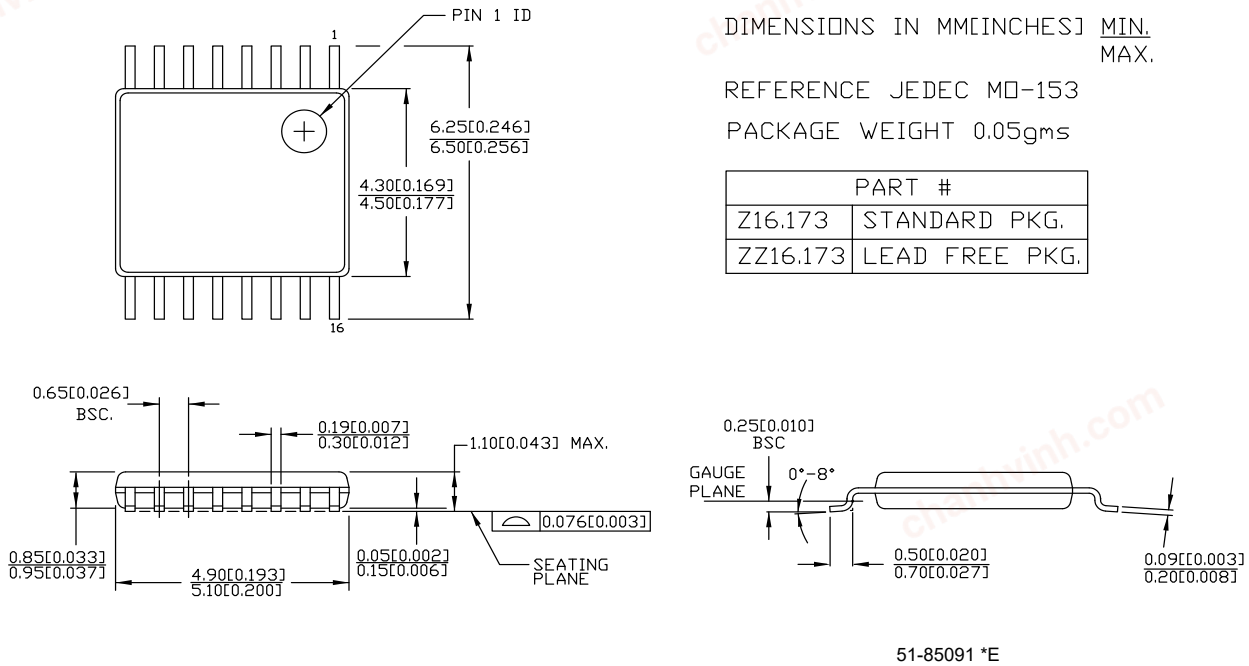
Notes

10. The CY22150ZC-xxx and CY22150ZI-xxx are factory programmed configurations. Factory programming is available for high volume design opportunities of 100 Ku/year or more in production. For more details, contact your local Cypress FAE or Cypress Sales Representative.

chanhvinh.com

Package Diagram

Figure 12. 16-pin TSSOP (4.40 mm Body) Package Outline, 51-85091



51-85091 *E

chanhvinh.com

Acronyms

Table 13. Acronyms Used in this Document

Acronym	Description	Acronym	Description
ACK	Acknowledge	LSB	Least Significant Bit
BSC	Basic Spacing between Centers	MA	Memory Address
CLKOE	Clock Output Enable	MSB	Most Significant Bit
CMOS	Complementary Metal Oxide Semiconductor	PFD	Phase Frequency Detector
DA	Device Address	PLL	Phase Locked Loop
ESD	Electrostatic Discharge	SCL	Serial interface Clock
ESR	Equivalent Series Resistance	SDA	Serial interface Data
FAE	Field Applications Engineer	TSSOP	Thin Shrunk Small Outline Package
I/O	Input / Output	USB	Universal Serial Bus
I2C	Inter Integrated Circuit	VCO	Voltage-Controlled Oscillator
JEDEC	Joint Electron Device Engineering Council		

Document Conventions

Units of Measure

Table 14. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µVrms	microvolts root-mean-square
dB	decibel	µW	microwatt
dBc/Hz	decibels relative to the carrier per Hertz	mA	milliampere
fC	femtocoulomb	mm	millimeter
fF	femtofarad	ms	millisecond
Hz	hertz	mV	millivolt
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nano volt
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolt	σ	sigma: one standard deviation

chanhvinh.com

Document History Page

Document Title: CY22150, One-PLL General-Purpose Flash-Programmable and I²C Programmable Clock Generator Document Number: 38-07104				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	107498	CKN	08/08/2001	New data sheet.
*A	110043	CKN	02/06/2002	Changed status from Preliminary to Final. Added Package Diagram.
*B	113514	CKN	05/01/2002	Updated Functional Overview: Updated I2C Interface Timing: Updated Acknowledge Pulse: Updated Figure 7 (Removed overline in “Register Address, Register Data” in caption). Updated Serial Bus specifications: Changed unit of CLK_{HIGH} parameter from ns to µs. Updated DC Electrical Characteristics: Updated details in “Description” column (Added (sink) at the end for $I_{OH3.3}$ and $I_{OL2.5}$ parameters, added (source) at the end for $I_{OL3.3}$ and $I_{OH2.5}$ parameters).
*C	121868	RBI	12/14/2002	Updated Absolute Maximum Conditions: Added t_{PU} parameter and its details.
*D	125453	CKN	05/19/2003	Updated Functional Overview: Updated Frequency Calculations and Register Definitions using the I2C Interface: Updated Table 1: Replaced 0 with 1 corresponding to D5 of 12H register. Updated Reference Frequency: Updated description (Reworded and reformatted Programmable Crystal Input Oscillator Gain Settings text). Updated Table 3: Replaced 0 with 1 corresponding to D5 of 12H register.
*E	242808	RGL	07/15/2004	Minor Change: Fixed the broken line in the block diagram
*F	252352	RGL	08/11/2004	Updated Functional Overview: Updated Frequency Calculations and Register Definitions using the I2C Interface: Updated Reference Frequency: Updated Table 2. Updated Package Diagram: spec 51-85091 – Changed revision from ** to *A.
*G	296084	RGL	12/06/2004	Updated Ordering Information: Updated part numbers (Added Pb-free devices).
*H	2440846	AESA	04/25/2008	Updated Ordering Information: Added Note “Not recommended for new designs.” Updated part numbers (Added part numbers CY22150KFC, CY22150KFCT, CY22150KFI, CY22150KFZXC, CY22150KFZXCT, CY22150KFZXI, CY22150KFZXIT, CY22150KZXI-xxxT, and CY22150KZI-xxxT). Replaced Lead Free with Pb-free. Updated to new template.
*I	2649578	KVM / PYRS	01/29/2009	Updated Ordering Information: Removed reference of Note “Not recommended for new designs” for the following parts: CY22150KFC, CY22150KFCT, CY22150KFI. Updated part numbers (Added CY22150KZI-xxx and removed CY22150ZC-xxx, CY22150ZC-xxxT and CY22150ZI-xxx). Replaced CY3672 with CY3672-USB, and moved to the bottom of the table.

chanhvinh.com

Document History Page (continued)

Document Title: CY22150, One-PLL General-Purpose Flash-Programmable and I²C Programmable Clock Generator Document Number: 38-07104				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	2900690	KVM	03/29/2010	Changed title from “One-PLL General-Purpose Flash-Programmable and 2-Wire Serially Programmable Clock Generator” to “One-PLL General-Purpose Flash-Programmable and I2C Programmable Clock Generator”. Updated Features: Replaced “Serial Programming Interface (SPI)” with “I2C Interface”. Updated Selection Guide. Updated Logic Block Diagram: Replaced “Serial Programming Interface (SPI)” with “I2C Interface”. Updated Ordering Information: Updated part numbers (Removed inactive parts). Added Possible Configurations. Updated Package Diagram: spec 51-85091 – Changed revision from *A to *B.
*K	3210225	CXQ	03/30/2011	Updated Functional Overview: Updated I2C Interface Timing: Updated Acknowledge Pulse: Updated Figure 7. Updated Serial Bus specifications: Changed minimum value of t_{DH} parameter from 0 ns to 100 ns. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagram: spec 51-85091 – Changed revision from *B to *C. Added Acronyms and Units of Measure. Completing Sunset Review.
*L	3402048	AJU	10/11/2011	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85091 – Changed revision from *C to *D.
*M	3846671	PURU	12/19/2012	Updated Ordering Information: Updated Possible Configurations: Updated part numbers (Removed all Non-K Devices and added K Devices).
*N	4379249	AJU	05/14/2014	Updated to new template. Completing Sunset Review.
*O	4575273	AJU	11/20/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagram: spec 51-85091 – Changed revision from *D to *E.
*P	5240950	TAVA	05/04/2016	Updated Functional Overview: Updated I2C Interface Timing: Updated Figure 3. Updated Data Frame: Added Figure 6. Updated Serial Bus specifications: Updated entire table. Updated Ordering Information: Updated Possible Configurations: Updated part numbers (Updated details in “Ordering Code” column). Updated to new template. Completing Sunset Review.

chanhvinh.com

Document History Page (continued)

Document Title: CY22150, One-PLL General-Purpose Flash-Programmable and I²C Programmable Clock Generator Document Number: 38-07104				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*Q	5747984	TAVA / PSR	05/25/2017	Replaced “SDAT” with “SDA” in all instances across the document. Replaced “SCLK” with “SCL” in all instances across the document. Updated Pin Definitions: Replaced “Input” with “Input/Output” in description column corresponding to “SDA” pin. Updated Functional Overview: Updated Default Startup Condition for the CY22150: Updated description. Updated Ordering Information: Updated part numbers. Updated to new template.
*R	6213085	XHT	06/20/2018	Updated to new template. Completing Sunset Review.

chanhvinh.com

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2001–2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

BP Microsystems is a trademark of BP Microsystems. HiLo Systems is a trademark of Hi-Lo Systems, Inc. CyClocks is a trademark of Cypress Semiconductor Corporation.