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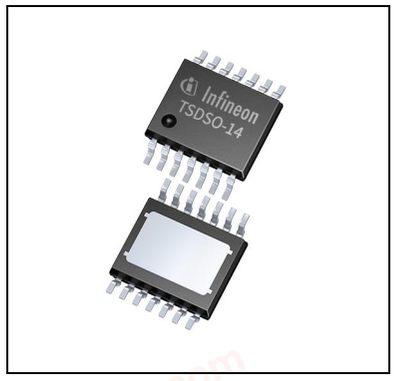
BTS7040-2EPA

PROFET™ +2 12V **2x 40 mΩ**

Smart High-Side Power Switch

AEC Qualified RoHS

Package	PG-TSDSO-14
Marking	7040-2A



1 Overview

Potential Applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Driving capability suitable for 3.5 A loads and high inrush current loads such as P27W + R5W lamps or equivalent electronic loads (e.g. LED modules)

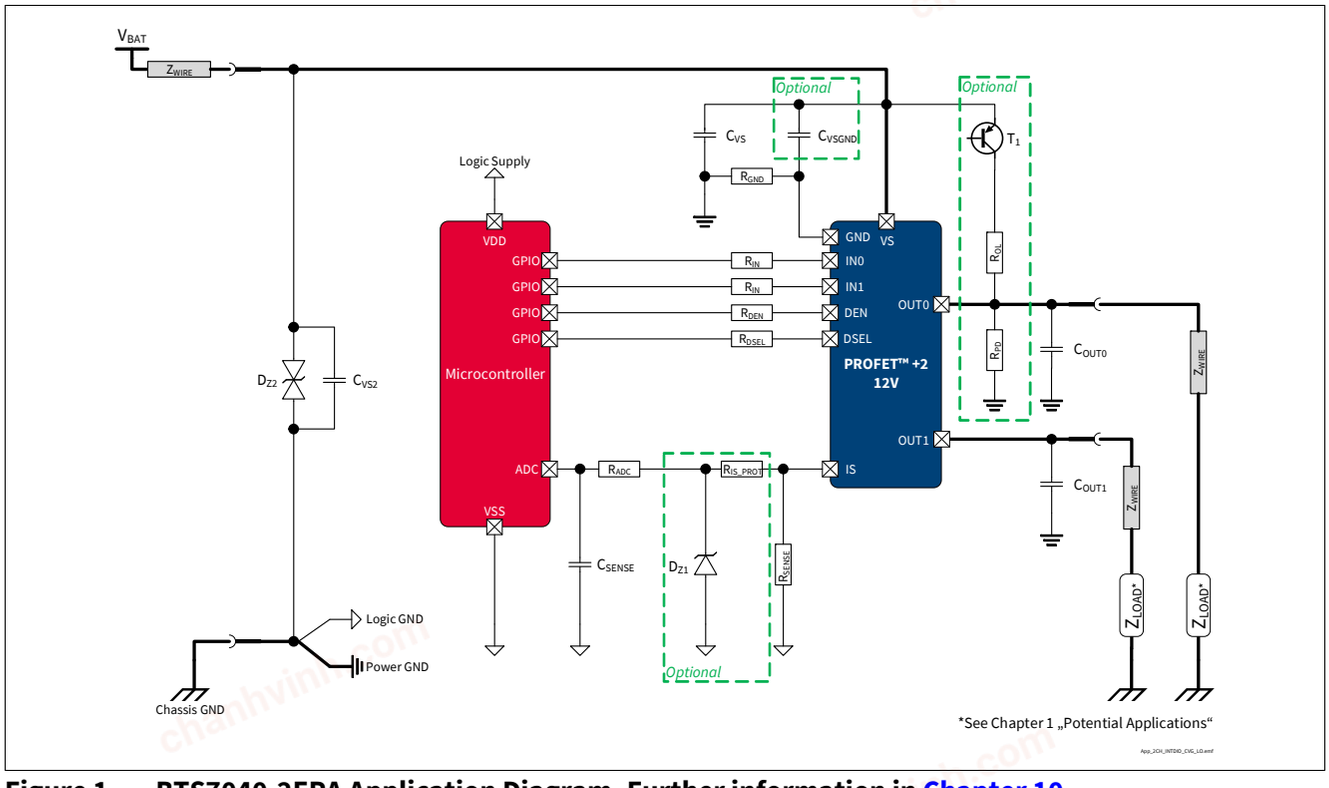


Figure 1 BTS7040-2EPA Application Diagram. Further information in Chapter 10

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Overview

Basic Features

- High-Side Switch with Diagnosis and Embedded Protection
- Part of PROFET™ +2 12V Family
- ReverseON for low power dissipation in Reverse Polarity
- Switch ON capability while Inverse Current condition (InverseON)
- Green Product (RoHS compliant)

Protection Features

- Absolute and dynamic temperature limitation with controlled restart
- Overcurrent protection (tripping) with Intelligent Restart Control
- Undervoltage shutdown
- Overvoltage protection with external components

Diagnostic Features

- Proportional load current sense
- Open Load in ON and OFF state
- Short circuit to ground and battery

Product Validation

Qualified for automotive applications. Product validation according to AEC-Q100 Grade 1.

Description

The BTS7040-2EPA is a Smart High-Side Power Switch, providing protection functions and diagnosis. The device is integrated in SMART7 technology.

Table 1 Product Summary

Parameter	Symbol	Values
Minimum Operating voltage (at switch ON)	$V_{S(OP)}$	4.1 V
Minimum Operating voltage (cranking)	$V_{S(UV)}$	3.1 V
Maximum Operating voltage	V_S	28 V
Minimum Overvoltage protection ($T_J \geq 25$ °C)	$V_{DS(CLAMP)_25}$	35 V
Maximum current in Sleep mode ($T_J \leq 85$ °C)	$I_{VS(SLEEP)_85}$	0.5 µA
Maximum operative current	$I_{GND(ACTIVE)}$	4 mA
Maximum ON-state resistance ($T_J = 150$ °C)	$R_{DS(ON)_150}$	36 mΩ
Nominal load current ($T_A = 85$ °C)	$I_{L(NOM)}$	3.5 A
Typical current sense ratio at $I_L = I_{L(NOM)}$	k_{ILIS}	1800

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2 Block Diagram and Terms

2.1 Block Diagram

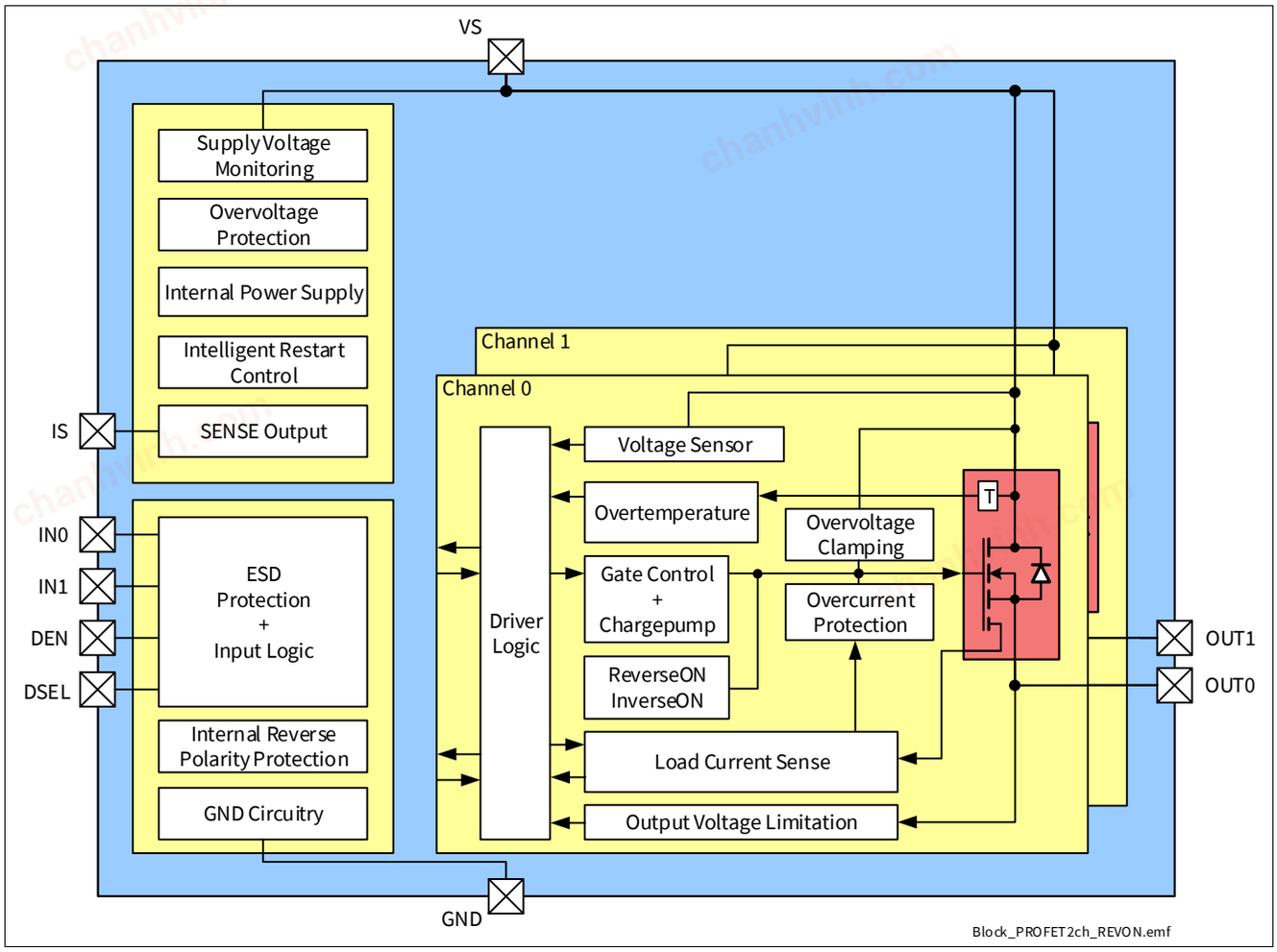


Figure 2 Block Diagram of BTS7040-2EPA

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2.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

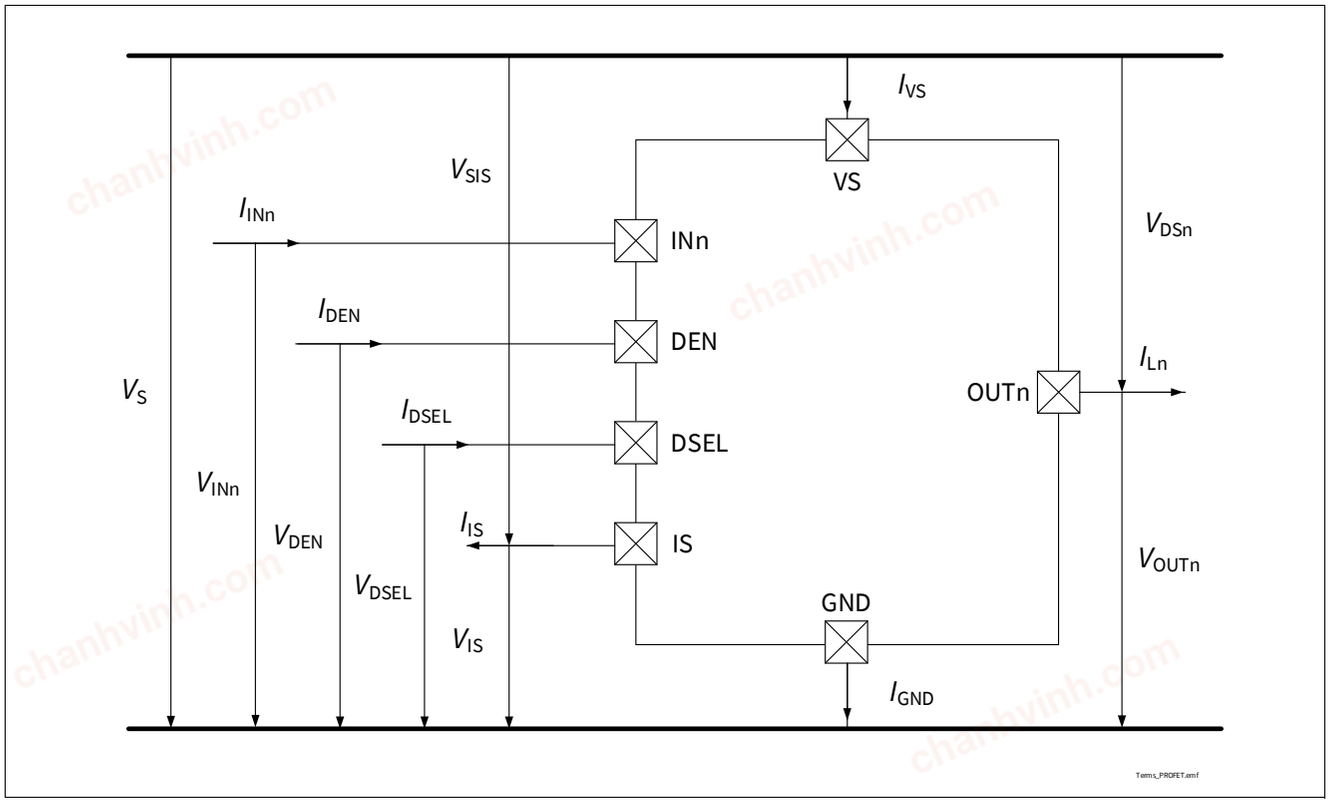


Figure 3 Voltage and Current Convention

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3 Pin Configuration

3.1 Pin Assignment

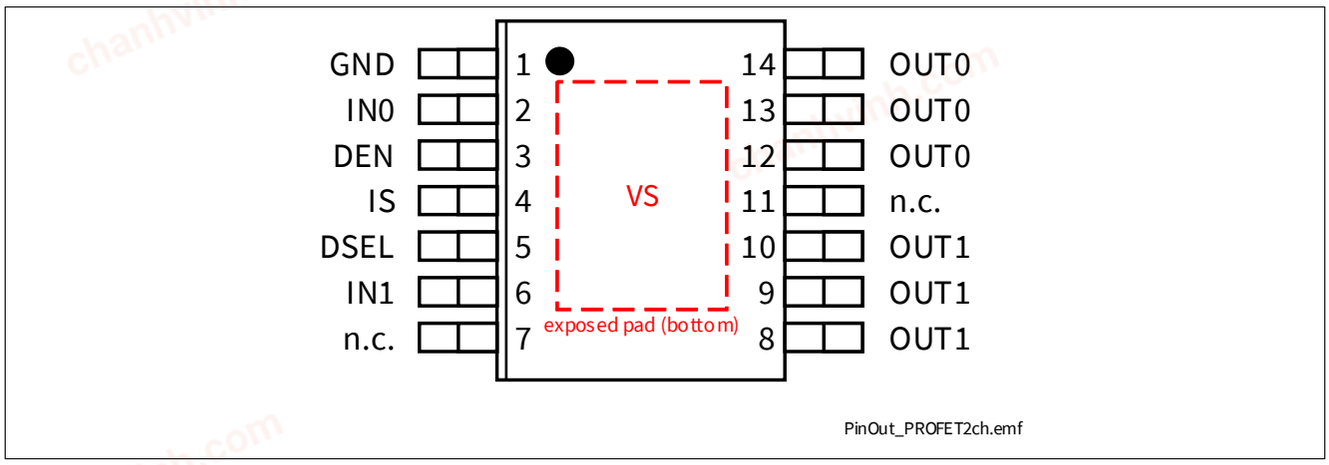


Figure 4 Pin Configuration

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3.2 Pin Definitions and Functions

Table 2 Pin Definition

Pin	Symbol	Function
EP	VS (exposed pad)	**Supply Voltage** Battery voltage
1	GND	**Ground** Signal ground
2, 6	INn	**Input Channel n** Digital signal to switch ON channel n (“high” active) If not used: connect with a 10 kΩ resistor either to GND pin or to module ground
3	DEN	**Diagnostic Enable** Digital signal to enable device diagnosis (“high” active) and to clear the protection counter of channel selected with DSEL pin If not used: connect with a 10 kΩ resistor either to GND pin or to module ground
4	IS	**SENSE current output** Analog/digital signal for diagnosis If not used: left open
5	DSEL	**Diagnosis Selection** Digital signal to select one channel to perform ON and OFF state diagnosis (“high” active) If not used: connect with a 10 kΩ resistor either to GND pin or to module ground
7, 11	n.c.	Not connected, internally not bonded
8-10, 12-14	OUTn	**Output n** Protected high-side power output channel n[1)]

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

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4 General Product Characteristics

4.1 Absolute Maximum Ratings - General

Table 3 Absolute Maximum Ratings[1)]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply pins							
Power Supply Voltage	V_S	-0.3	–	28	V	–	P_4.1.0.1
Load Dump Voltage	$V_{BAT(LD)}$	–	–	35	V	suppressed Load Dump acc. to ISO16750-2 (2010). R_i = 2 Ω	P_4.1.0.3
Supply Voltage for Short Circuit Protection	$V_{BAT(SC)}$	0	–	24	V	Setup acc. to AEC-Q100-012	P_4.1.0.25
Reverse Polarity Voltage	$-V_{BAT(REV)}$	–	–	16	V	$t \leq 2$ min T_A = +25 °C Setup as described in **Chapter 10**	P_4.1.0.5
Current through GND Pin	I_{GND}	-50	–	50	mA	R_{GND} according to **Chapter 10**	P_4.1.0.9
Logic & control pins (Digital Input = DI) DI = INn, DEN, DSEL							
Current through DI Pin	I_{DI}	-1	–	2	mA	2)	P_4.1.0.14
Current through DI Pin Reverse Battery Condition	$I_{DI(REV)}$	-1	–	10	mA	2) $t \leq 2$ min	P_4.1.0.36
IS pin							
Voltage at IS Pin	V_{IS}	-1.5	–	V_S	V	I_{IS} = 10 µA	P_4.1.0.16
Current through IS Pin	I_{IS}	-25	–	$I_{IS(SAT),MAX}$	mA	–	P_4.1.0.18
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_4.1.0.19
Storage Temperature	T_{STG}	-55	–	150	°C	–	P_4.1.0.20

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Table 3 Absolute Maximum Ratings[1)] (continued)

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD Susceptibility							
ESD Susceptibility all Pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	HBM[3)]	P_4.1.0.21
ESD Susceptibility OUTn vs GND and VS connected (HBM)	$V_{ESD(HBM)_OUT}$	-4	–	4	kV	HBM[3)]	P_4.1.0.22
ESD Susceptibility all Pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	CDM[4)]	P_4.1.0.23
ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	$V_{ESD(CDM)_CRN}$	-750	–	750	V	CDM[4)]	P_4.1.0.24

1) Not subject to production test - specified by design.
2) Maximum V_{DI} to be considered for Latch-Up tests: 5.5 V.
3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.
4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

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4.2 Absolute Maximum Ratings - Power Stages

4.2.1 Power Stage - 40 mΩ

Table 4 Absolute Maximum Ratings[1)]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum Energy Dissipation Single Pulse	E_{AS}	–	–	36	mJ	$I_L = 2*I_{L(NOM)}$ $T_{J(0)}$ = 150 °C V_S = 28 V	P_4.2.6.1
Maximum Energy Dissipation Repetitive Pulse	E_{AR}	–	–	13	mJ	$I_L = I_{L(NOM)}$ $T_{J(0)}$ = 85 °C V_S = 13.5 V 1M cycles	P_4.2.6.2
Load Current	$\|I_L\|$	–	–	$I_{L(OVL),MAX}$	A	–	P_4.2.6.3

1) Not subject to production test - specified by design.

4.3 Functional Range

Table 5 Functional Range - Supply Voltage and Temperature[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	6	13.5	18	V	–	P_4.3.0.1
Lower Extended Supply Voltage Range for Operation	$V_{S(EXT,LOW)}$	3.1	–	6	V	2)3) (parameter deviations possible)	P_4.3.0.2
Supply Voltage Range reached after Overload Protection activation leading to “Undervoltage on V_S” condition	$V_{S(EXT,CVG)}$	–	–	3.1	V	C_{VSGND} is required when the Overload Protection is triggered (see **Chapter 8.2**) and the observed number of retries is different from what specified in **Chapter 8.3.1**	P_4.3.0.7

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Table 5 Functional Range - Supply Voltage and Temperature[1)] (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Upper Extended Supply Voltage Range for Operation	$V_{S(EXT,UP)}$	18	–	28	V	[3)] (parameter deviations possible)	P_4.3.0.3
Junction Temperature	T_J	-40	–	150	°C	–	P_4.3.0.5

1) Not subject to production test - specified by design.
2) In case of V_S voltage decreasing: $V_{S(EXT,LOW),MIN}$ = 3.1 V. In case of V_S voltage increasing: $V_{S(EXT,LOW),MIN}$ = 4.1 V.
3) Protection functions still operative.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics tables.

4.4 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 6 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Characterization Parameter Junction-Top	Ψ_{JTOP}	–	2.4	4.1	K/W	[2)]	P_4.4.0.1
Thermal Resistance Junction-to-Case	R_{thJC}	–	1.6	2.7	K/W	[2)] simulated at exposed pad	P_4.4.0.2
Thermal Resistance Junction-to-Ambient	R_{thJA}	–	31.8	–	K/W	[2)]	P_4.4.0.3

1) Not subject to production test - specified by design.
2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_A = 105°C, $P_{DISSIPATION}$ = 1 W.

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4.4.1 PCB Setup

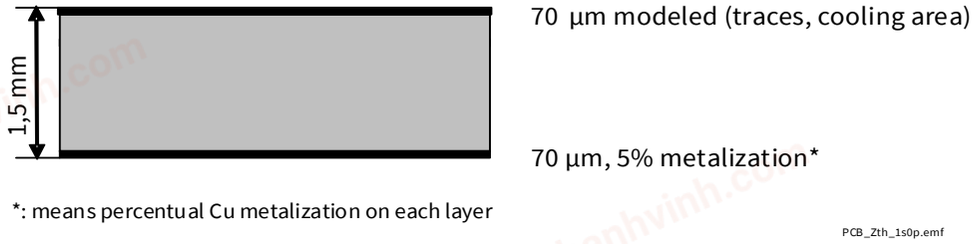


Figure 5 1s0p PCB Cross Section

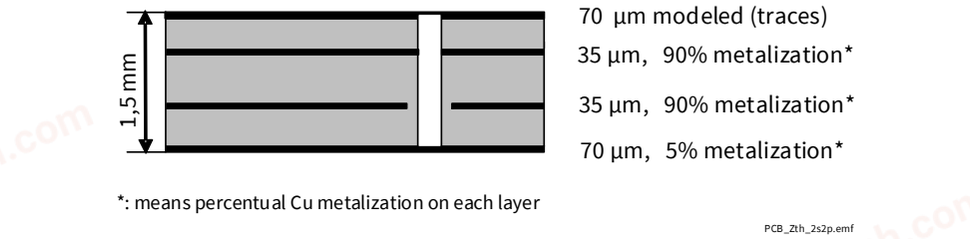


Figure 6 2s2p PCB Cross Section

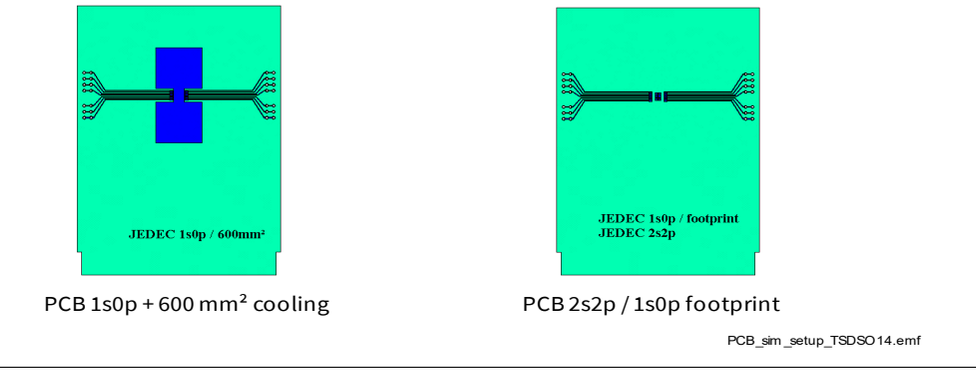


Figure 7 PCB setup for thermal simulations

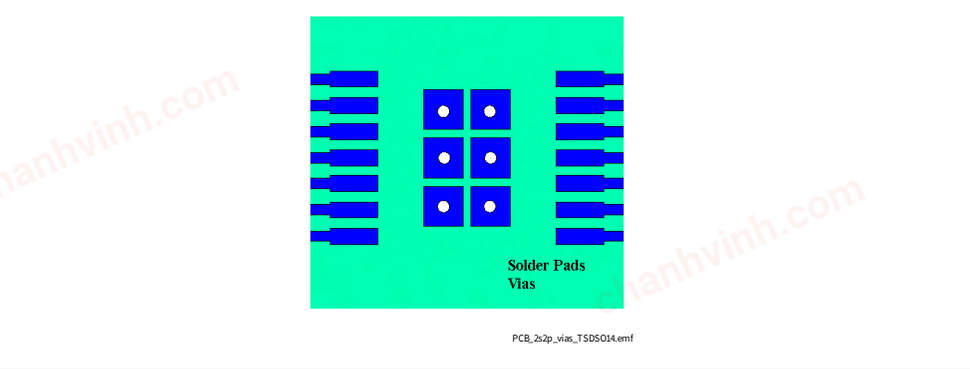


Figure 8 Thermal vias on PCB for 2s2p PCB setup

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4.4.2 Thermal Impedance

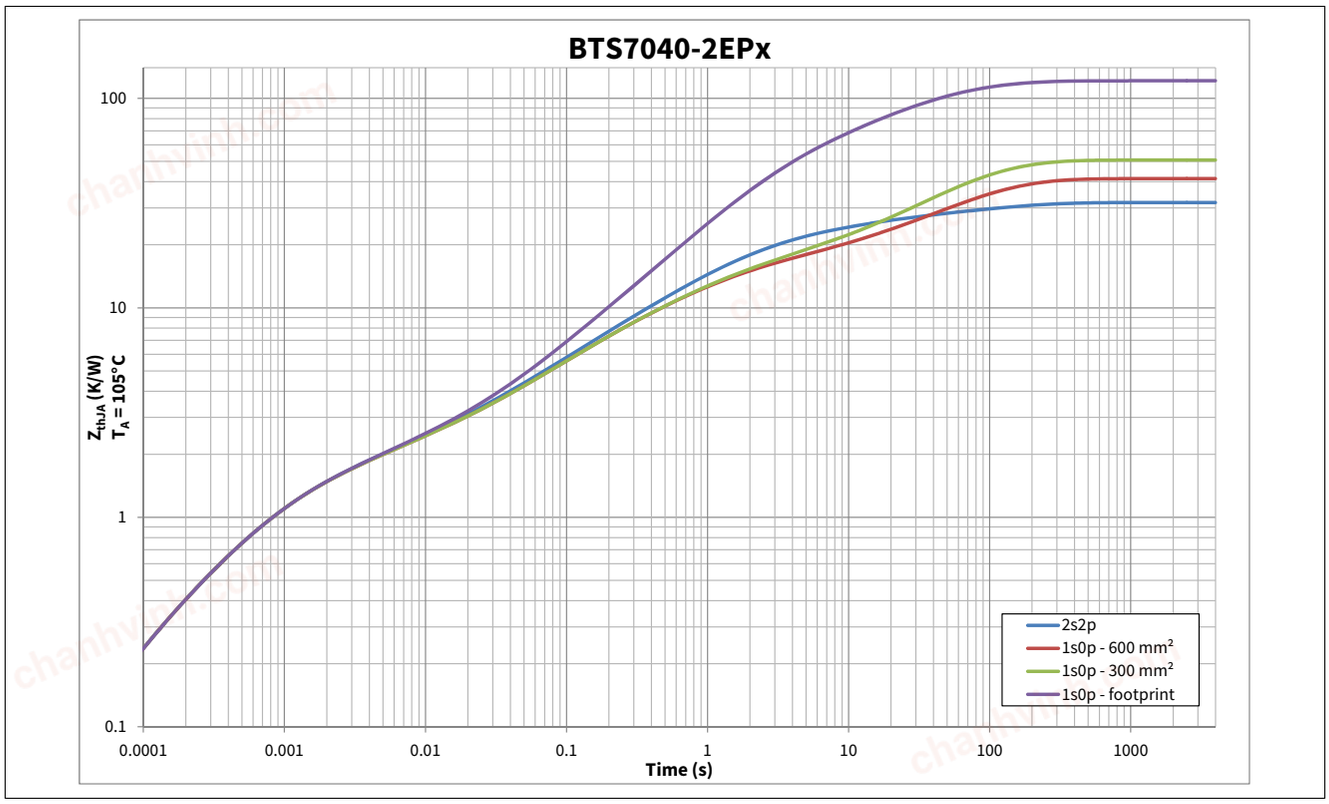


Figure 9 Typical Thermal Impedance. PCB setup according Chapter 4.4.1

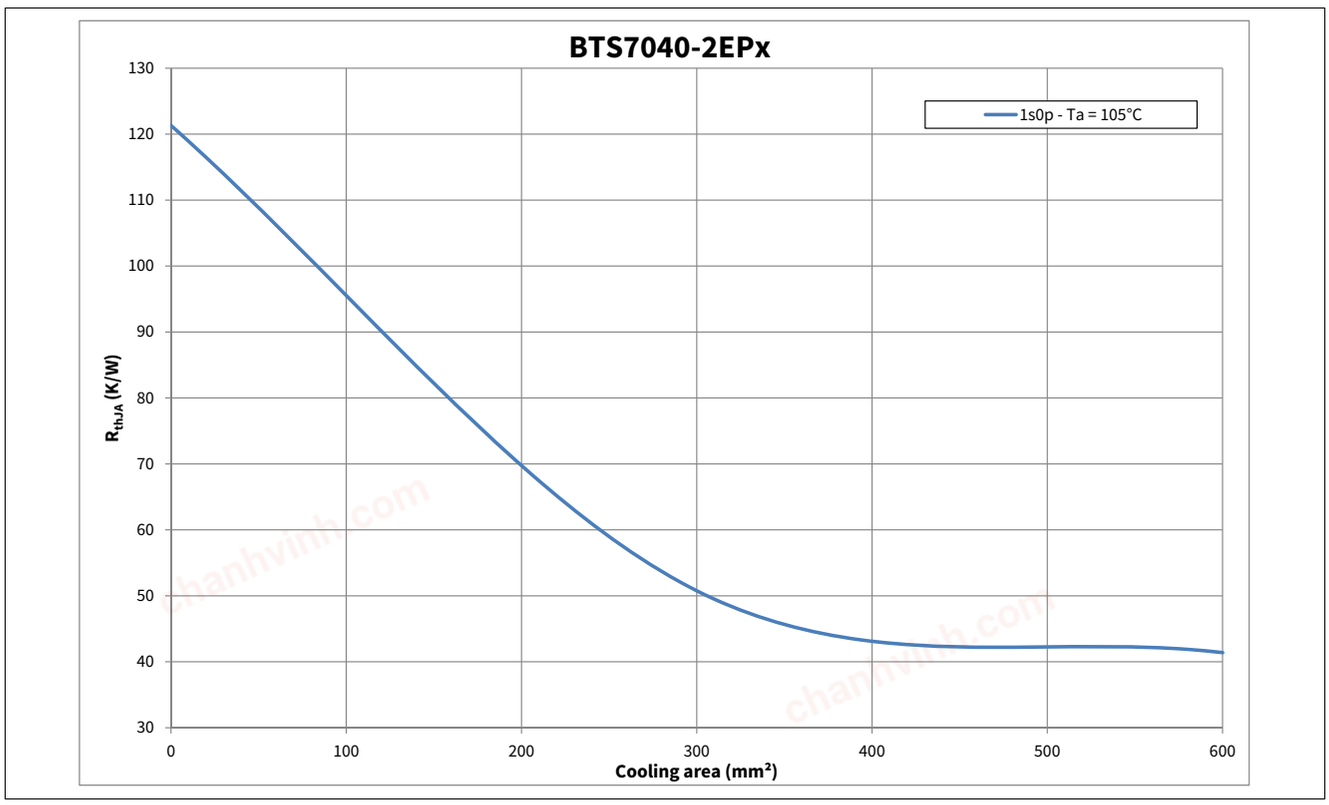


Figure 10 Thermal Resistance on 1s0p PCB with various cooling surfaces

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5 Logic Pins

The device has 4 digital pins for direct control.

5.1 Input Pins (INn)

The input pins IN0, IN1 activate the corresponding output channel. The input circuitry is compatible with 3.3V and 5V microcontroller (see **Chapter 10** for the complete application setup overview). The electrical equivalent of the input circuitry is shown in **Figure 11**. In case the pin is not used, it must be connected with a 10 kΩ resistor either to GND pin or to module ground.

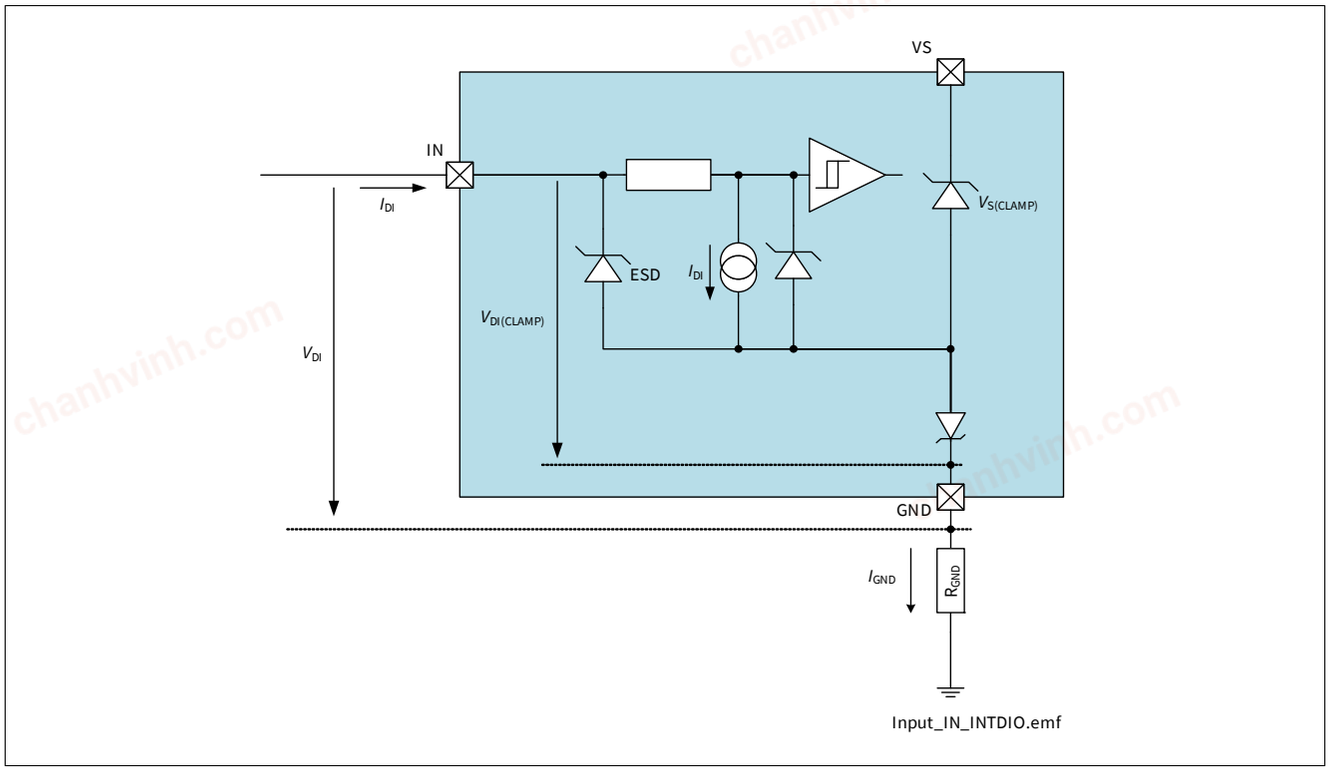


Figure 11 Input circuitry

The logic thresholds for “low” and “high” states are defined by parameters $V_{DI(TH)}$ and $V_{DI(HYS)}$. The relationship between these two values is shown in **Figure 12**. The voltage V_{IN} needed to ensure a “high” state is always higher than the voltage needed to ensure a “low” state.

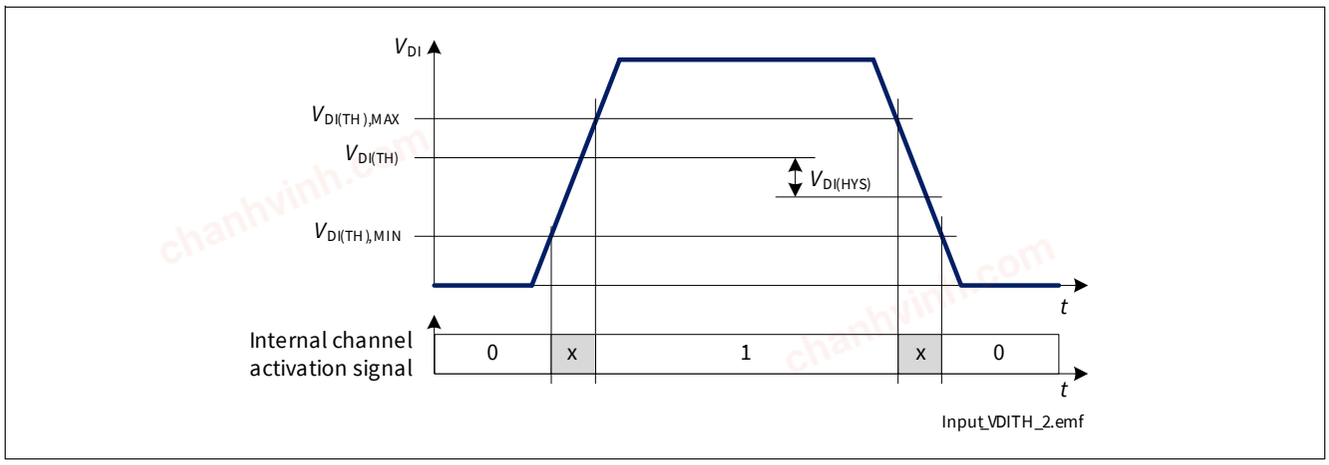


Figure 12 Input Threshold voltages and hysteresis

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5.2 Diagnosis Pin

The Diagnosis Enable (DEN) pin controls the diagnosis circuitry and the protection circuitry. When DEN pin is set to “high”, the diagnosis is enabled (see **Chapter 9.2** for more details). When it is set to “low”, the diagnosis is disabled (IS pin is set to high impedance).

The Diagnosis Selection (DSEL) pin selects the channel where diagnosis is performed (see **Chapter 9.1.1**).

The transition from “high” to “low” of DEN pin clears the protection latch of the channel selected with DSEL pin depending on the logic state of IN pin and DEN pulse length (see **Chapter 8.3** for more details). The internal structure of diagnosis pins is the same as the one of input pins. See **Figure 11** for more details.

5.3 Electrical Characteristics Logic Pins

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Digital Input (DI) pins = IN, DEN, DSEL

Table 7 Electrical Characteristics: Logic Pins - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Input Voltage Threshold	$V_{DI(TH)}$	0.8	1.3	2	V	See **Figure 11** and **Figure 12**	P_5.4.0.1
Digital Input Clamping Voltage	$V_{DI(CLAMP1)}$	–	7	–	V	1) I_{DI} = 1 mA See **Figure 11** and **Figure 12**	P_5.4.0.2
Digital Input Clamping Voltage	$V_{DI(CLAMP2)}$	6.5	7.5	8.5	V	I_{DI} = 2 mA See **Figure 11** and **Figure 12**	P_5.4.0.3
Digital Input Hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	1) See **Figure 11** and **Figure 12**	P_5.4.0.4
Digital Input Current (“high”)	$I_{DI(H)}$	2	10	25	µA	V_{DI} = 2 V See **Figure 11** and **Figure 12**	P_5.4.0.5
Digital Input Current (“low”)	$I_{DI(L)}$	2	10	25	µA	V_{DI} = 0.8 V See **Figure 11** and **Figure 12**	P_5.4.0.6

1) Not subject to production test - specified by design.

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6 Power Supply

The BTS7040-2EPA is supplied by V_S, which is used for the internal logic as well as supply for the power output stages. V_S has an undervoltage detection circuit, which prevents the activation of the power output stages and diagnosis in case the applied voltage is below the undervoltage threshold.

6.1 Operation Modes

BTS7040-2EPA has the following operation modes:

- Sleep mode
- Active mode
- Stand-by mode

The transition between operation modes is determined according to these variables:

- Logic level at INn pins
- Logic level at DEN pin

The state diagram including the possible transitions is shown in **Figure 13**. The behavior of BTS7040-2EPA as well as some parameters may change in dependence from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors V_S supply voltage, some changes within the same operation mode can be seen accordingly.

There are three parameters describing each operation mode of BTS7040-2EPA:

- Status of the output channels
- Status of the diagnosis
- Current consumption at VS pin (measured by I_{VS} in Sleep mode, I_{GND} in all other operative modes)

Table 8 shows the correlation between operation modes, V_S supply voltage, and the state of the most important functions (channel status, diagnosis).

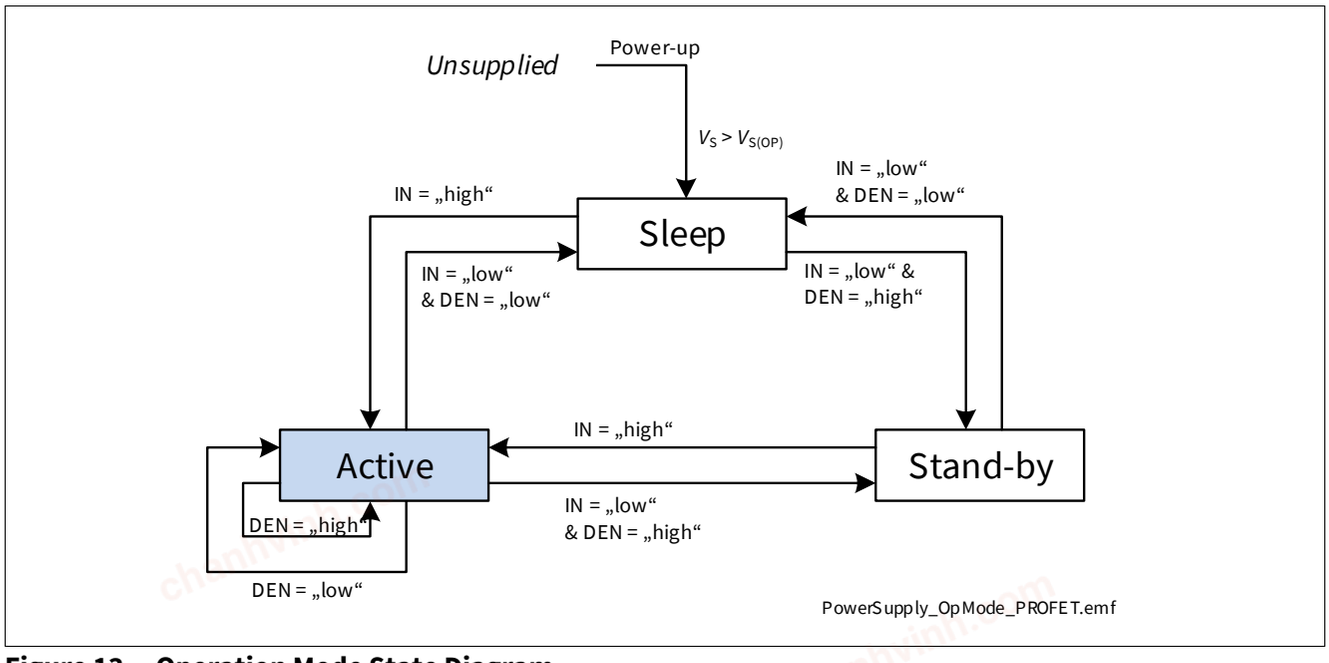


Figure 13 Operation Mode State Diagram

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Table 8 Device function in relation to operation modes and V_S voltage

Operative Mode	Function	V_S in undervoltage	V_S not in undervoltage
Sleep	Channels	OFF	OFF
	Diagnosis	OFF	OFF
Active	Channels	OFF	available
	Diagnosis	OFF	available in OFF and ON states
Stand-by	Channels	OFF	OFF
	Diagnosis	OFF	available in OFF state

6.1.1 Unsupplied

In this state, the device is either unsupplied (no voltage applied to VS pin) or the supply voltage is below the undervoltage threshold.

6.1.2 Power-up

The Power-up condition is entered when the supply voltage (V_S) is applied to the device. The supply is rising until it is above the undervoltage threshold $V_{S(OP)}$ therefore the internal Power-On signals are set.

6.1.3 Sleep mode

The device is in Sleep mode when all Digital Input pins (INn, DEN, DSEL) are set to “low”. When BTS7040-2EPA is in Sleep mode, all outputs are OFF. The current consumption is minimum (see parameter $I_{VS(SLEEP)}$). No Overtemperature or Overload protection mechanism is active when the device is in Sleep mode. The device can go in Sleep mode only if the protection is not active (counter = 0, see **Chapter 8.3.1** for further details).

6.1.4 Stand-by mode

The device is in Stand-by mode as long as DEN pin is set to “high” while input pins are set to “low”. All channels are OFF therefore only Open Load in OFF diagnosis is possible. Depending on the load condition, either a fault current $I_{IS(FAULT)}$ or an Open Load in OFF current $I_{IS(OLOFF)}$ may be present at IS pin. In such situation, the current consumption of the device is increased.

6.1.5 Active mode

Active mode is the normal operation mode of BTS7040-2EPA. The device enters Active mode as soon as one IN pin is set to “high”. Device current consumption is specified with $I_{GND(ACTIVE)}$ (measured at GND pin because the current at VS pin includes the load current). Overload, Overtemperature and Overvoltage protections are active. Diagnosis is available.

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6.2 Undervoltage on V_S

Between $V_{S(OP)}$ and $V_{S(UV)}$ the undervoltage mechanism is triggered. If the device is operative (in Active mode) and the supply voltage drops below the undervoltage threshold $V_{S(UV)}$, the internal logic switches OFF the output channels.

As soon as the supply voltage V_S is above the operative threshold $V_{S(OP)}$, the channels having the corresponding input pin set to “high” are switched ON again. The restart is delayed with a time $t_{DELAY(UV)}$ which protects the device in case the undervoltage condition is caused by a short circuit event (according to AEC-Q100-012), as shown in **Figure 14**.

If the device is in Sleep mode and one input is set to “high”, the corresponding channel is switched ON if $V_S > V_{S(OP)}$ without waiting for $t_{DELAY(UV)}$.

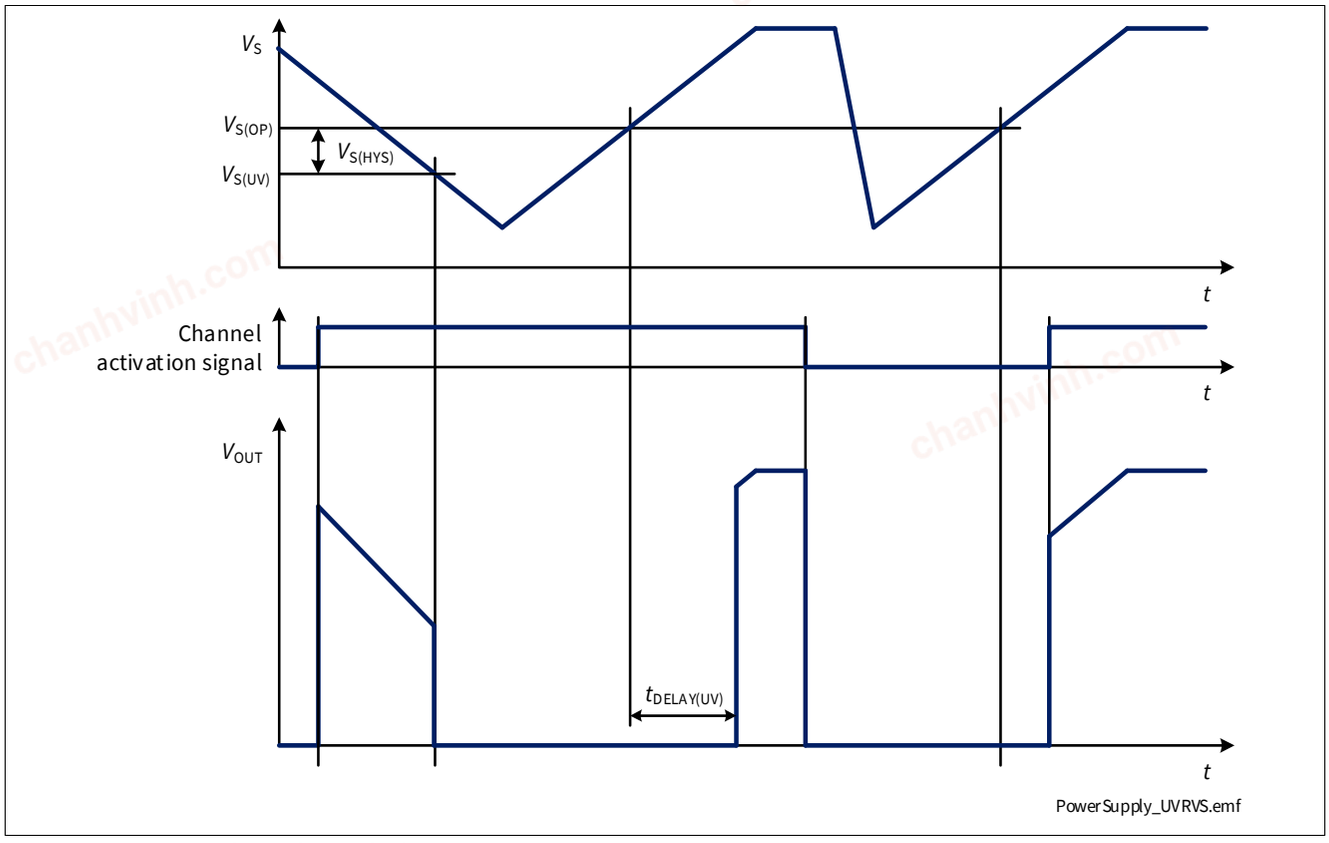


Figure 14 V_S undervoltage behavior

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6.3 Electrical Characteristics Power Supply

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

R_L = 3.3 Ω

Table 9 Electrical Characteristics: Power Supply - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VS pin							
Power Supply Undervoltage Shutdown	$V_{S(UV)}$	1.8	2.3	3.1	V	V_S decreasing IN = “high” From $V_{DS} \le 0.5$ V to $V_{DS} = V_S$ See **Figure 14**	P_6.4.0.1
Power Supply Minimum Operating Voltage	$V_{S(OP)}$	2.0	3.0	4.1	V	V_S increasing IN = “high” From $V_{DS} = V_S$ to $V_{DS} \le 0.5$ V See **Figure 14**	P_6.4.0.3
Power Supply Undervoltage Shutdown Hysteresis	$V_{S(HYS)}$	–	0.7	–	V	1) $V_{S(OP)} - V_{S(UV)}$ See **Figure 14**	P_6.4.0.6
Power Supply Undervoltage Recovery Time	$t_{DELAY(UV)}$	2.5	5	7.5	ms	$dV_S/dt \le 0.5$ V/µs $V_S \ge -1$ V See **Figure 14**	P_6.4.0.7
Breakdown Voltage between GND and VS Pins in Reverse Battery	$-V_{S(REV)}$	16	–	30	V	1) $I_{GND(REV)}$ = 7 mA T_J = 150 °C	P_6.4.0.9

1) Not subject to production test - specified by design.

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6.4 Electrical Characteristics Power Supply - Product Specific

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

R_L = 3.3 Ω

6.4.1 BTS7040-2EPA

Table 10 Electrical Characteristics: Power Supply BTS7040-2EPA

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply Current Consumption in Sleep Mode with Loads at $T_J \leq 85$ °C	$I_{VS(SLEEP)_85}$	–	0.03	0.5	µA	1) V_S = 18 V V_{OUT} = 0 V IN = DEN = “low” $T_J \leq 85$ °C	P_6.5.6.1
Power Supply Current Consumption in Sleep Mode with Loads at T_J = 150 °C	$I_{VS(SLEEP)_150}$	–	3.5	14	µA	V_S = 18 V V_{OUT} = 0 V IN = DEN = “low” T_J = 150 °C	P_6.5.6.2
Operating Current in Active Mode (all Channels ON)	$I_{GND(ACTIVE)}$	–	3	4	mA	V_S = 18 V IN = DEN = “high”	P_6.5.6.3
Operating Current in Stand-by Mode	$I_{GND(STBY)}$	–	1.2	1.8	mA	V_S = 18 V IN = “low” DEN = “high”	P_6.5.6.5

1) Not subject to production test - specified by design.

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7 Power Stages

The high-side power stages are built using a N-channel vertical Power MOSFET with charge pump.

7.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on junction temperature T_J. **Figure 15** shows the variation of $R_{DS(ON)}$ across the whole T_J range. The value “2” on the y-axis corresponds to the maximum $R_{DS(ON)}$ measured at T_J = 150 °C.

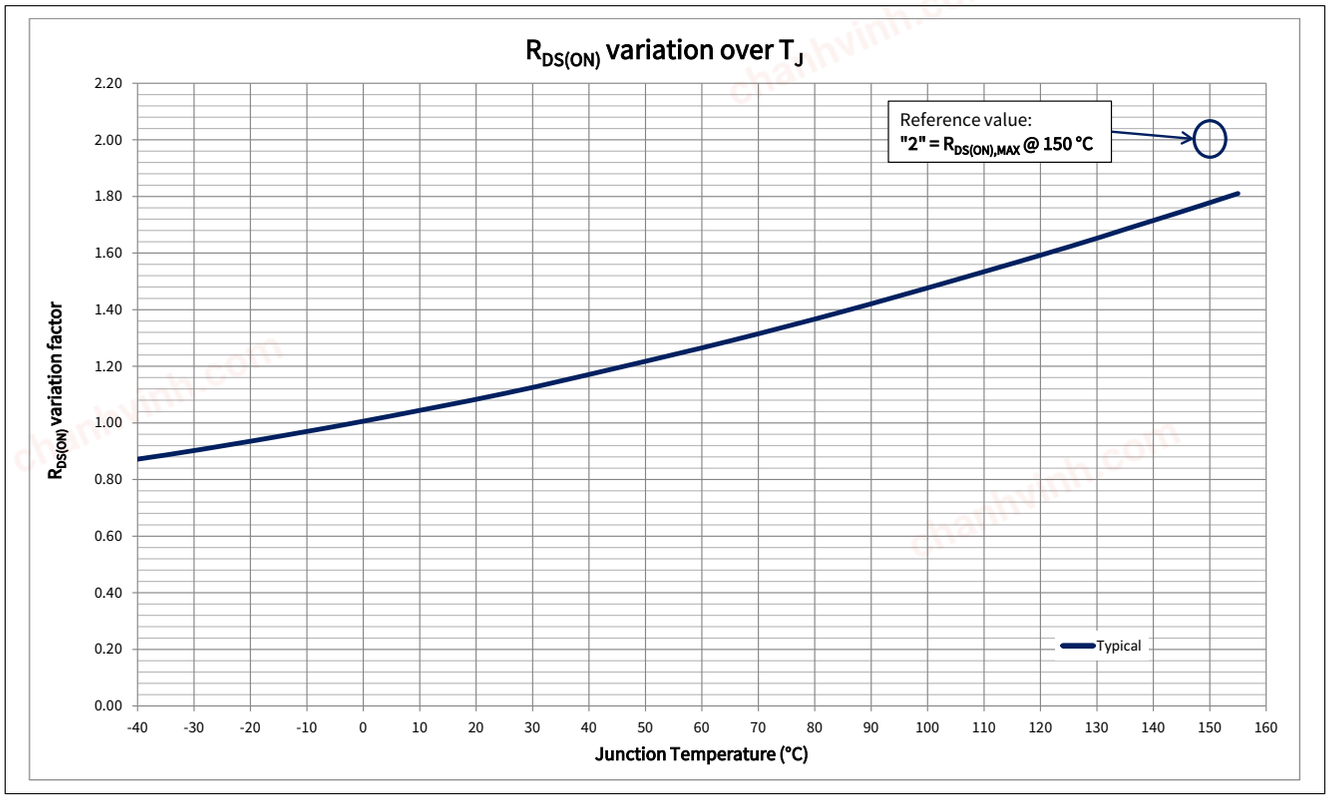


Figure 15 $R_{DS(ON)}$ variation factor

The behavior in Reverse Polarity is described in **Chapter 8.4.1**.

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7.2 Switching loads

7.2.1 Switching Resistive Loads

When switching resistive loads, the switching times and slew rates shown in **Figure 16** can be considered. The switch energy values E_{ON} and E_{OFF} are proportional to load resistance and times t_{ON} and t_{OFF}.

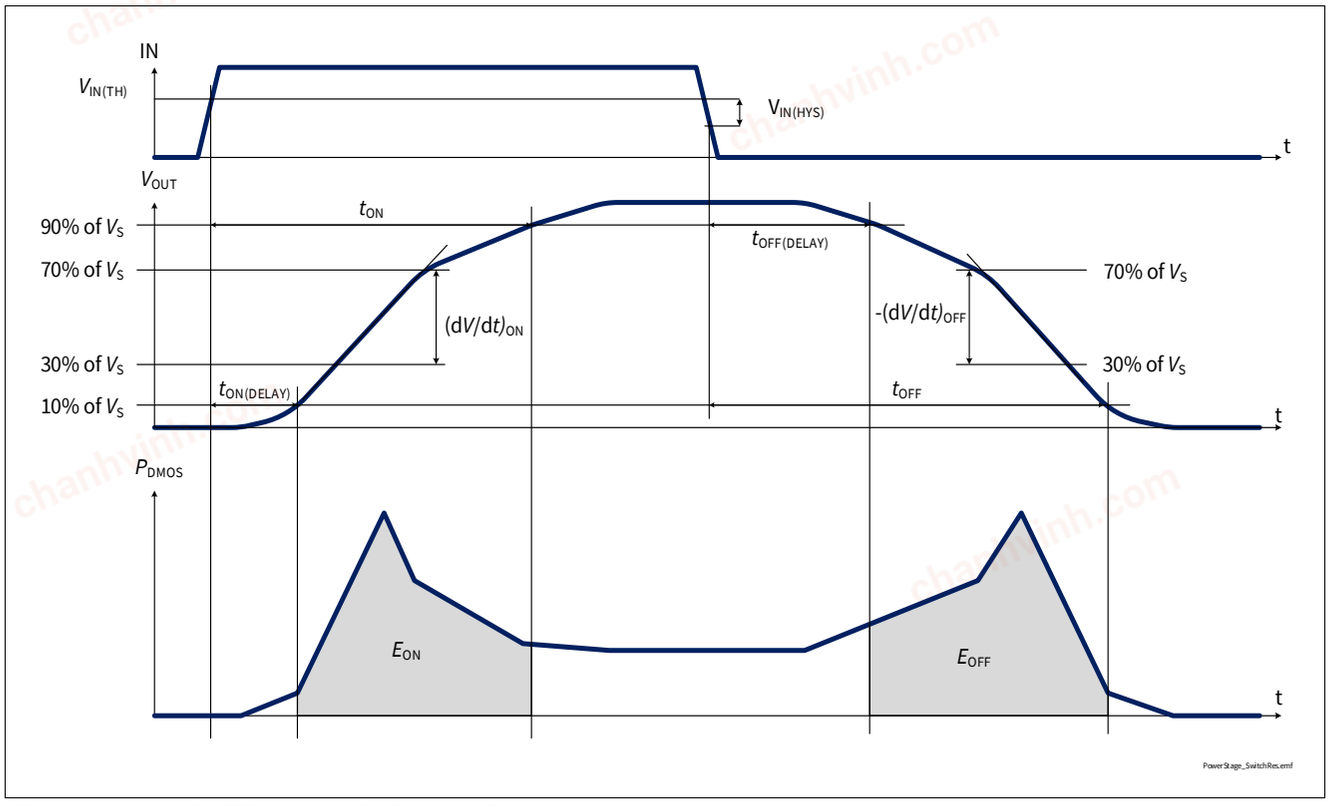


Figure 16 Switching a Resistive Load

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7.2.2 Switching Inductive Loads

When switching OFF inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, a voltage clamp mechanism is implemented. The clamping structure limits the negative output voltage so that $V_{DS} = V_{DS(CLAMP)}$. **Figure 17** shows a concept drawing of the implementation. The clamping structure protects the device in all operation modes listed in **Chapter 6.1**.

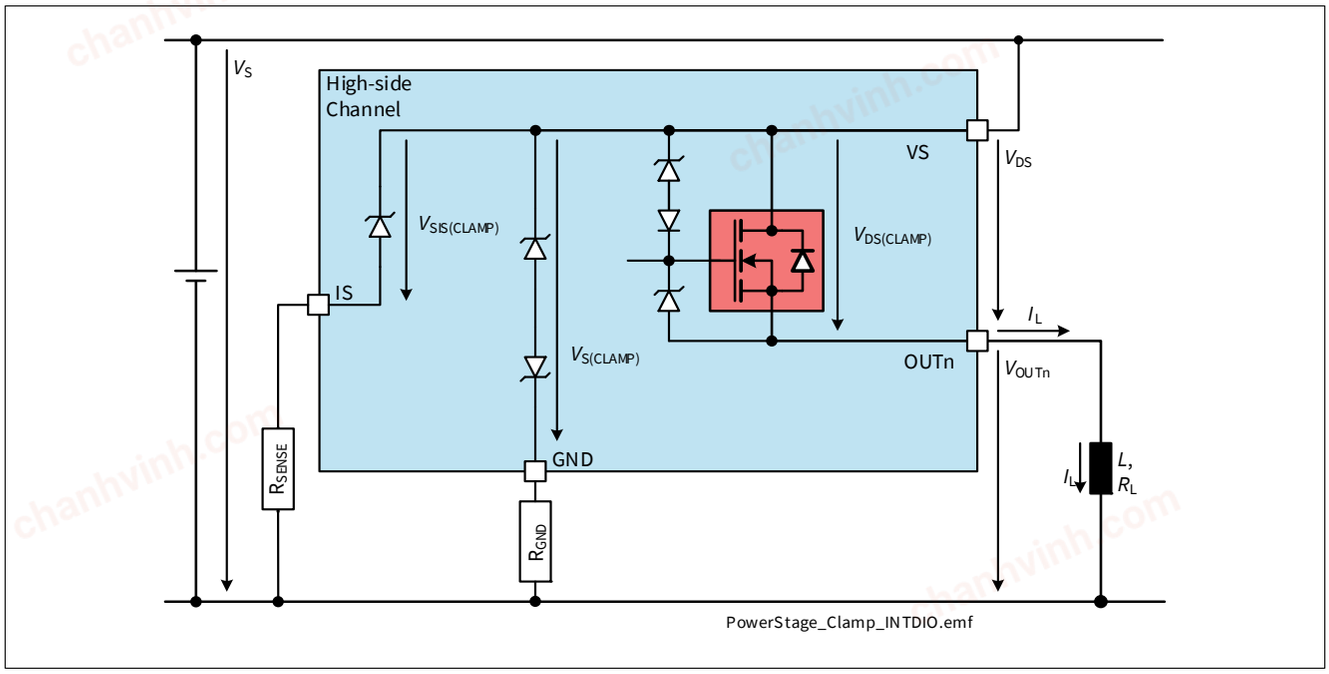


Figure 17 Output Clamp concept

During demagnetization of inductive loads, energy has to be dissipated in BTS7040-2EPA. The energy can be calculated with **Equation (7.1)**:

$$E = V_{DS(CLAMP)} \cdot \left[\frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}}\right) + I_L \right] \cdot \frac{L}{R_L} \quad (7.1)$$

The maximum energy, therefore the maximum inductance for a given current, is limited by the thermal design of the component.

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7.2.3 Output Voltage Limitation

To increase the current sense accuracy, V_{DS} voltage is monitored. When the output current I_L decreases while the channel is diagnosed (DEN pin set to “high”, channel selected with DSEL pins - see **Figure 18**) bringing V_{DS} equal or lower than $V_{DS(SLC)}$, the output DMOS gate is partially discharged. This increases the output resistance so that $V_{DS} = V_{DS(SLC)}$ even for very small output currents. The V_{DS} increase allows the current sensing circuitry to work more efficiently, providing better k_{ILIS} accuracy for output current in the low range.

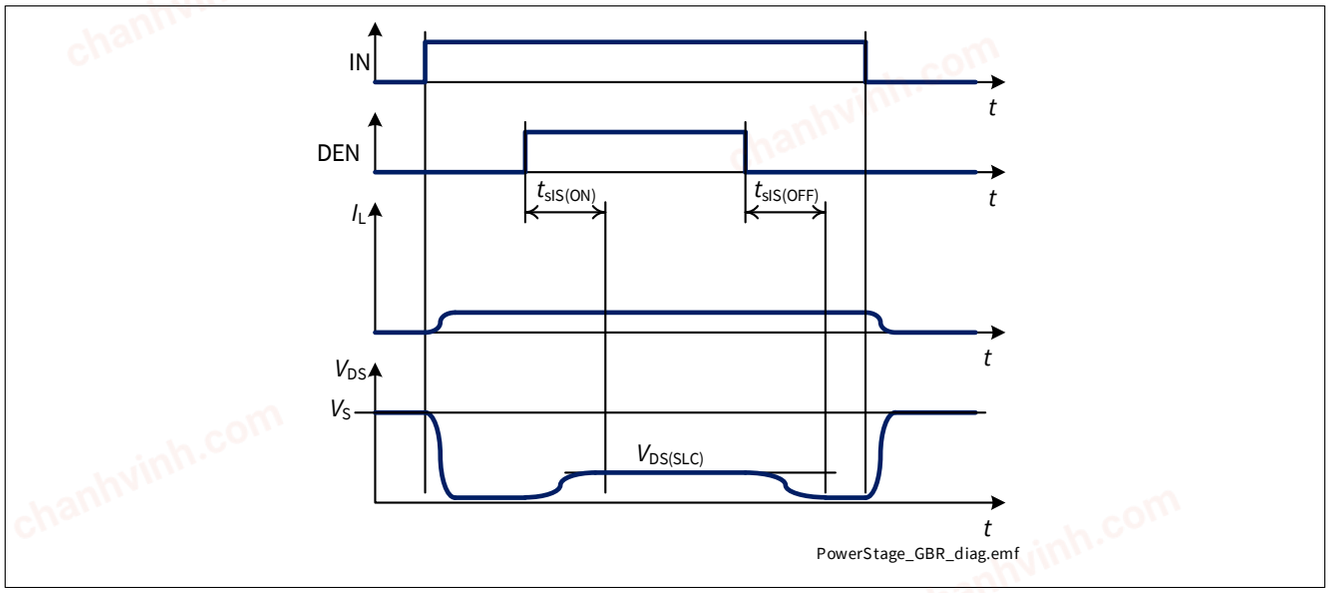


Figure 18 Output Voltage Limitation activation during diagnosis

7.3 Advanced Switching Characteristics

7.3.1 Inverse Current behavior

When $V_{OUT} > V_S$, a current I_{INV} flows into the power output transistor (see **Figure 19**). This condition is known as “Inverse Current”.

If the channel is in OFF state, the current flows through the intrinsic body diode generating high power losses therefore an increase of overall device temperature. This may lead to a switch OFF of unaffected channels due to Overtemperature. If the channel is in ON state, $R_{DS(INV)}$ can be expected and power dissipation in the output stage is comparable to normal operation in $R_{DS(ON)}$.

During Inverse Current condition, the channel remains in ON or OFF state as long as $I_{INV} < I_{L(INV)}$. If one channel has inverse current applied, the neighbor channel is not influenced, meaning that switching ON and OFF timings, protection (Overcurrent, Overtemperature) and current sensing (k_{ILIS}) are still within specified limits.

With InverseON, it is possible to switch ON the channel during Inverse Current condition as long as $I_{INV} < I_{L(INV)}$ (see **Figure 20**).

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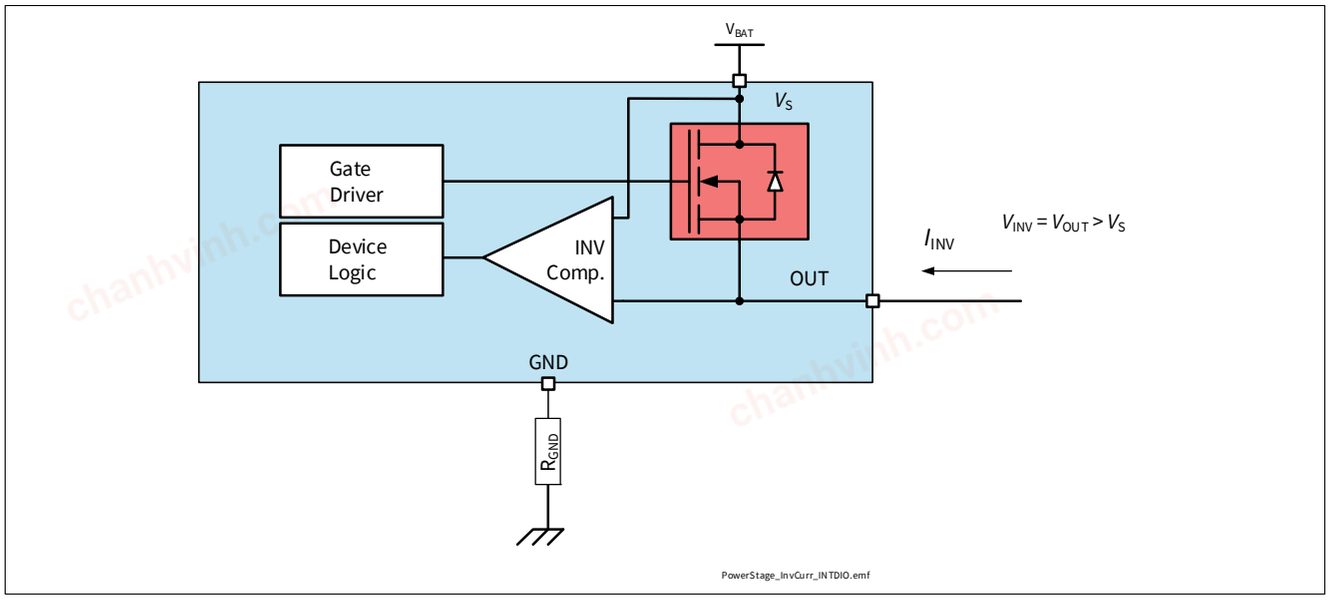


Figure 19 Inverse Current Circuitry

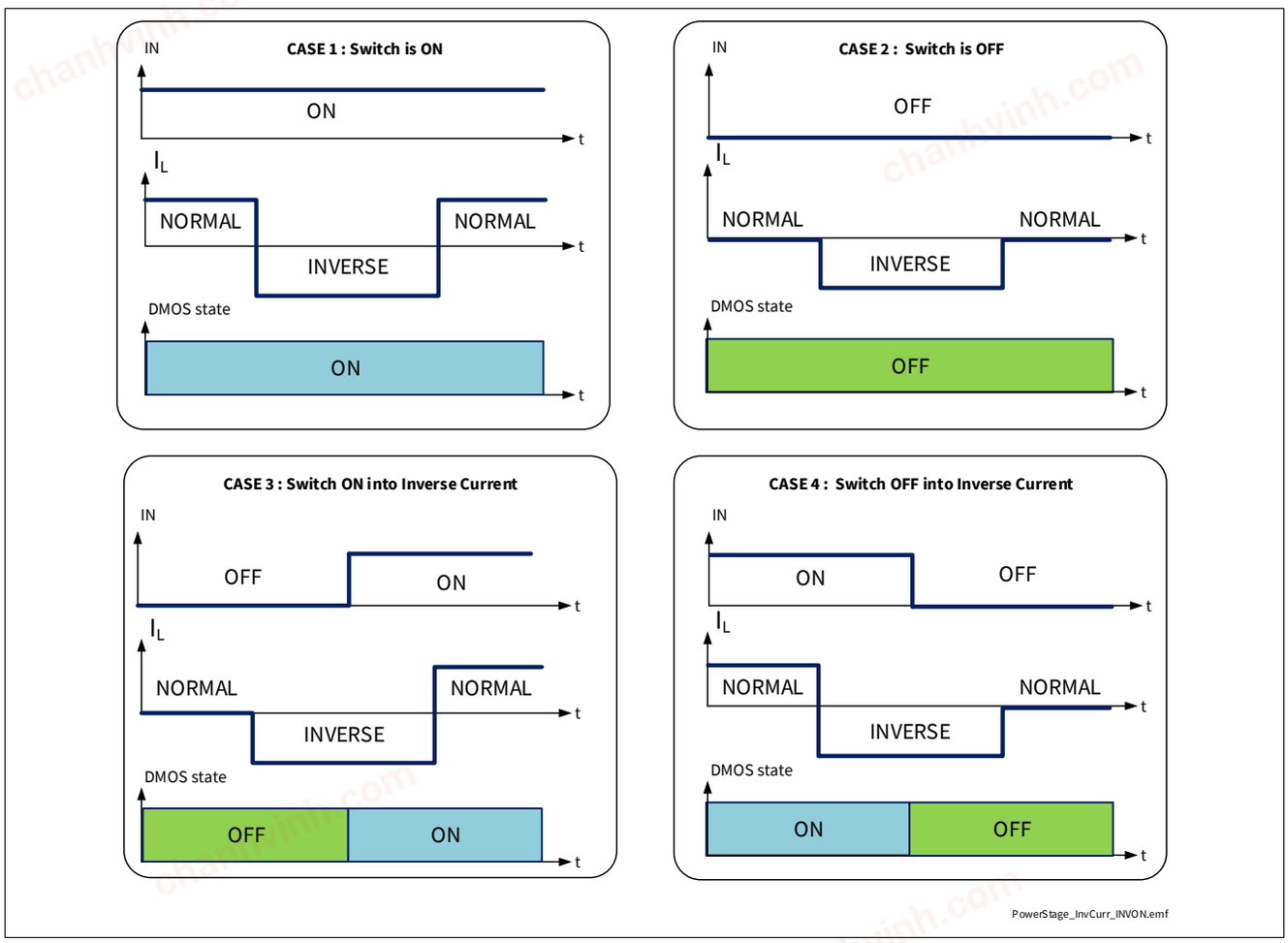


Figure 20 InverseON - Channel behavior in case of applied Inverse Current

Note: No protection mechanism like Overtemperature or Overload protection is active during applied Inverse Currents.

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7.3.2 Switching Channels in Parallel

In case of appearance of a short circuit with connected in parallel to drive a single load, it may happen that the two channels switch OFF asynchronously, therefore bringing an additional thermal stress to the channel that switches OFF last. For this reason it is not recommended to use the device with channels in parallel.

7.3.3 Cross Current robustness with H-Bridge configuration

When BTS7040-2EPA is used as high-side switch e.g. in a bridge configuration (therefore paired with a low-side switch as shown in **Figure 21**), the maximum slew rate applied to the output by the low-side switch must be lower than $|\,dV_{OUT}\,/\,dt\,|$.

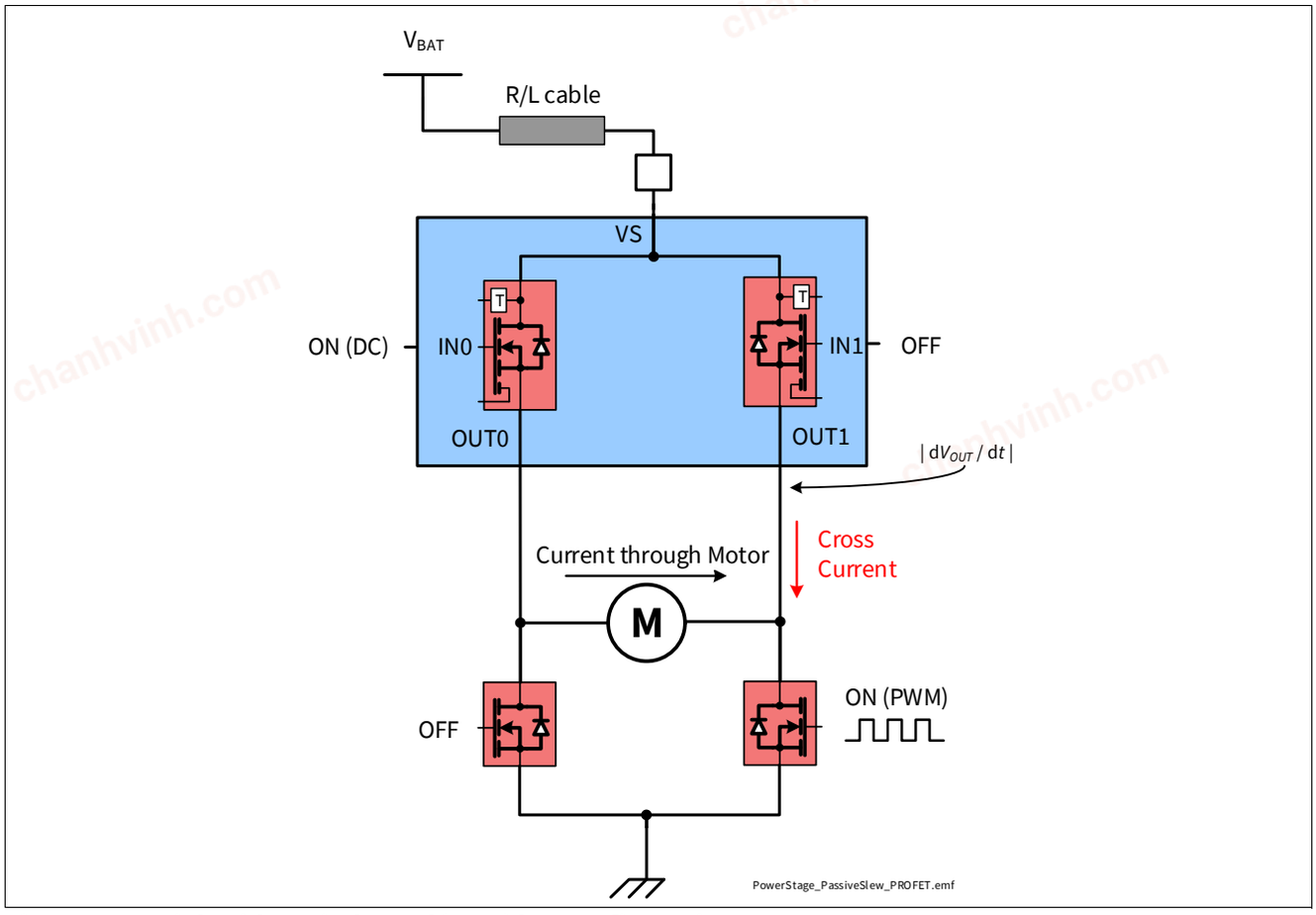


Figure 21 High-Side switch used in Bridge configuration

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7.4 Electrical Characteristics Power Stages

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

R_L = 3.3 Ω

Table 11 Electrical Characteristics: Power Stages - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Drain to Source Clamping Voltage at T_J = -40 °C	$V_{DS(CLAMP)_-40}$	33	36.5	42	V	I_L = 5 mA T_J = -40°C See **Figure 17**	P_7.4.0.1
Drain to Source Clamping Voltage at $T_J \geq$ 25 °C	$V_{DS(CLAMP)_25}$	35	38	44	V	1) I_L = 5 mA $T_J \geq$ 25°C See **Figure 17**	P_7.4.0.2

1) Tested at T_J = 150°C.

7.4.1 Electrical Characteristics Power Stages - PROFET™

Table 12 Electrical Characteristics: Power Stages - PROFET™

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Timings							
Switch-ON Delay	$t_{ON(DELAY)}$	10	35	60	µs	V_S = 13.5 V V_{OUT} = 10% V_S See **Figure 16**	P_7.4.1.1
Switch-OFF Delay	$t_{OFF(DELAY)}$	10	25	50	µs	V_S = 13.5 V V_{OUT} = 90% V_S See **Figure 16**	P_7.4.1.2
Switch-ON Time	t_{ON}	30	60	110	µs	V_S = 13.5 V V_{OUT} = 90% V_S See **Figure 16**	P_7.4.1.3
Switch-OFF Time	t_{OFF}	15	50	100	µs	V_S = 13.5 V V_{OUT} = 10% V_S See **Figure 16**	P_7.4.1.4
Switch-ON/OFF Matching t_{ON} - t_{OFF}	Δt_{SW}	-20	20	60	µs	V_S = 13.5 V	P_7.4.1.5

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Table 12 Electrical Characteristics: Power Stages - PROFET™ (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage Slope							
Switch-ON Slew Rate	$(dV/dt)_{ON}$	0.3	0.6	0.9	V/µs	V_S = 13.5 V V_{OUT} = 30% to 70% of V_S See **Figure 16**	P_7.4.1.6
Switch-OFF Slew Rate	$-(dV/dt)_{OFF}$	0.3	0.6	0.9	V/µs	V_S = 13.5 V V_{OUT} = 70% to 30% of V_S See **Figure 16**	P_7.4.1.7
Slew Rate Matching $(dV/dt)_{ON}$ - $(dV/dt)_{OFF}$	$\Delta(dV/dt)_{SW}$	-0.15	0	0.15	V/µs	V_S = 13.5 V	P_7.4.1.8
Voltages							
Output Voltage Drop Limitation at Small Load Currents	$V_{DS(SLC)}$	2	7	18	mV	1) DEN = “high” channel selected with DSEL pin $I_L = I_{L(OL)}$ = 20 mA See **Figure 18**	P_7.4.1.9

1) Not subject to production test - specified by design.

7.5 Electrical Characteristics - Power Output Stages

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

R_L = 3.3 Ω

7.5.1 Power Output Stage - 40 mΩ

Table 13 Electrical Characteristics: Power Stages - 40 mΩ

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output characteristics							
ON-State Resistance at T_J = 25 °C	$R_{DS(ON)_25}$	–	19	–	mΩ	1) T_J = 25 °C	P_7.5.6.1
ON-State Resistance at T_J = 150 °C	$R_{DS(ON)_150}$	–	–	36	mΩ	T_J = 150 °C I_L = 2 A	P_7.5.6.2
ON-State Resistance in Cranking	$R_{DS(ON)_CRANK}$	–	–	45	mΩ	T_J = 150 °C V_S = 3.1 V I_L = 0.75 A	P_7.5.6.3

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Table 13 Electrical Characteristics: Power Stages - 40 mΩ (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON-State Resistance in Inverse Current at T_J = 25 °C	$R_{DS(INV)_25}$	–	21	–	mΩ	[1] T_J = 25 °C V_S = 13.5 V I_L = -2 A DEN = “low” see **Figure 19**	P_7.5.6.4
ON-State Resistance in Inverse Current at T_J = 150 °C	$R_{DS(INV)_150}$	–	–	45	mΩ	T_J = 150 °C V_S = 13.5 V I_L = -2 A DEN = “low” see **Figure 19**	P_7.5.6.5
ON-State Resistance in Reverse Polarity at T_J = 25 °C	$R_{DS(REV)_25}$	–	21	–	mΩ	[1] T_J = 25 °C V_S = -13.5 V I_L = -2 A R_{SENSE} = 1.2 kΩ	P_7.5.6.6
ON-State Resistance in Reverse Polarity at T_J = 150 °C	$R_{DS(REV)_150}$	–	–	74	mΩ	T_J = 150 °C V_S = -13.5 V I_L = -2 A R_{SENSE} = 1.2 kΩ	P_7.5.6.7
Nominal Load Current per Channel (all Channels Active)	$I_{L(NOM)}$	–	3.5	–	A	[1] T_A = 85 °C $T_J \leq$ 150 °C	P_7.5.6.8
Output Leakage Current at $T_J \leq$ 85 °C	$I_{L(OFF)_85}$	–	0.01	0.5	µA	[1] V_{OUT} = 0 V V_{IN} = “low” $T_A \leq$ 85 °C	P_7.5.6.9
Output Leakage Current at T_J = 150 °C	$I_{L(OFF)_150}$	–	1.2	4	µA	V_{OUT} = 0 V V_{IN} = “low” T_A = 150 °C	P_7.5.6.10
Inverse Current Capability	$I_{L(INV)}$	–	3.5	–	A	[1] $V_S < V_{OUT}$ IN = “high” see **Figure 19**	P_7.5.6.11
Voltage Slope							
Passive Slew Rate (e.g. for Half Bridge Configuration)	$\lvert dV_{OUT} / dt \rvert$	–	–	10	V/µs	[1] V_S = 13.5 V see **Figure 21**	P_7.5.6.12
Voltages							
Drain Source Diode Voltage	$\lvert V_{DS(DIODE)} \rvert$	–	650	700	mV	I_L = -190 mA T_J = 150 °C	P_7.5.6.13

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Table 13 Electrical Characteristics: Power Stages - 40 mΩ (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Switching Energy							
Switch-ON Energy	E_{ON}	–	0.44	–	mJ	1) V_S = 18 V see **Figure 16**	P_7.5.6.14
Switch-OFF Energy	E_{OFF}	–	0.55	–	mJ	1) V_S = 18 V see **Figure 16**	P_7.5.6.15

1) Not subject to production test - specified by design.

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8 Protection

The BTS7040-2EPA is protected against Overtemperature, Overload, Reverse Battery (with ReverseON) and Overvoltage. Overtemperature and Overload protections are working when the device is not in Sleep mode. Overvoltage protection works in all operation modes. Reverse Battery protection works when the GND and VS pins are reverse supplied.

8.1 Overtemperature Protection

The device incorporates both an absolute ($T_{J(ABS)}$) and a dynamic ($T_{J(DYN)}$) temperature protection circuitry for each channel. An increase of junction temperature T_J above either one of the two thresholds ($T_{J(ABS)}$ or $T_{J(DYN)}$) switches OFF the overheated channel to prevent destruction. The channel remains switched OFF until junction temperature has reached the “Restart” condition described in **Table 14**. The behavior is shown in **Figure 22** (absolute Overtemperature Protection) and **Figure 23** (dynamic Overtemperature Protection). $T_{J(REF)}$ is the reference temperature used for dynamic temperature protection.

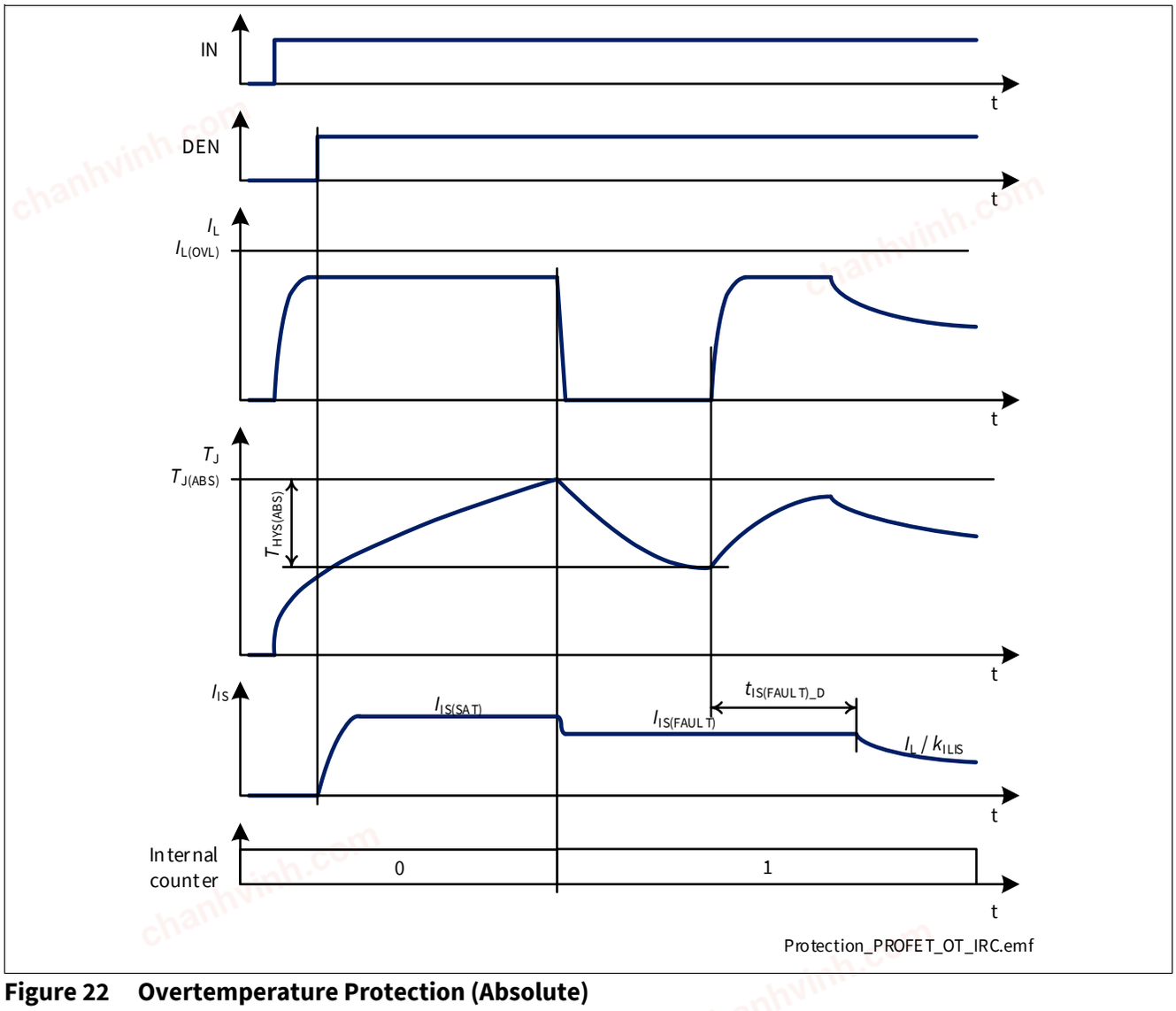


Figure 22 Overtemperature Protection (Absolute)

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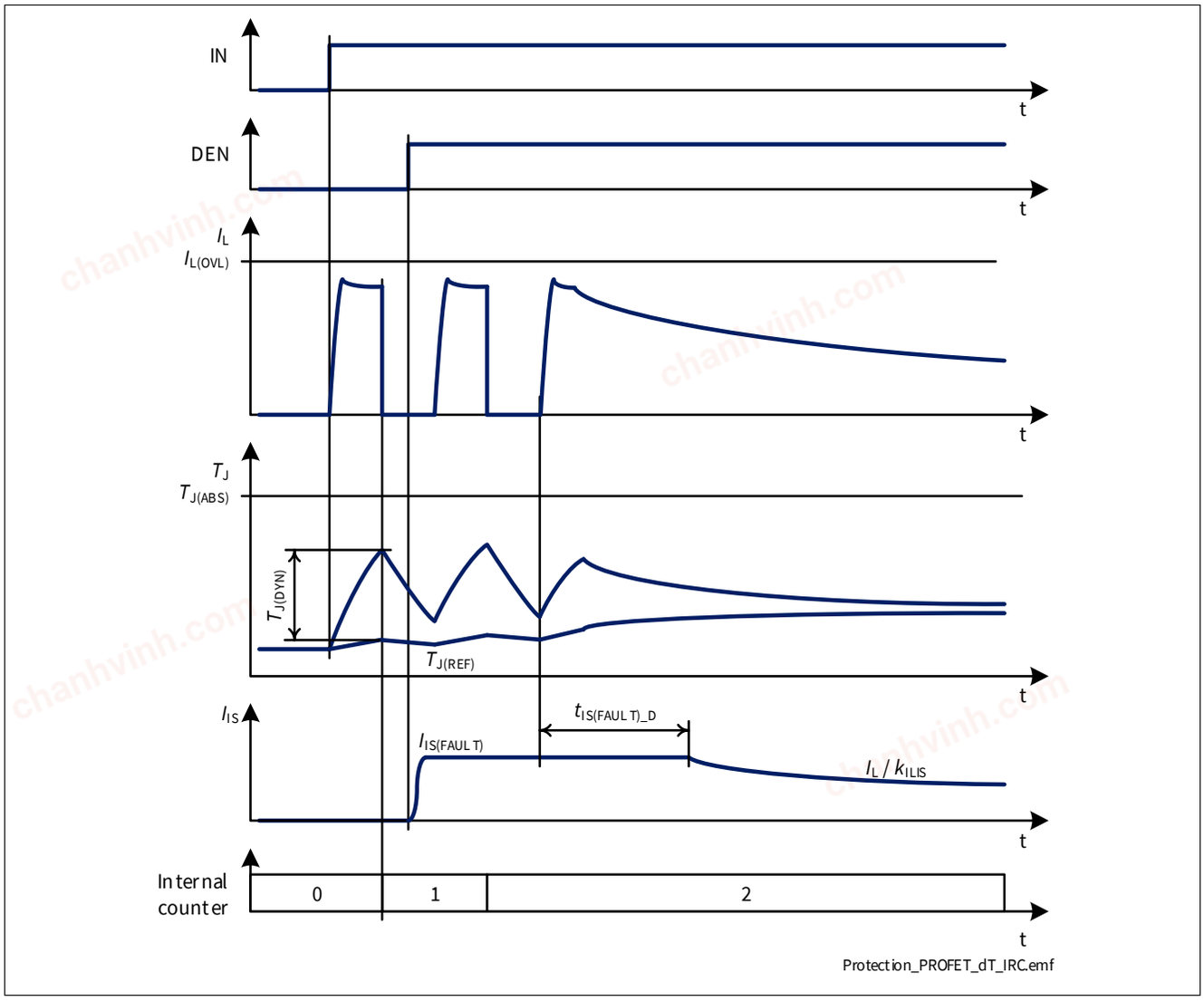


Figure 23 Overtemperature Protection (Dynamic)

When the Overtemperature protection circuitry allows the channel to be switched ON again, the retry strategy described in **Chapter 8.3** is followed.

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8.2 Overload Protection

The BTS7040-2EPA is protected in case of Overload or short circuit to ground. Two Overload thresholds are defined (see **Figure 24**) and selected automatically depending on the voltage V_{DS} across the power DMOS:

- $I_{L(OVL0)}$ when V_{DS} < 13 V
- $I_{L(OVL1)}$ when V_{DS} > 22 V

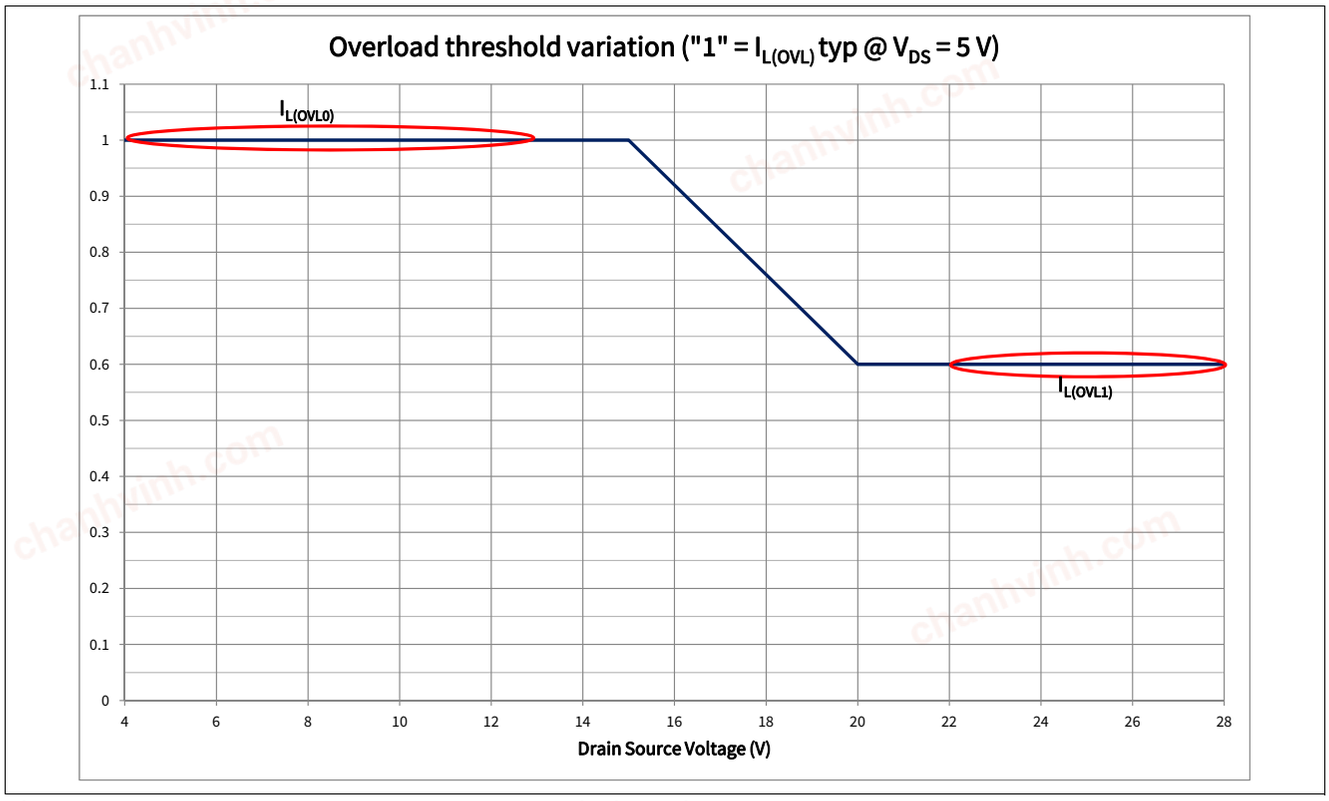


Figure 24 Overload Current Thresholds variation with V_{DS}

In order to allow a higher load inrush at low ambient temperature, Overload threshold is maximum at low temperature and decreases when T_J increases (see **Figure 25**). $I_{L(OVL0)}$ typical value remains approximately constant up to a junction temperature of +75 °C.

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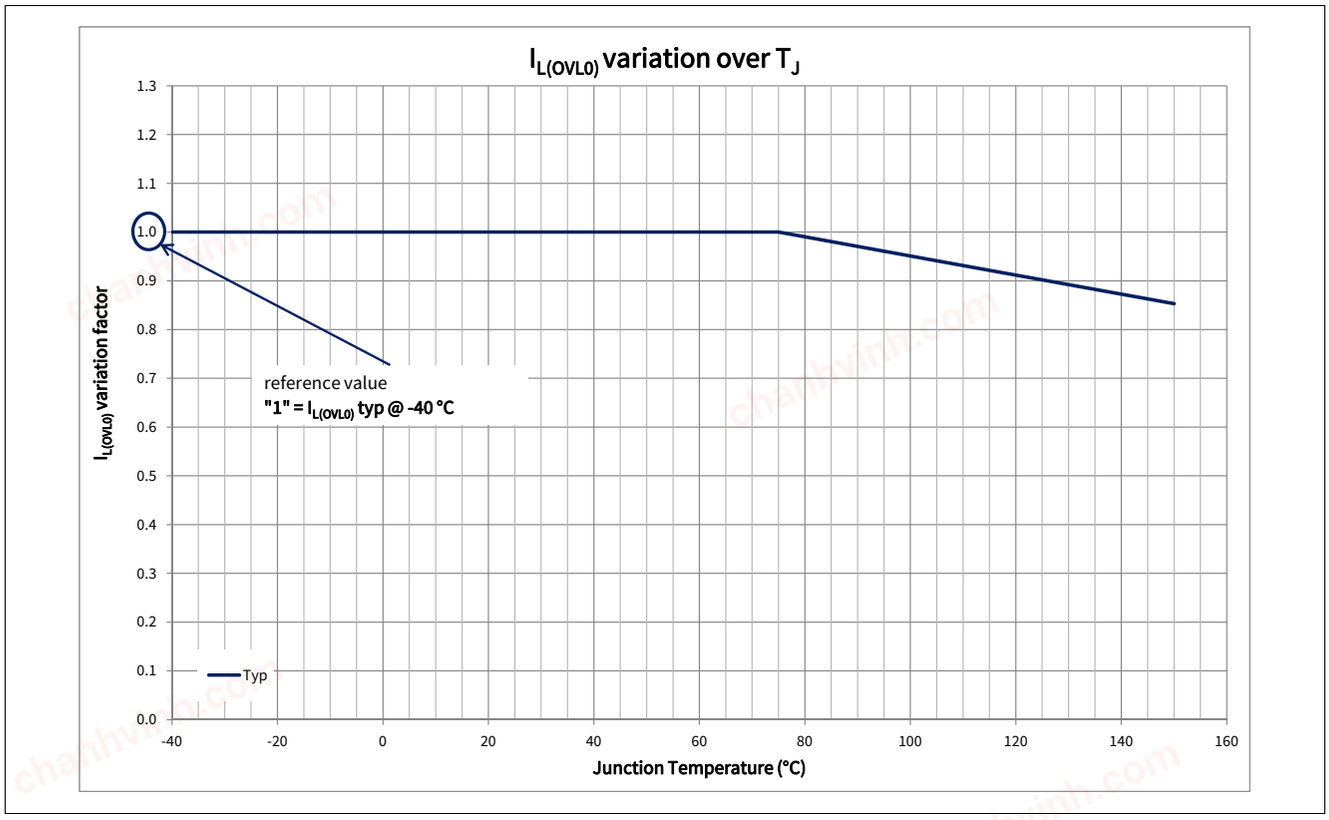


Figure 25 Overload Current Thresholds variation with T_J

Power supply voltage V_S can increase above 18 V for short time, for instance in Load Dump or in Jump Start condition. Whenever $V_S \geq V_{S(JS)}$, the overload detection current is set to $I_{L(OVL_JS)}$ as shown in **Figure 26**.

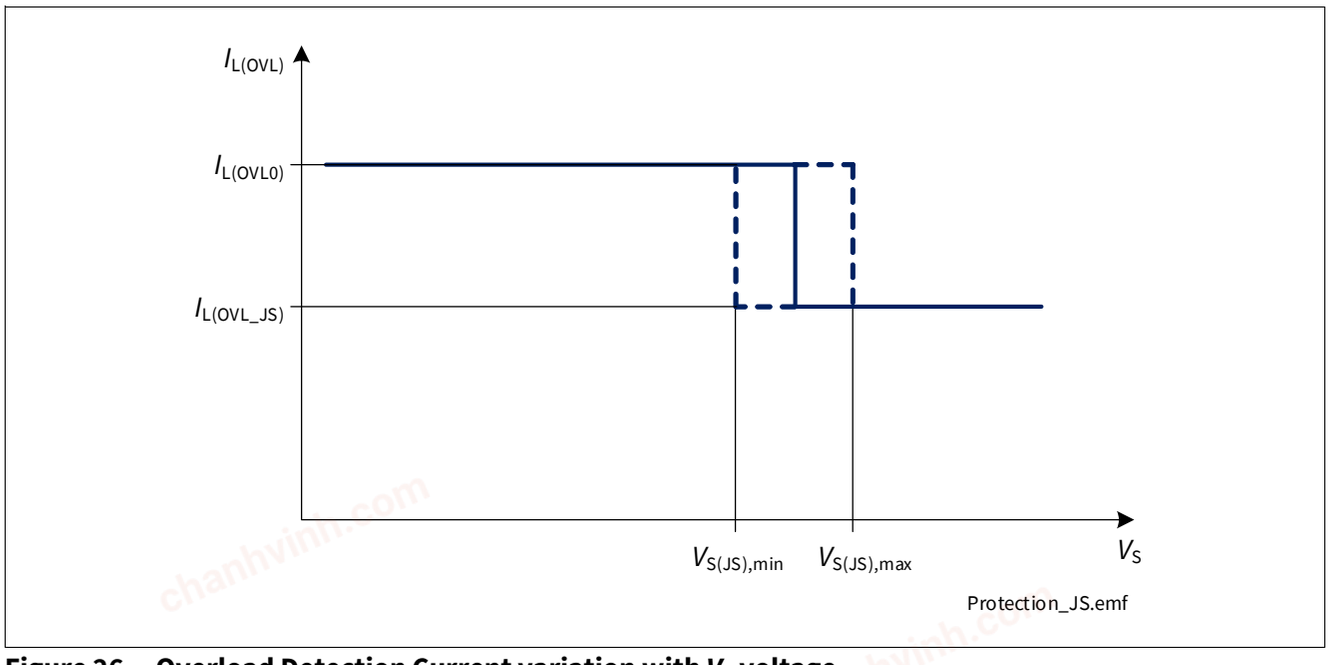


Figure 26 Overload Detection Current variation with V_S voltage

When $I_L \geq I_{L(OVL)}$ (either $I_{L(OVL0)}$, $I_{L(OVL1)}$ or $I_{L(OVL_JS)}$), the channel is switched OFF. The channel is allowed to restart according to the retry strategy described in **Chapter 8.3**.

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8.3 Protection and Diagnosis in case of Fault

Any event that triggers a protection mechanism (either Overtemperature or Overload) has 2 consequences:

- The affected channel switches OFF and the internal counter is incremented
- If the diagnosis is active for the affected channel, a current $I_{IS(FAULT)}$ is provided by IS pin (see **Chapter 9.2.2** for further details)

The channel can be switched ON again if all the protection mechanisms fulfill the “restart” conditions described in **Table 14**. Furthermore, the device has an internal retry counter (one for each channel) to maximize the robustness in case of fault.

Table 14 Protection “Restart” Condition

Fault condition	Switch OFF event	“Restart” Condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)
Overload	$I_L \geq I_{L(OVL)}$	$I_L < 50$ mA T_J within $T_{J(ABS)}$ and $T_{J(DYN)}$ ranges (including hysteresis)

8.3.1 Retry Strategy

When IN is set to “high”, the channel is switched ON. In case of fault condition the output stage is switched OFF. The channel can be allowed to restart only if the “restart” conditions for the protection mechanisms are fulfilled (see **Table 14**).

The channel is allowed to switch ON for $n_{RETRY(CR)}$ times before switching OFF. After a time t_{RETRY}, if the input pin is set to “high”, the channel switches ON again for $n_{RETRY(NT)}$ times before switching OFF again (“retry” cycle). After $n_{RETRY(CYC)}$ consecutive “retry” cycles, the channel latches OFF. It is necessary to set the input pin to “low” for a time longer than $t_{DELAY(CR)}$ to de-latch the channel (“counter reset delay” time) and to reset the internal counter to the default value.

During the “counter reset delay” time, if the input is set to “high” the channel remains switched OFF and the timer counting $t_{DELAY(CR)}$ is reset, starting to count again as soon as the input pin is set to “low” again. If the input pin remains “low” for a time longer than $t_{DELAY(CR)}$ the internal retry counter is reset to the default value, allowing $n_{RETRY(CR)}$ retries at the next channel activation.

The retry strategy is shown in **Figure 29** (flowchart), **Figure 27** (timing diagram - input pin always “high”) and **Figure 28** (timing diagram - channel controlled in PWM).

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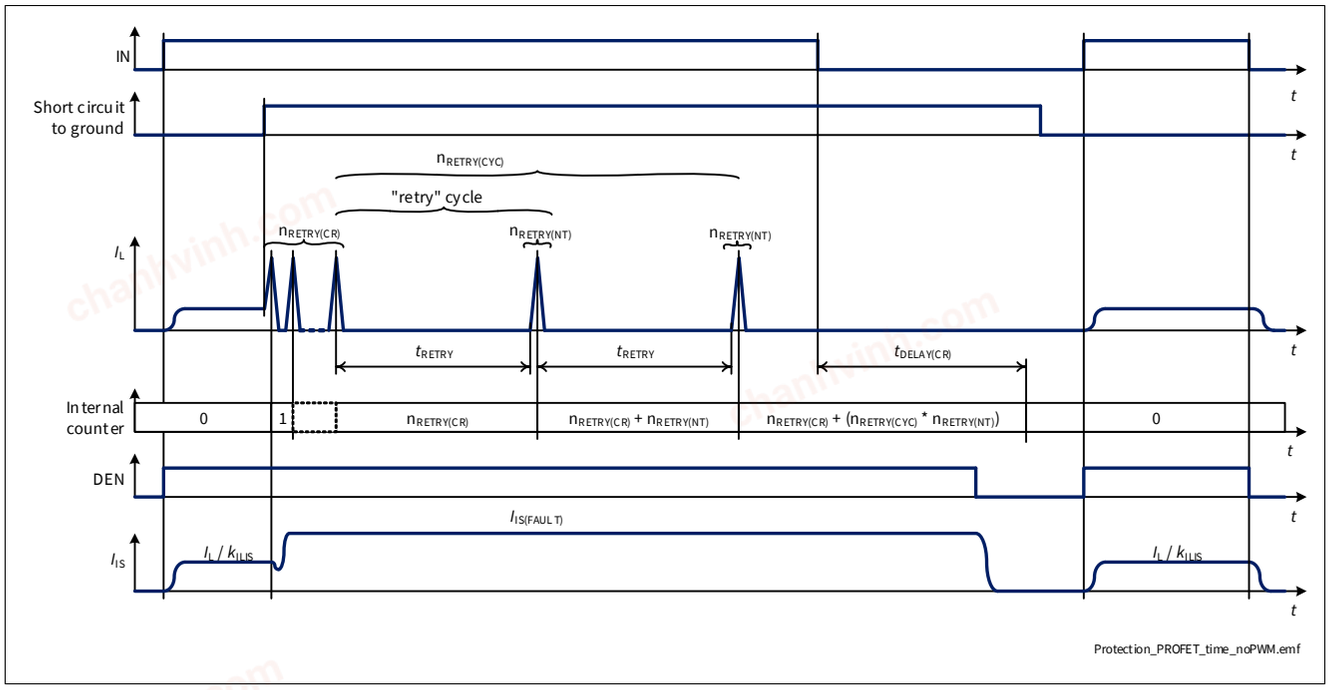


Figure 27 Retry Strategy Timing Diagram

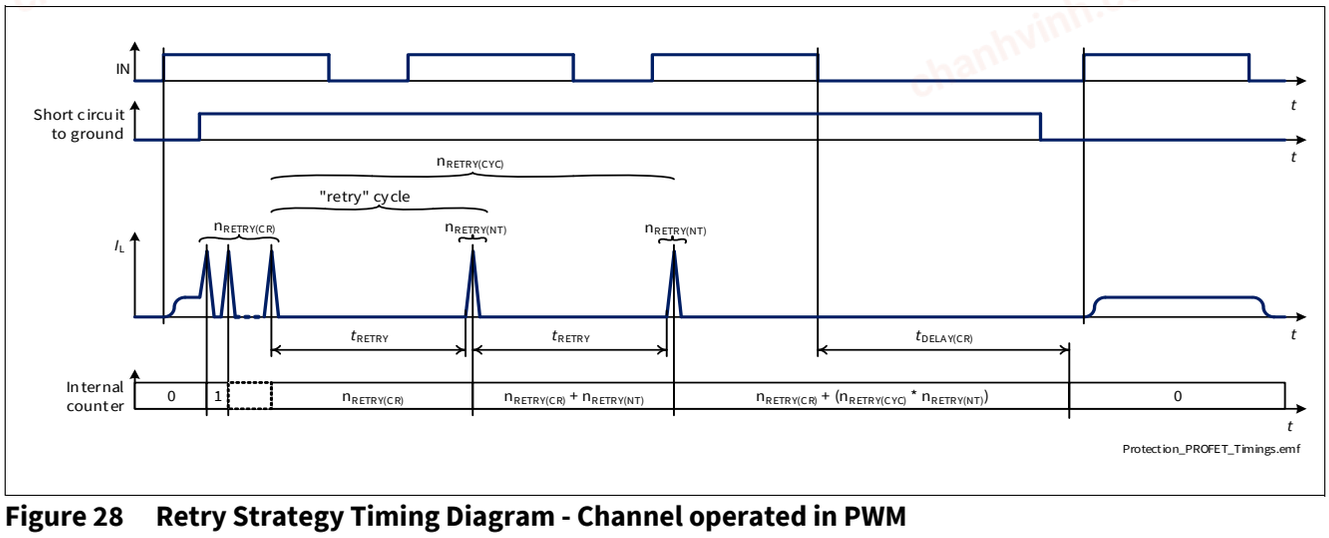


Figure 28 Retry Strategy Timing Diagram - Channel operated in PWM

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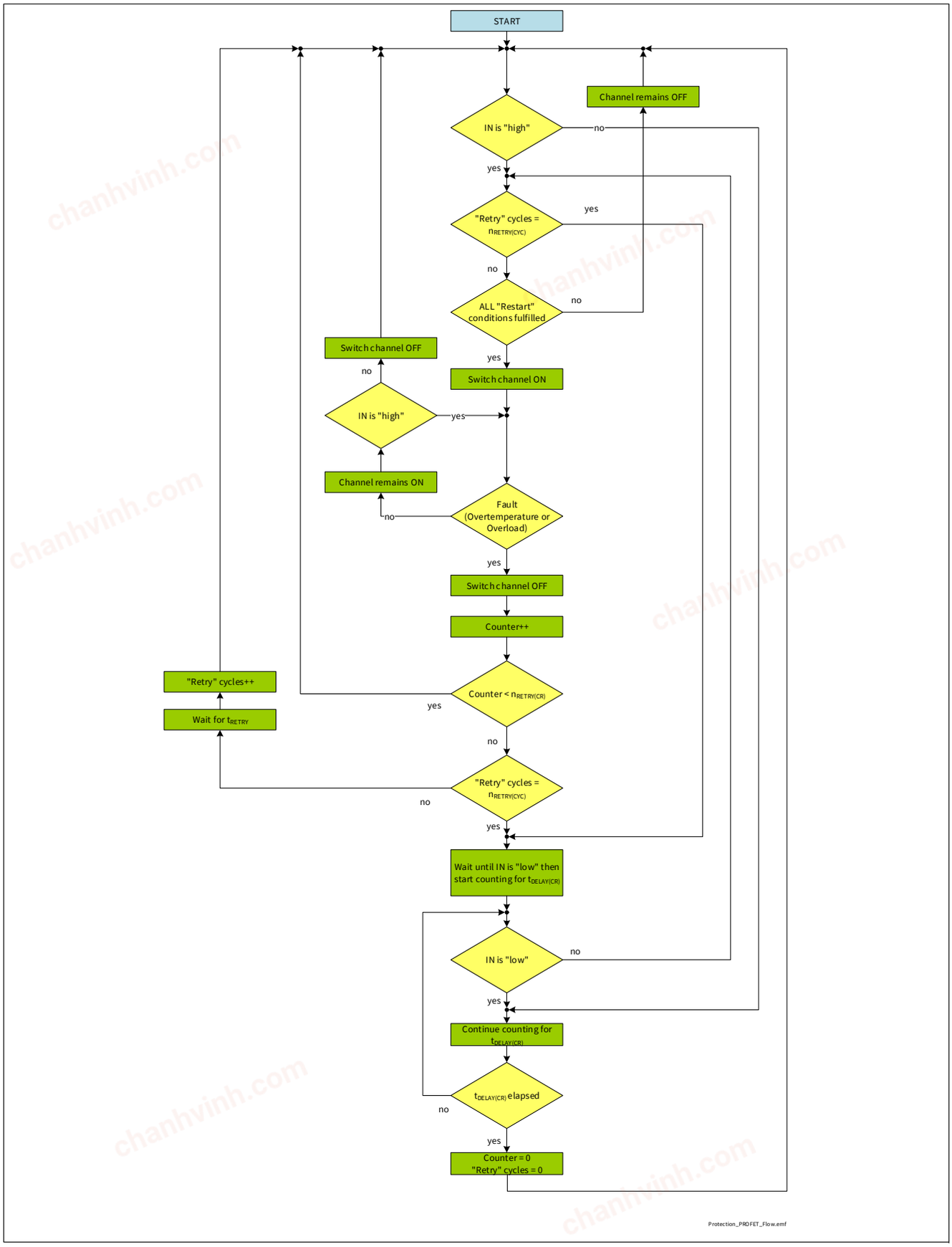


Figure 29 Retry Strategy Flowchart

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It is possible to “force” a reset of the internal counter without waiting for $t_{DELAY(CR)}$ by applying a pulse (rising edge followed by a falling edge) to the DEN pin while IN pin is “low”. The pulse applied to DEN pin must have a duration longer than $t_{DEN(CR)}$ to ensure a reset of the internal counter. The DSEL pin must select the channel that has to be de-latched and keep the same logic value while DEN pin toggles twice (rising edge followed by a falling edge).

The timings are shown in **Figure 30**.

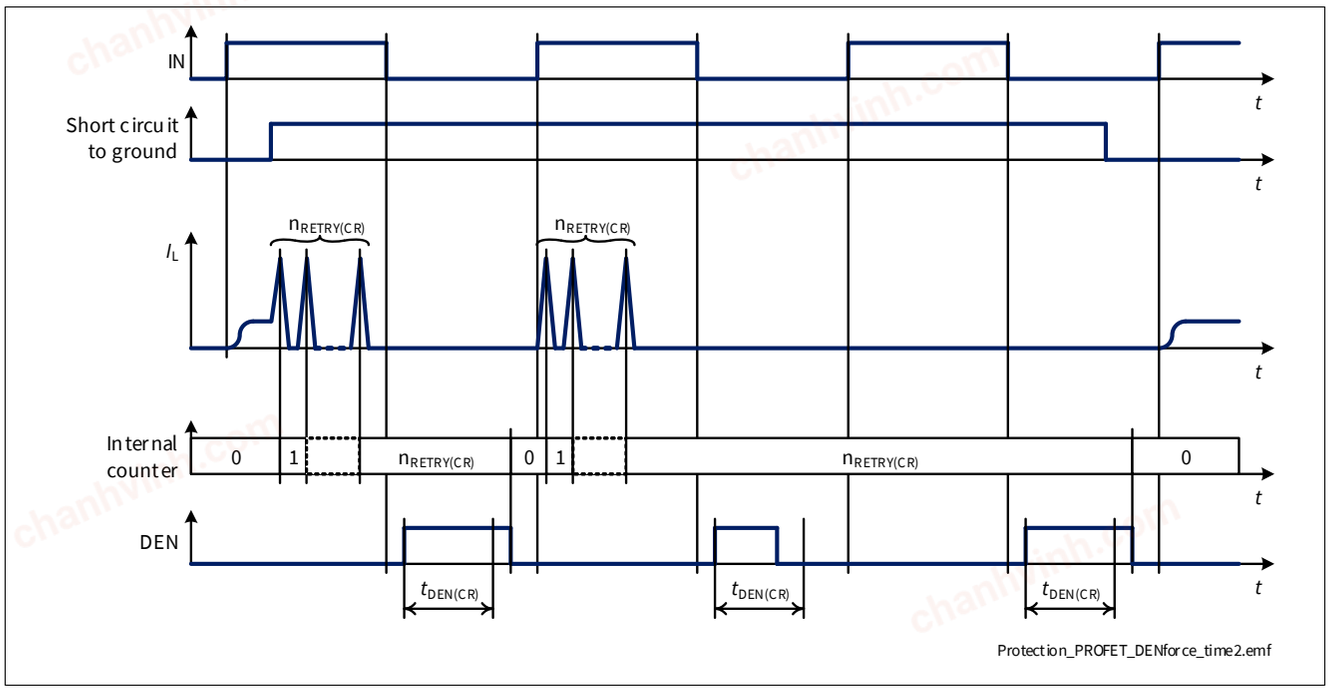


Figure 30 Retry Strategy Timing Diagram with Forced Reset

8.4 Additional protections

8.4.1 Reverse Polarity Protection

In Reverse Polarity condition (also known as Reverse Battery), the output stages are switched ON (see parameter $R_{DS(REV)}$) because of ReverseON feature which limits the power dissipation in the output stages. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the output stages must be limited by the connected loads. The current through Digital Input pins has to be limited as well by an external resistor (please refer to the Absolute Maximum Ratings listed in **Chapter 4.1** and to Application Information in **Chapter 10**).

Figure 31 shows a typical application including a device with ReverseON. A current flowing into GND pin ($-I_{GND}$) during Reverse Polarity condition is necessary to activate ReverseON, therefore a resistive path between module ground and device GND pin must be present.

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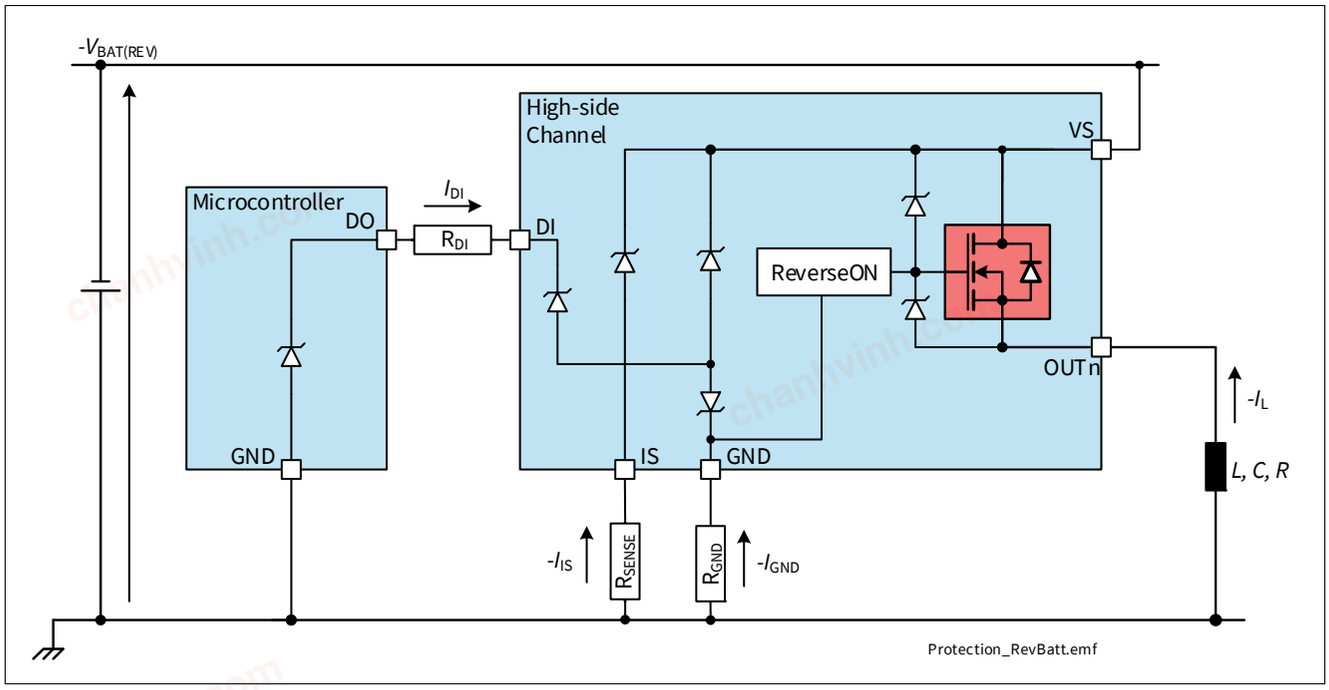


Figure 31 Reverse Battery Protection (application example)

8.4.2 Overvoltage Protection

In the case of supply voltages between $V_{S(EXT,UP)}$ and $V_{BAT(LD)}$, the output transistors are still operational and follow the input pin. In addition to the output clamp for inductive loads as described in **Chapter 7.2.2**, there is a clamp mechanism available for Overvoltage protection for the logic and the output channels, monitoring the voltage between VS and GND pins ($V_{S(CLAMP)}$).

8.5 Protection against loss of connection

8.5.1 Loss of Battery and Loss of Load

The loss of connection to battery or to the load has no influence on device robustness when load and wire harness are purely resistive. In case of driving an inductive load, the energy stored in the inductance must be handled. PROFET™ +2 12V devices can handle the inductivity of the wire harness up to 10 µH with $I_{L(NOM)}$. In case of applications where currents and/or the aforementioned inductivity are exceeded, an external suppressor diode (like diode D_{Z2} shown in **Chapter 10**) is recommended to handle the energy and to provide a well-defined path to the load current.

8.5.2 Loss of Ground

In case of loss of device ground, it is recommended to have a resistor connected between any Digital Input pin and the microcontroller to ensure a channel switch OFF (as described in **Chapter 10**).

Note: In case any Digital Input pin is pulled to ground (either by a resistor or active) a parasitic ground path is available, which could keep the device operational during loss of device ground.

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8.6 Electrical Characteristics Protection

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

R_L = 3.3 Ω

Table 15 Electrical Characteristics: Protection - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Shutdown Temperature (Absolute)	$T_{J(ABS)}$	150	175	200	°C	1)2) See **Figure 22**	P_8.6.0.1
Thermal Shutdown Hysteresis (Absolute)	$T_{HYS(ABS)}$	–	30	–	K	3) See **Figure 22**	P_8.6.0.2
Thermal Shutdown Temperature (Dynamic)	$T_{J(DYN)}$	–	80	–	K	3) See **Figure 23**	P_8.6.0.3
Power Supply Clamping Voltage at T_J = -40 °C	$V_{S(CLAMP)_-40}$	33	36.5	42	V	I_{VS} = 5 mA T_J = -40 °C See **Figure 17**	P_8.6.0.6
Power Supply Clamping Voltage at $T_J \geq$ 25 °C	$V_{S(CLAMP)_25}$	35	38	44	V	2) I_{VS} = 5 mA $T_J \geq$ 25 °C See **Figure 17**	P_8.6.0.7
Power Supply Voltage Threshold for Overcurrent Threshold Reduction in case of Short Circuit	$V_{S(JS)}$	20.5	22.5	24.5	V	3) Setup acc. to AEC-Q100-012	P_8.6.0.8

1) Functional test only.
2) Tested at T_J = 150°C only.
3) Not subject to production test - specified by design.

8.6.1 Electrical Characteristics Protection - PROFET™

Table 16 Electrical Characteristics: Protection - PROFET™

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Automatic Retries in Case of Fault after a Counter Reset	$n_{RETRY(CR)}$	–	5	–		1) See **Figure 27** and **Figure 28**	P_8.6.1.1
Automatic Retries in Case of Fault after the First t_{RETRY} Activation	$n_{RETRY(NT)}$	–	1	–		1) See **Figure 27** and **Figure 28**	P_8.6.1.3
Maximum “Retry” Cycles allowed before Channel Latch OFF	$n_{RETRY(CYC)}$	–	2	–		1) See **Figure 27** and **Figure 28**	P_8.6.1.4

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Table 16 Electrical Characteristics: Protection - PROFET™ (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Auto Retry Time after Fault Condition	t_{RETRY}	40	70	100	ms	1) See **Figure 27** and **Figure 28**	P_8.6.1.5
Counter Reset Delay Time after Fault Condition	$t_{DELAY(CR)}$	40	70	100	ms	1) See **Figure 27** and **Figure 28**	P_8.6.1.6
Minimum DEN Pulse Duration for Counter Reset	$t_{DEN(CR)}$	50	100	150	µs	2) See **Figure 30**	P_8.6.1.7

1) Functional test only.

2) Not subject to production test - specified by design.

8.7 Electrical Characteristics Protection - Power Output Stages

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

R_L = 3.3 Ω

8.7.1 Protection Power Output Stage - 40 mΩ

Table 17 Electrical Characteristics: Protection - 40 mΩ

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overload Detection Current at T_J = -40 °C	$I_{L(OVL0)_-40}$	42	47	52	A	1) T_J = -40 °C dI/dt = 0.2 A/µs see **Figure 24** and **Figure 25**	P_8.7.6.1
Overload Detection Current at T_J = 25 °C	$I_{L(OVL0)_25}$	40	46	52	A	2) T_J = 25 °C dI/dt = 0.2 A/µs see **Figure 24** and **Figure 25**	P_8.7.6.7
Overload Detection Current at T_J = 150 °C	$I_{L(OVL0)_150}$	34	39	45	A	2) T_J = 150 °C dI/dt = 0.2 A/µs see **Figure 24** and **Figure 25**	P_8.7.6.8

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Table 17 Electrical Characteristics: Protection - 40 mΩ (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overload Detection Current at High V_{DS}	$I_{L(OVL1)}$	–	26	–	A	2) dI/dt = 0.2 A/µs see **Figure 24**	P_8.7.6.5
Overload Detection Current Jump Start Condition	$I_{L(OVL_JS)}$	–	26	–	A	2) $V_S > V_{S(JS)}$ dI/dt = 0.2 A/µs see **Figure 26**	P_8.7.6.6

1) Functional test only.
2) Not subject to production test - specified by design.

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9 Diagnosis

For diagnosis purpose, the BTS7040-2EPA provides a combination of digital and analog signals at pin IS. These signals are generically named SENSE and written I_{IS}. In case of disabled diagnostic (DEN pin set to “low”), IS pin becomes high impedance.

A sense resistor R_{SENSE} must be connected between IS pin and module ground if the current sense diagnosis is used. R_{SENSE} value has to be higher than 820 Ω (or 400 Ω when a central Reverse Battery protection is present on the battery feed) to limit the power losses in the sense circuitry. A typical value is R_{SENSE} = 1.2 kΩ.

Due to the internal connection between IS pin and V_S supply voltage, it is not recommended to connect the IS pin to the sense current output of other devices, if they are supplied by a different battery feed.

See **Figure 32** for details as an overview.

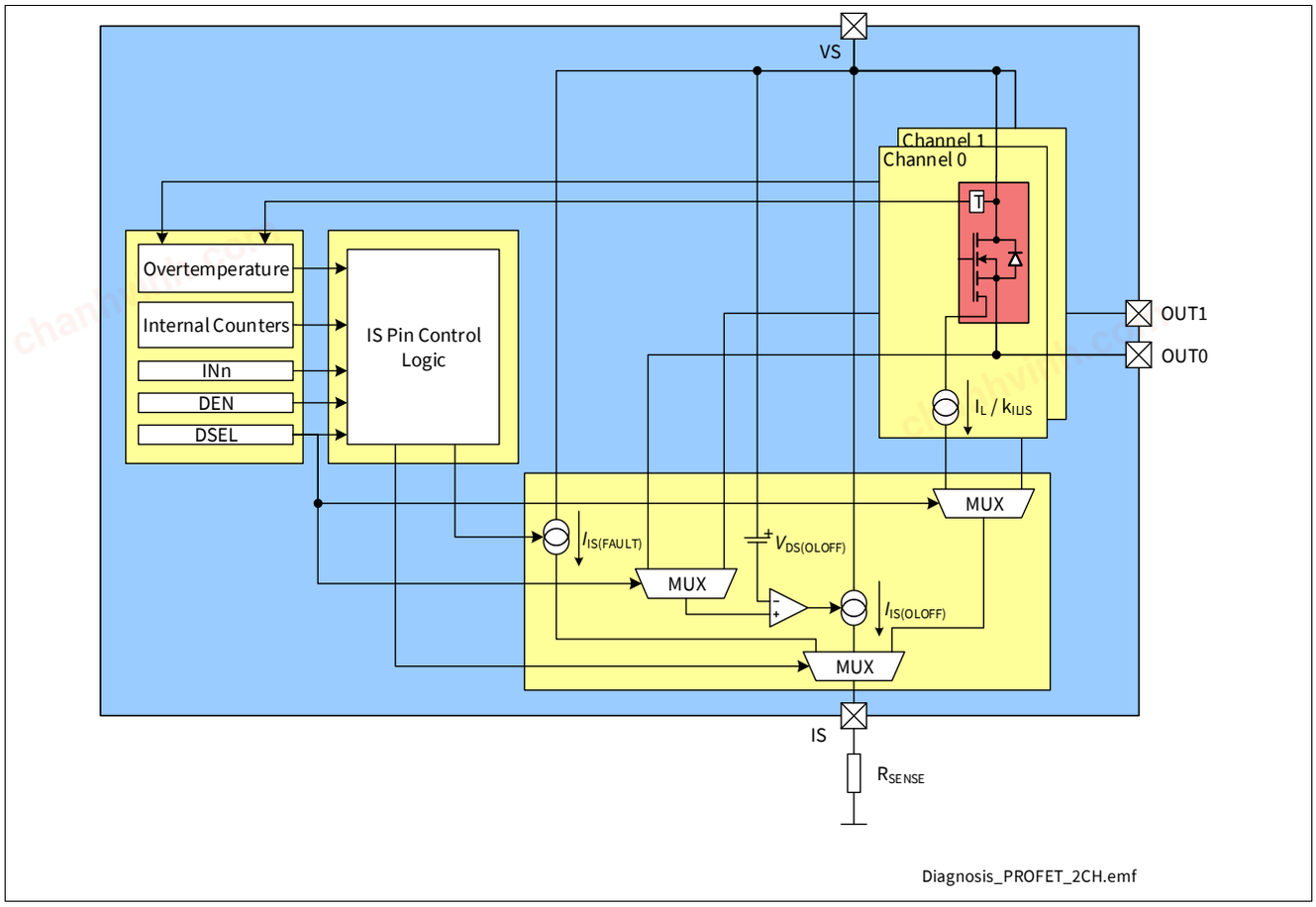


Figure 32 Diagnosis Block Diagram

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9.1 Overview

Table 18 gives a quick reference to the state of the IS pin during BTS7040-2EPA operation.

Table 18 SENSE Signal, Function of Application Condition

Application Condition	Input level	DEN level	V_{OUT}	Diagnostic Output
Normal operation	“low”	“high”	~ GND	Z $I_{IS(FAULT)}$ if counter > 0
Short circuit to GND			~ GND	Z $I_{IS(FAULT)}$ if counter > 0
Overtemperature			Z	$I_{IS(FAULT)}$
Short circuit to V_S			V_S	$I_{IS(OLOFF)}$ ($I_{IS(FAULT)}$ if counter > 0)
Open Load			< V_S - $V_{DS(OLOFF)}$ > V_S - $V_{DS(OLOFF)}$ [1]	Z $I_{IS(OLOFF)}$ (in both cases $I_{IS(FAULT)}$ if counter > 0)
Inverse current			~ V_{INV} = V_{OUT} > V_S	$I_{IS(OLOFF)}$ ($I_{IS(FAULT)}$ if counter > 0)
Normal operation	“high”		~ V_S	$I_{IS} = I_L / k_{ILIS}$
Overcurrent			< V_S	$I_{IS(FAULT)}$
Short circuit to GND			~ GND	$I_{IS(FAULT)}$
Overtemperature			Z	$I_{IS(FAULT)}$
Short circuit to V_S			V_S	$I_{IS} < I_L / k_{ILIS}$
Open Load			~ V_S [2]	$I_{IS} = I_{IS(EN)}$
Under load (e.g. Output Voltage Limitation condition)			~ V_S [3]	$I_{IS(EN)} < I_{IS} < I_{L(NOM)} / k_{ILIS}$
Inverse current			~ V_{INV} = V_{OUT} > V_S	$I_{IS} = I_{IS(EN)}$
All conditions	n.a.	“low”	n.a.	Z

1) With additional pull-up resistor.
2) The output current has to be smaller than $I_{L(OL)}$.
3) The output current has to be higher than $I_{L(OL)}$.

9.1.1 SENSE signal truth table

In case DEN is set to “high”, the SENSE for the selected channel is enabled or disabled using DSEL pin. Table 19 gives the truth table.

Table 19 Diagnostic Truth Table

DEN	DSEL	IS
“low”	not relevant	Z
“high”	“low”	SENSE output 0
“high”	“high”	SENSE output 1

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9.2 Diagnosis in ON state

A current proportional to the load current (ratio $k_{ILIS} = I_L / I_{IS}$) is provided at pin IS when the following conditions are fulfilled:

- The power output stage is switched ON with $V_{DS} < V_{DS(OLOFF)}$
- The diagnosis is enabled for that channel
- No fault (as described in **Chapter 8.3**) is present or was present and not cleared yet (see **Chapter 9.2.2** for further details)

If a “hard” failure mode is present or was present and not cleared yet a current $I_{IS(FAULT)}$ is provided at IS pin.

9.2.1 Current Sense (k_{ILIS})

The accuracy of the sense current depends on temperature and load current. I_{IS} increases linearly with I_L output current until it reaches the saturation current $I_{IS(SAT)}$. In case of Open Load at the output stage (I_L close to 0 A), the maximum sense current $I_{IS(EN)}$ (no load, diagnosis enabled) is specified. This condition is shown in **Figure 34**. The blue line represents the ideal k_{ILIS} line, while the red lines show the behavior of a typical product.

An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1 µs for the RC filter is recommended).

The k_{ILIS} factor is specified with limits that take into account effects due to temperature, supply voltage and manufacturing process. Tighter limits are possible (within a defined current window) with calibration:

- A well-defined and precise current ($I_{L(CAL)}$) is applied at the output during End of Line test at customer side
- The corresponding current at IS pin is measured and the k_{ILIS} is calculated (k_{ILIS} @ $I_{L(CAL)}$)
- Within the current range going from $I_{L(CAL)_L}$ to $I_{L(CAL)_H}$ the k_{ILIS} is equal to k_{ILIS} @ $I_{L(CAL)}$ with limits defined by Δk_{ILIS}

The derating of k_{ILIS} after calibration is calculated using the formulas in **Figure 33** and it is specified by Δk_{ILIS}

$$\Delta k_{ILIS,MAX} = 100 \cdot MAX\left(\frac{k_{ILIS}@I_{L(CAL)_L}}{k_{ILIS}@I_{L(CAL)}} - 1, \frac{k_{ILIS}@I_{L(CAL)_H}}{k_{ILIS}@I_{L(CAL)}} - 1\right)$$

$$\Delta k_{ILIS,MIN} = 100 \cdot MIN\left(\frac{k_{ILIS}@I_{L(CAL)_L}}{k_{ILIS}@I_{L(CAL)}} - 1, \frac{k_{ILIS}@I_{L(CAL)_H}}{k_{ILIS}@I_{L(CAL)}} - 1\right)$$

Diagnosis_dkILIS.emf

Figure 33 Δk_{ILIS} calculation formulas

The calibration is intended to be performed at $T_{A(CAL)}$ = 25°C. The parameter Δk_{ILIS} includes the drift overtemperature as well as the drift over the current range from $I_{L(CAL)_L}$ to $I_{L(CAL)_H}$.

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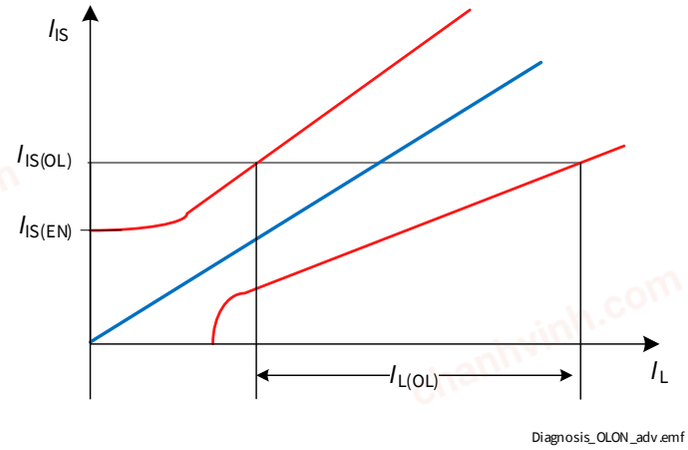


Figure 34 Current Sense Ratio in Open Load at ON condition

9.2.2 Fault Current ($I_{IS(FAULT)}$)

As soon a protection event occurs, changing the value of the internal retry counter (see **Chapter 8.3** for more details) from its reset state, a current $I_{IS(FAULT)}$ is provided by pin IS when DEN is set to “high” and the affected channel is selected. The following 3 situations may occur:

- If the channel is ON and the number of retries is lower than “$n_{RETRY(CR)} + n_{RETRY(CYC)} * n_{RETRY(NT)}$”, the current $I_{IS(FAULT)}$ is provided for a time $t_{IS(FAULT)_D}$ after the channel is allowed to restart, after which $I_{IS} = I_L / k_{ILIS}$ (as shown in **Figure 35**). During a retry cycle (while timer t_{RETRY} is running) the current $I_{IS(FAULT)}$ is provided each time the channel diagnosis is checked
- If the channel is ON and the number of retries is equal than “$n_{RETRY(CR)} + n_{RETRY(CYC)} * n_{RETRY(NT)}$”, the current $I_{IS(FAULT)}$ is provided until the internal counter is reset (either by expiring of $t_{DELAY(CR)}$ time or by DEN pin pulse, as described in **Chapter 8.3.1**)
- If the channel is OFF and the internal counter is not in the reset state, the current $I_{IS(FAULT)}$ is provided each time the channel diagnosis is checked

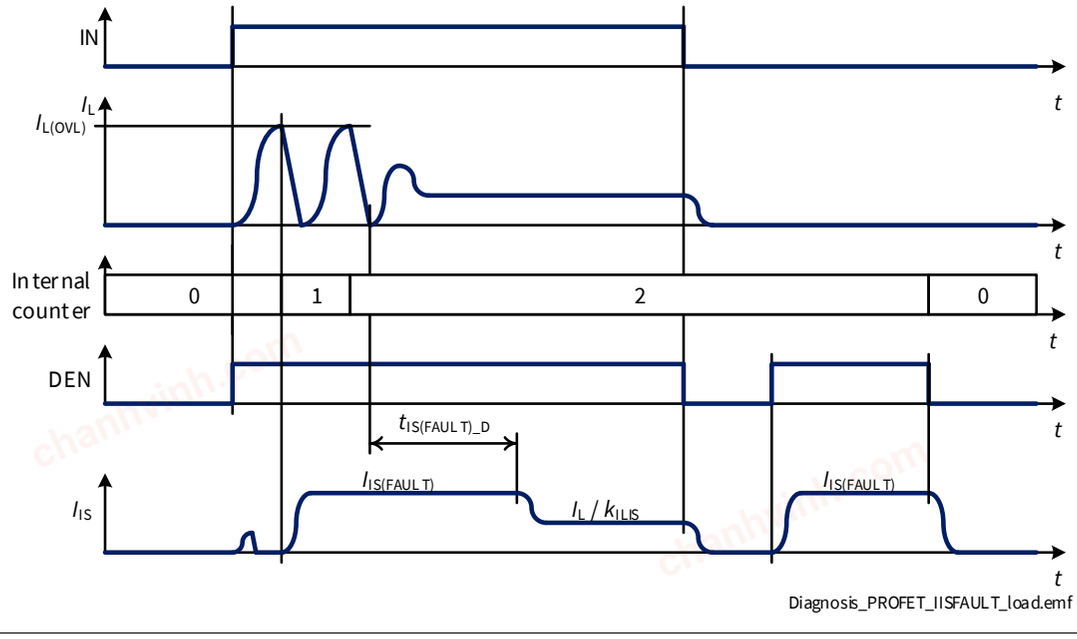


Figure 35 $I_{IS(FAULT)}$ at Load Switching

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Figure 36 adds the behavior of SENSE signal to the timing diagram seen in **Figure 28**, while **Figure 37** shows the relation between $I_{IS} = I_L / k_{ILIS}$, $I_{IS(SAT)}$ and $I_{IS(FAULT)}$.

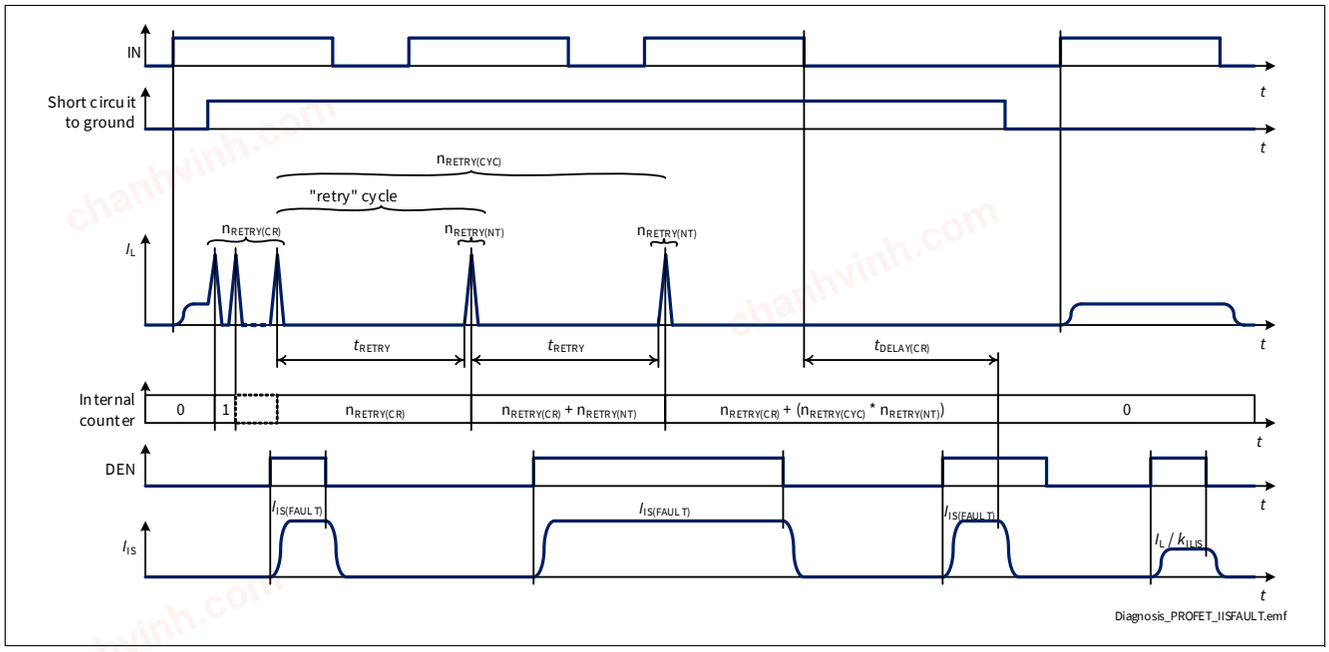


Figure 36 SENSE behavior in Fault condition

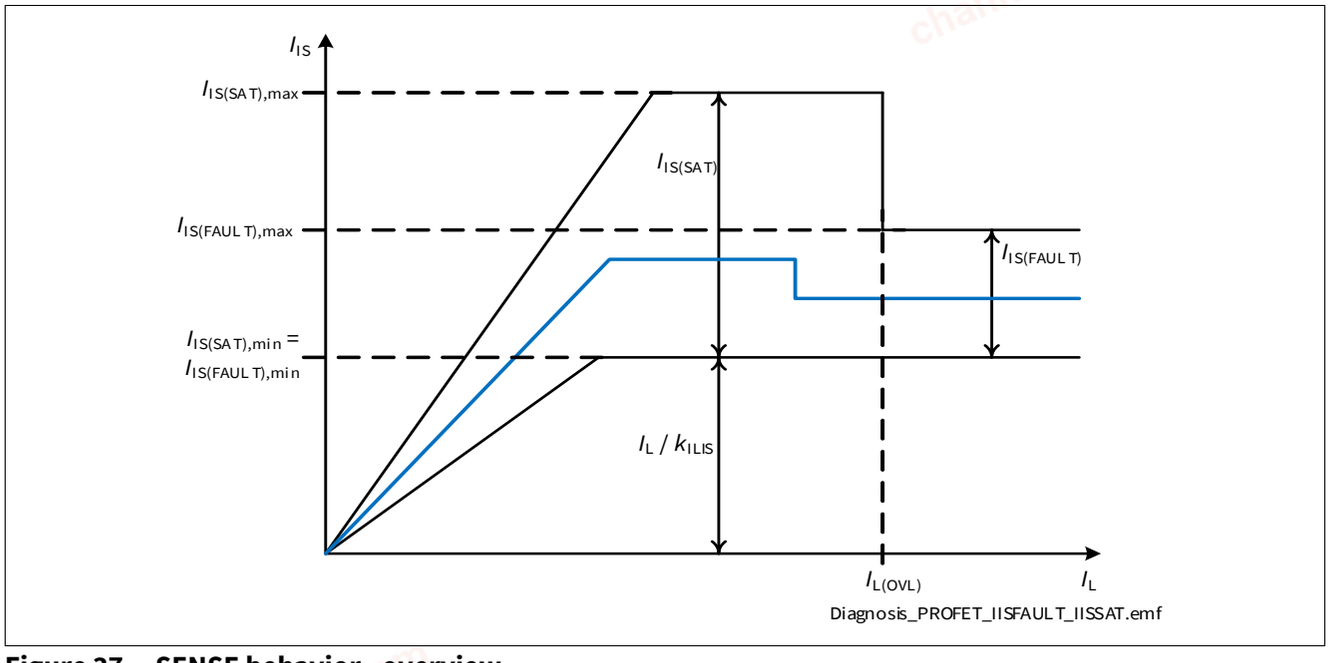


Figure 37 SENSE behavior - overview

9.3 Diagnosis in OFF state

When a power output stage is in OFF state, the BTS7040-2EPA can measure the output voltage and compare it with a threshold voltage. In this way, using some additional external components (a pull-down resistor and a switchable pull-up current source), it is possible to detect if the load is missing or if there is a short circuit to battery. If a Fault condition was detected by the device (the internal counter has a value different from the reset value, as described in **Chapter 9.2.2**) a current $I_{IS(FAULT)}$ is provided by IS pin each time the channel diagnosis is checked also in OFF state.

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9.3.1 Open Load current ($I_{IS(OLOFF)}$)

In OFF state, when DEN pin is set to “high” and a channel is selected using DSEL pin, the V_{DS} voltage is compared with a threshold voltage $V_{DS(OLOFF)}$. If the load is properly connected and there is no short circuit to battery, V_{DS} ~ V_S therefore V_{DS} > $V_{DS(OLOFF)}$. When the diagnosis is active and V_{DS} ≤ $V_{DS(OLOFF)}$, a current $I_{IS(OLOFF)}$ is provided by IS pin. **Figure 38** shows the relationship between $I_{IS(OLOFF)}$ and $I_{IS(FAULT)}$ as functions of V_{DS}. The two currents do not overlap making it always possible to differentiate between Open Load in OFF and Fault condition.

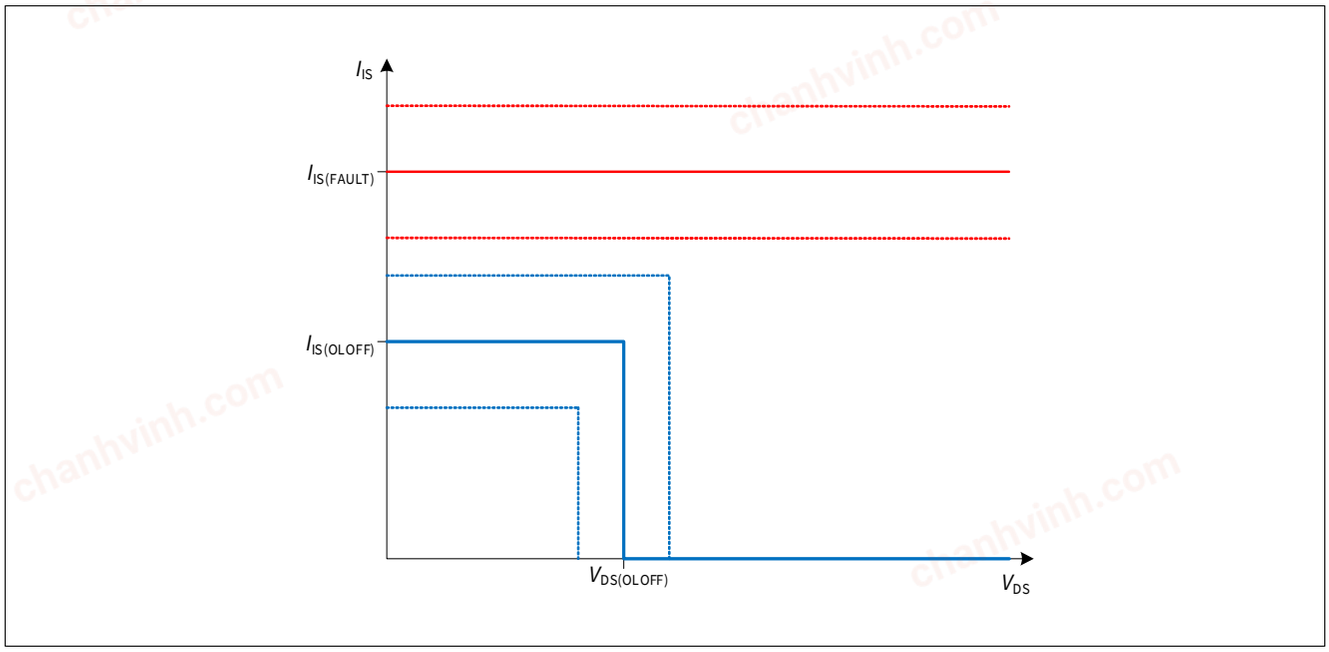


Figure 38 I_{IS} in OFF State

It is necessary to wait a time $t_{IS(OLOFF)_D}$ between the falling edge of the input pin and the sensing at pin IS for Open Load in OFF diagnosis to allow the internal comparator to settle. In **Figure 39** the timings for an Open Load detection are shown - the load is always disconnected.

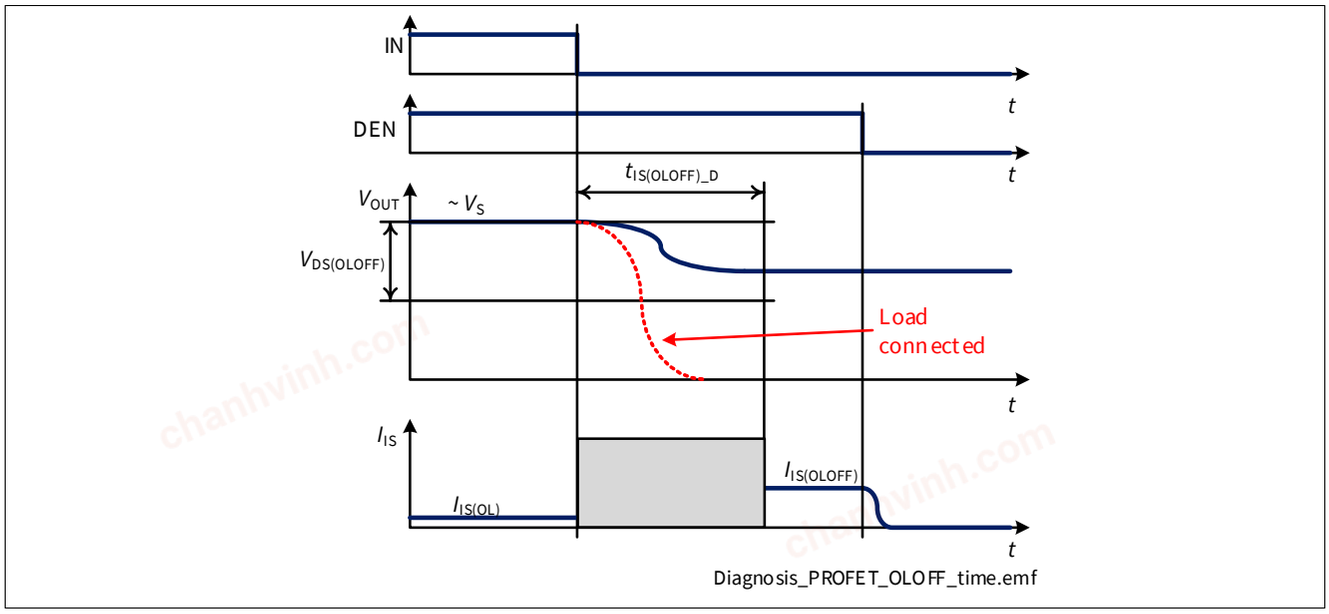


Figure 39 Open Load in OFF Timings - load disconnected

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9.4 SENSE Timings

Figure 40 and **Figure 42** show the timing during settling $t_{sIS(ON)}$ and disabling $t_{sIS(OFF)}$ of the SENSE (including the case of load change). As a proper signal cannot be established before the load current is stable (therefore before t_{ON}), $t_{sIS(DIAG)} = t_{sIS(ON)} + t_{ON}$.

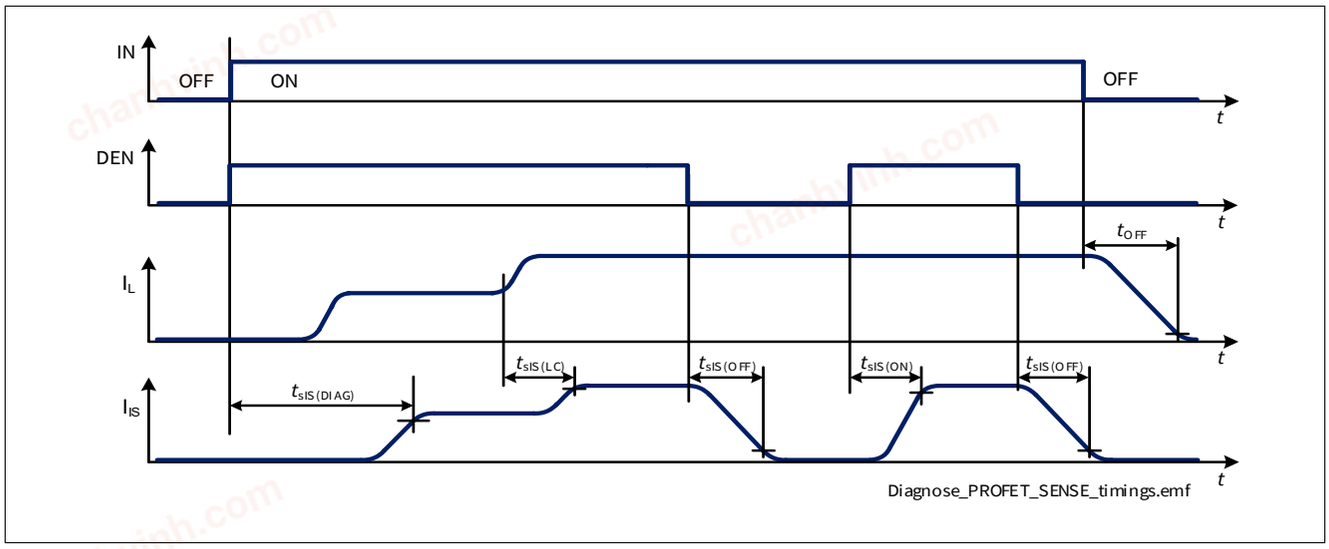


Figure 40 SENSE Settling / Disabling Timing

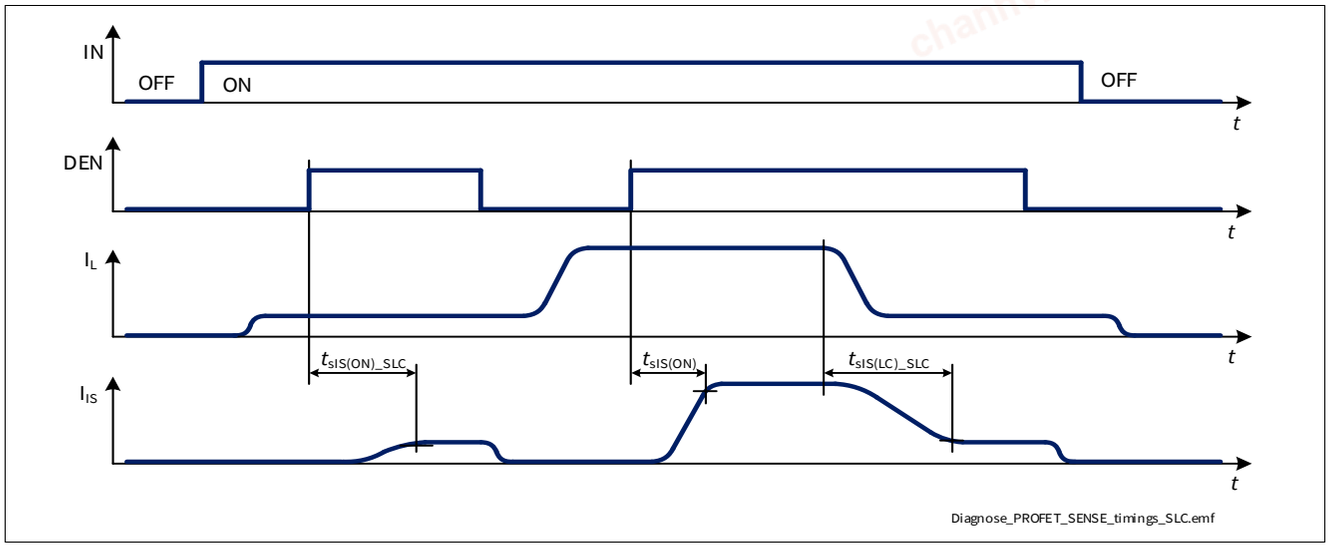


Figure 41 SENSE Timing with Small Load Current

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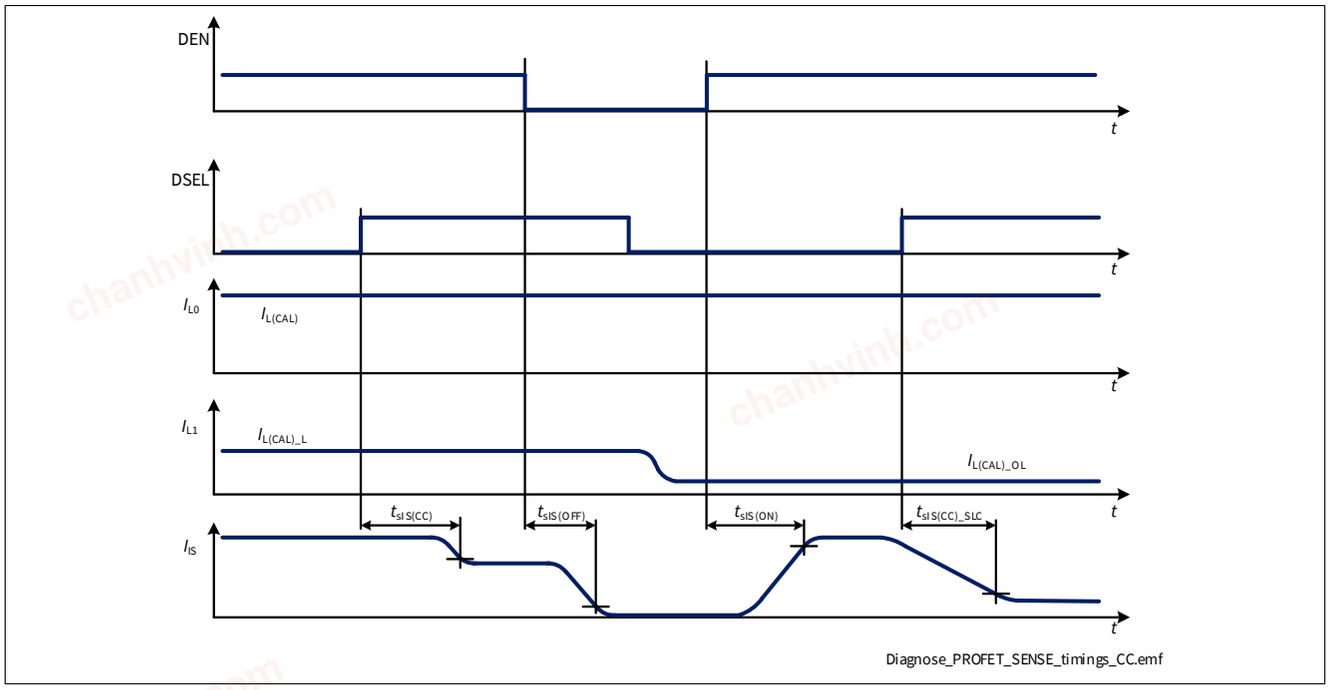


Figure 42 SENSE Settling Timing - Channel Change

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9.5 Electrical Characteristics Diagnosis

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

R_L = 3.3 Ω

Table 20 Electrical Characteristics: Diagnosis - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SENSE Saturation Current	$I_{IS(SAT)}$	4.4	–	15	mA	[1] V_S = 8 V to 18 V R_{SENSE} = 1.2 kΩ See **Figure 37**	P_9.6.0.13
SENSE Saturation Current	$I_{IS(SAT)}$	4.1	–	15	mA	[1] V_S = 6 V to 18 V R_{SENSE} = 1.2 kΩ See **Figure 37**	P_9.6.0.14
SENSE Leakage Current when Disabled	$I_{IS(OFF)}$	–	0.01	0.5	µA	DEN = “low” $I_L \geq I_{L(NOM)}$ V_{IS} = 0 V	P_9.6.0.2
SENSE Leakage Current when Enabled at $T_J \leq 85$ °C	$I_{IS(EN)_85}$	–	0.2	1	µA	[1] $T_J \leq 85$ °C DEN = “high” I_L = 0 A See **Figure 34**	P_9.6.0.3
SENSE Leakage Current when Enabled at T_J = 150 °C	$I_{IS(EN)_150}$	–	0.2	1	µA	T_J = 150 °C DEN = “high” I_L = 0 A See **Figure 34**	P_9.6.0.4
Saturation Voltage in k_{ILIS} Operation (V_S - V_{IS})	V_{SIS_k}	–	0.5	1	V	[1] V_S = 6 V IN = DEN = “high” $I_L \leq 1.2 * I_{L(NOM)}$	P_9.6.0.6
Saturation Voltage in Open Load at OFF Diagnosis (V_S - V_{IS})	V_{SIS_OL}	–	0.5	1	V	[1] V_S = 6 V IN = “low” DEN = “high”	P_9.6.0.7
Saturation Voltage in Fault Diagnosis (V_S - V_{IS})	V_{SIS_F}	–	0.5	1	V	[1] V_S = 6 V IN = “low” DEN = “high” counter >0	P_9.6.0.8

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Table 20 Electrical Characteristics: Diagnosis - General (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply to IS Pin Clamping Voltage at T_J = -40 °C	$V_{SIS(CLAMP)_-40}$	33	36.5	42	V	I_{IS} = 1 mA T_J = -40 °C See **Figure 17**	P_9.6.0.9
Power Supply to IS Pin Clamping Voltage at $T_J \geq$ 25 °C	$V_{SIS(CLAMP)_25}$	35	38	44	V	2) I_{IS} = 1 mA $T_J \geq$ 25 °C See **Figure 17**	P_9.6.0.10

1) Not subject to production test - specified by design.
2) Tested at T_J = 150°C.

9.5.1 Electrical Characteristics Diagnosis - PROFET™

Table 21 Electrical Characteristics: Diagnosis - PROFET™

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SENSE Fault Current	$I_{IS(FAULT)}$	4.4	5.5	10	mA	See **Figure 37** and **Figure 38**	P_9.6.1.1
SENSE Open Load in OFF Current	$I_{IS(OLOFF)}$	1.9	2.5	3.5	mA	See **Figure 37** and **Figure 38**	P_9.6.1.2
SENSE Delay Time at Channel Switch ON after Last Fault Condition	$t_{IS(FAULT)_D}$	–	500	–	µs	1) See **Figure 35**	P_9.6.1.3
SENSE Open Load in OFF Delay Time	$t_{IS(OLOFF)_D}$	30	70	120	µs	$V_{DS} < V_{OL(OFF)}$ from IN falling edge to $I_{IS} = I_{S(OLOFF),MIN} * 0.9$ DEN = “high” counter = 0 See **Figure 39**	P_9.6.1.4
Open Load V_{DS} Detection Threshold in OFF State	$V_{DS(OLOFF)}$	1.3	1.8	2.3	V	See **Figure 38**	P_9.6.1.5
SENSE Settling Time with Nominal Load Current Stable	$t_{sIS(ON)}$	–	5	20	µs	$I_L = I_{L(CAL)}$ from DEN rising edge to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) * 0.9$ See **Figure 40**	P_9.6.1.6
SENSE Settling Time with Small Load Current Stable	$t_{sIS(ON)_SLC}$	–	–	60	µs	1) $I_L = I_{L(CAL)_OL}$ from DEN rising edge to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) * 0.9$	P_9.6.1.13

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Table 21 Electrical Characteristics: Diagnosis - PROFET™ (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SENSE Disable Time	$t_{sIS(OFF)}$	–	5	20	µs	[1] From DEN falling edge to $I_{IS} = I_{IS(OFF)}$ See **Figure 40**	P_9.6.1.8
SENSE Settling Time after Load Change	$t_{sIS(LC)}$	–	5	20	µs	[1] from $I_L = I_{L(CAL)_L}$ to $I_L = I_{L(CAL)}$ (see $\Delta k_{ILIS(NOM)}$) See **Figure 40**	P_9.6.1.9
SENSE Settling Time after Load Change with Small Load Current	$t_{sIS(LC)_SLC}$	–	250	400	µs	[1] DEN = “high” from Load Change to $I_{IS} = I_L / (k_{ILIS} @ I_L)$ from $I_{L(CAL)}$ to $I_{L(CAL)_OL}$	P_9.6.1.14
SENSE Settling Time after Channel Change	$t_{sIS(CC)}$	–	5	20	µs	[1] Start channel: $I_L = I_{L(CAL)}$ End channel: $I_L = I_{L(CAL)_L}$ (see $\Delta k_{ILIS(NOM)}$) See **Figure 42**	P_9.6.1.10
SENSE Settling Time after Channel Change with Small Load Current	$t_{sIS(CC)_SLC}$	–	–	60	µs	[1] DEN = “high” from DSEL toggling to $I_{IS} = I_L / (k_{ILIS,MIN} @ I_L) * 1.1$ Start channel: $I_L = I_{L(CAL)}$ End Channel: $I_L = I_{L(CAL)_OL}$ (see $\Delta k_{ILIS(NOM)}$ and $\Delta k_{ILIS(OL)}$)	P_9.6.1.15

1) Not subject to production test - specified by design.

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9.6 Electrical Characteristics Diagnosis - Power Output Stages

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

R_L = 3.3 Ω

9.6.1 Diagnosis Power Output Stage - 40 mΩ

Table 22 Electrical Characteristics: Diagnosis - 40 mΩ

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Open Load Output Current at I_{IS} = 4 µA	$I_{L(OL)_4u}$	1	6	11	mA	$I_{IS} = I_{IS(OL)}$ = 4 µA See **Figure 34**	P_9.7.6.1
Current Sense Ratio at $I_L = I_{L02}$	k_{ILIS02}	-26.0%	1750	+26.0%		I_{L02} = 20 mA	P_9.7.6.6
Current Sense Ratio at $I_L = I_{L04}$	k_{ILIS04}	-23.5%	1750	+23.5%		I_{L04} = 50 mA	P_9.7.6.8
Current Sense Ratio at $I_L = I_{L05}$	k_{ILIS05}	-20.5%	1750	+20.5%		I_{L05} = 100 mA	P_9.7.6.9
Current Sense Ratio at $I_L = I_{L08}$	k_{ILIS08}	-19.0%	1750	+19.0%		I_{L08} = 250 mA	P_9.7.6.12
Current Sense Ratio at $I_L = I_{L11}$	k_{ILIS11}	-9.5%	1800	+9.5%		I_{L11} = 1 A	P_9.7.6.15
Current Sense Ratio at $I_L = I_{L13}$	k_{ILIS13}	-6.0%	1800	+6.0%		I_{L13} = 2 A	P_9.7.6.17
Current Sense Ratio at $I_L = I_{L15}$	k_{ILIS15}	-4.5%	1800	+4.5%		I_{L15} = 4 A	P_9.7.6.19
SENSE Current Derating with Low Current Calibration	$\Delta k_{ILIS(OL)}$	-30	0	+30	%	1) $I_{L(CAL)_OL} = I_{L04}$ $I_{L(CAL)_OL_H} = I_{L05}$ $I_{L(CAL)_OL_L} = I_{L02}$ $T_{A(CAL)}$ = 25 °C See **Figure 33**	P_9.7.6.27
SENSE Current Derating with Nominal Current Calibration	$\Delta k_{ILIS(NOM)}$	-4	0	+4	%	1) $I_{L(CAL)} = I_{L13}$ $I_{L(CAL)_H} = I_{L15}$ $I_{L(CAL)_L} = I_{L11}$ $T_{A(CAL)}$ = 25 °C See **Figure 33**	P_9.7.6.29

1) Not subject to production test - specified by design.

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10 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

10.1 Application Setup

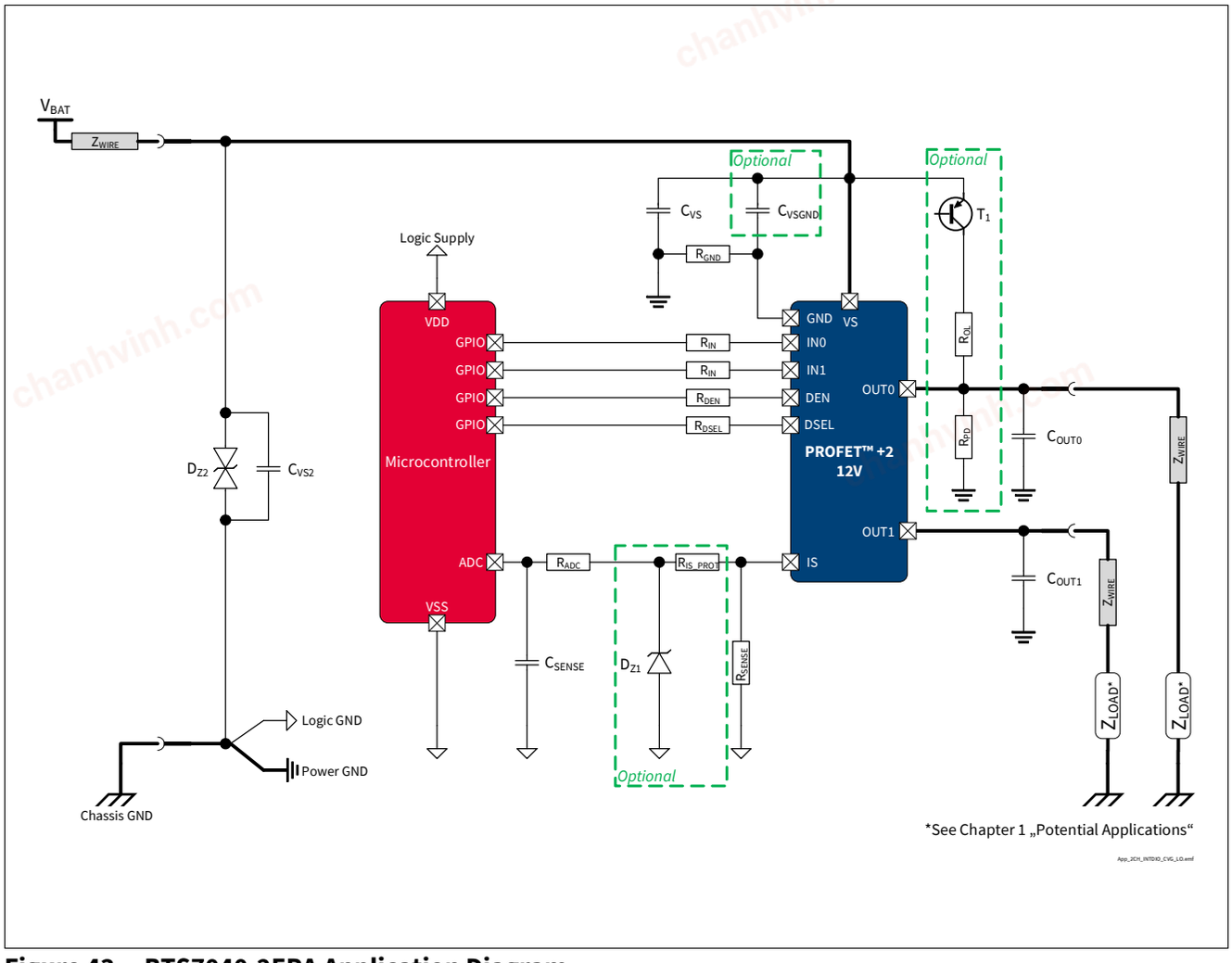


Figure 43 BTS7040-2EPA Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 23 Loads considered for Reverse Polarity setup (see P_4.1.0.5)

Output	$R_{DS(ON),max}$ @ T_J = 150 °C	Load connected
40 mΩ	36 mΩ	P27W + R5W

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10.2 External Components

Table 24 Suggested Component values

Reference	Value	Purpose
R_{IN}	4.7 kΩ	Protection of the microcontroller during Overvoltage and Reverse Polarity Necessary to switch OFF BTS7040-2EPA output during Loss of Ground
R_{DEN}	4.7 kΩ	Protection of the microcontroller during Overvoltage and Reverse Polarity Necessary to switch OFF BTS7040-2EPA output during Loss of Ground
R_{DSEL}	4.7 kΩ	Protection of the microcontroller during Overvoltage and Reverse Polarity Necessary to switch OFF BTS7040-2EPA output during Loss of Ground
R_{PD}	47 kΩ	Output polarization (pull-down) Ensures polarization of BTS7040-2EPA outputs to distinguish between Open Load and Short to V_S in OFF Diagnosis
R_{OL}	1.5 kΩ	Output polarization (pull-up) Ensures polarization of BTS7040-2EPA output during Open Load in OFF diagnosis
C_{OUT}	10 nF	Protection of BTS7040-2EPA output during ESD events and BCI
T_1	BC 807	Switch the battery voltage for Open Load in OFF diagnosis
C_{VS}	100 nF	Filtering of voltage spikes on the battery line
C_{VSGND}	47 nF	Buffer capacitor for fast transient See **Table 5** (P_4.3.0.7) for the boundary conditions A placeholder on PCB layout is recommended
D_{Z2}	33 V TVS Diode	Transient Voltage Suppressor diode Protection during Overvoltage and in case of Loss of Battery while driving an inductive load
C_{VS2}	–	Filtering / buffer capacitor located at V_{BAT} connector
R_{SENSE}	1.2 kΩ	SENSE resistor
R_{IS_PROT}	4.7 kΩ	Protection during Overvoltage, Reverse Polarity, Loss of Ground Value to be tuned according to microcontroller specifications
D_{Z1}	7 V Z-Diode	Protection of microcontroller during Overvoltage
R_{ADC}	4.7 kΩ	Protection of microcontroller ADC input during Overvoltage, Reverse Polarity, Loss of Ground Value to be tuned according to microcontroller specifications
C_{SENSE}	220 pF	Sense signal filtering A time constant (R_{ADC} * C_{SENSE}) longer than 1 µs is recommended
R_{GND}	47 Ω	Protection in case of Overvoltage and Loss of Battery while driving inductive loads

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10.3 Further Application Information

- Please contact us for information regarding the Pin FMEA
- For further information you may contact **http://www.infineon.com/**

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11 Package Outlines

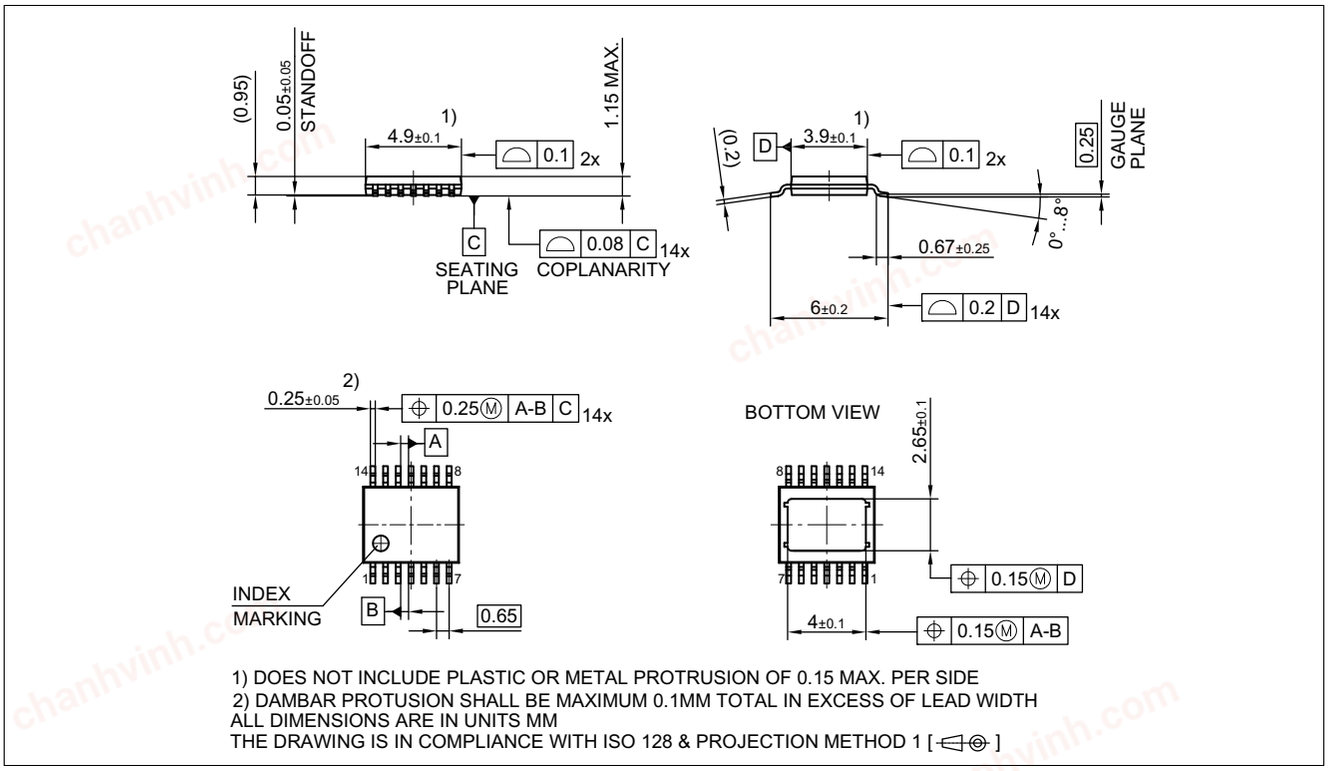


Figure 44 PG-TSDSO-14 (Thin (Slim) Dual Small Outline 14 pins) **Package Outline**

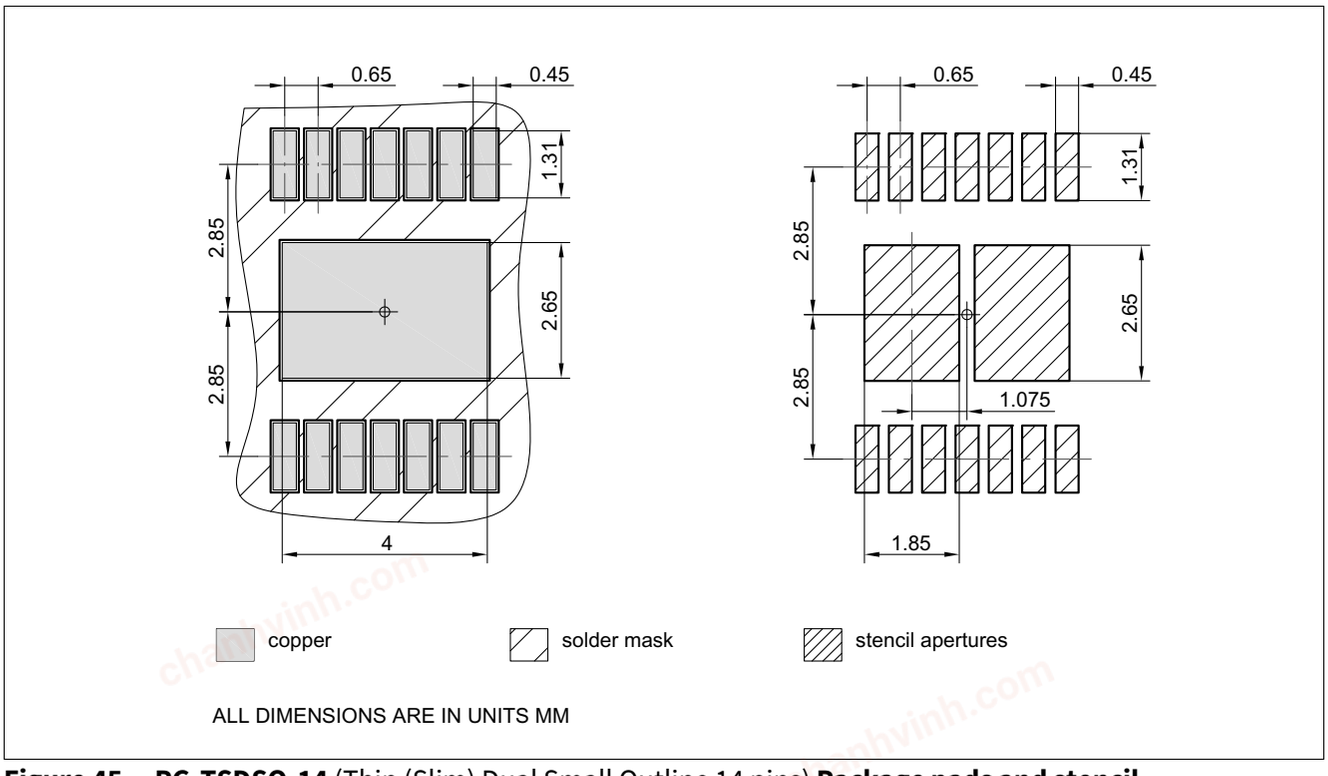


Figure 45 PG-TSDSO-14 (Thin (Slim) Dual Small Outline 14 pins) **Package pads and stencil**

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Package Outlines

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

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12 Revision History

Table 25 BTS7040-2EPA - List of changes

Revision	Changes
1.10, 2020-12-14	Typo fixed (PROFET™+2 → PROFET™ +2) **Figure 26**, **Figure 38** updated **Chapter 8.2** updated **Chapter 8.4.1** updated (typo fixed) P_9.6.0.6 updated (Parameter: SENSE Operative Range for k_{ILIS} Operation (V_S - V_{IS}) → Saturation Voltage in k_{ILIS} Operation (V_S - V_{IS})) P_9.6.0.7 updated (Parameter: SENSE Operative Range for Open Load at OFF Diagnosis (V_S - V_{IS}) → Saturation Voltage in Open Load at OFF Diagnosis (V_S - V_{IS})) P_9.6.0.8 updated (Parameter: SENSE Operative Range for Fault Diagnosis (V_S - V_{IS}) → Saturation Voltage in Fault Diagnosis (V_S - V_{IS}))
1.06, 2019-10-30	P_9.7.6.15 updated (Min./Typ./Max.: -9.7%/1805/+9.7% → -9.5%/1800/+9.5%) P_9.7.6.17, P_9.7.6.19 updated (Typ.: 1805 → 1800)
1.05, 2019-10-15	P_8.7.6.1, P_8.7.6.7, P_8.7.6.8 updated (added in Note or Test Condition: link to **Figure 25**) P_8.7.6.6 updated (added in Note or Test Condition: link to **Figure 26**) P_7.5.6.4, P_7.5.6.5 updated (added in Note or Test Condition: DEN = “low”; link to **Figure 19**) P_7.5.6.12 updated (added in Note or Test Condition: see **Figure 21**; deleted unnecessary space in Symbol: |dVOUT / dt | → |dVOUT / dt|) P_9.7.6.1 updated (added in Note or Test Condition: See **Figure 34**) P_9.7.6.6 updated (Min./Typ./Max.: -40%/1800/+40% → -26.0%/1750/+26.0%) P_9.7.6.8 updated (Min./Typ./Max.: -35%/1800/+35% → -23.5%/1750/+23.5%) P_9.7.6.9 updated (Min./Typ./Max.: -30%/1800/+30% → -20.5%/1750/+20.5%) P_9.7.6.12 updated (Min./Typ./Max.: -26%/1800/+26% → -19.0%/1750/+19.0%) P_9.7.6.15 updated (Min./Typ./Max.: -11%/1800/+11% → -9.7%/1805/+9.7%) P_9.7.6.17 updated (Min./Typ./Max.: -6%/1800/+6% → -6.0%/1805/+6.0%) P_9.7.6.19 updated (Min./Typ./Max.: -5%/1800/+5% → -4.5%/1805/+4.5%) P_7.5.6.11 updated (added in Note or Test Condition: see **Figure 19**) **Figure 1**, **Figure 43** updated **Chapter 1** updated (or LED equivalent → or equivalent electronic loads (e.g. LED modules)) P_4.3.0.7 added **Table 24** updated **Chapter 5.1** updated (added: see **Chapter 10** for the complete application setup overview)

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Revision History

Table 25 BTS7040-2EPA - List of changes

Revision	Changes
1.04, 2019-06-26	**Chapter 9.2** updated (2 V → $V_{DS(OLOFF)}$) General: updated (ReverSave™ → ReverseON) **Chapter 1** updated ((inserted headline "Product Validation"), (Qualified in accordance with AEC Q100 grade 1 → Qualified for automotive applications. Product validation according to AEC-Q100 Grade 1.)) General: updated Product Name (PROFET™+2 → PROFET™+2 12V) Page 1: updated figure product **Table 24** updated punctuation **Chapter 9.3.1** updated (typo) Page 1: updated (Package PG-TSDSO-14-22 → Package PG-TSDSO-14) **Figure 29** updated **Figure 44** updated (PG-TSDSO-14-22 (Thin (Slim) Dual Small Outline 14 pins) Package Outline → PG-TSDSO-14 (Thin (Slim) Dual Small Outline 14 pins) Package Outline) **Figure 45** updated (PG-TSDSO-14-22 (Thin (Slim) Dual Small Outline 14 pins) Package pads and stencil → PG-TSDSO-14 (Thin (Slim) Dual Small Outline 14 pins) Package pads and stencil) **Table 1** updated ((Symbol: $I_{VS(SLEEP)}$ → $I_{VS(SLEEP)_85}$), (Parameter: Minimum Overvoltage protection (T_J = 25 °C) → Minimum Overvoltage protection (T_J ≥ 25 °C)) P_9.6.0.6 updated (Note or Test Condition: removed unnecessary line-break)
1.03, 2018-06-14	**Chapter 7.4.1** updated chapter title (PROFET → PROFET™) **Table 12** updated table title (PROFET → PROFET™) **Chapter 8.6.1** updated chapter title (PROFET → PROFET™) **Table 16** updated table title (PROFET → PROFET™) **Chapter 9.5.1** updated chapter title (PROFET → PROFET™) **Table 21** updated table title (PROFET → PROFET™) P_4.1.0.21, P_4.1.0.22, P_4.1.0.23, P_4.1.0.24 updated (footnote ESD standards) **Table 1** updated ($R_{DS(ON)}$ → $R_{DS(ON)_150}$), ($V_{DS(CLAMP)}$ → $V_{DS(CLAMP)_25}$) **Chapter 8.5.2** updated phrasing P_7.5.6.14 Table subheading "Switching Energy" added P_7.5.6.15 Table subheading "Switching Energy" added **Chapter 6.4** added conditions **Chapter 7.5** added conditions P_7.5.6.14 updated (Test condition: add "See Figure") P_7.5.6.15 updated (Test condition: add "See Figure") **Chapter 8.7** added conditions **Chapter 9.6** added conditions P_9.7.6.27 updated (Test condition: add "See Figure") P_9.7.6.29 updated (Test condition: add "See Figure") **Chapter 7.3.1** typo corrected (link to **Figure 19** added)
1.02, 2017-11-17	**Table 6** footnote updated ("Specified RthJA value is" removed) **Figure 17** symbol updated ($V_{IS(CLAMP)}$ → $V_{SIS(CLAMP)}$)

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Revision History

Table 25 BTS7040-2EPA - List of changes

Revision	Changes
1.01, 2017-10-24	Figures updated (straight lines for signals that are crossing, points for connections; typos, capitalization/lower case printing) Typos and misspelling corrected according to style guidelines, inconsistencies among document resolved P_4.1.0.36 updated (symbol: $I_{DI} \rightarrow I_{DI(REV)}$) P_5.4.0.5 symbol updated ($I_{DI} \rightarrow I_{DI(H)}$) P_5.4.0.6 symbol updated ($I_{DI} \rightarrow I_{DI(L)}$) **Chapter 7.3.3** updated **Table 24** updated (R_{DSEL} included)
1.00, 2017-08-24	Data Sheet available

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Table of Contents

Table of Contents

1 Overview ... 1
2 Block Diagram and Terms ... 3
2.1 Block Diagram ... 3
2.2 Terms ... 4
3 Pin Configuration ... 5
3.1 Pin Assignment ... 5
3.2 Pin Definitions and Functions ... 6
4 General Product Characteristics ... 7
4.1 Absolute Maximum Ratings - General ... 7
4.2 Absolute Maximum Ratings - Power Stages ... 9
4.2.1 Power Stage - 40 mΩ ... 9
4.3 Functional Range ... 9
4.4 Thermal Resistance ... 10
4.4.1 PCB Setup ... 11
4.4.2 Thermal Impedance ... 12
5 Logic Pins ... 13
5.1 Input Pins (INn) ... 13
5.2 Diagnosis Pin ... 14
5.3 Electrical Characteristics Logic Pins ... 14
6 Power Supply ... 15
6.1 Operation Modes ... 15
6.1.1 Unsupplied ... 16
6.1.2 Power-up ... 16
6.1.3 Sleep mode ... 16
6.1.4 Stand-by mode ... 16
6.1.5 Active mode ... 16
6.2 Undervoltage on V_S ... 17
6.3 Electrical Characteristics Power Supply ... 18
6.4 Electrical Characteristics Power Supply - Product Specific ... 19
6.4.1 BTS7040-2EPA ... 19
7 Power Stages ... 20
7.1 Output ON-State Resistance ... 20
7.2 Switching loads ... 21
7.2.1 Switching Resistive Loads ... 21
7.2.2 Switching Inductive Loads ... 22
7.2.3 Output Voltage Limitation ... 23
7.3 Advanced Switching Characteristics ... 23
7.3.1 Inverse Current behavior ... 23
7.3.2 Switching Channels in Parallel ... 25
7.3.3 Cross Current robustness with H-Bridge configuration ... 25
7.4 Electrical Characteristics Power Stages ... 26
7.4.1 Electrical Characteristics Power Stages - PROFET™ ... 26
7.5 Electrical Characteristics - Power Output Stages ... 27
7.5.1 Power Output Stage - 40 mΩ ... 27

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Table of Contents

8 Protection ... 30
8.1 Overtemperature Protection ... 30
8.2 Overload Protection ... 32
8.3 Protection and Diagnosis in case of Fault ... 34
8.3.1 Retry Strategy ... 34
8.4 Additional protections ... 37
8.4.1 Reverse Polarity Protection ... 37
8.4.2 Overvoltage Protection ... 38
8.5 Protection against loss of connection ... 38
8.5.1 Loss of Battery and Loss of Load ... 38
8.5.2 Loss of Ground ... 38
8.6 Electrical Characteristics Protection ... 39
8.6.1 Electrical Characteristics Protection - PROFET™ ... 39
8.7 Electrical Characteristics Protection - Power Output Stages ... 40
8.7.1 Protection Power Output Stage - 40 mΩ ... 40

9 Diagnosis ... 42
9.1 Overview ... 43
9.1.1 SENSE signal truth table ... 43
9.2 Diagnosis in ON state ... 44
9.2.1 Current Sense (k_{ILIS}) ... 44
9.2.2 Fault Current ($I_{IS(FAULT)}$) ... 45
9.3 Diagnosis in OFF state ... 46
9.3.1 Open Load current ($I_{IS(OLOFF)}$) ... 47
9.4 SENSE Timings ... 48
9.5 Electrical Characteristics Diagnosis ... 50
9.5.1 Electrical Characteristics Diagnosis - PROFET™ ... 51
9.6 Electrical Characteristics Diagnosis - Power Output Stages ... 53
9.6.1 Diagnosis Power Output Stage - 40 mΩ ... 53

10 Application Information ... 54
10.1 Application Setup ... 54
10.2 External Components ... 55
10.3 Further Application Information ... 56

11 Package Outlines ... 57

12 Revision History ... 59

Table of Contents ... 62

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