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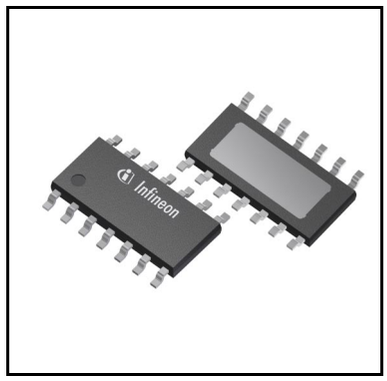
# PROFET™+ 24V

## BTF6070-2ERV

## Smart High-Side Power Switch Dual Channel, 60 mΩ

AEC Qualified RoHS

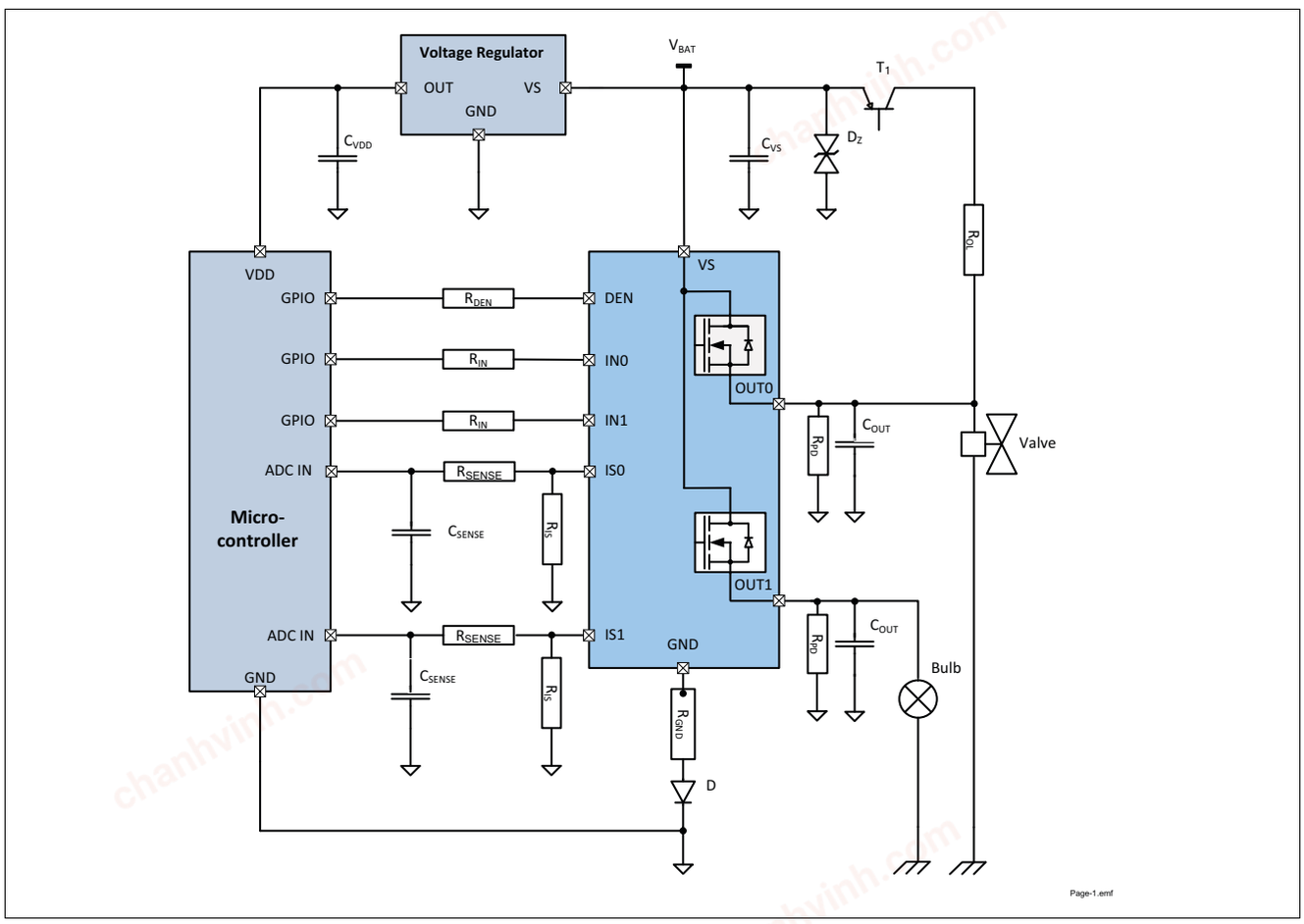
| | |
|---|---|
| **Package** | PG-TDSO-14 |
| **Marking** | 6070-2ERV |




## 1 Overview

### Application

- Suitable for 12 V and 24 V Trucks and Transportation Systems
- Specially designed to drive Valve Applications
- Can be used for PWM frequencies up to 1.5 kHz
- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits




**Application Diagram with BTF6070-2ERV**

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## Overview

### Basic Features

- Dual channel device
- Fast switching device
- For 12 V and 24 V grounded loads
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state
- Green product (RoHS compliant)
- AEC qualified

### Description

The BTF6070-2ERV is a 60 mΩ dual channel Smart High-Side Power Switch, embedded in a PG-TDSO-14, Exposed Pad package, providing protective functions and diagnosis. The power transistor is built by a N-channel vertical power MOSFET with charge pump. The device is integrated in Smart6 HV technology. It is specially designed to drive Valve Applications in the harsh automotive environment. For lighting applications the nominal bulb load of P10W+P5W 24 V or P10W 12 V is considered.

**Table 1 Product Summary**

| Parameter | Symbol | Value |
|---|---|---|
| Operating voltage range | $V_{S(OP)}$ | 5 V ... 36 V |
| Maximum supply voltage | $V_{S(LD)}$ | 65 V |
| Maximum ON state resistance at $T_J$ = 150°C per channel | $R_{DS(ON)}$ | 135 mΩ |
| Nominal load current (one channel active) | $I_{L(NOM)1}$ | 3 A |
| Nominal load current (all channels active) | $I_{L(NOM)2}$ | 2.3 A |
| Typical current sense ratio | $k_{ILIS}$ | 1730 |
| Minimum current limitation | $I_{L5(SC)}$ | 9 A |
| Maximum standby current with load at $T_J$ = 25°C | $I_{S(OFF)}$ | 500 nA |

### Diagnostic Functions

- Proportional load current sense for the 2 channels
- Open load detection in ON and OFF
- Short circuit to battery and ground indication
- Overtemperature switch off detection
- Stable diagnostic signal during short circuit
- Enhanced $k_{ILIS}$ dependency with temperature and load current

### Protection Functions

- Stable behavior during undervoltage
- Reverse polarity protection with external components
- Secure load turn-off during logic ground disconnection with external components

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## Overview

- Overtemperature protection with latch
- Overvoltage protection with external components
- Enhanced short circuit operation

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# 2 Block Diagram

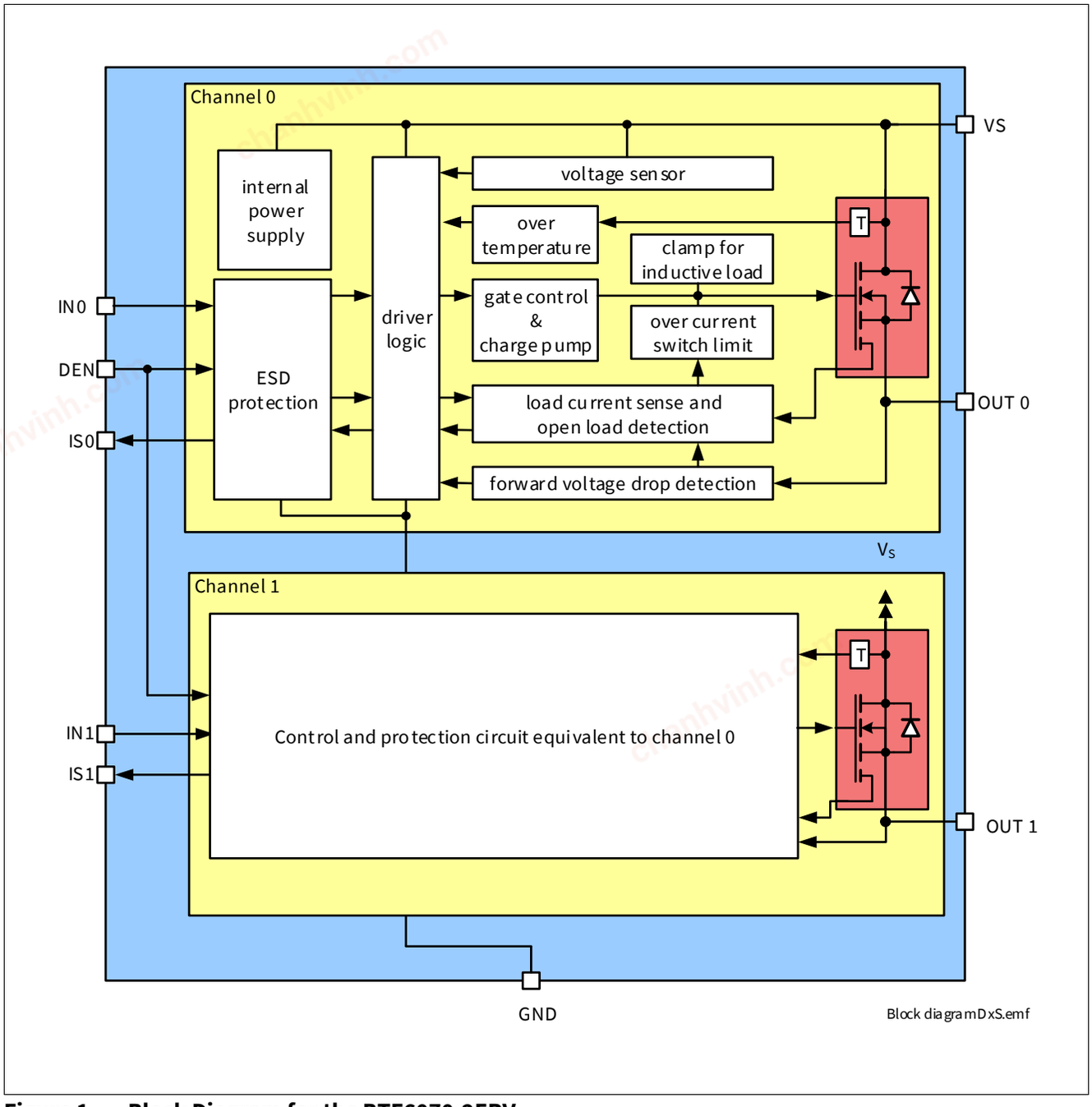



**Figure 1 Block Diagram for the BTF6070-2ERV**

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# 3 Pin Configuration

## 3.1 Pin Assignment

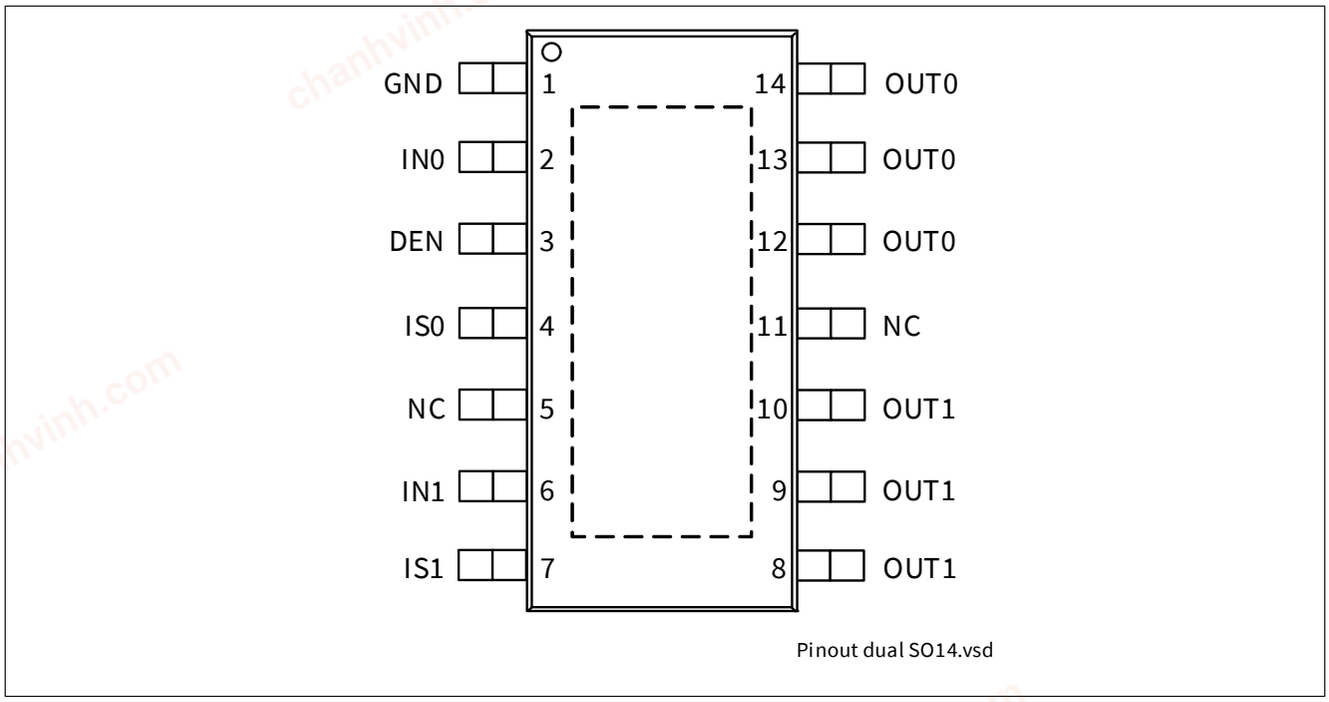



**Figure 2 Pin Configuration**

## 3.2 Pin Definitions and Functions

**Table 2 Pin Definition and Functions**

| Pin | Symbol | Function |
|---|---|---|
| 1 | GND | **GrouND;** Ground connection |
| 2 | IN0 | **INput channel 0;** Input signal for channel 0 activation |
| 3 | DEN | **Diagnostic ENable;** Digital signal to enable/disable the diagnosis of the device |
| 4 | IS0 | **Sense 0;** Sense current of the channel 0 |
| 5, 11 | NC | **Not Connected;** No internal connection to the chip |
| 6 | IN1 | **INput channel 1;** Input signal for channel 1 activation |
| 7 | IS1 | **Sense 1;** Sense current of the channel 1 |
| 8, 9, 10 | OUT1 | **OUTput 1;** Protected high side power output channel 1[1)] |
| 12, 13, 14 | OUT0 | **OUTput 0;** Protected high side power output channel 0[1)] |
| Cooling Tab | VS | **Voltage Supply;** Battery voltage |

1) All output pins of a given channel must be connected together on the PCB. All pins of an output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

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## 3.3 Voltage and Current Definition

**Figure 3** shows all terms used in this data sheet, with associated convention for positive values.

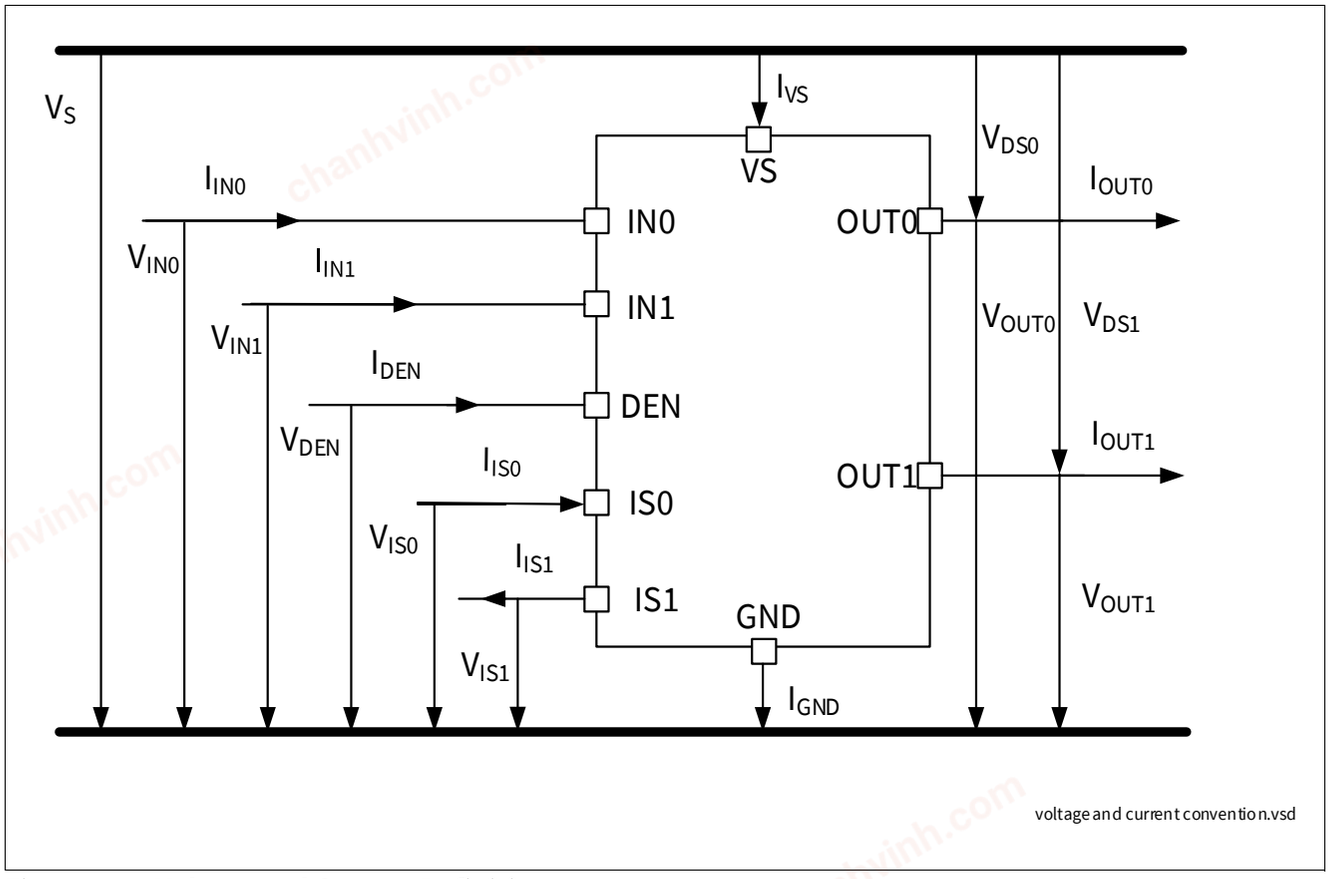



**Figure 3 Voltage and Current Definition**

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# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings [1)]**

$T_J$ = -40°C to 150°C; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Supply Voltages** | | | | | | | |
| Supply voltage | $V_S$ | -0.3 | - | 48 | V | - | P_4.1.1 |
| Reverse polarity voltage | $-V_{S(REV)}$ | 0 | - | 28 | V | $t$ < 2 min<br>$T_A$ = 25°C<br>$R_L$ ≥ 25 Ω | P_4.1.2 |
| Supply voltage for short circuit protection | $V_{BAT(SC)}$ | 0 | - | 36 | V | $R_{ECU}$ = 30 mΩ<br>$R_{Supply}$ = 10 mΩ<br>$L_{Supply}$ = 5 µH<br>$R_{Cable}$= 7 mΩ/m<br>$L_{Cable}$= 1 µH/m,<br>$l$ = 0 to 40 m<br>See **Chapter 6** and **Figure 29** | P_4.1.3 |
| Supply voltage for Load dump protection | $V_{S(LD)}$ | - | - | 65 | V | [2)] $R_I$ = 2 Ω<br>$R_L$ = 25 Ω | P_4.1.12 |
| **Short Circuit Capability** | | | | | | | |
| Permanent short circuit IN pin toggles | $n_{RSC1}$ | - | - | 100 | k cycles | [3)] $V_{Supply}$ = 28 V<br>$R_{ECU}$ = 20 mΩ<br>$R_{Supply}$ = 10 mΩ<br>$L_{Supply}$= 5 µH<br>$R_{Cable}$ = 0 mΩ $L_{Cable}$ = < 1 µH | P_4.1.4 |
| Permanent short circuit IN pin toggles | $n_{RSC_highL}$ | - | - | 100 | k cycles | [3)] $V_{Supply}$ = 28 V<br>$R_{ECU}$ = 30 mΩ<br>$R_{Supply}$ = 10 mΩ<br>$L_{Supply}$ = 5 µH<br>$R_{Cable}$ = 280 mΩ<br>$L_{Cable}$ = 40 µH | P_4.1.5 |
| **Input Pins** | | | | | | | |
| Voltage at INPUT pins | $V_{IN}$ | -0.3 | - | 6 | V | - | P_4.1.13 |
| Voltage at INPUT pins | $V_{IN}$ | - | - | 7 | V | $t$ < 2 min | P_4.1.6 |
| Current through INPUT pins | $I_{IN}$ | -2 | - | 2 | mA | - | P_4.1.14 |
| Voltage at DEN pin | $V_{DEN}$ | -0.3 | - | 6 | V | - | P_4.1.15 |
| Voltage at DEN pin | $V_{DEN}$ | - | | 7 | V | $t$ < 2 min | P_4.1.50 |
| Current through DEN pin | $I_{DEN}$ | -2 | - | 2 | mA | - | P_4.1.16 |

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**Table 3 Absolute Maximum Ratings [1)]**

$T_J$ = -40°C to 150°C; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Sense Pin** | | | | | | | |
| Voltage at IS pin | $V_{IS}$ | -0.3 | - | $V_S$ | V | - | P_4.1.19 |
| Current through IS pin | $I_{IS}$ | -25 | - | 50 | mA | - | P_4.1.20 |
| **Power Stage** | | | | | | | |
| Load current | $\|I_L\|$ | - | - | $I_{L(LIM)}$ | A | - | P_4.1.21 |
| Power dissipation (DC) | $P_{TOT}$ | - | - | 1.8 | W | $T_A$ = 85°C<br>$T_J$ < 150°C | P_4.1.22 |
| Maximum energy dissipation repetitive pulse (one channel) | $E_{AR_2A}$ | - | - | 40 | mJ | 20 Mio. cycles<br>$I_{L(0)}$ = 2 A<br>$T_{J(0)}$ = 105°C | P_4.1.24 |
| Negative voltage slope at output (inductive clamping) | $-dV_{OUT}/dt$ | - | - | -20 | V/µs | [1)] $V_{OUT}$ = 28 V to 28 V - $V_{DS(AZ)}$ $V_{IN}$ = 0 V | P_4.1.35 |
| Positive voltage slope at output | $dV_{OUT}/dt$ | - | - | 20 | V/µs | [1)] $V_{OUT}$ = 0 V to 28 V $V_{IN}$ = 0 V | P_4.1.36 |
| Voltage at power transistor | $V_{DS}$ | - | - | 65 | V | - | P_4.1.26 |
| **Currents** | | | | | | | |
| Current through ground pin | $I_{GND}$ | -20 | - | 20 | mA | - | P_4.1.27 |
| Current through ground pin | $I_{GND}$ | -150 | - | 20 | mA | $t$ < 2 min | P_4.1.7 |
| **Temperatures** | | | | | | | |
| Junction temperature | $T_J$ | -40 | - | 150 | °C | - | P_4.1.28 |
| Storage temperature | $T_{STG}$ | -55 | - | 150 | °C | - | P_4.1.30 |
| **ESD Susceptibility** | | | | | | | |
| ESD susceptibility (all pins) | $V_{ESD}$ | -2 | - | 2 | kV | [4)] HBM | P_4.1.31 |
| ESD susceptibility OUT Pin vs. GND and $V_S$ connected | $V_{ESD}$ | -5 | - | 5 | kV | [4)] HBM | P_4.1.32 |
| ESD susceptibility | $V_{ESD}$ | -500 | - | 500 | V | [5)] CDM | P_4.1.33 |
| ESD susceptibility pin (corner pins) | $V_{ESD}$ | -750 | - | 750 | V | [5)] CDM | P_4.1.34 |

1) Not subject to production test. Specified by design
2) $V_{S(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1
3) Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short-circuit capability on the Back Cover of this document
4) ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002
5) ESD susceptibility, Charged Device Model “CDM” according to AEC Q100-011

**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

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2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

**Table 4 Functional Range $T_J$ = -40°C to 150°C; (unless otherwise specified)**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Nominal operating voltage | $V_{NOM}$ | 8 | 28 | 36 | V | - | P_4.2.1 |
| Extended operating voltage | $V_{S(OP)}$ | 5 | - | 48 | V | 1)3) $V_{IN}$ = 4.5 V<br>$R_L$ = 25 Ω<br>$V_{DS}$ < 0.5 V | P_4.2.2 |
| Minimum functional supply voltage | $V_{S(OP)_MIN}$ | 3.8 | 4.3 | 5 | V | 2) $V_{IN}$ = 4.5 V<br>$R_L$ = 25 Ω<br>From $I_{OUT}$ = 0 A<br>to $V_{DS}$ < 0.5 V;<br>see **Figure 16** | P_4.2.3 |
| Undervoltage shutdown | $V_{S(UV)}$ | 3 | 3.5 | 4.1 | V | 2) $V_{IN}$ = 4.5 V<br>$V_{DEN}$ = 0 V<br>$R_L$ = 25 Ω<br>From $V_{DS}$ < 1 V<br>to $I_{OUT}$ = 0 A<br>See **Figure 16** | P_4.2.4 |
| Undervoltage shutdown hysteresis | $V_{S(UV)_HYS}$ | - | 850 | - | mV | 3) - | P_4.2.13 |
| Operating current<br>One channel active | $I_{GND_1}$ | - | 5 | 7 | mA | $V_{IN}$ = 5.5 V<br>$V_{DEN}$ = 5.5 V<br>Device in $R_{DS(ON)}$<br>$V_S$ = 36 V | P_4.2.5 |
| Operating current<br>All channels active | $I_{GND_2}$ | - | 8.3 | 12 | mA | $V_{IN}$ = 5.5 V<br>$V_{DEN}$ = 5.5 V<br>Device in $R_{DS(ON)}$<br>$V_S$ = 36 V | P_4.2.6 |
| Standby current for whole device with load (ambient) | $I_{S(OFF)}$ | - | 0.1 | 0.5 | µA | 2) $V_S$ = 36 V<br>$V_{OUT}$ = 0 V<br>$V_{IN}$ floating<br>$V_{DEN}$ floating<br>$T_J \leq$ 85°C | P_4.2.7 |

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**Table 4 Functional Range $T_J$ = -40°C to 150°C; (unless otherwise specified)**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Maximum standby current for whole device with load | $I_{S(OFF)_150}$ | - | - | 10 | µA | $V_S$ = 36 V<br>$V_{OUT}$ = 0 V<br>$V_{IN}$ floating<br>$V_{DEN}$ floating<br>$T_J$ = 150°C | P_4.2.10 |
| Standby current for whole device with load, diagnostic active | $I_{S(OFF_DEN)}$ | - | 1.15 | - | mA | 3) $V_S$ = 36 V<br>$V_{OUT}$ = 0 V<br>$V_{IN}$ floating<br>$V_{DEN}$ = 5.5 V | P_4.2.8 |

1) Parameter deviation possible: $R_{DSON}$, $I_{IS(FAULT)}$ & timing parameters. Protection functions are working.
2) Test at $T_J$ = -40°C only
3) Not subject to production test. Specified by design.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

**Table 5 Thermal Resistance**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to case | $R_{thJC}$ | - | 2 | - | K/W | 1) | P_4.3.1 |
| Junction to ambient<br>All channels active | $R_{thJA}$ | - | 27 | - | K/W | 1)2) | P_4.3.2 |

1) Not subject to production test. Specified by design.
2) Specified $R_{thJA}$ value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board with 1 W power dissipation equally dissipated for both channels at $T_A$=105°C ; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacts the first inner copper layer. Please refer to **Figure 4**.

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### 4.3.1 PCB Set-up

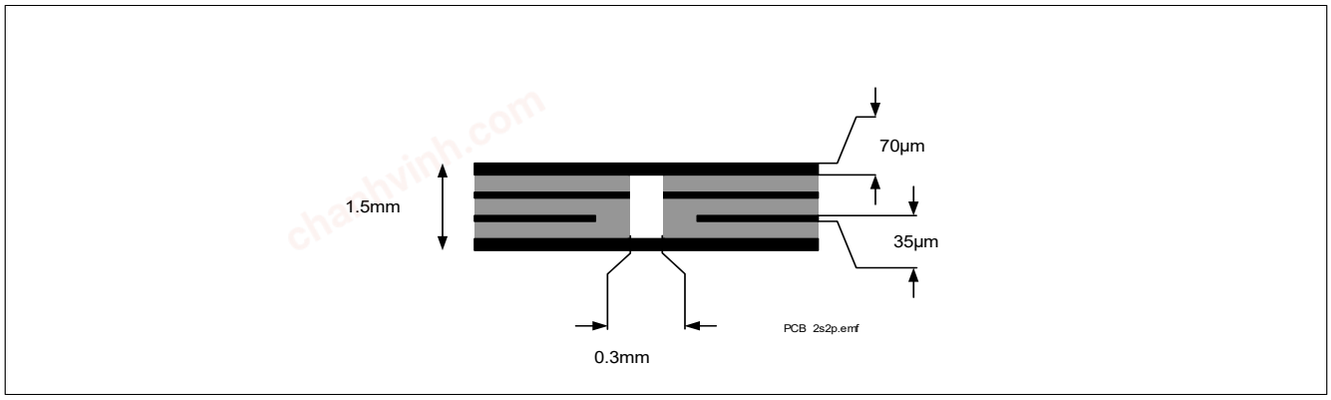



**Figure 4 2s2p PCB Cross Section**

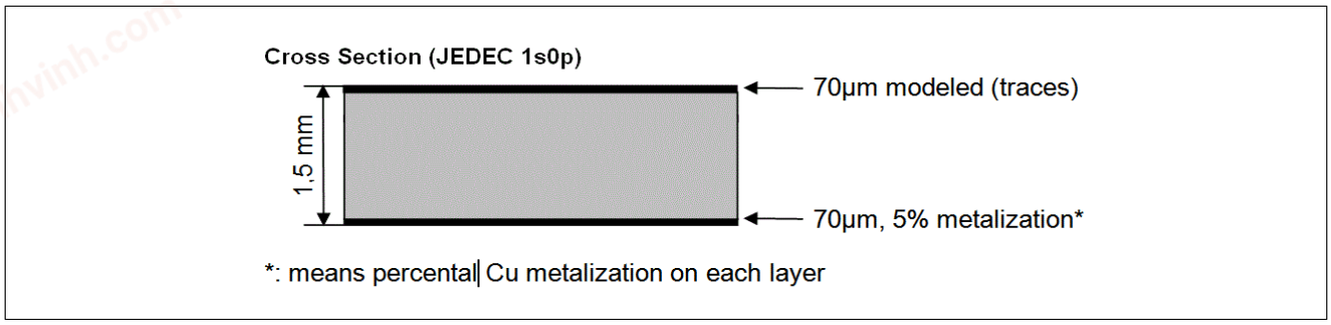



**Figure 5 1s0p PCB Cross Section**

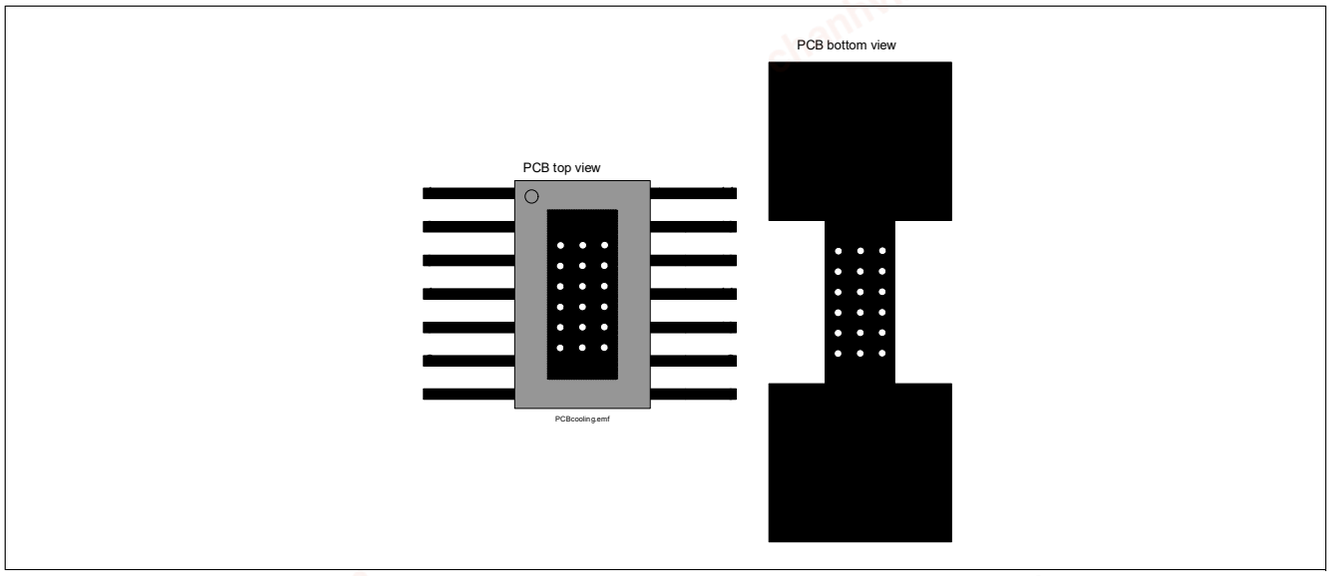



**Figure 6 PC Board Top and Bottom View for Thermal Simulation with 600 mm² Cooling Area**

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### 4.3.2 Thermal Impedance

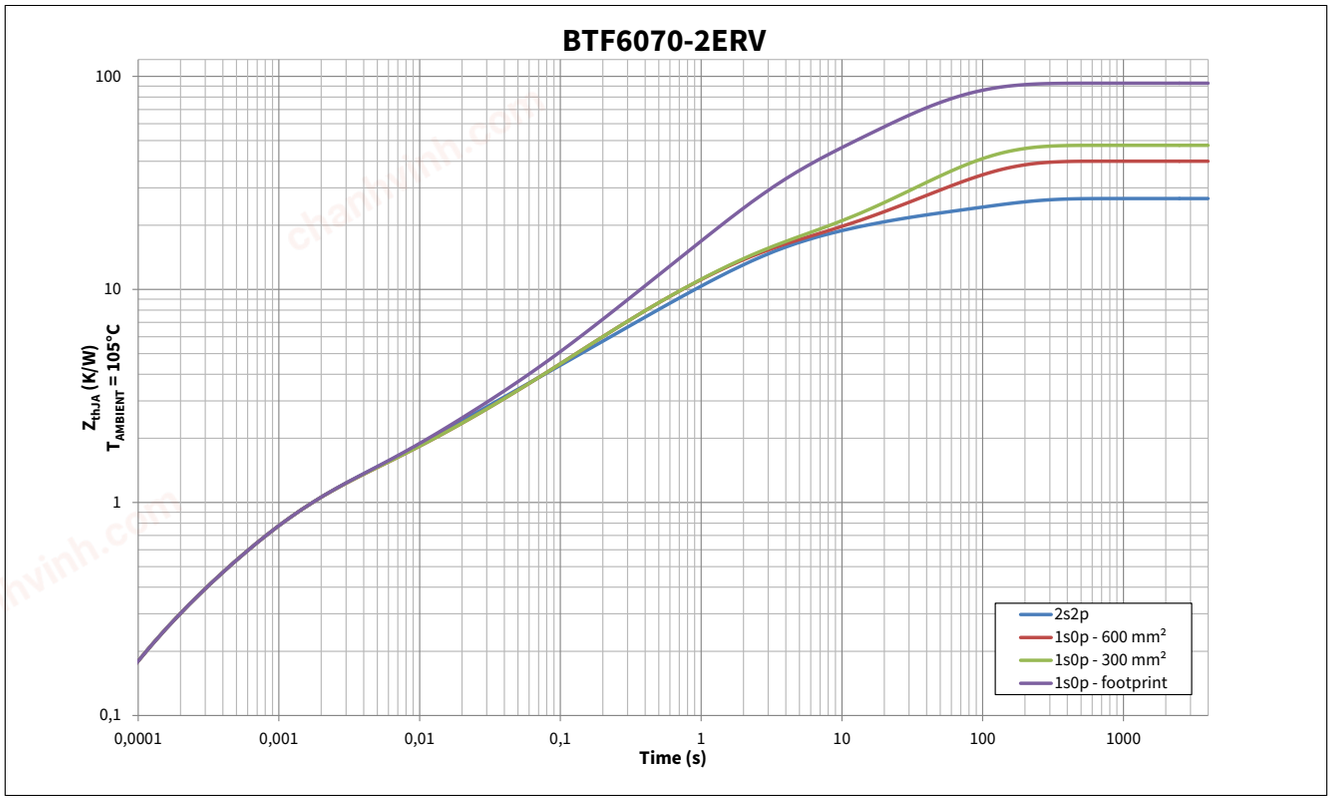



**Figure 7 Typical Thermal Impedance. Both channels active. $T_A$= 85°C. PCB set-up according Figure 4 / Figure 5**

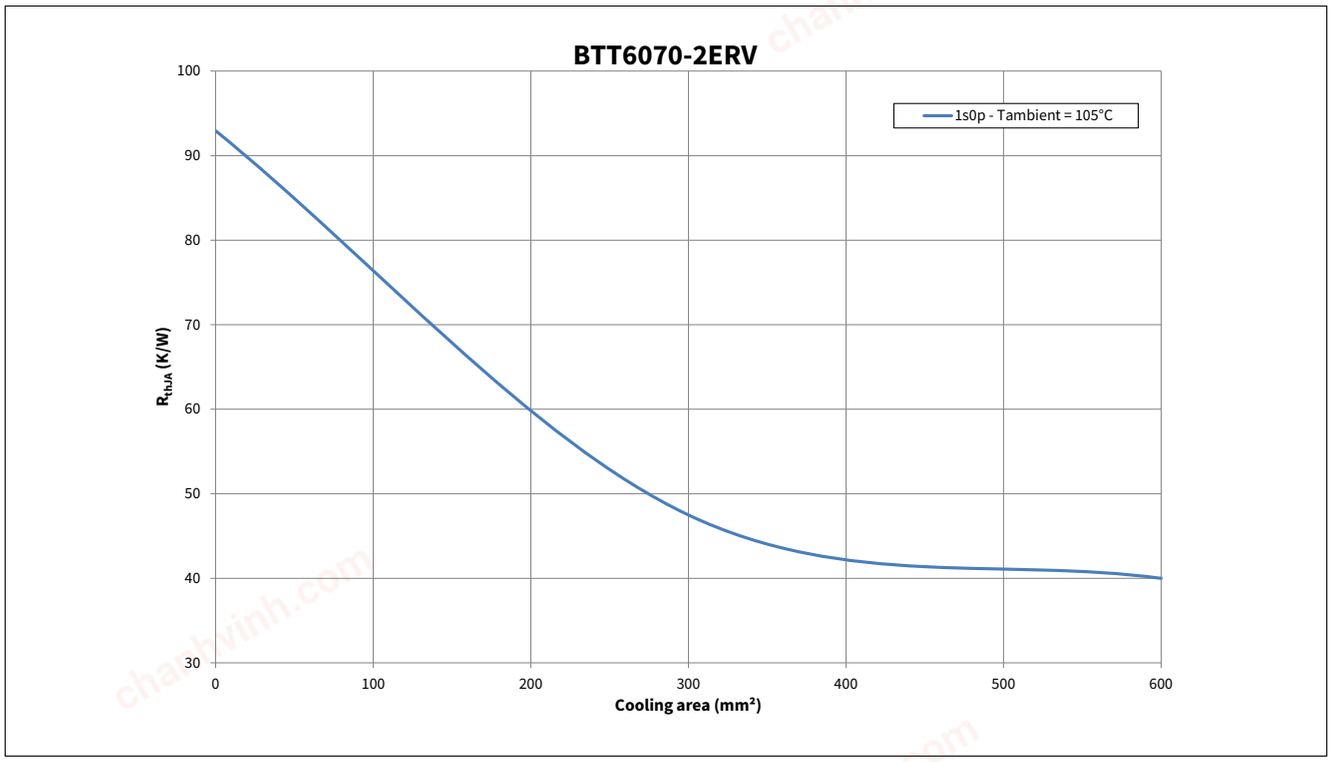



**Figure 8 Typical Thermal Resistance. Both channels active. $T_A$=85°C. PCB set-up 1s0p**

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# 5 Power Stage

The power stages are built using an N-channel vertical power MOSFET (DMOS) with charge pump.

## 5.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature $T_J$. **Figure 9** shows the dependencies in terms of temperature and supply voltage for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

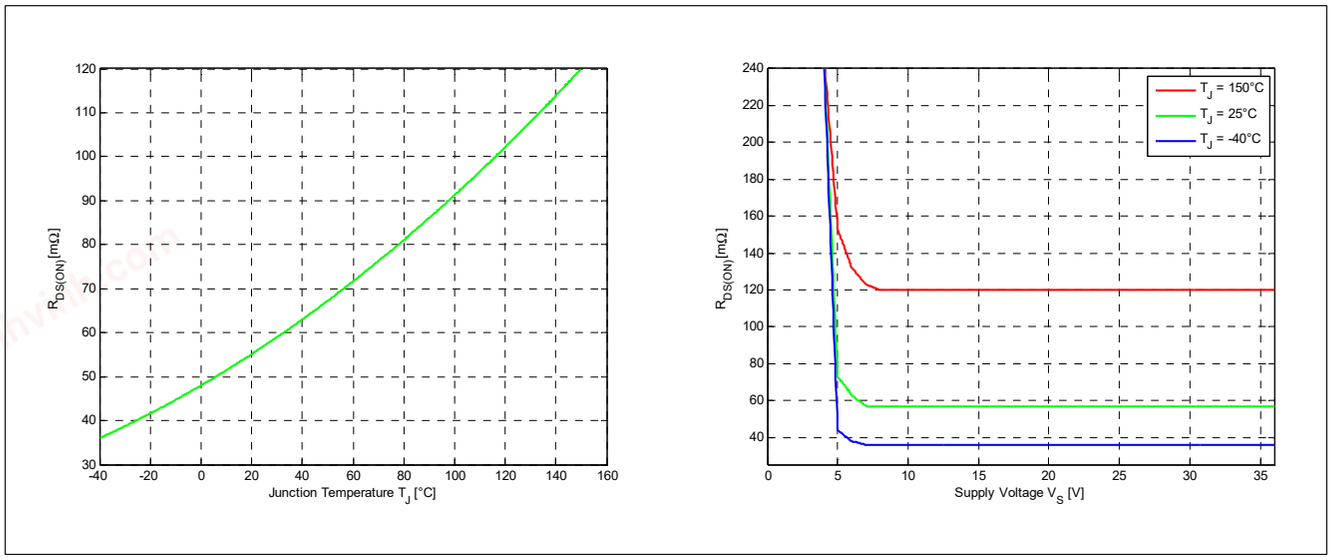



**Figure 9 Typical ON-State Resistance**

A high signal at the input pin (see **Chapter 8**) causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

## 5.2 Turn ON/OFF Characteristics with Resistive Load

**Figure 10** shows the typical timing when switching a resistive load.

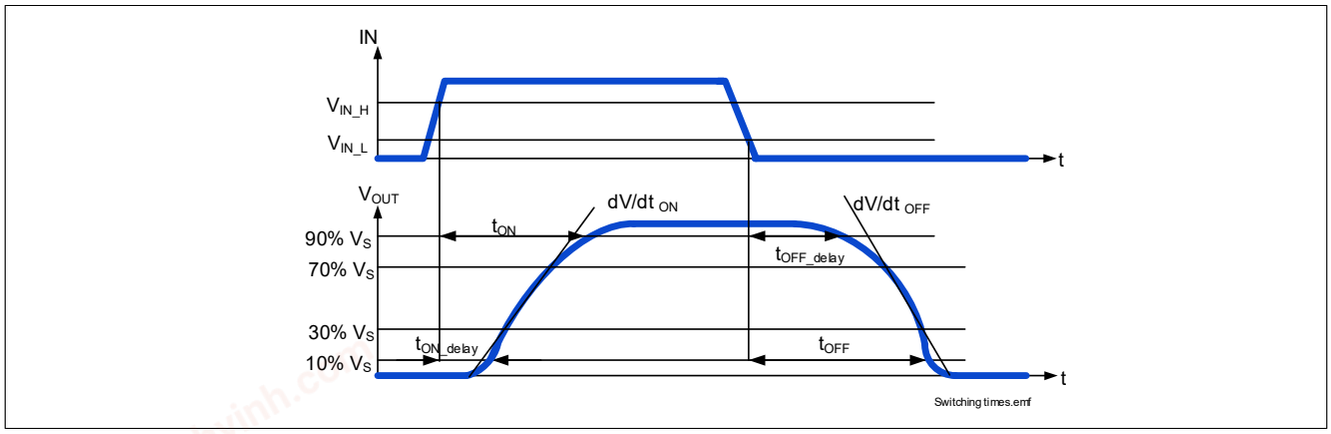



**Figure 10 Switching a Resistive Load Timing**

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## 5.3 Inductive Load

### 5.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage $V_{OUT}$ drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism $Z_{DS(AZ)}$ implemented that limits negative output voltage to a certain level ($V_S$ - $V_{DS(AZ)}$). Please refer to **Figure 11** and **Figure 12** for details. Nevertheless, the maximum allowed load inductance is limited.

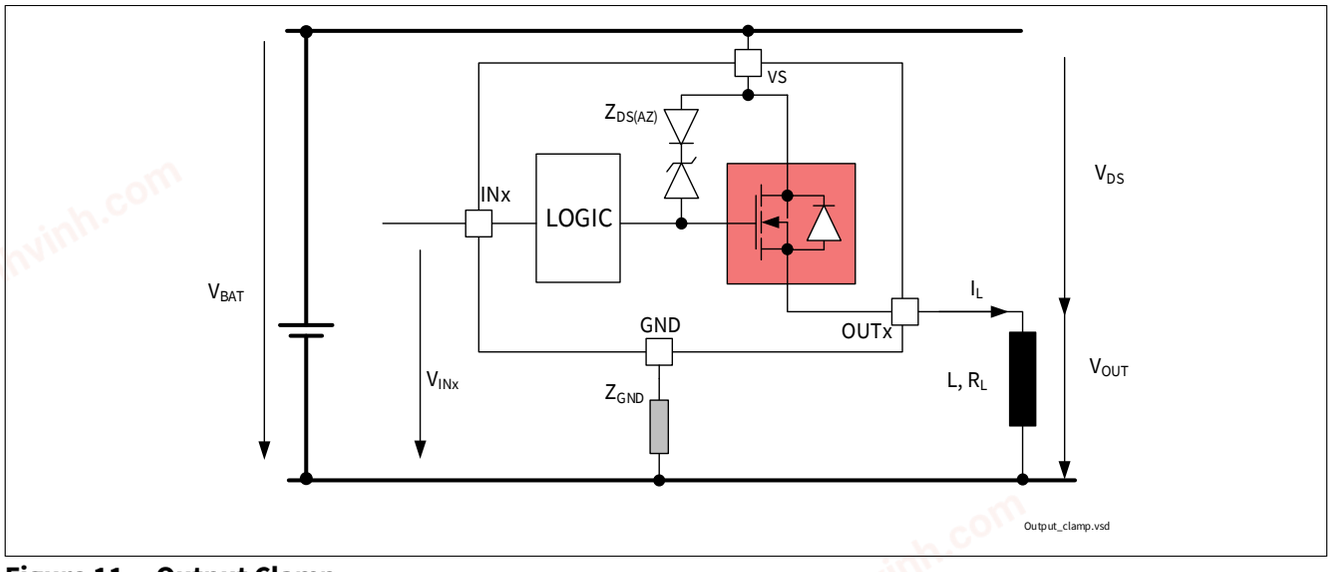



**Figure 11 Output Clamp**

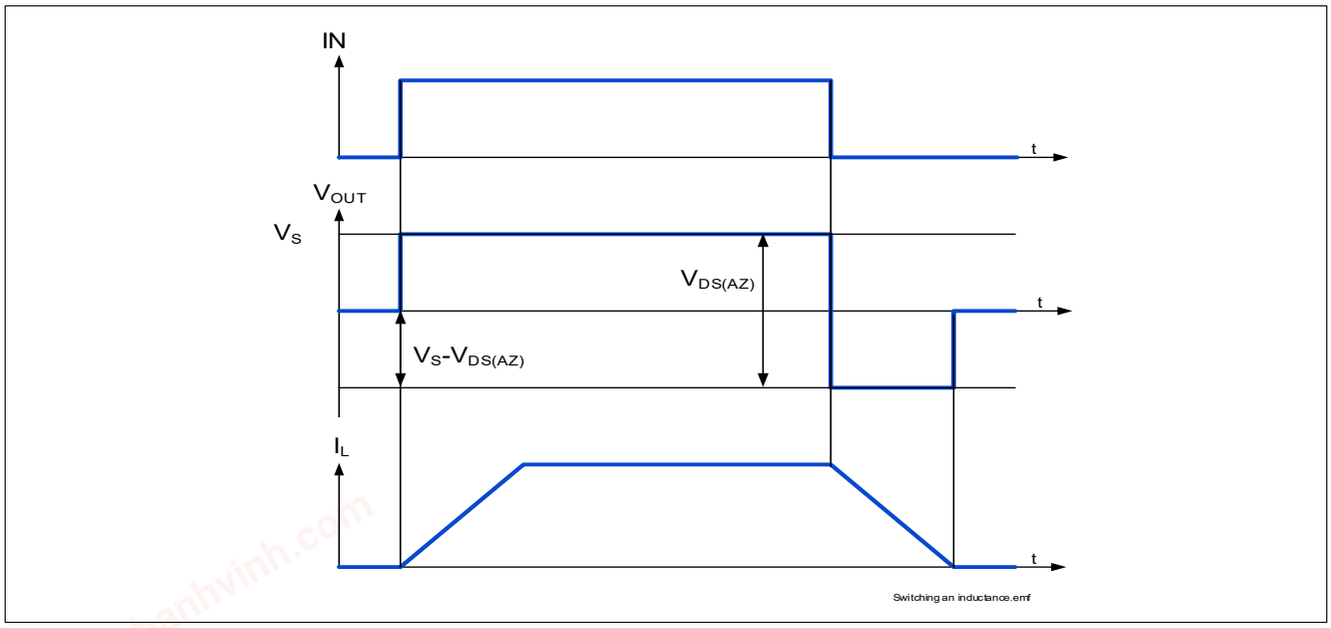



**Figure 12 Switching an Inductive Load Timing**

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### 5.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTF6070-2ERV. This energy can be calculated with following equation:

$$E = V_{DS(AZ)} \cdot \frac{L}{R_L} \cdot \left[ \frac{V_S - V_{DS(AZ)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(AZ)}}\right) + I_L \right] \quad (5.1)$$

Following equation simplifies under the assumption of $R_L = 0\ \Omega$.

$$E = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right) \quad (5.2)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 13** for the maximum allowed energy dissipation as a function of the load current.

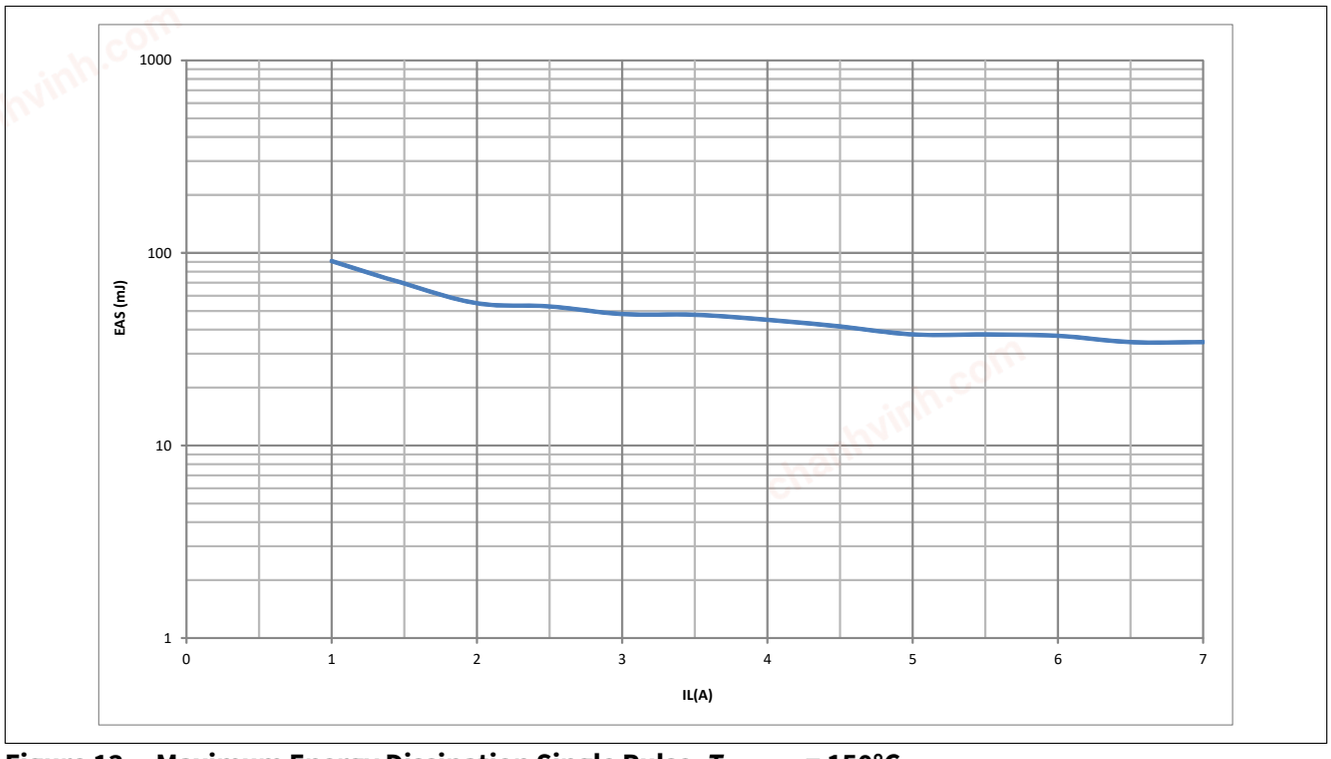



**Figure 13 Maximum Energy Dissipation Single Pulse, $T_{J_START}$ = 150°C**

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## 5.4 Inverse Current Capability

In case of inverse current, meaning a voltage $V_{INV}$ at the OUTput higher than the supply voltage $V_S$, a current $I_{INV}$ will flow from output to $V_S$ pin via the body diode of the power transistor (please refer to **Figure 14**). The output stage follows the state of the IN pin, except if the IN pin goes from OFF to ON during inverse.In that particular case, the output stage is kept OFF until the inverse current disappears. Nevertheless, the current $I_{INV}$ should not be higher than $I_{L(INV)}$. $I_{L(INV)}$ can be considered as 3 A.
If the channel is OFF, the diagnostic will detect an open load at OFF. If the affected channel is ON, the diagnostic will detect open load at ON (the overtemperature signal is inhibited). At the appearance of $V_{INV}$, a parasitic diagnostic can be observed. After, the diagnosis is valid and reflects the output state. At $V_{INV}$ vanishing, the diagnosis is valid and reflects the output state. During inverse current, no protection functions are available.

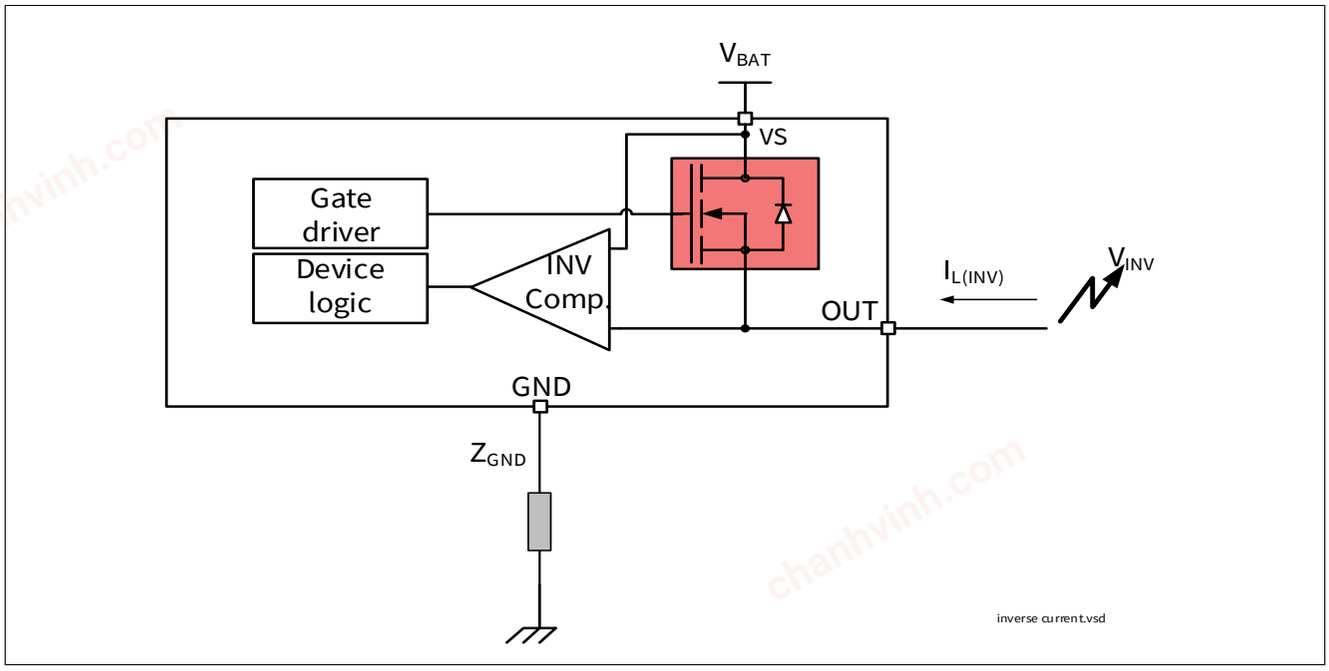



**Figure 14 Inverse Current Circuitry**

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## 5.5 Electrical Characteristics Power Stage

**Table 6 Electrical Characteristics: Power Stage**

$V_S$ = 8 V to 36 V, $T_J$ = -40°C to 150°C (unless otherwise specified).
Typical values are given at $V_S$ = 28 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| ON-state resistance per channel | $R_{DS(ON)_150}$ | 90 | 120 | 135 | mΩ | $I_L = I_{L4}$ = 4 A<br>$V_{IN}$ = 4.5 V<br>$T_J$ = 150°C<br>See **Figure 9** | P_5.5.1 |
| ON-state resistance per channel | $R_{DS(ON)_25}$ | - | 60 | - | mΩ | 1) $T_J$ = 25°C | P_5.5.21 |
| Nominal load current One channel active | $I_{L(NOM)1}$ | - | 3 | - | A | 1) $T_A$ = 85°C<br>$T_J$ < 150°C | P_5.5.2 |
| Nominal load current All channels active | $I_{L(NOM)2}$ | - | 2.3 | - | A | | P_5.5.3 |
| Output voltage drop limitation at small load currents | $V_{DS(NL)}$ | - | 10 | 22 | mV | $I_L = I_{L0}$ = 50 mA | P_5.5.4 |
| Drain to source clamping voltage $V_{DS(AZ)} = (V_S - V_{OUT})$ | $V_{DS(AZ)}$ | 65 | 70 | 75 | V | $I_{DS}$ = 20 mA<br>See **Figure 12** | P_5.5.5 |
| Output leakage current per channel $T_J \leq 85°C$ | $I_{L(OFF)}$ | - | 0.1 | 0.5 | µA | 2) $V_{IN}$ floating<br>$V_{OUT}$ = 0 V<br>$T_J \leq 85°C$ | P_5.5.6 |
| Output leakage current per channel $T_J$ = 150°C | $I_{L(OFF)_150}$ | - | 1 | 8 | µA | $V_{IN}$ floating<br>$V_{OUT}$ = 0 V<br>$T_J$ = 150°C | P_5.5.8 |
| Slew rate 30% to 70% $V_S$ | $dV/dt_{ON}$ | 1 | 2.4 | 4.5 | V/µs | $R_L$ = 25 Ω<br>$V_S$ = 28 V<br>See **Figure 10** | P_5.5.11 |
| Slew rate 70% to 30% $V_S$ | $-dV/dt_{OFF}$ | 1 | 2.4 | 4.5 | V/µs | | P_5.5.12 |
| Slew rate matching $dV/dt_{ON} - dV/dt_{OFF}$ | $\Delta dV/dt$ | -0.5 | 0 | 0.5 | V/µs | | P_5.5.13 |
| Turn-ON time to $V_{OUT}$ = 90% $V_S$ | $t_{ON}$ | 5 | 28 | 70 | µs | | P_5.5.14 |
| Turn-OFF time to $V_{OUT}$ = 10% $V_S$ | $t_{OFF}$ | 5 | 28 | 70 | µs | | P_5.5.15 |
| Turn-ON / OFF matching $t_{OFF} - t_{ON}$ | $\Delta t_{SW}$ | -20 | 5 | 20 | µs | | P_5.5.16 |
| Turn-ON time to $V_{OUT}$ = 10% $V_S$ | $t_{ON_delay}$ | - | 17 | 40 | µs | | P_5.5.17 |
| Turn-OFF time to $V_{OUT}$ = 90% $V_S$ | $t_{OFF_delay}$ | - | 17 | 40 | µs | | P_5.5.18 |

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## Power Stage

**Table 6 Electrical Characteristics: Power Stage** (cont'd)

$V_S$ = 8 V to 36 V, $T_J$ = -40°C to 150°C (unless otherwise specified).
Typical values are given at $V_S$ = 28 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Switch ON energy | $E_{ON}$ | - | 115 | - | µJ | 1) $R_L$ = 25 Ω<br>$V_{OUT}$ = 90% $V_S$<br>$V_S$ = 36 V | P_5.5.19 |
| Switch OFF energy | $E_{OFF}$ | - | 173 | - | µJ | 1) $R_L$ = 25 Ω<br>$V_{OUT}$ = 10% $V_S$<br>$V_S$ = 36 V | P_5.5.20 |

1) Not subject to production test, specified by design.
2) Test at $T_J$ = -40°C only

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# 6 Protection Functions

The device provides integrated protection functions. These functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

## 6.1 Loss of Ground Protection

In case of loss of the module ground and the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pins.

In case of loss of device ground, it’s recommended to use input resistors between the microcontroller and the BTF6070-2ERV to ensure switching OFF of channels.

In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 15** sketches the situation.

$Z_{GND}$ is recommended to be a resistor in series to a diode.

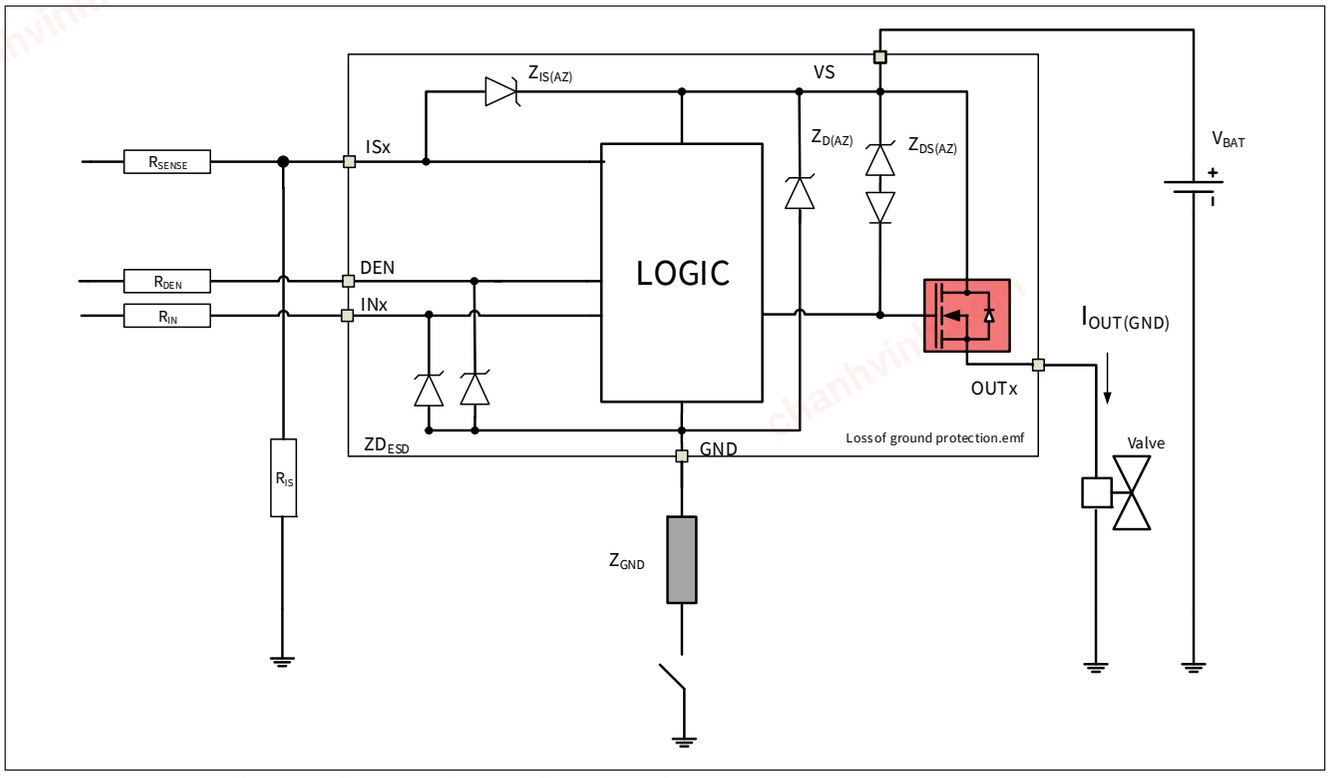



**Figure 15 Loss of Ground Protection with External Components**

## 6.2 Undervoltage Protection

Between $V_{S(UV)}$ and $V_{S(OP)}$, the undervoltage mechanism is triggered. $V_{S(OP)}$ represents the minimum voltage where the switching ON and OFF can takes place. $V_{S(UV)}$ represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism $V_{S(UV)}$, the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism $V_{S(OP)}$, then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until $V_S$ is in the $V_{NOM}$ range. **Figure 16** sketches the undervoltage mechanism.

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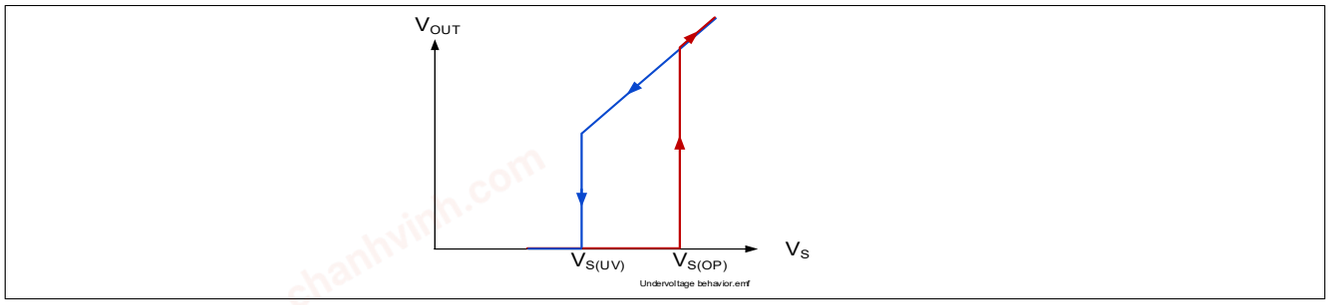



**Figure 16 Undervoltage Behavior**

## 6.3 Overvoltage Protection

There is an integrated clamp mechanism for overvoltage protection ($Z_{D(AZ)}$). To guarantee this mechanism operates properly in the application, the current in the Zener diode has to be limited by a ground resistor. **Figure 17** shows a typical application to withstand overvoltage issues. In case of supply voltage higher than $V_{S(AZ)}$, the power transistor switches ON and in addition the voltage across the logic section is clamped. As a result, the internal ground potential rises to $V_S$ - $V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at pin INx and DEN rises almost to that potential, depending on the impedance of the connected circuitry. In the case the device was ON, prior to overvoltage, the BTF6070-2ERV remains ON. In the case the BTF6070-2ERV was OFF, prior to overvoltage, the power transistor can be activated. In the case the supply voltage is in above $V_{BAT(SC)}$ and below $V_{DS(AZ)}$, the output transistor is still operational and follows the input. If at least one channel is in the ON state, parameters are no longer guaranteed and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy $E_{AS}$ capability. The values for $Z_{IS(A)}$, $Z_{D(AZ)}$ and $Z_{DS(AZ)}$ are included in the parameter P_6.6.3. $Z_{GND}$ is recommended to be a resistor in series to a diode.

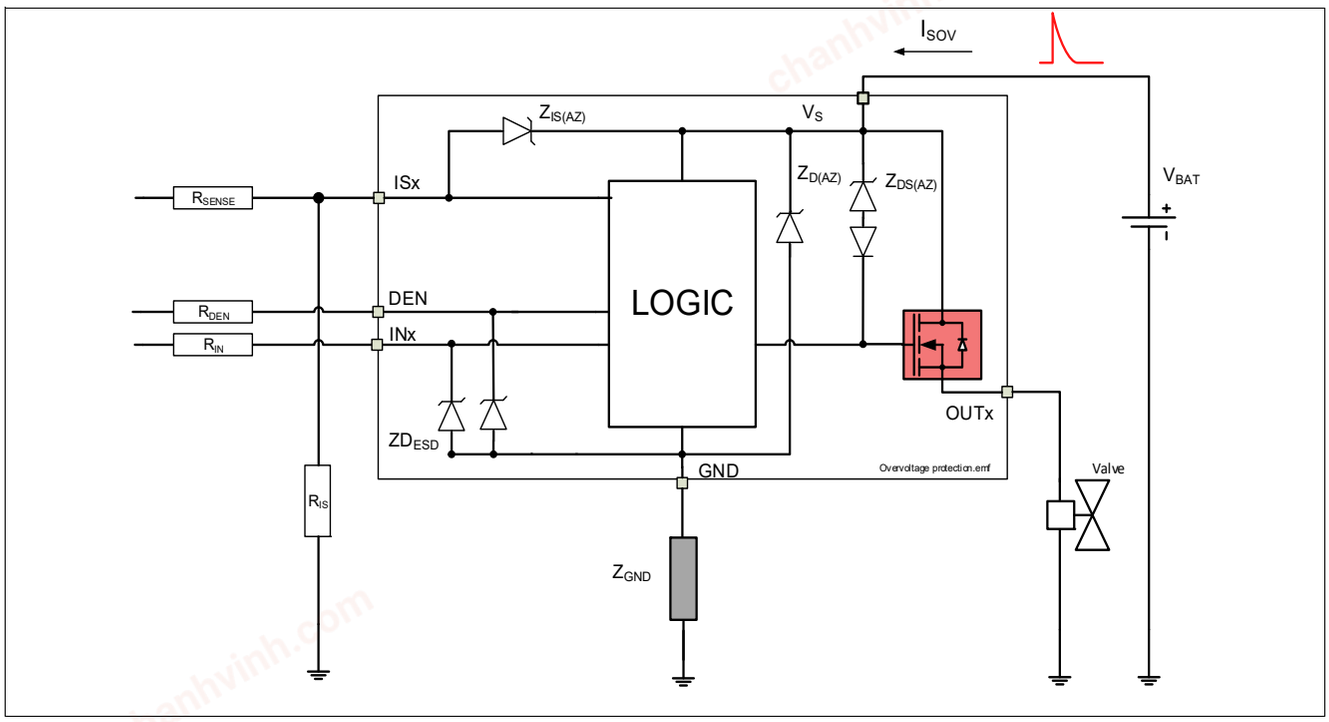



**Figure 17 Overvoltage Protection with External Components**

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## 6.4 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diodes of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logic pins has to be limited to the maximum current described in **Chapter 4.1** with an external resistor. **Figure 18** shows a typical application. $R_{GND}$ resistor is used to limit the current in the Zener protection of the device. Resistors $R_{DEN}$, and $R_{IN}$ are used to limit the current in the logic of the device and in the ESD protection stage. $R_{SENSE}$ is used to limit the current in the sense transistor which behaves as a diode. The recommended value for $R_{DEN} = R_{IN} = 10\ k\Omega$. $Z_{GND}$ is recommended to be a resistor in series to a diode.

During reverse polarity, no protection functions are available.

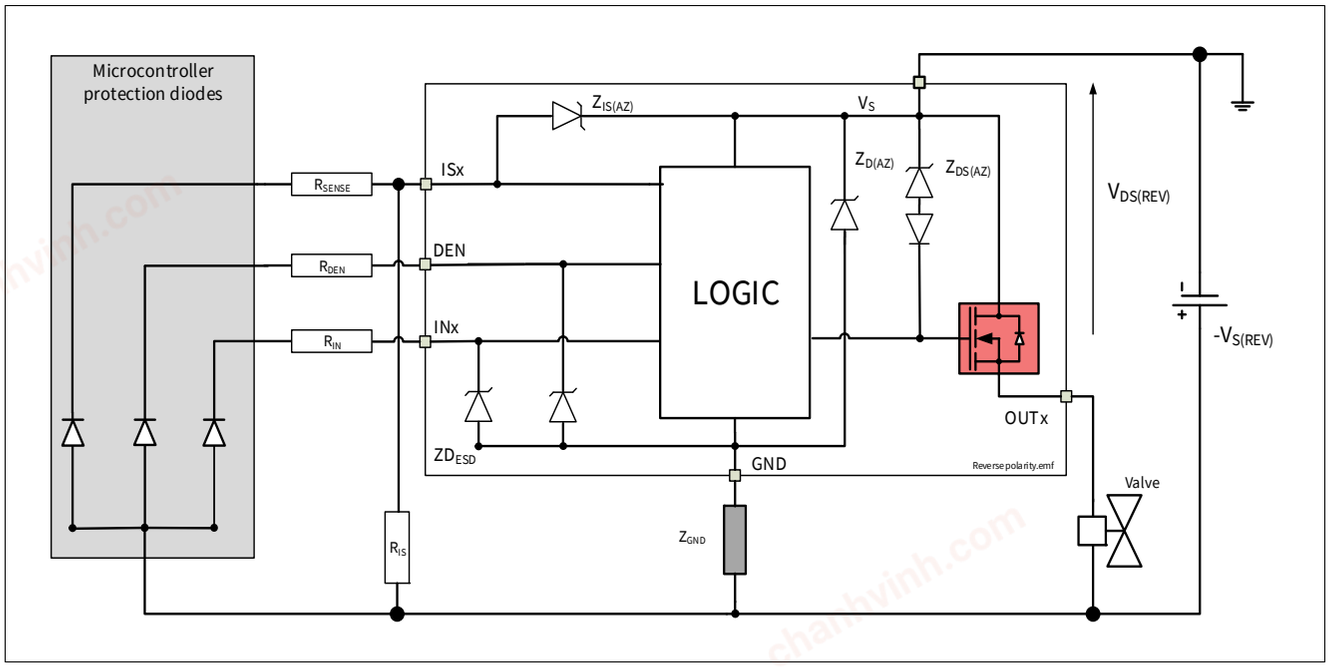



**Figure 18 Reverse Polarity Protection with External Components**

## 6.5 Overload Protection

In case of overload, such as high inrush of cold lamp filament, or short circuit to ground, the BTF6070-2ERV offers several protection mechanisms.

### 6.5.1 Current Limitation

At first step, the instantaneous power in the switch is maintained at a safe value by limiting the current to the maximum current allowed in the switch $I_{L(SC)}$. During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS.

### 6.5.2 Temperature Limitation in the Power DMOS

Each channel incorporates both an absolute ($T_{J(SC)}$) and a dynamic ($T_{J(SW)}$) temperature sensor. Activation of either sensor will cause an overheated channel to switch OFF to prevent destruction. Any protective switch OFF latches the output until the temperature has reached an acceptable value. **Figure 19** gives a sketch of the situation.

No retry strategy is implemented such that when the DMOS temperature has cooled down enough, the switch is switched ON again. Only the IN pin signal toggling can re-activate the power stage (latch behavior).

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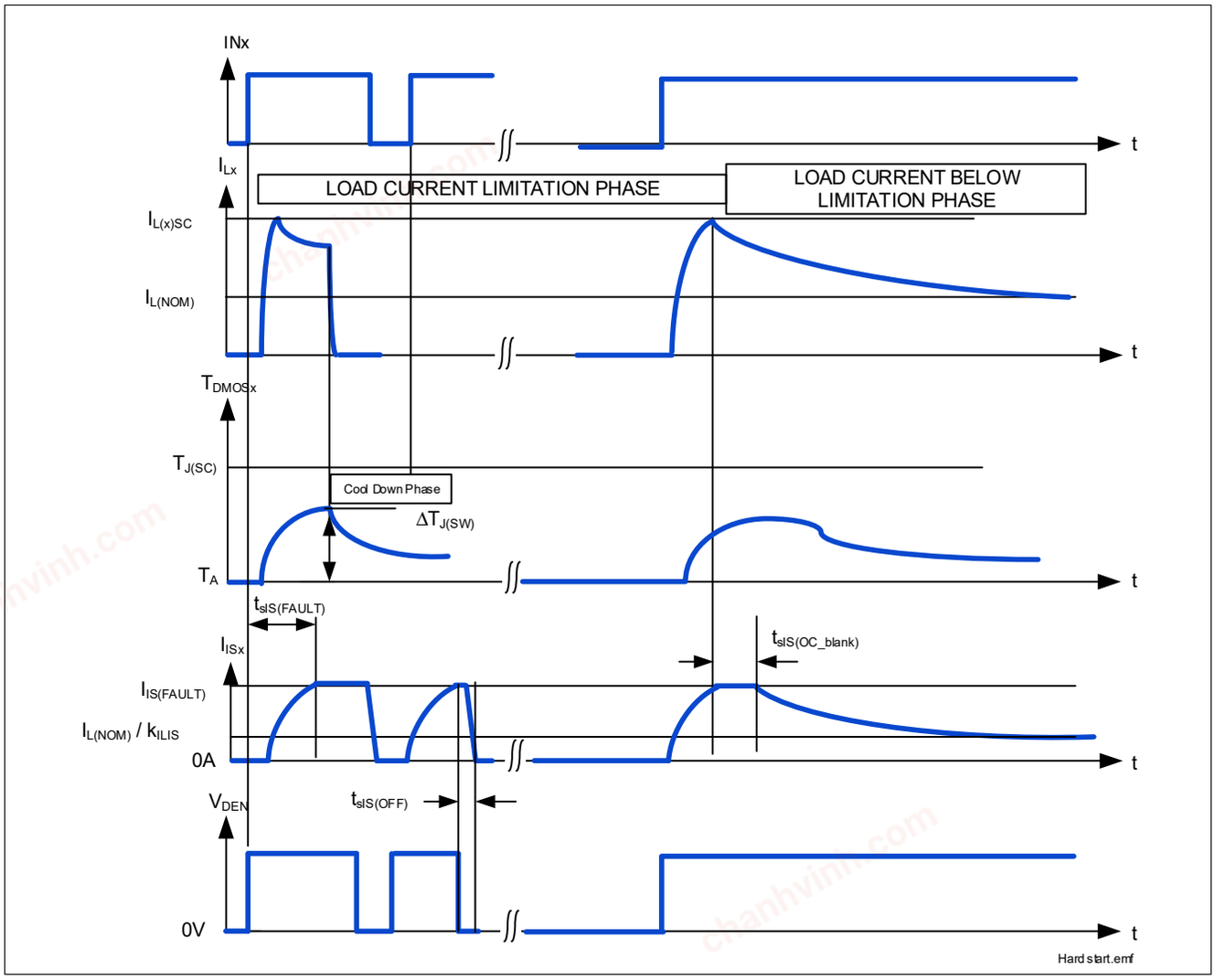



**Figure 19 Overload Protection**

*Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.*

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## 6.6 Electrical Characteristics for the Protection Functions

**Table 7 Electrical Characteristics: Protection**

$V_S$ = 8 V to 36 V, $T_J$ = -40°C to 150°C (unless otherwise specified).
Typical values are given at $V_S$ = 28 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Loss of Ground** | | | | | | | |
| Output leakage current while GND disconnected | $I_{OUT(GND)}$ | - | 0.1 | - | µA | 1)2) $V_S$ = 45 V<br>See **Figure 15** | P_6.6.1 |
| **Reverse Polarity** | | | | | | | |
| Drain source diode voltage during reverse polarity | $V_{DS(REV)}$ | 400 | 650 | 700 | mV | $I_L$ = - 2 A<br>$T_J$ = 150°C<br>See **Figure 18** | P_6.6.2 |
| **Overvoltage** | | | | | | | |
| Overvoltage protection | $V_{S(AZ)}$ | 65 | 70 | 75 | V | $I_{SOV}$ = 5 mA<br>See **Figure 17** | P_6.6.3 |
| **Overload Condition** | | | | | | | |
| Load current limitation | $I_{L5(SC)}$ | 9 | 11 | 14 | A | 3) $V_{DS}$ = 10 V<br>See **Figure 19** | P_6.6.4 |
| Dynamic temperature increase while switching | $\Delta T_{J(SW)}$ | - | 80 | - | K | 4) 3) See **Figure 19** | P_6.6.8 |
| Thermal shutdown temperature | $T_{J(SC)}$ | 150 | 170 4) | 200 4) | °C | 5) See **Figure 19** | P_6.6.10 |
| Thermal shutdown hysteresis | $\Delta T_{J(SC)}$ | - | 30 | - | K | 2) See **Figure 19** | P_6.6.11 |

1) All pins are disconnected except VS and OUT.
2) Not Subject to production test, specified by design
3) Test at $T_J$ = -40°C only
4) Functional test only
5) Test at $T_J$ = +150°C only

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# 7 Diagnostic Functions

For diagnosis purpose, the BTF6070-2ERV provides a combination of digital and analog signals at the IS Pins (IS0 and IS1). These signals are called SENSE. In case the diagnostic is disabled via DEN, pins IS become high impedance. In case DEN is activated, the sense current of both channels is enabled. **Table 8** gives the truth table.

**Table 8 Diagnostic Truth Table**

| DEN | IS0 | IS1 |
|---|---|---|
| 0 | Z | Z |
| 1 | Sense output 0 $I_{IS(0)}$ | Sense output 1 $I_{IS(1)}$ |

## 7.1 IS Pins

The BTF6070-2ERV provides a sense signal called $I_{IS}$ at pins ISx. As long as no “hard” failure mode occurs (short circuit to GND / current limitation / overtemperature / excessive dynamic temperature increase or open load at OFF) a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_{IS}$) is provided. The complete IS pins and diagnostic mechanism is described on **Figure 20**. The accuracy of the sense current depends on temperature and load current. Due to the ESD protection, in connection to $V_S$, it is not recommended to share the IS pins with other devices if these devices are using another battery feed. The consequence is that the unsupplied device would be fed via the IS pin of the supplied device.

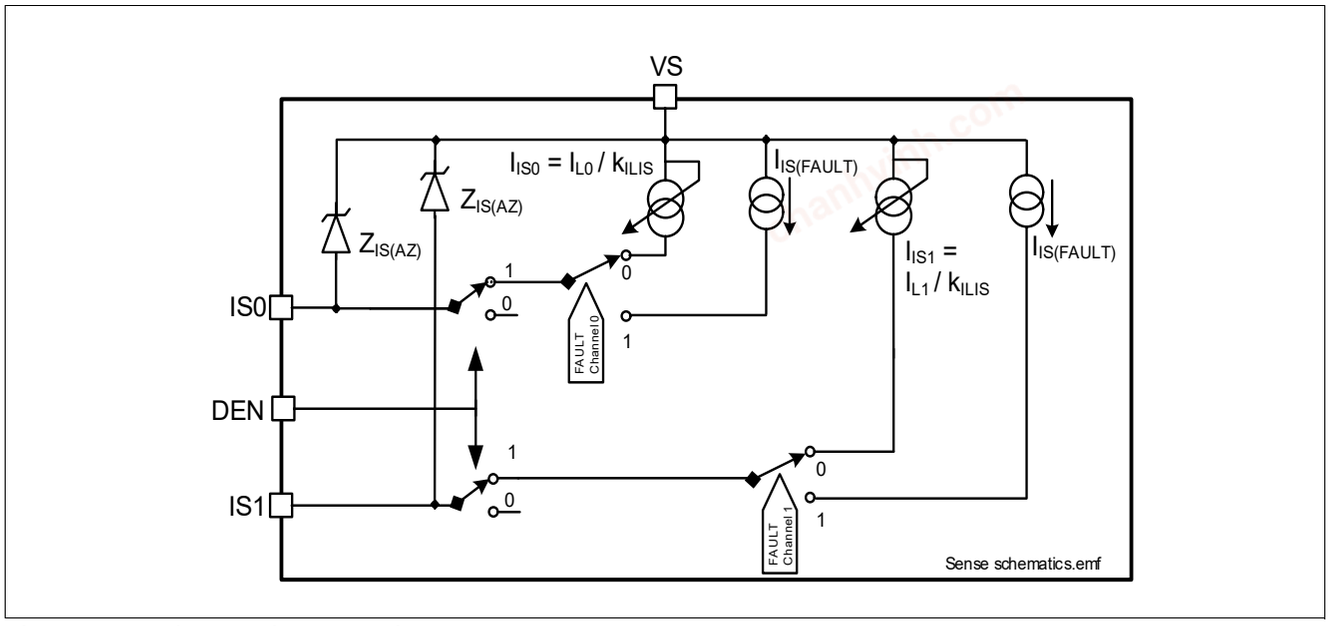



**Figure 20 Diagnostic Block Diagram**

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## 7.2 SENSE Signal in Different Operating Modes

Table 9 gives a quick reference for the state of the IS pins during device operation.

**Table 9 Sense Signal, Function of Operation Mode**

| Operation Mode | Input level Channel X | DEN | Output Level | Diagnostic Output at ISx |
|---|---|---|---|---|
| Normal operation | OFF | H | Z | Z |
| Short circuit to GND | | | ~ GND | Z |
| Overtemperature | | | Z | Z |
| Short circuit to $V_S$ | | | $V_S$ | $I_{IS(FAULT)}$ |
| Open Load | | | $< V_{OL(OFF)}$<br>$> V_{OL(OFF)}$ [1] | Z<br>$I_{IS(FAULT)}$ |
| Inverse current | | | ~ $V_{INV}$ | $I_{IS(FAULT)}$ |
| Normal operation | ON | | ~ $V_S$ | $I_{IS} = I_L / k_{ILIS}$ |
| Current limitation | | | $< V_S$ | $I_{IS(FAULT)}$ |
| Short circuit to GND | | | ~ GND | $I_{IS(FAULT)}$ |
| Overtemperature $T_{J(SW)}$ event | | | Z | $I_{IS(FAULT)}$ |
| Short circuit to $V_S$ | | | $V_S$ | $I_{IS} < I_L / k_{ILIS}$ |
| Open Load | | | ~ $V_S$ [2] | $I_{IS} < I_{IS(OL)}$ |
| Inverse current | | | ~ $V_{INV}$ | $I_{IS} < I_{IS(OL)}$ [3] |
| Underload | | | ~ $V_S$ [4] | $I_{IS(OL)} < I_{IS} < I_L / k_{ILIS}$ |
| Don’t care | Don’t care | L | Don’t care | Z |

1) Stable with additional pull-up resistor.
2) The output current has to be smaller than $I_{L(OL)}$.
3) After maximum $t_{INV}$.
4) The output current has to be higher than $I_{L(OL)}$.

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## 7.3 SENSE Signal in the Nominal Current Range

**Figure 21** and **Figure 22** show the current sense as a function of the load current in the power DMOS. Usually a pull-down resistor $R_{IS}$ is connected to the current sense IS pin. This resistor has to be higher than 560 Ω to limit the power losses in the sense circuitry. A typical value is 1.8 kΩ. The blue curve represents the ideal sense current, assuming an ideal $k_{ILIS}$ factor value. The red curves shows the accuracy the device provides across full temperature range at a defined current.

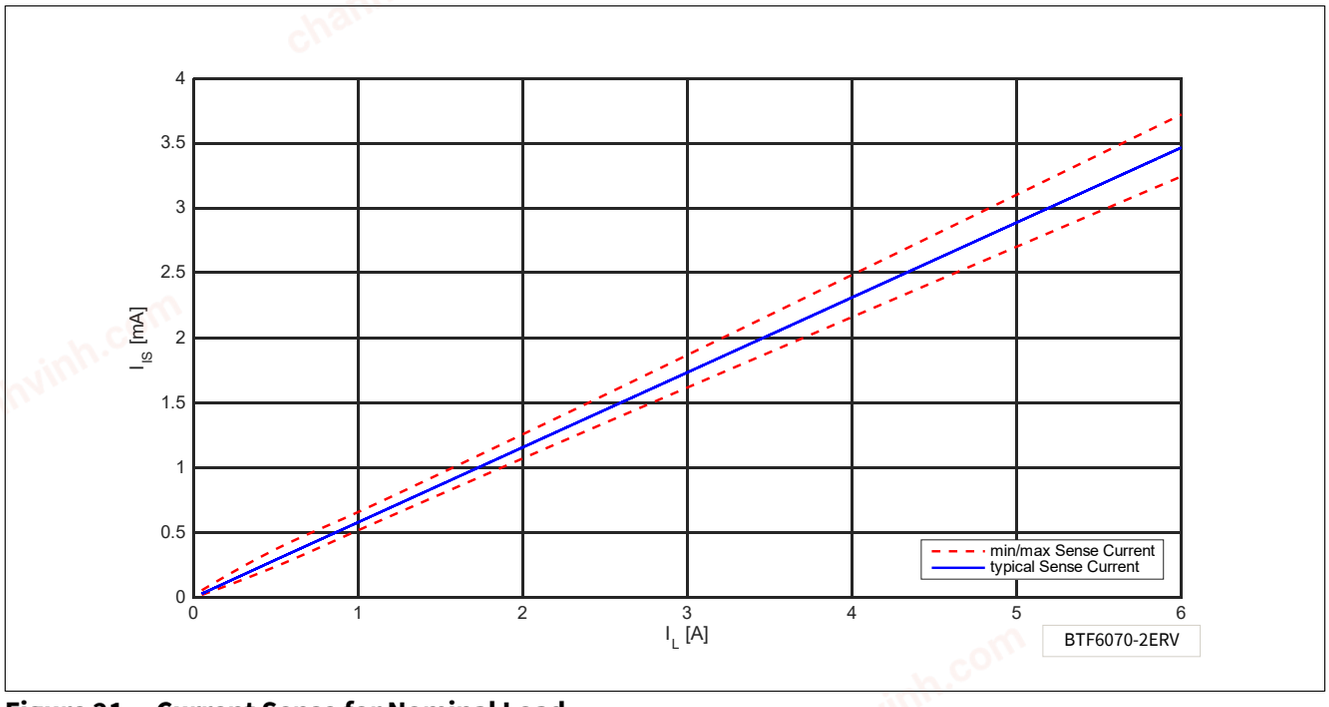



**Figure 21 Current Sense for Nominal Load**

### 7.3.1 SENSE Signal Variation as a Function of Temperature and Load Current

In some applications a better accuracy is required at smaller currents. To achieve this accuracy requirement, a calibration on the application is possible. To avoid multiple calibration points at different load and temperature conditions, the BTF6070-2ERV allows limited derating of the $k_{ILIS}$ value, at a given point ($T_J$= +25°C). This derating is described by the parameter $\Delta k_{ILIS}$. **Figure 22** shows the behavior of the sense current, assuming one calibration point at nominal load at +25°C.

The blue line indicates the ideal $k_{ILIS}$ ratio.

The red lines indicate the derating on the parameter across temperature and voltage, assuming one calibration point at nominal temperature and nominal battery voltage.

The black lines indicate the $k_{ILIS}$ accuracy without calibration.

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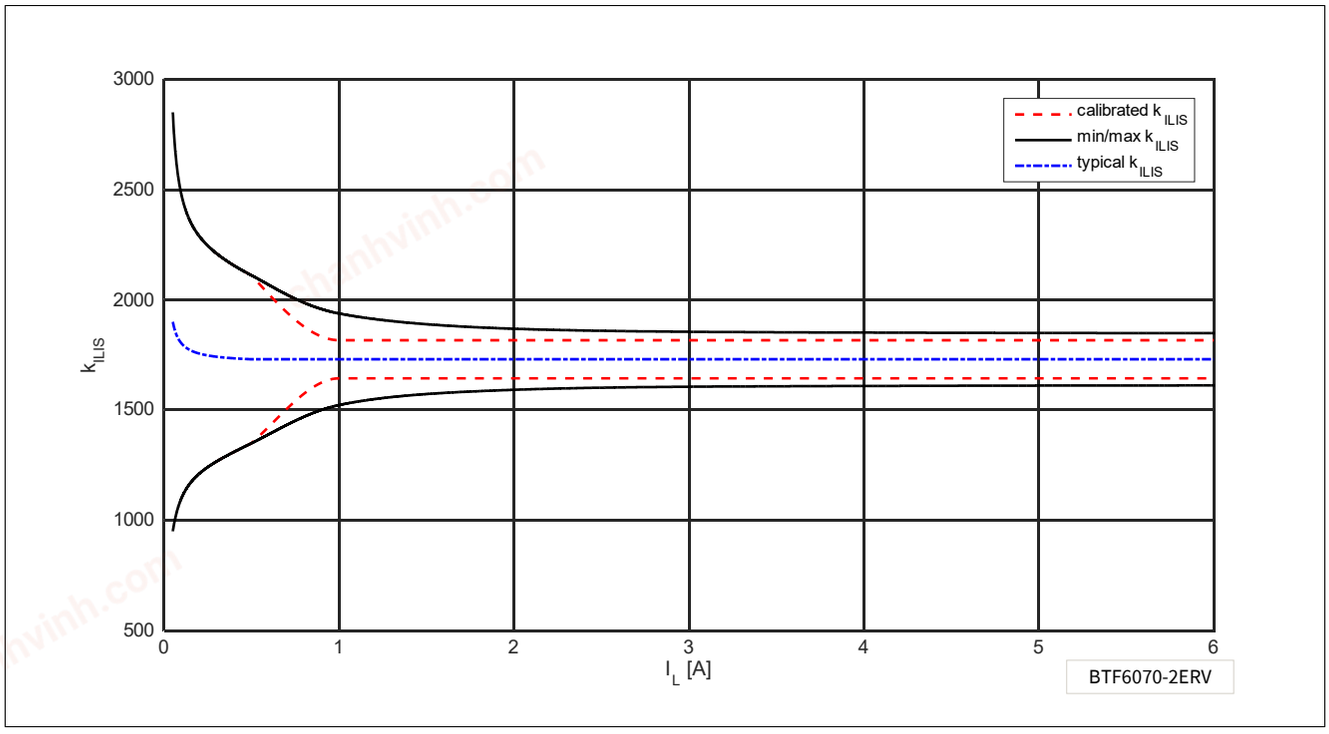



**Figure 22 Improved Current Sense Accuracy with One Calibration Point**

### 7.3.2 SENSE Signal Timing

**Figure 23** shows the timing during settling and disabling of the SENSE.

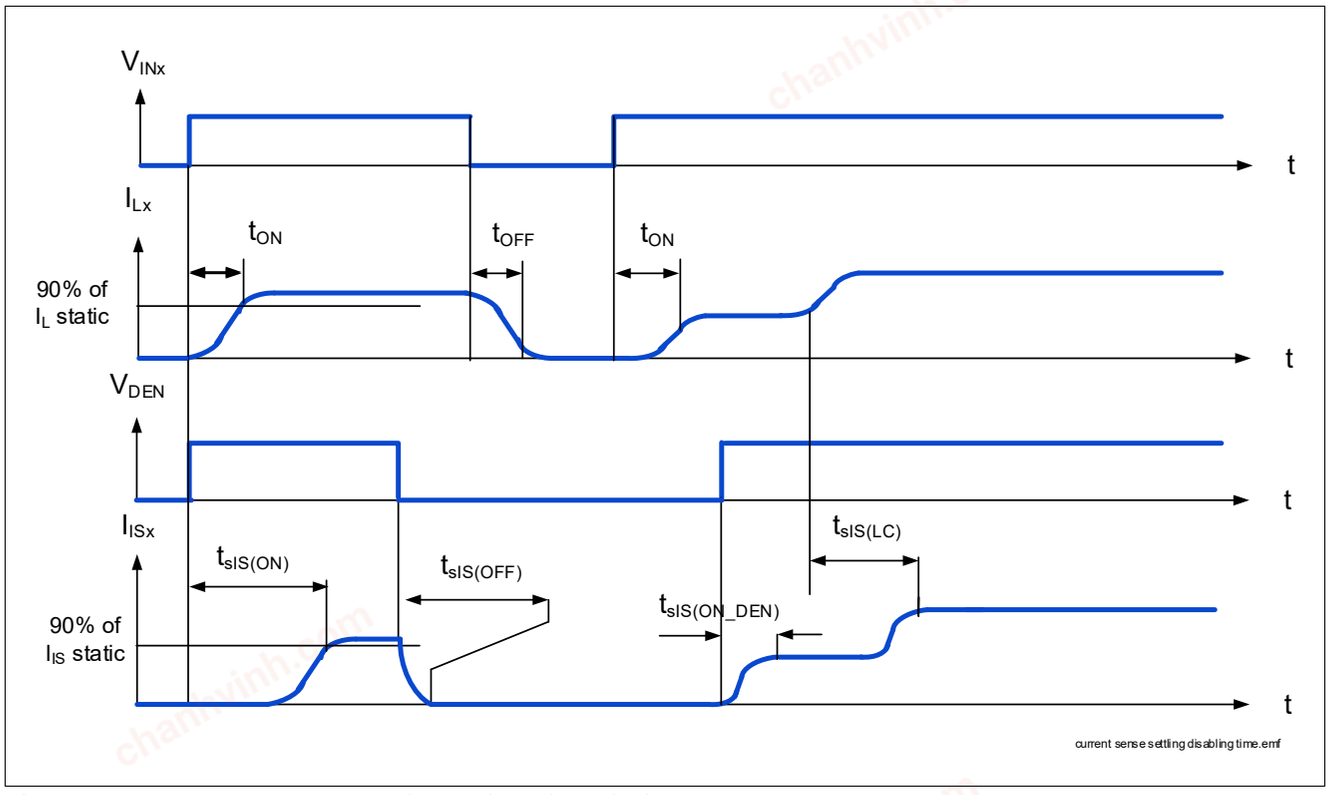



**Figure 23 Current Sense Settling / Disabling Timing**

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### 7.3.3 SENSE Signal in Open Load

#### 7.3.3.1 Open Load in ON Diagnostic

If the channel is ON, a leakage current can still flow through an open load, for example due to humidity. The parameter $I_{L(OL)}$ gives the threshold of recognition for this leakage current. If the current $I_L$ flowing out the power DMOS is below this value, the device recognizes a failure, if the DEN is selected. In that case, the SENSE current is below $I_{IS(OL)}$. Otherwise, the minimum SENSE current is given above parameter $I_{IS(OL)}$. **Figure 24** shows the SENSE current behavior in this area. The red curve shows a typical product curve. The blue curve shows the ideal current sense.

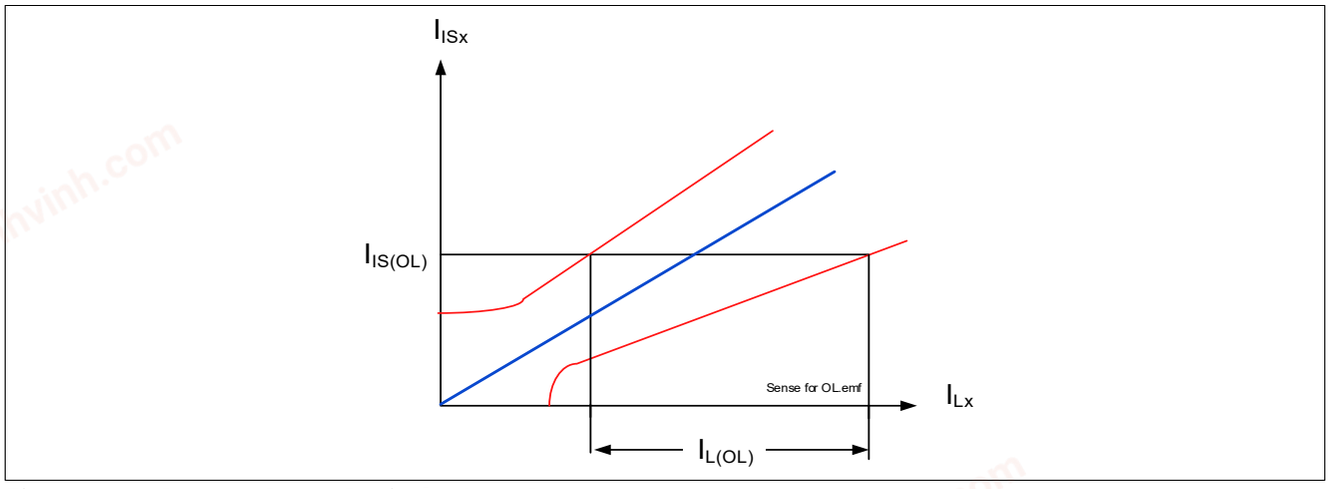



**Figure 24 Current Sense Ratio for Low Currents**

#### 7.3.3.2 Open Load in OFF Diagnostic

For open load diagnosis in OFF-state, an external output pull-up resistor ($R_{OL}$) is recommended. For the calculation of pull-up resistor value, the leakage currents and the open load threshold voltage $V_{OL(OFF)}$ have to be taken into account. **Figure 25** gives a sketch of the situation. $I_{leakage}$ defines the leakage current in the complete system, including $I_{L(OFF)}$ (see **Chapter 5.5**) and external leakages, e.g, due to humidity, corrosion, etc... in the application.

To reduce the stand-by current of the system, an open load resistor switch $S_{OL}$ is recommended. If the channel x is OFF, the output is no longer pulled down by the load and $V_{OUT}$ voltage rises to nearly $V_S$. This is recognized by the device as an open load. The voltage threshold is given by $V_{OL(OFF)}$. In that case, the SENSE signal is switched to the $I_{IS(FAULT)}$.

An additional $R_{PD}$ resistor can be used to pull $V_{OUT}$ to 0 V. Otherwise, the OUT pin is floating. This resistor can be used as well for short circuit to battery detection, see **Chapter 7.3.4**.

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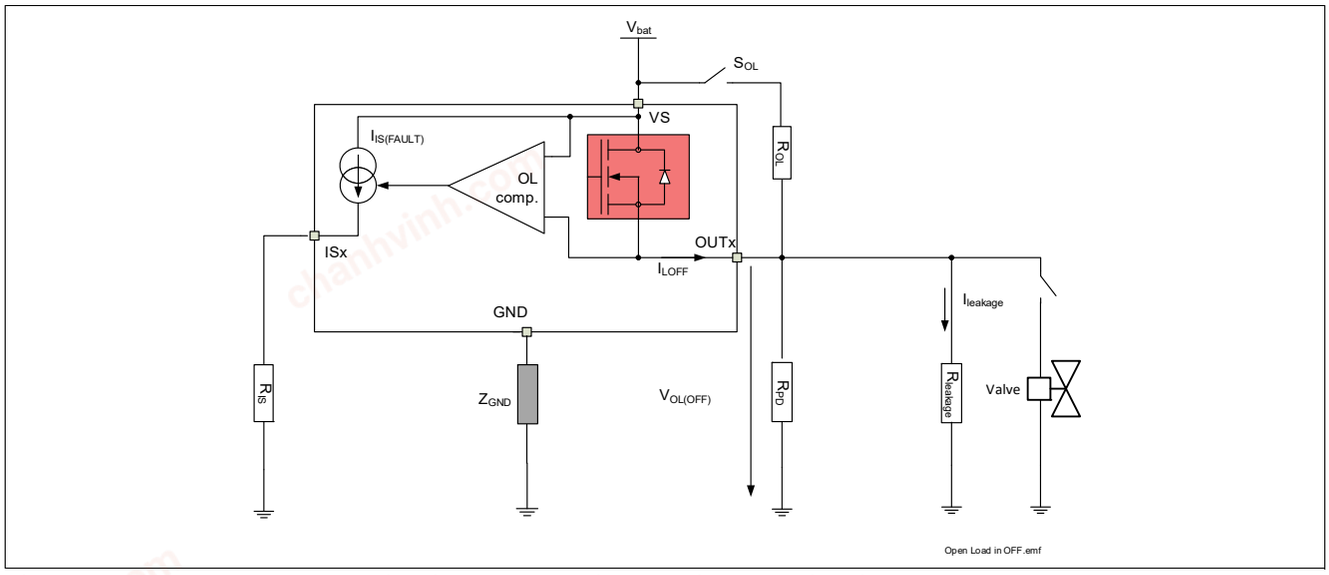



**Figure 25 Open Load Detection in OFF Electrical Equivalent Circuit**

### 7.3.3.3 Open Load Diagnostic Timing

**Figure 26** shows the timing during either Open Load in ON or OFF condition when the DEN pin is HIGH. Please note that a delay $t_{sIS(FAULT_OL_OFF)}$ has to be respected after the falling edge of the input, when applying an open load in OFF diagnosis request, otherwise the diagnosis can be wrong.

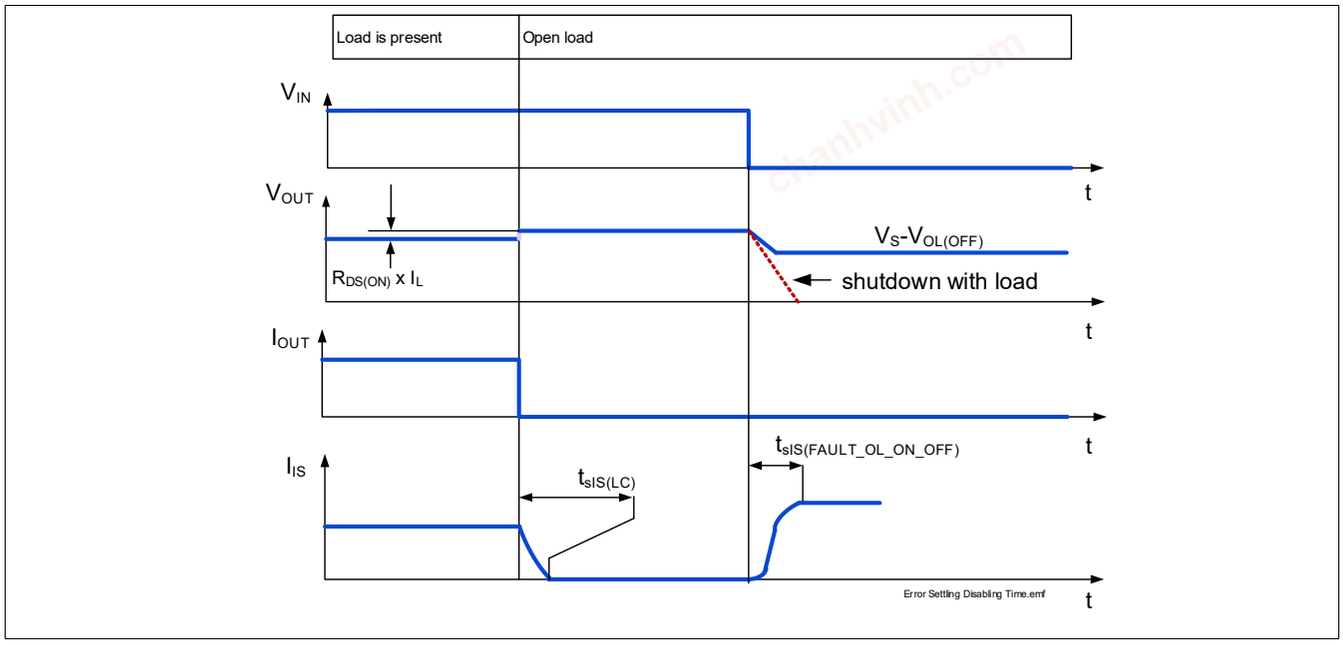



**Figure 26 Sense Signal in Open Load Timing**

### 7.3.4 SENSE Signal with OUT in Short Circuit to $V_S$

In case of a short circuit between the OUTput-pin and the $V_S$ pin, all or portion (depending on the short circuit impedance) of the load current will flow through the short circuit. As a result, a lower current compared to the normal operation will flow through the DMOS of the BTF6070-2ERV, which can be recognized at the current sense signal. The open load at OFF detection circuitry can also be used to distinguish a short circuit to $V_S$. In that case, an external resistor to ground $R_{SC_VS}$ is required. **Figure 27** gives a sketch of the situation.

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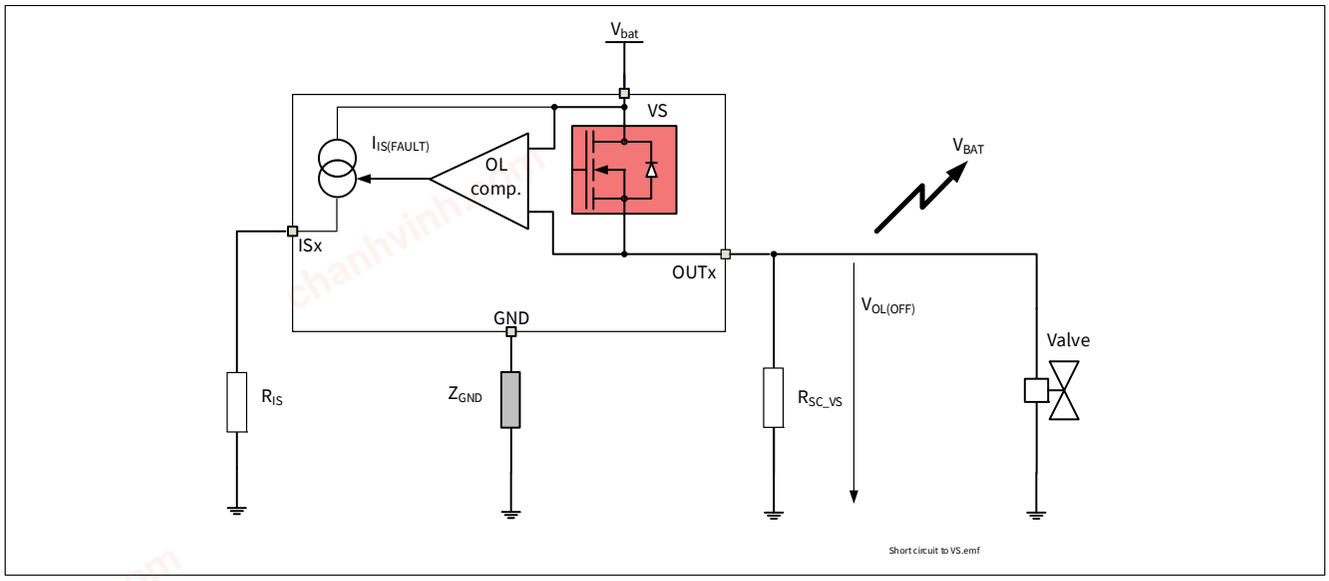



**Figure 27 Short Circuit to Battery Detection in OFF Electrical Equivalent Circuit**

### 7.3.5 SENSE Signal in Case of Overload

An overload condition is defined by a current flowing out of the DMOS reaching the current limitation and / or the absolute dynamic temperature swing $T_{J(SW)}$ is reached, and / or the junction temperature reaches the thermal shutdown temperature $T_{J(SC)}$. Please refer to **Chapter 6.5** for details.

In that case, the SENSE signal given is by $I_{IS(FAULT)}$ when the diagnostic is selected.

The device has a thermal latch behavior, such that when the overtemperature or the exceed dynamic temperature condition has disappeared, the DMOS is reactivated only when the IN is toggled LOW to HIGH. If the DEN pin is activated the SENSE follows the output stage. If no reset of the latch occurs, the device remains in the latching phase and $I_{S(FAULT)}$ at the IS pin, even though the DMOS is OFF.

### 7.3.6 SENSE Signal in Case of Inverse Current

In the case of inverse current, the sense signal of the affected channel will indicate open load in OFF state and indicate open load in ON state. The unaffected channels indicate normal behavior as long as the $I_{INV}$ current is not exceeding the maximum value specified in **Chapter 5.4**.

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## 7.4 Electrical Characteristics Diagnostic Functions

**Table 10 Electrical Characteristics: Diagnostics**

$V_S$ = 8 V to 36 V, $T_J$ = -40°C to 150°C (unless otherwise specified).
Typical values are given at $V_S$ = 28 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Load Condition Threshold for Diagnostic** | | | | | | | |
| Open load detection threshold in OFF state | $V_S - V_{OL(OFF)}$ | 4 | - | 6 | V | $V_{IN}$ = 0 V<br>$V_{DEN}$ = 4.5 V<br>See **Figure 26** | P_7.5.1 |
| Open load detection threshold in ON state | $I_{L(OL)}$ | 5 | - | 35 | mA | $V_{IN} = V_{DEN}$ = 4.5 V<br>$I_{IS(OL)}$ = 10 µA<br>See **Figure 24** | P_7.5.2 |
| Open load detection threshold in ON state (10 mA) | $I_{L2(OL)}$ | 10 | - | 50 | mA | $V_{IN} = V_{DEN}$ = 4.5 V<br>$I_{IS(OL)}$ = 16 µA | P_7.5.36 |
| **Sense Pin** | | | | | | | |
| IS pin leakage current when sense is disabled | $I_{IS_(DIS)}$ | - | 0.02 | 1 | µA | $V_{IN}$ = 4.5 V<br>$V_{DEN}$ = 0 V<br>$I_L = I_{L4}$ = 4 A | P_7.5.4 |
| Sense signal saturation voltage | $V_S - V_{IS(RANGE)}$ | 1.5 | - | 3.5 | V | $V_{IN}$ = 0 V<br>$V_{OUT} = V_S$ > 10 V<br>$V_{DEN}$ = 4.5 V<br>$I_{IS}$ = 6 mA | P_7.5.6 |
| Sense signal maximum current in fault condition | $I_{IS(FAULT)}$ | 6 | 12.5 | 30 | mA | $V_{IS} = V_{IN}$ = 0 V<br>$V_{OUT} = V_S$ > 10 V<br>$V_{DEN}$ = 4.5 V<br>See **Figure 20** | P_7.5.7 |
| Sense pin maximum voltage | $V_{IS(AZ)}$ | 65 | 70 | 75 | V | $I_{IS}$ = 5 mA<br>See **Figure 20** | P_7.5.3 |
| **Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition** | | | | | | | |
| Current sense ratio $I_{L0}$ = 50 mA | $k_{ILIS0}$ | -50% | 1900 | +50% | | $V_{IN}$ = 4.5 V<br>$V_{DEN}$ = 4.5 V<br>See **Figure 21**<br>$T_J$ = -40°C; 150°C | P_7.5.8 |
| Current sense ratio $I_{L1}$ = 0.5 A | $k_{ILIS1}$ | -22% | 1730 | +22% | | | P_7.5.9 |
| Current sense ratio $I_{L2}$ = 1 A | $k_{ILIS2}$ | -12% | 1730 | +12% | | | P_7.5.10 |
| Current sense ratio $I_{L3}$ = 2 A | $k_{ILIS3}$ | -8% | 1730 | +8% | | | P_7.5.11 |
| Current sense ratio $I_{L4}$ = 4 A | $k_{ILIS4}$ | -7% | 1730 | +7% | | | P_7.5.12 |

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**Table 10 Electrical Characteristics: Diagnostics** (cont'd)

$V_S$ = 8 V to 36 V, $T_J$ = -40°C to 150°C (unless otherwise specified).
Typical values are given at $V_S$ = 28 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| $k_{ILIS}$ derating with current and temperature | $\Delta k_{ILIS}$ | -5 | 0 | +5 | % | 1) $k_{ILIS3}$ versus $k_{ILIS2}$ See **Figure 22** | P_7.5.17 |
| $k_{ILIS}$ derating with current and temperature ($k_{ILIS2}$ -$k_{ILIS1}$) | $\Delta k_{ILIS}$ | -8 | 0 | +8 | % | 1) $k_{ILIS2}$ versus $k_{ILIS1}$ | P_7.5.37 |
| **Diagnostic Timing in Normal Condition** | | | | | | | |
| Current sense settling to 90% of $I_{IS}$ static after positive input slope on both INput and DEN | $t_{sIS(ON)}$ | - | - | 90 | µs | 2)3) $V_{DEN}$ = $V_{IN}$ = 0 to 4.5 V<br>$V_S$ = 28 V<br>$R_{IS}$ = 1.8 kΩ<br>$C_{SENSE}$ < 100 pF<br>$R_L$ = 25 Ω<br>See **Figure 23** | P_7.5.18 |
| Current sense settling time with load current stable and transition of the DEN | $t_{sIS(ON_DEN)}$ | - | - | 10 | µs | $V_{IN}$ = 4.5 V<br>$V_{DEN}$ = 0 to 4.5 V<br>$R_{IS}$ = 1.8 kΩ<br>$C_{SENSE}$ < 100 pF<br>$I_L$ = $I_{L3}$ = 2 A<br>See **Figure 23** | P_7.5.19 |
| Current sense settling time to $I_{IS}$ stable after positive input slope on current load | $t_{sIS(LC)}$ | - | - | 20 | µs | 1) $V_{IN}$ = 4.5 V<br>$V_{DEN}$ = 4.5 V<br>$R_{IS}$ = 1.8 kΩ<br>$C_{SENSE}$ < 100 pF<br>$I_L$ = $I_{L3}$ = 2 A to $I_L$ = $I_{L4}$ = 4 A<br>See **Figure 23** | P_7.5.20 |
| **Diagnostic Timing in Open Load Condition** | | | | | | | |
| Current sense settling time for open load detection in OFF state | $t_{sIS(FAULT_OL_OFF)}$ | - | - | 90 | µs | $V_{IN}$ = 0 V<br>$V_{DEN}$ = 0 to 4.5 V<br>$R_{IS}$ = 1.8 kΩ<br>$C_{SENSE}$ < 100 pF<br>$V_{OUT}$ = $V_S$ = 28 V | P_7.5.22 |
| Current sense settling time for open load detection in ON-OFF transition | $t_{sIS(FAULT_OL_ON_OFF)}$ | - | 200 | 350 | µs | 1) $V_{IN}$ = 4.5 to 0V<br>$V_{DEN}$ = 4.5 V<br>$R_{IS}$ = 1.8 kΩ<br>$C_{SENSE}$ < 100 pF<br>$V_{OUT}$ = $V_S$ = 28 V<br>See **Figure 26** | P_7.5.23 |

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**Table 10 Electrical Characteristics: Diagnostics** (cont'd)

$V_S$ = 8 V to 36 V, $T_J$ = -40°C to 150°C (unless otherwise specified).
Typical values are given at $V_S$ = 28 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Diagnostic Timing in Overload Condition** | | | | | | | |
| Current sense settling time for overload detection | $t_{sIS(FAULT)}$ | - | - | 90 | µs | 2)3) $V_{IN}$ =$V_{DEN}$= 0 to 4.5 V<br>$V_S$ =13.5 V<br>$R_{IS}$ = 1.8 kΩ<br>$C_{SENSE}$< 100 pF<br>$V_{DS}$ = 10 V<br>See **Figure 19** | P_7.5.24 |
| Current sense over current blanking time | $t_{sIS(OC_blank)}$ | - | 350 | - | µs | 1) $V_{IN}$ = $V_{DEN}$ = 4.5 V<br>$R_{IS}$ = 1.8 kΩ<br>$C_{SENSE}$ < 100 pF<br>$V_{DS}$= 5 V to 0 V<br>See **Figure 19** | P_7.5.32 |
| Diagnostic disable time DEN transition to $I_{IS}$ < 50% $I_L$ / $k_{ILIS}$ | $t_{sIS(OFF)}$ | - | - | 20 | µs | 1) $V_{IN}$ = 4.5 V<br>$V_{DEN}$ = 4.5 V to 0 V<br>$R_{IS}$ = 1.8 kΩ<br>$C_{SENSE}$ < 100 pF<br>$I_L$ = $I_{L3}$ = 2 A<br>See **Figure 23** | P_7.5.25 |

1) Not subject to production test, specified by design
2) Test at $T_J$ = -40°C only
3) Production test for functionality within parameter limits

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# 8 Input Pins

## 8.1 Input Circuitry

The input circuitry is compatible with 3.3 and 5 V microcontrollers. The concept of the input pin is to react to voltage thresholds. An implemented Schmitt trigger avoids any undefined state if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state. The input circuitry is compatible with PWM applications. **Figure 28** shows the electrical equivalent input circuitry. In case the pin is not needed, it must be left opened, or must be connected to device ground (and not module ground) via an 10 kΩ input resistor.

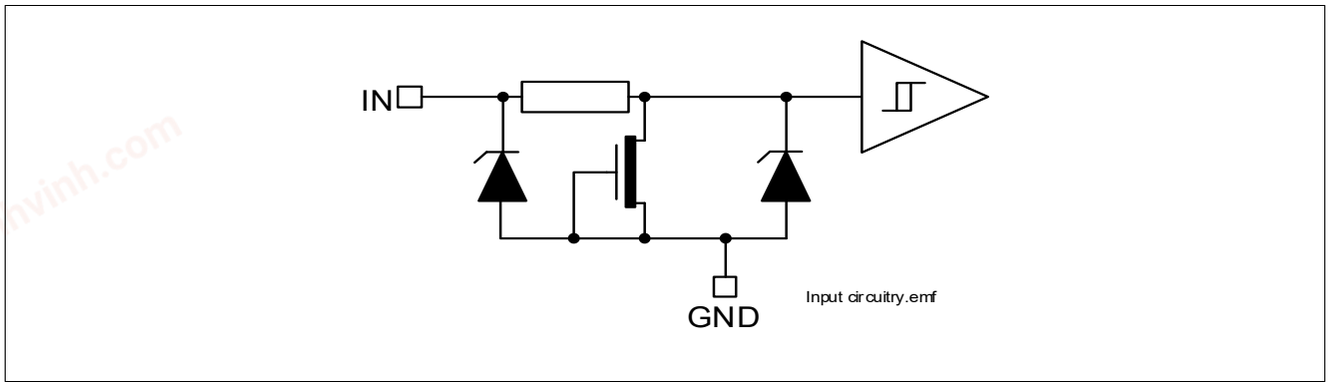



**Figure 28 Input Pin Circuitry**

## 8.2 DEN Pin

The DEN pin enable and disable the diagnostic functionality of the device. The pins have the same structure as the INput pins, please refer to **Figure 28**.

## 8.3 Input Pin Voltage

The IN and DEN use a comparator with hysteresis. The switching ON / OFF takes place in a defined region, set by the thresholds $V_{IN(L)}$ Max. and $V_{IN(H)}$ Min. The exact value where the ON and OFF take place are unknown and depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, a hysteresis is implemented. This ensures a certain immunity to noise.

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## 8.4 Electrical Characteristics

**Table 11 Electrical Characteristics: Input Pins**

$V_S$ = 8 V to 36 V, $T_J$ = -40°C to 150°C (unless otherwise specified).
Typical values are given at $V_S$ = 28 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **INput Pins Characteristics** | | | | | | | |
| Low level input voltage range | $V_{IN(L)}$ | -0.3 | - | 0.8 | V | | P_8.4.1 |
| High level input voltage range | $V_{IN(H)}$ | 2 | - | 6 | V | | P_8.4.2 |
| Input voltage hysteresis | $V_{IN(HYS)}$ | - | 250 | - | mV | 1) | P_8.4.3 |
| Low level input current | $I_{IN(L)}$ | 1 | 10 | 25 | µA | $V_{IN}$ = 0.8 V | P_8.4.4 |
| High level input current | $I_{IN(H)}$ | 2 | 10 | 25 | µA | $V_{IN}$ = 5.5 V | P_8.4.5 |
| **DEN Pin** | | | | | | | |
| Low level input voltage range | $V_{DEN(L)}$ | -0.3 | - | 0.8 | V | - | P_8.4.6 |
| High level input voltage range | $V_{DEN(H)}$ | 2 | - | 6 | V | - | P_8.4.7 |
| Input voltage hysteresis | $V_{DEN(HYS)}$ | - | 250 | - | mV | 1) | P_8.4.8 |
| Low level input current | $I_{DEN(L)}$ | 1 | 10 | 25 | µA | $V_{DEN}$ = 0.8 V | P_8.4.9 |
| High level input current | $I_{DEN(H)}$ | 2 | 10 | 25 | µA | $V_{DEN}$ = 5.5 V | P_8.4.10 |

1) Not subject to production test, specified by design

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# 9 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

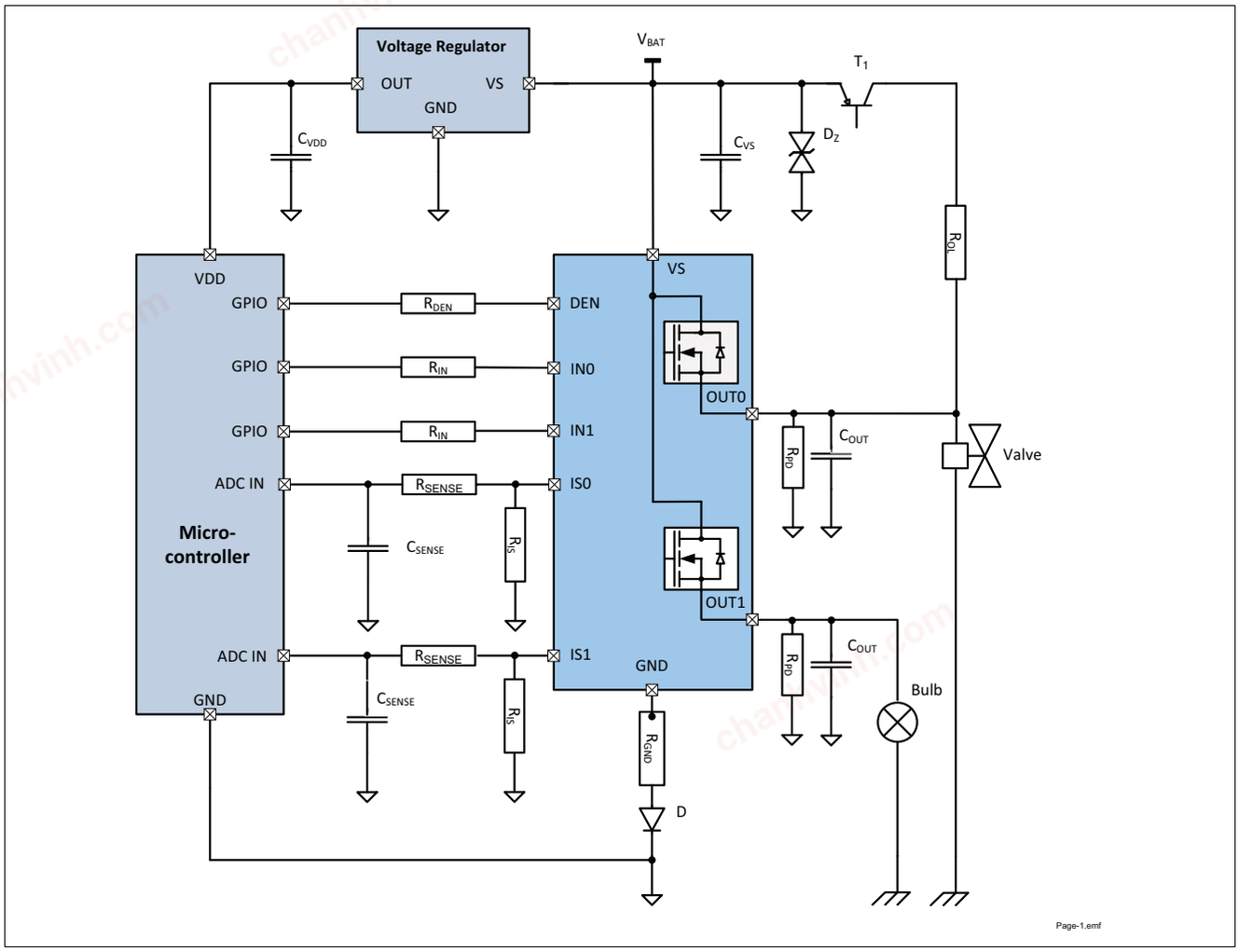



**Figure 29 Application Diagram with BTF6070-2ERV**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

**Table 12 Bill of Material**

| Reference | Value | Purpose |
|---|---|---|
| $R_{IN}$ | 10 kΩ | Protection of the microcontroller during overvoltage, reverse polarity<br>Guarantee BTF6070-2ERV channels OFF during loss of ground |
| $R_{DEN}$ | 10 kΩ | Protection of the microcontroller during overvoltage, reverse polarity |
| $R_{PD}$ | 47 kΩ | Polarization of the output for short circuit to $V_S$ detection<br>Improve BTF6070-2ERV immunity to electromagnetic noise |
| $R_{OL}$ | 1.5 kΩ | Ensures polarization of the BTF6070-2ERV output during open load in OFF diagnostic |

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**Table 12 Bill of Material** (cont'd)

| Reference | Value | Purpose |
|---|---|---|
| $R_{IS}$ | 1.8 kΩ | Sense resistor |
| $R_{SENSE}$ | 4.7 kΩ | Overvoltage, reverse polarity, loss of ground. Value to be tuned with microcontroller specification. |
| $C_{SENSE}$ | 100 pF | Sense signal filtering. |
| $C_{OUT}$ | 10 nF | Protection of the device during ESD and BCI |
| T1 | Dual NPN/PNP | Switch the battery voltage for open load in OFF diagnostic |
| $R_{GND}$ | 27 Ω | Protection of the BTF6070-2ERV during overvoltage |
| D | BAS21 | Protection of the BTF6070-2ERV during reverse polarity |
| $Z$ | 58 V Zener diode | Protection of the device during overvoltage |
| $C_{VS}$ | 100 nF | Filtering of voltage spikes at the battery line |

## 9.1 Further Application Information

- Please contact us to get the pin FMEA
- Existing App. Notes
- For further information you may visit **www.infineon.com**

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# 10 Package Outlines

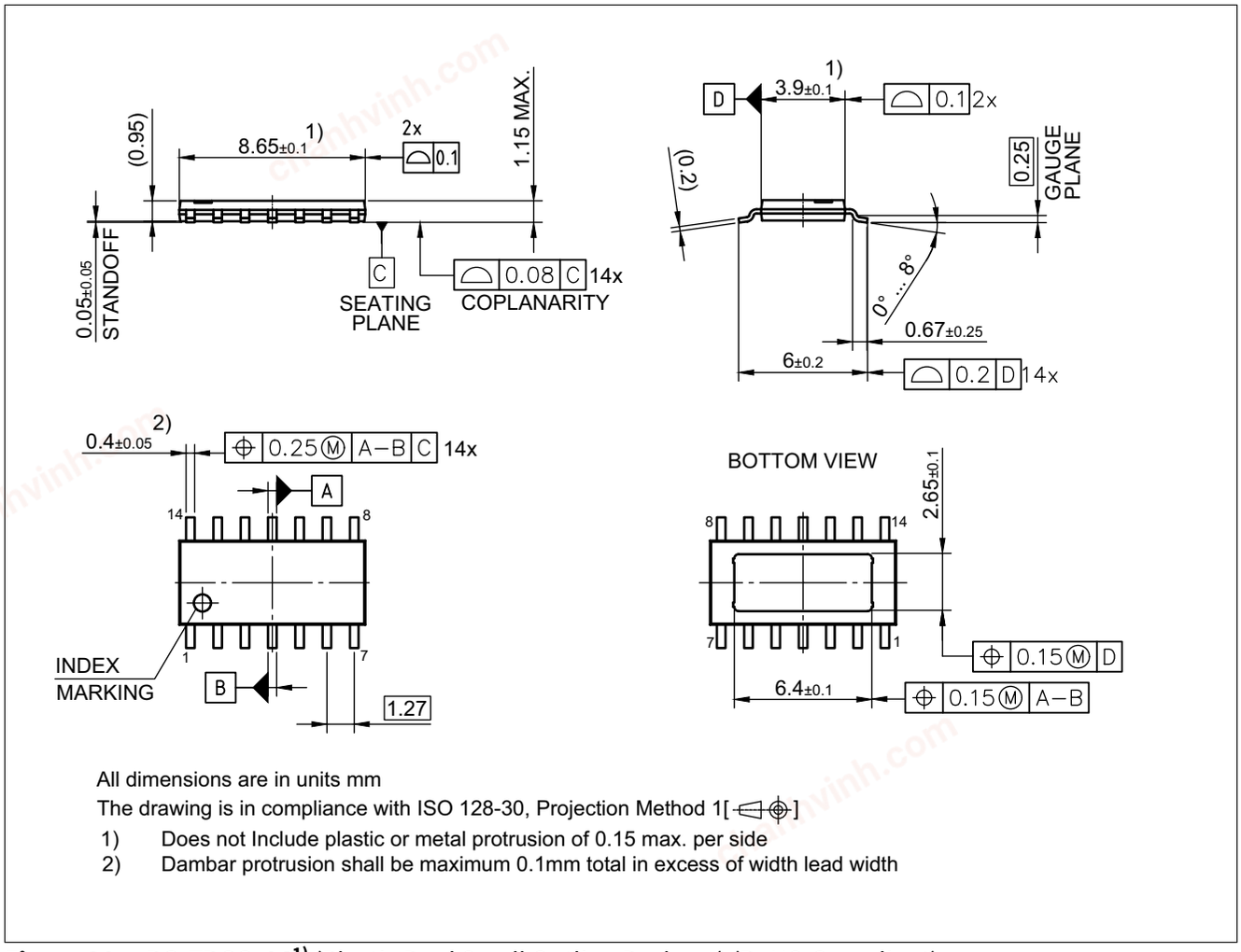



**Figure 30 PG-TDSO-14[1)]** (Plastic Dual Small Outline Package) (RoHS-Compliant)

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Legal Disclaimer for Short-Circuit Capability

Infineon disclaims any warranties and liablilities, whether expressed or implied, for any short-circuit failures below the threshold limit.

### Further information on packages

**https://www.infineon.com/packages**

1) Dimensions in mm

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# 11 Revision History

| Version | Date | Changes |
|---|---|---|
| Rev. 1.00 | 2019-04-25 | Creation of the document |

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