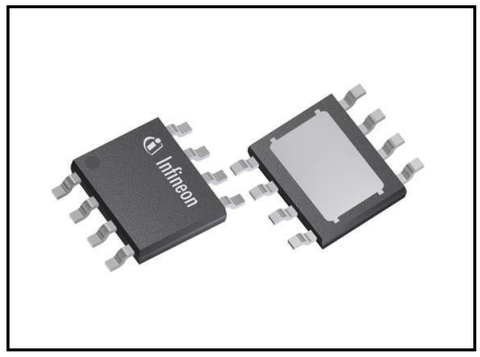
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BTF3050EJ

Smart Low-Side Power Switch

AEC Qualified RoHS



1 Overview

Features

- Single channel device
- 3.3V and 5V compatible logic input
- PWM switching capability 20kHz for 10-90% duty cycle
- Electrostatic discharge protection (ESD)
- Adjustable switching speed
- Digital latch feedback signal
- Very low power DMOS leakage current in OFF state
- DMOS turn on capability in inverse current situation
- Green Product (RoHS compliant)

Potential applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Allows high inrush currents and active freewheeling

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The BTF3050EJ is a 50 mΩ single channel Smart Low-Side Power Switch with in a PG-TDSO-8-31 package providing embedded protective functions. The power transistor is built by an N-channel vertical power MOSFET.
The device is monolithically integrated. The BTF3050EJ is automotive qualified and is optimized for 12V automotive and industrial applications.

Table 1 Product Summary

Operating voltage range	V_{OUT}	3 .. 28 V
Maximum battery voltage	$V_{BAT(LD)}$	40 V
Operating supply voltage range	V_{DD}	3.0 .. 5.5 V
Maximum input voltage	V_{IN}	5.5 V
Maximum On-State resistance at T_j = 150°C, V_{DD} = 5V, V_{IN} = 5V	$R_{DS(ON)}$	100 mΩ

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Overview

Table 1 Product Summary (cont'd)

Nominal load current	$I_{L(NOM)}$	4 A
Minimum current limitation	$I_{L(LIM)}$	10 A
Minimum current limitation trigger level	$I_{L(LIM)TRIGGER}$	29 A
Maximum OFF state load current at $T_J \leq 85°C$	$I_{L(OFF)}$	2 µA
Maximum stand-by supply current at $T_J = 25°C$	$I_{DD(OFF)}$	6 µA

Type	Package	Marking
BTF3050EJ	PG-TDSO-8-31	F3050EJ

Diagnostic Functions

- Short circuit to battery
- Over temperature shut down
- Stable latching diagnostic signal

Protection Functions

- Over temperature shutdown with auto-restart
- Active clamp over voltage protection of the output (OUT, cooling tab)
- Current limitation
- Enhanced short circuit protection

Detailed Description

The device is able to switch all kind of resistive, inductive and capacitive loads, limited by maximum clamping energy and maximum current capabilities.

The BTF3050EJ offers dedicated ESD protection on the IN, V_{DD}, ENABLE, STATUS and SRP pin which refers to the GND ground pin, as well as an over voltage clamping of the OUT to Source/GND.

The over voltage protection gets activated during inductive turn off conditions or other over voltage events (like load dump). The power MOSFET is limiting the drain-source voltage, if it rises above the $V_{OUT(CLAMP)}$.

The over temperature protection prevents the device from overheating due to overload and/or bad cooling conditions.

The BTF3050EJ has an auto-restart thermal shutdown function. The device will turn on again, if input is still high, after the measured temperature has dropped below the thermal hysteresis.

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2 Block Diagram

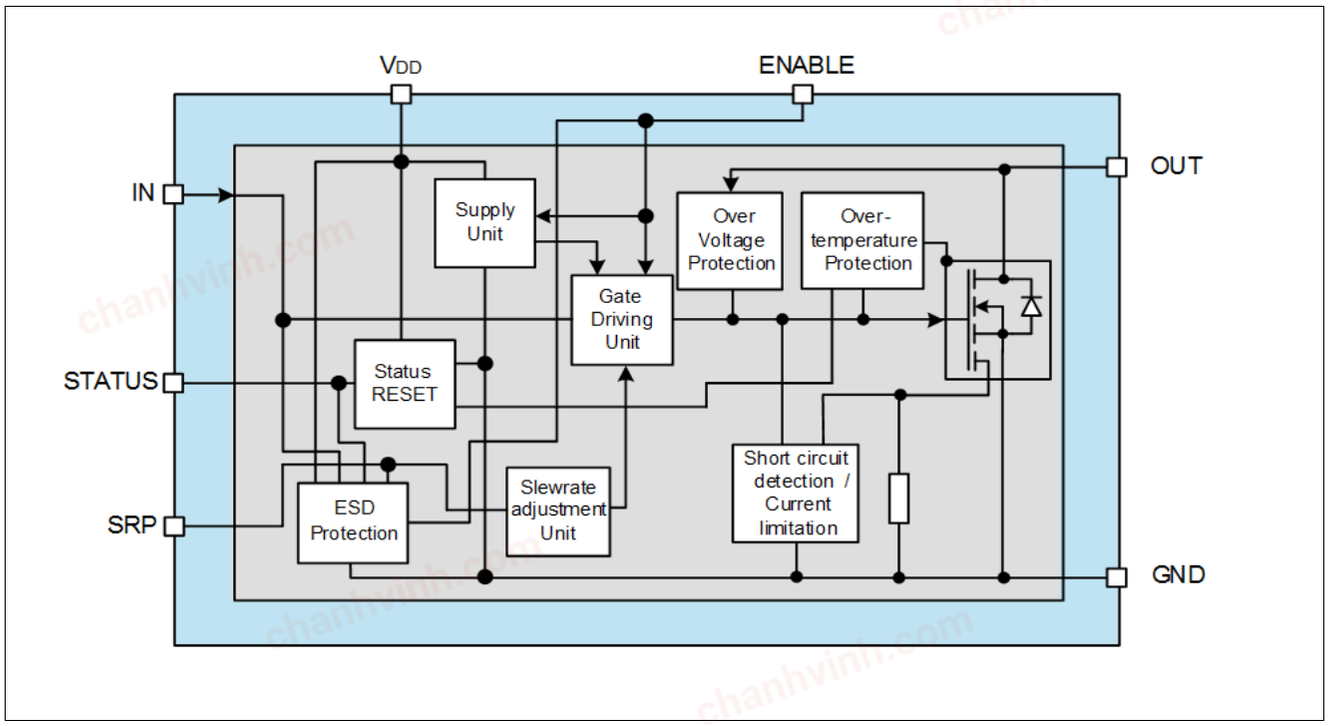


Figure 1 Block Diagram

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3 Pin Assignment

3.1 Pin Configuration

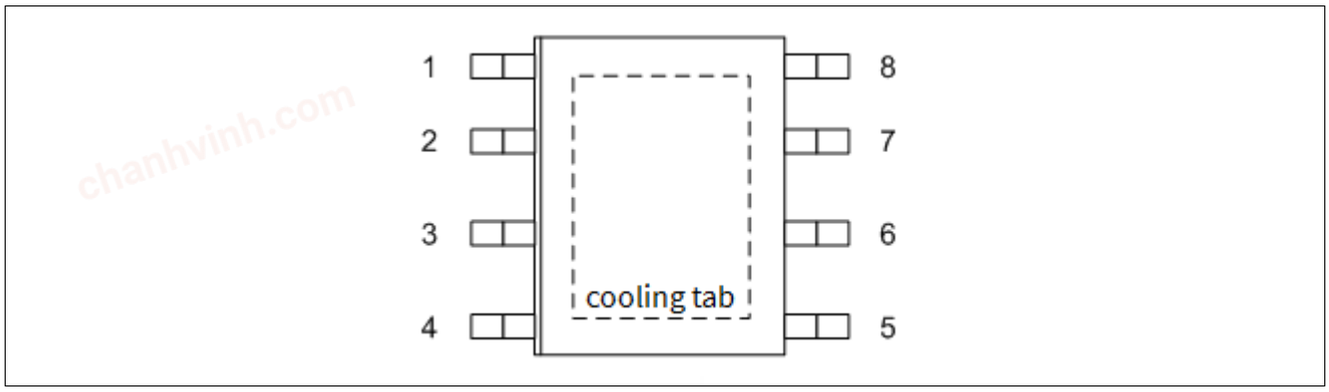


Figure 2 Pin configuration

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1	IN	Input	If IN logic is high, switches ON the Power DMOS If IN logic is low, switches OFF the Power DMOS only if pin ENABLE is logic high
2	V_{DD}	Input	Logic supply voltage, 3V to 5.5V
3	STATUS	Input	Reset of latches by microcontroller pull-up
		Output	If STATUS logic is high, device is under normal operation If STATUS logic is low, device is in over temperature condition
4	SRP	Input	Slewrate control with external resistor
5	ENABLE	Input	If ENABLE logic is high, IN pin is enabled If ENABLE logic is low, IN pin is disabled and leakages are minimum
6,7,8	GND	I/O	SOURCE of power DMOS and Logic, GND pins must be connected together
Cooling tab	OUT	I/O	DRAIN of power DMOS. Connected to Load.

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3.3 Voltage and Current Definition

Figure 3 shows all external terms used in this data sheet, with associated convention for positive values.

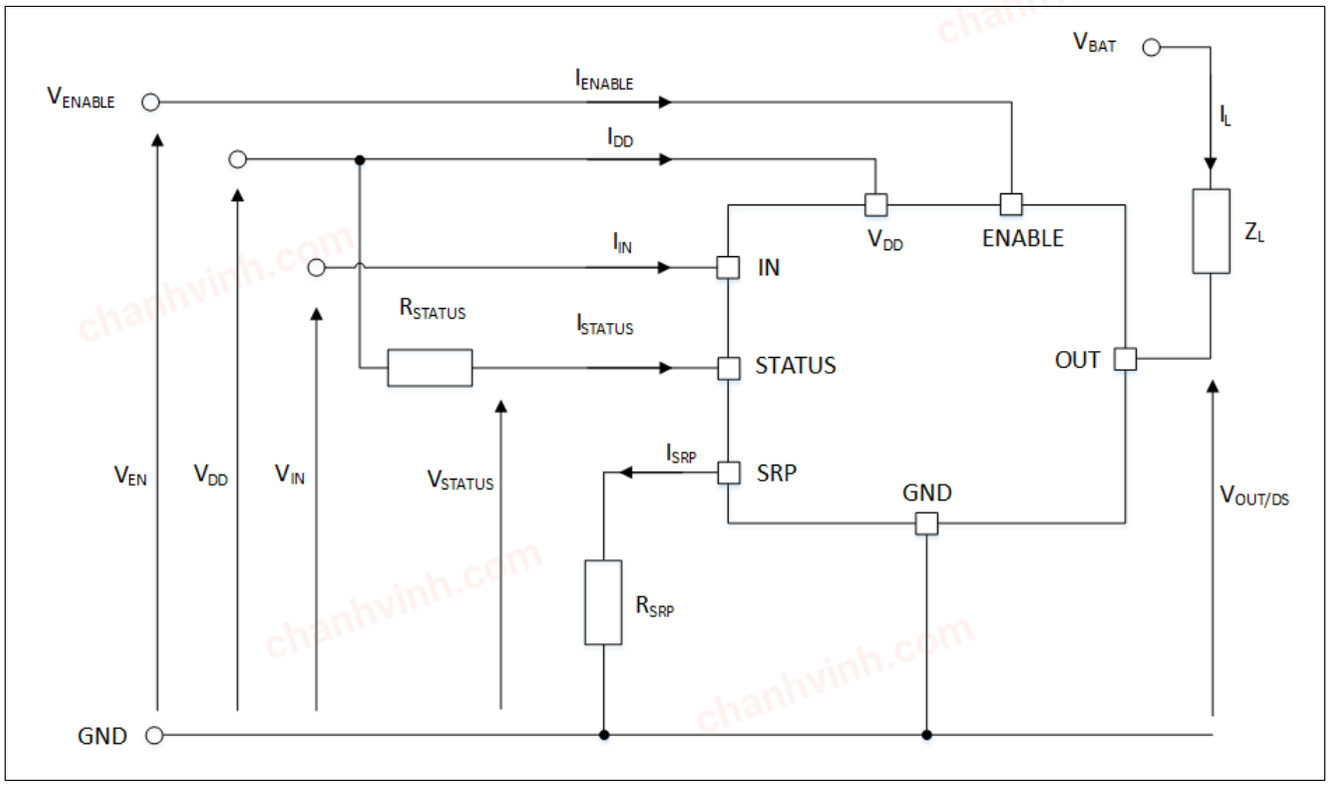


Figure 3 Naming Definition of electrical parameters

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4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1)]

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_{DD}	-0.3	–	5.5	V		P_4.1.1
Output voltage	V_{OUT}	–	–	40	V		P_4.1.2
Battery voltage for short circuit protection	$V_{BAT(SC)}$	–	–	31	V	[1)] l = 0 or 5m R_{SC} = 30 mΩ+ R_{Cable} R_{Cable} = l * 16 mΩ/m L_{SC} = 5 µH + L_{Cable} L_{Cable} = l * 1 µH/m V_{DD}=5V; V_{IN}=5V; V_{ENABLE}=5V	P_4.1.3
Battery voltage for load dump protection ($V_{BAT(LD)}$ = V_A + V_S with V_A = 13.5V)	$V_{BAT(LD)}$	–	–	40	V	[2)] R_i = 2 Ω, R_L = 4.7 Ω, t_d = 400 ms, suppressed pulse	P_4.1.4
Control pins voltages							
Input Voltage	V_{IN}	-0.3	–	5.5	V	–	P_4.1.8
SRP pin Voltage	V_{SRP}	-0.3	–	5.5	V	$V_{SRP} \le V_{DD}$	P_4.1.9
STATUS pin Voltage	V_{STATUS}	-0.3	–	5.5	V		P_4.1.10
ENABLE pin Voltage	V_{ENABLE}	-0.3	–	5.5	V		P_4.1.11
Power Stage							
Load current	$\|I_L\|$	–	–	$I_{L(LIM)}$		T_J < 150°C	P_4.1.12
Power Dissipation	P_{TOT}	–	–	1.60	W	DC operation, T_A = 85°C, T_J < 150°C, I_L = I_{NOM}	P_4.1.47
Energies							
Unclamped single inductive energy single pulse	E_{AS}	–	–	94	mJ	$I_{L(0)}$ = $I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{j(0)}$ = 150°C	P_4.1.16
Unclamped repetitive inductive energy pulse with 10k cycles	$E_{AR(10k)}$	–	–	90	mJ	$I_{L(0)}$ = $I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{j(0)}$ = 85 °C	P_4.1.26

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Table 2 Absolute Maximum Ratings[1)] (cont'd)

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Unclamped repetitive inductive energy pulse with 100k cycles	$E_{AR(100k)}$	–	–	85	mJ	$I_{L(0)} = I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{J(0)}$ = 85 °C	P_4.1.31
Temperatures							
Operating temperature	T_j	-40	–	+150	°C	–	P_4.1.39
Storage temperature	T_{stg}	-55	–	+150	°C	–	
ESD robustness							
ESD robustness (all pins)	V_{ESD}	-2	–	2	kV	HBM[3)]	P_4.1.41
ESD robustness OUT pin vs. GND	V_{ESD}	-4	–	4	kV	HBM[3)]	P_4.1.42
ESD robustness	V_{ESD}	-500	–	500	V	CDM[4)]	P_4.1.43
ESD robustness corner pins	V_{ESD}	-750	–	750	V	CDM [5)]	P_4.1.44

1) Not subject to production test, specified by design.

2) $V_{BAT(LD)}$ is setup without the DUT connected to the generator per ISO7637-1;
R_i is the internal resistance of the load dump test pulse generator;
t_d is the pulse duration time for load dump pulse (pulse 5) according ISO 7637-1, -2.

3) ESD robustness, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)

4) ESD robustness, Charged Device Model "CDM" ESDA STM5.3.1 or JESD22-C101

5) ESD robustness, Charged Device Model "CDM" ESDA STM5.3.1 or JESD22-C101

Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation*

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4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Nominal Operation	$V_{DD(NOR)}$	3.0	5.0	5.5	V		P_4.2.1
Supply current continuous ON operation	$I_{DD(ON)}$	–	1.3	2.5	mA	Supply current continuous ON operation is specified forR_{SRP}=0. It is lower (0.7mA typ) forR_{SRP}=5.8k 1)	P_4.2.4
Standby supply current (ambient)	$I_{DD(OFF)}$	–	1.5	6	µA	T_J = 25°C 1)	P_4.2.8
Maximum standby supply current (hot)	$I_{DD(OFF)_150}$	–	6	14	µA	T_J = 150°C	P_4.2.9
Battery Voltage Range for Nominal Operation	$V_{BAT(NOR)}$	6	13.5	18	V	1)	P_4.2.10
Extended Battery Voltage Range for Operation	$V_{BAT(EXT)}$	0	–	29	V	parameter deviations possible	P_4.2.11
SRP pin resistor for adjustable operation	$R_{SRP(NOR)}$	5	–	70	kΩ	refer to graphic **Figure 16** 1)	P_4.2.12
SRP pin resistor for fast operation	$R_{SRP(EXTF)}$	0	–	1.5	kΩ	1)	P_4.2.13
SRP pin resistor for slow operation	$R_{SRP(EXTS)}$	>160	–	–	kΩ	Pin can be left open 1)	P_4.2.14
DIAGNOSIS							
STATUS Pin voltage operation range	V_{STATUS}	-0.3	–	5.5	V	normal and reset mode 1)	P_4.2.15
STATUS Pin Leakage current	I_{STATUS}	–	1.5	12	µA	$V_{STATUS} \leq 5V$ 1)	P_4.2.17
STATUS Pin voltage drop Fault	$V_{STATUS(FAULT)}$		0.5	0.8	V	$I_{STATUS(FAULT)}$=1mA	P_4.2.18
STATUS Current Reset	$I_{STATUS(RESET)}$	5	–	7	mA		P_4.2.19

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

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4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 T_J = -40°C to +150°CV_{DD} = 3.0 V to 5.5 VV_{BAT} = 6 V to 18 Vall voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	3	–	K/W	1) 2)	P_4.3.3
Junction to Ambient (2s2p)	$R_{thJA(2s2p)}$	–	35	–	K/W	1) 3)	P_4.3.9
Junction to Ambient (1s0p+600mm^2 Cu)	$R_{thJA(1s0p)}$	–	46	–	K/W	1) 4)	P_4.3.14

1) Not subject to production test, specified by design
2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (bottom of package is fixed to ambient temperature).
T_C = 85°C. Device is loaded with 1W power.
3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board;
The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the ex posed pad contacted the first inner copper layer.
T_a = 85°C, Device is loaded with 1W power.
4) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board;
The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm^2 and 70 mm thickness. T_a = 85°C, Device is loaded with 1W power.

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4.3.1 PCB set up

The following PCB setup was implemented to determine the transient thermal impedance. The setup is according to JEDEC standard JESD51-2A and related.

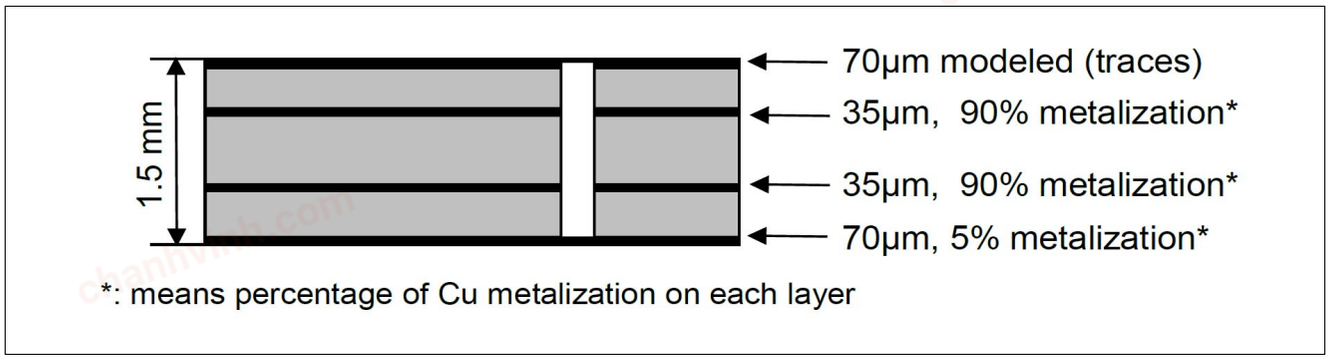


Figure 4 Cross-section JEDEC2s2p

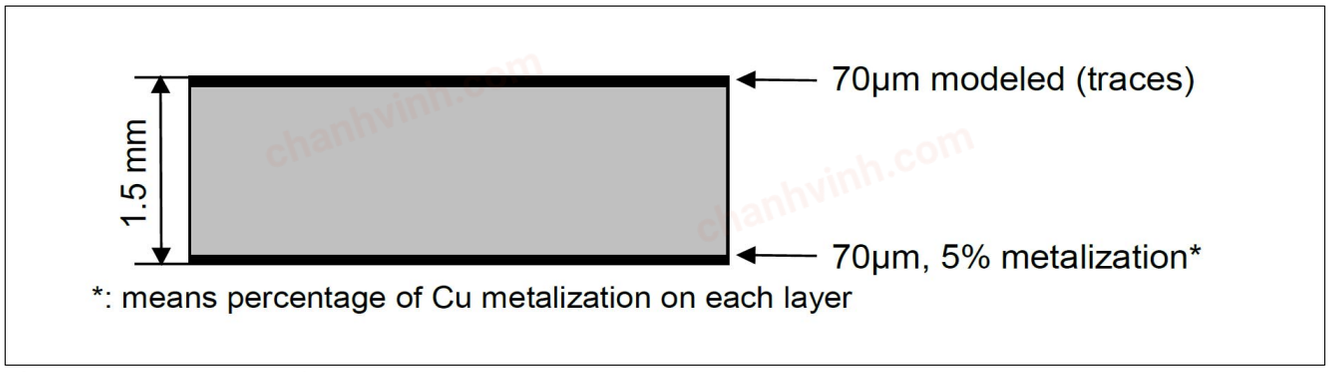


Figure 5 Cross-section JEDEC1s0p

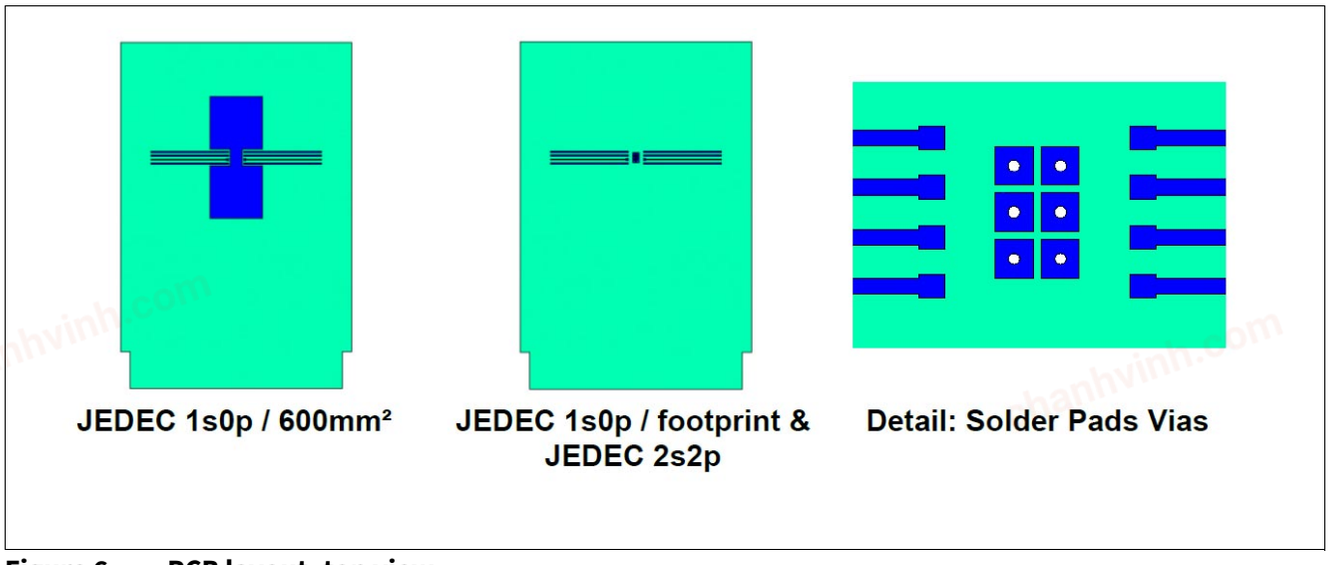


Figure 6 PCB layout, top view

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4.3.2 Transient Thermal Impedance

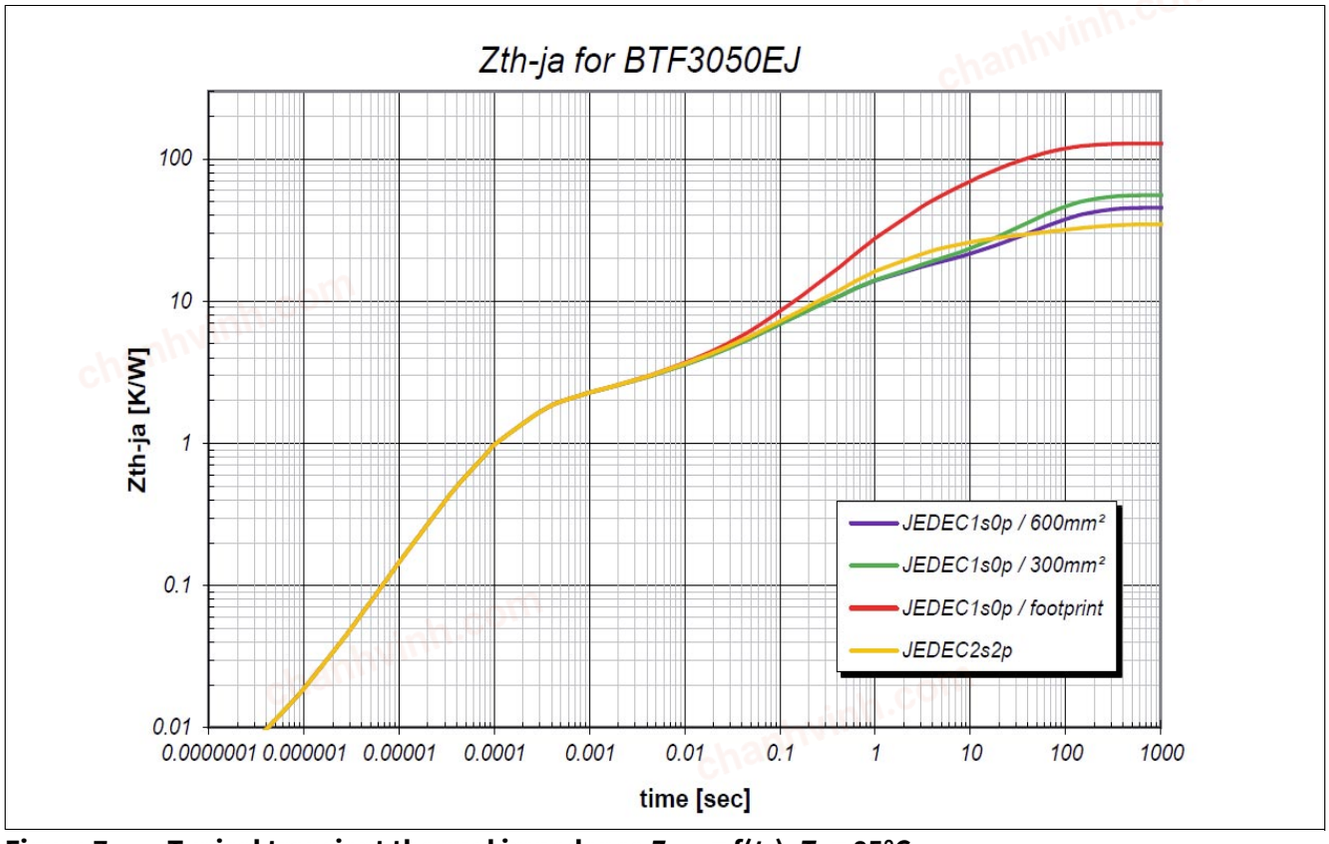


Figure 7 Typical transient thermal impedance $Z_{thJA} = f(t_p)$, $T_a = 85°C$
Value is according to Jedec JESD51-2,-7 at natural convection on FR4 boards; The product (Chip+Package) was simulated with the respective PCB setups, according to the JEDEC standard. Where applicable a thermal via array under the ex posed pad contacted the first inner copper layer. Device is dissipating 1 W power.

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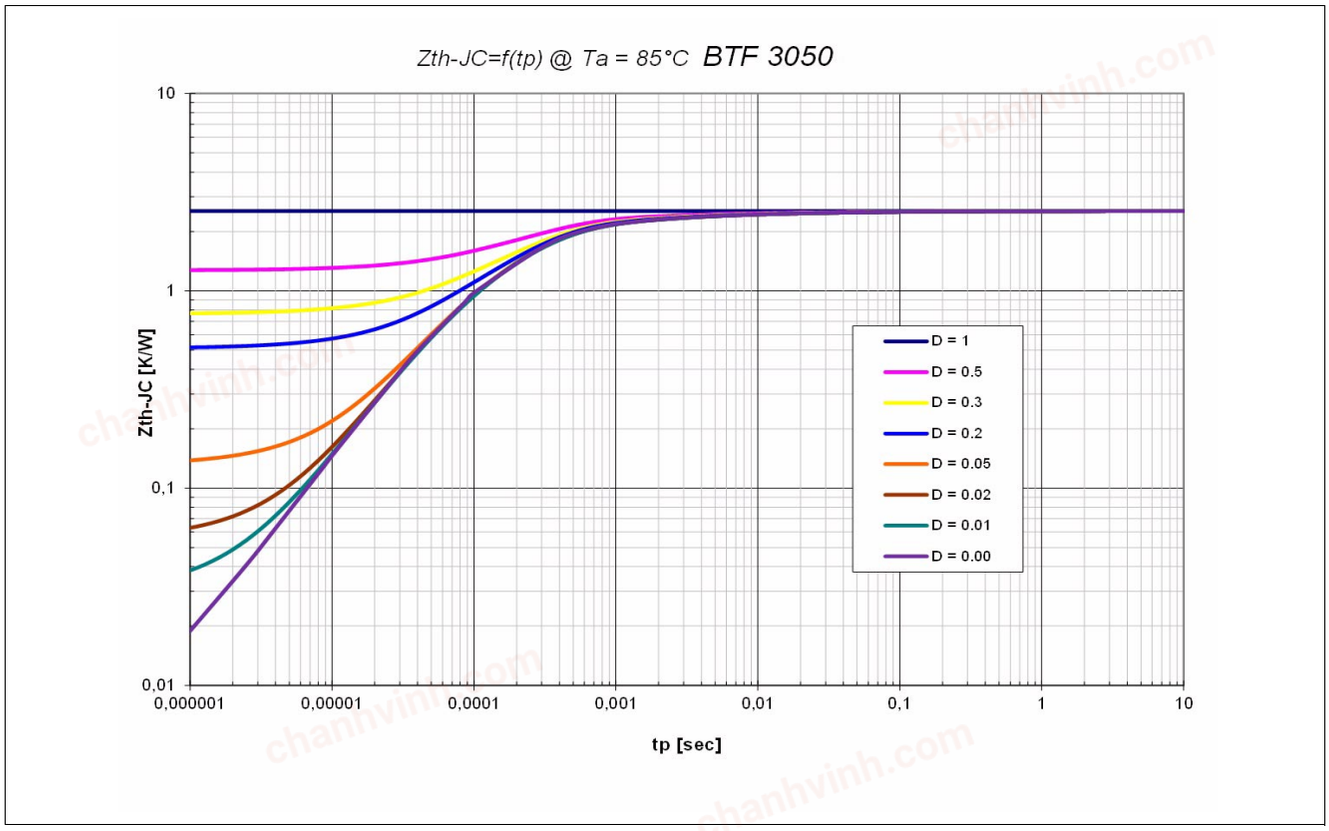


Figure 8 **$Z_{th(JC)}$ vs. duty cycle**

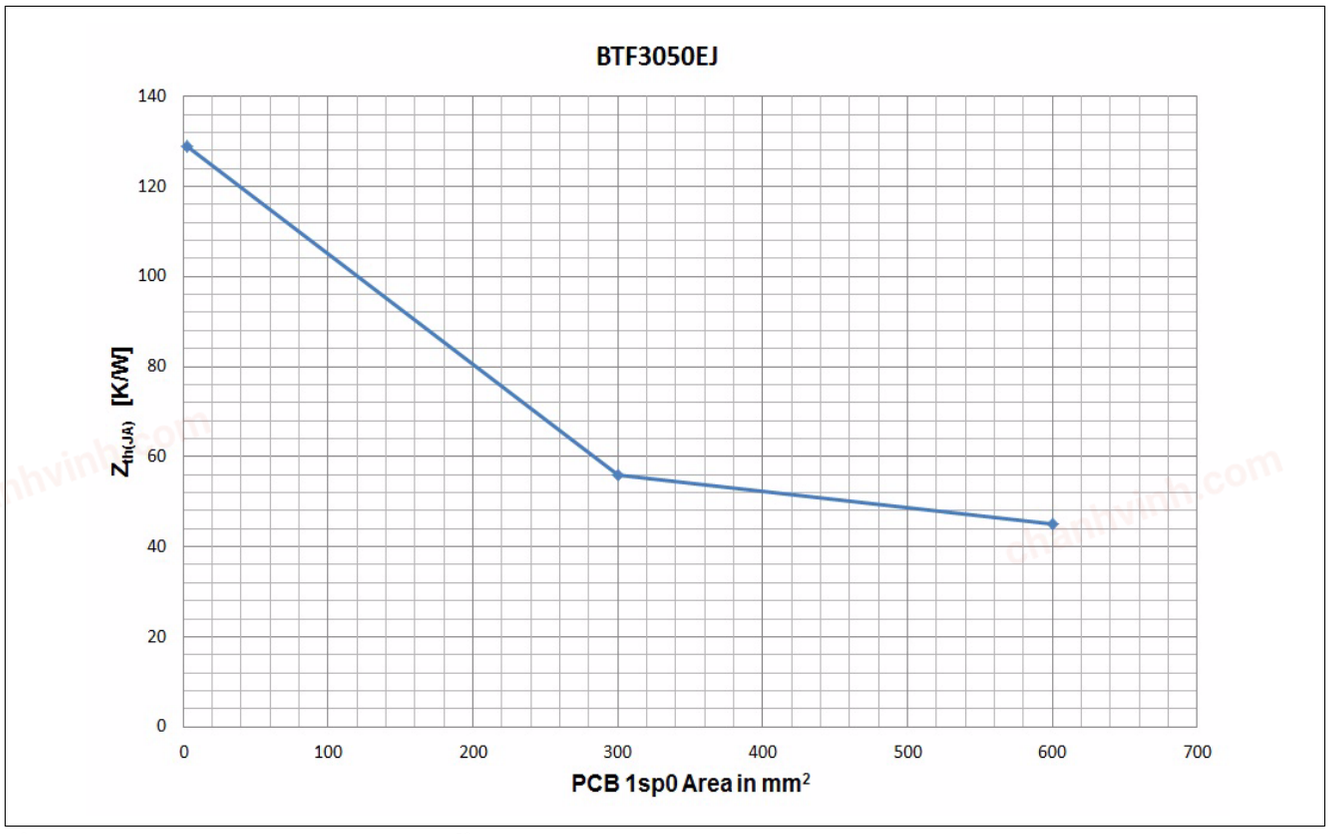


Figure 9 **PCB 1sp0 - R_{thja} vs. cooling areas**

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5 Power Stage

5.1 Output On-state Resistance

The on-state resistance depends on the supply voltage and on the junction temperature T_J. **Figure 10** shows this dependencies in terms of temperature and voltage for the typical on-state resistance $R_{DS(ON)}$. The behavior in reverse polarity is described in chapter**"Inverse Current Capability" on Page 20**.

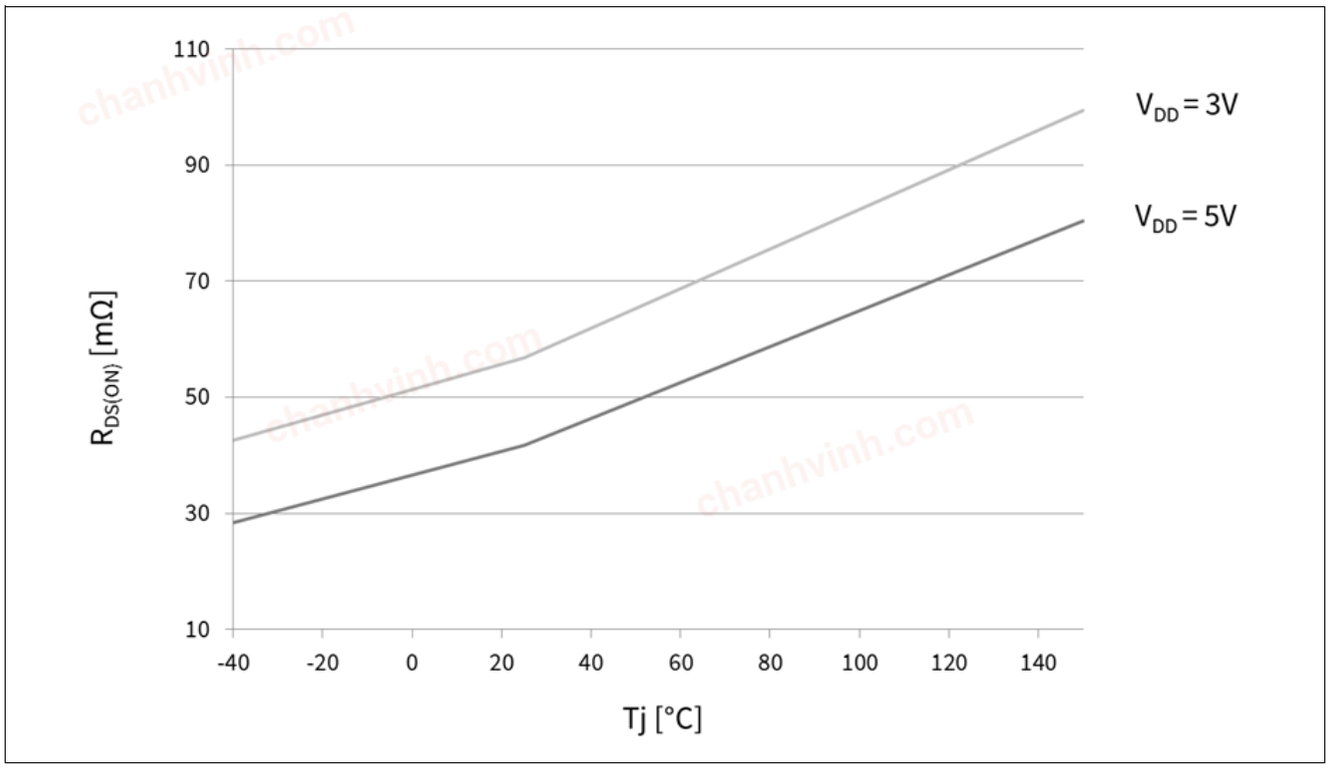


Figure 10 Trend of On-State Resistance $R_{DS(ON)}$ = f(T_J), V_{DD} = 5V or 3V, V_{IN} = high

At V_{IN}= high the power DMOS switches ON with a dedicated slope.

To achieve a reasonable $R_{DS(ON)}$and the specified switching speed a 5V supply is required.

5.2 Functional description of ENABLE pin

The physical digital input ENABLE allows power down mode when IN pin toggling is not needed.

When ENABLE is set to logic low, the DMOS is switched off (regardless of the status of the input IN) and the device will be in Power Down mode. It allows the lowest possible leakage current through OUT and V_{DD} pins.

The STATUS pin will not be available during this stage and the device is reset.

When the ENABLE pin is switched to logic high, the device logic and DMOS are available with full functionalities, after a dead time defined as masking time - $t_{ENABLE(MASKING)}$"(**Table "tENABLE(MASKING)" on Page 36**), .

Then, depending on the status of the IN pin the DMOS is switched on or off, see **Chapter 5.3** and **Figure 11 "VOUT in relation to VENABLE and VIN" on Page 16**. The STATUS pin will also be available. For the electrical characteristics see **Table 8**, **Page 35**.

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5.3 Functional description of IN pin

The IN pin is a digital input. As described in **Chapter 5.2** using the physical IN pin requires the ENABLE pin to be set to logic high.

If IN is set to logic low, the DMOS is switched off.

If IN is set to logic high, the DMOS is switched on.

In addition, an high frequency PWM signal source can be connected. At a frequency of 20kHz the duty cycle can be selected between 10% and 90%. .

5.4 Resistive Load Output Timing

Figure 12 shows the typical timing when switching a resistive load.

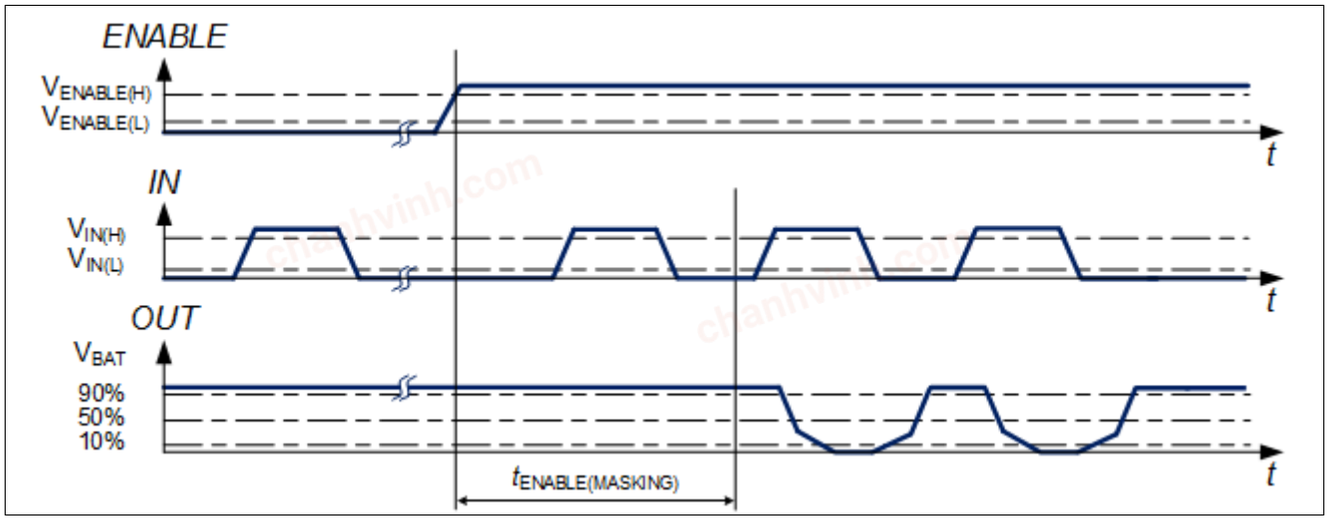


Figure 11 V_{OUT} in relation to V_{ENABLE} and V_{IN}

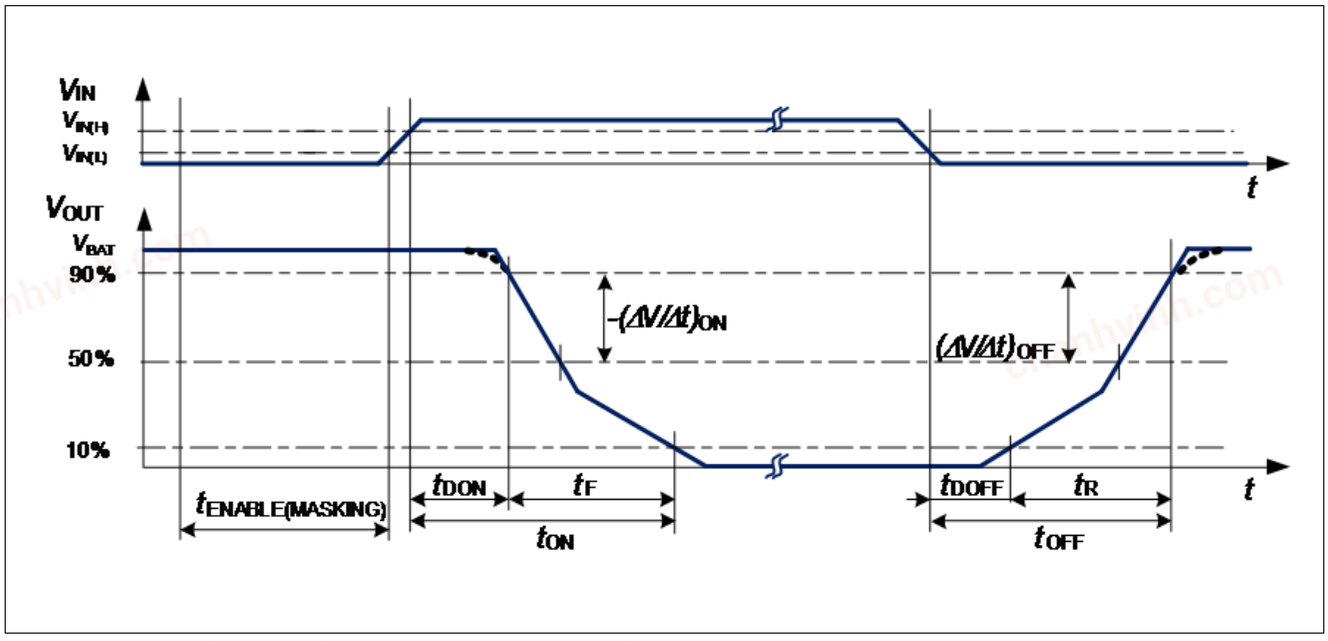


Figure 12 Definition of Power Output Timing for Resistive Load

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5.5 Inductive Load

5.5.1 Output Clamping

When switching off inductive loads with low side switches, the drain-source voltage V_{OUT} rises above battery potential, because the inductance intends to continue driving the current. To prevent unwanted high voltages the device has a voltage clamping mechanism to keep the voltage at $V_{OUT(CLAMP)}$. During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See **Figure 13** and **Figure 14** for more details.

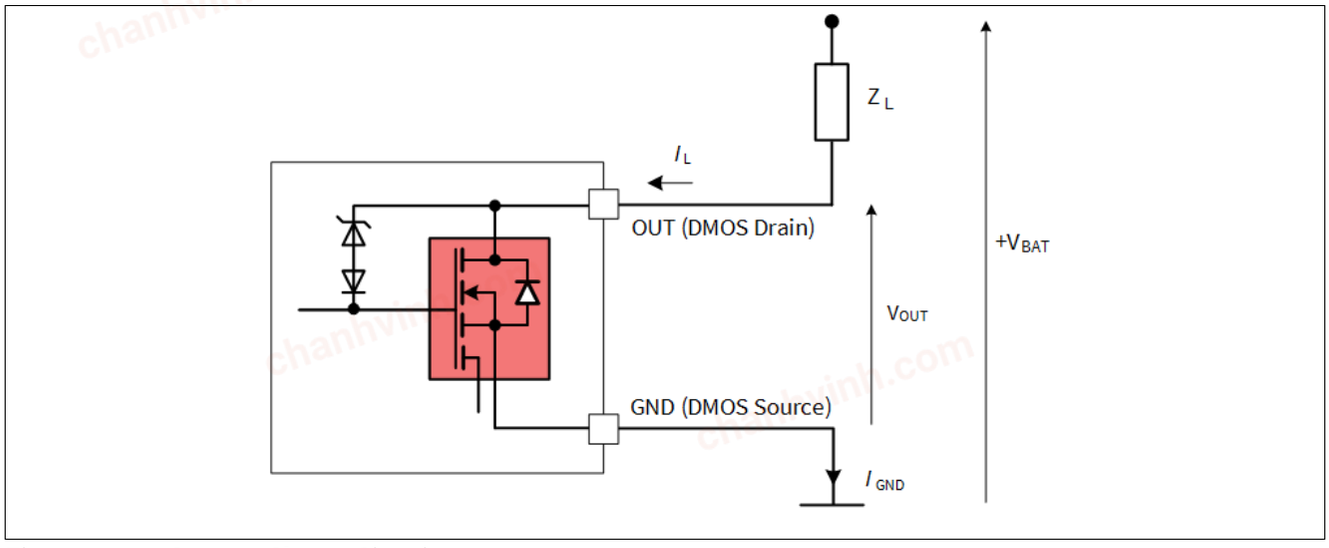


Figure 13 Output Clamp Circuitry

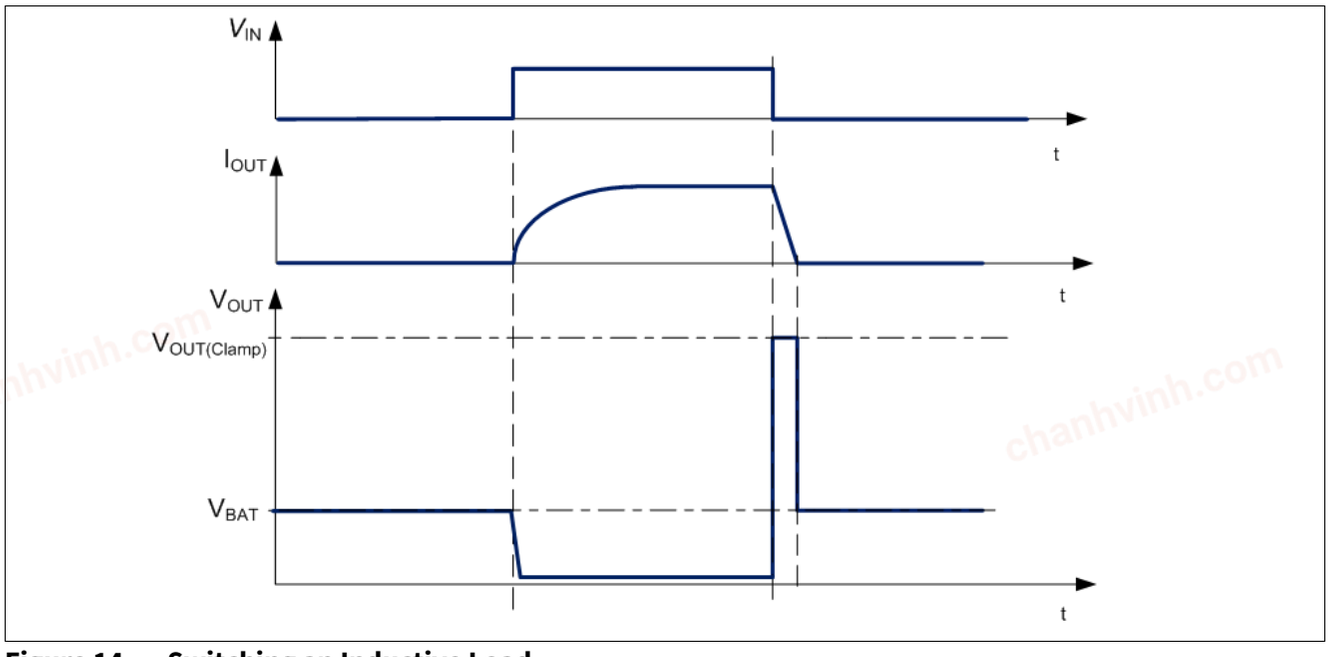


Figure 14 Switching an Inductive Load

Note: Repetitive switching of inductive load by VDD instead of using the input is a not recommended operation and may affect the device reliability and reduce the lifetime.

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5.5.2 Maximum Load Inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTF3050EJ.
This energy can be calculated by the following equation:

$$E = V_{OUT(CLAMP)} \times \left[\frac{V_{BAT} - V_{OUT(CLAMP)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_{BAT} - V_{OUT(CLAMP)}}\right) + I_L \right] \times \frac{L}{R_L} \quad (5.1)$$

Following equation simplifies under assumption of $R_L = 0$

$$E = \frac{1}{2} L I_L^2 \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CLAMP)}}\right) \quad (5.2)$$

The figure below shows the inductance / current combination the BTF3050EJ can handle.
For maximum single avalanche energy refer to EAS value in **Table 2**.

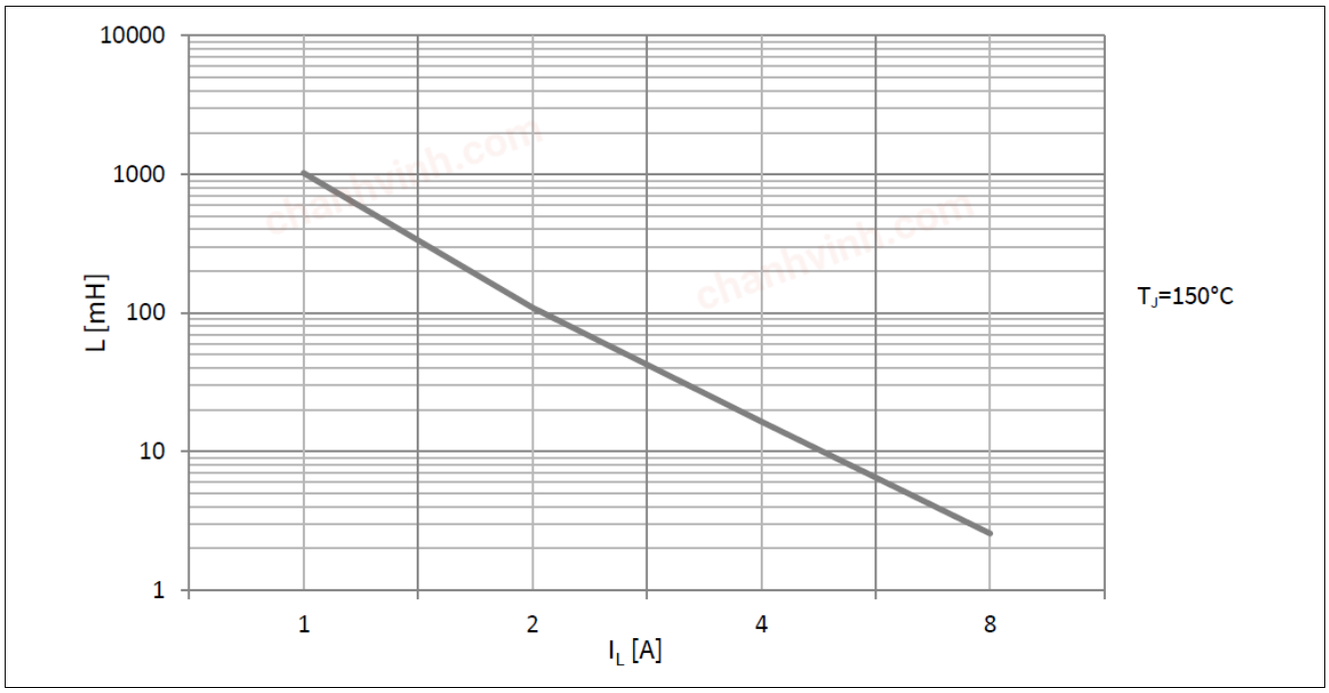


Figure 15 Maximum load inductance for single pulse
$L = f(I_L)$, $T_{J,start} = 150°C$, $V_{BAT} = 13.5V$

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5.6 Adjustable Switching Speed / Slew Rate

In order to optimize electromagnetic emission, the switching speed of the MOSFET can be adjusted by connecting an external resistor between SRP pin and GND. This allows for balancing between electromagnetic emissions and power dissipation. Shorting the SRP pin to GND represents the fastest switching speed. Open pin represents the slowest switching speed.

The accuracy of the switching speed adjustment is dependent on the precision of the external resistor used and on the parasitic capacitance on the SRP pin. It is recommended to use accurate resistors and place them as close as possible to the SRP pin with the shortest way possible to the GND of the device.

Figure 16 shows the simplified relation between the resistor value and the switching times

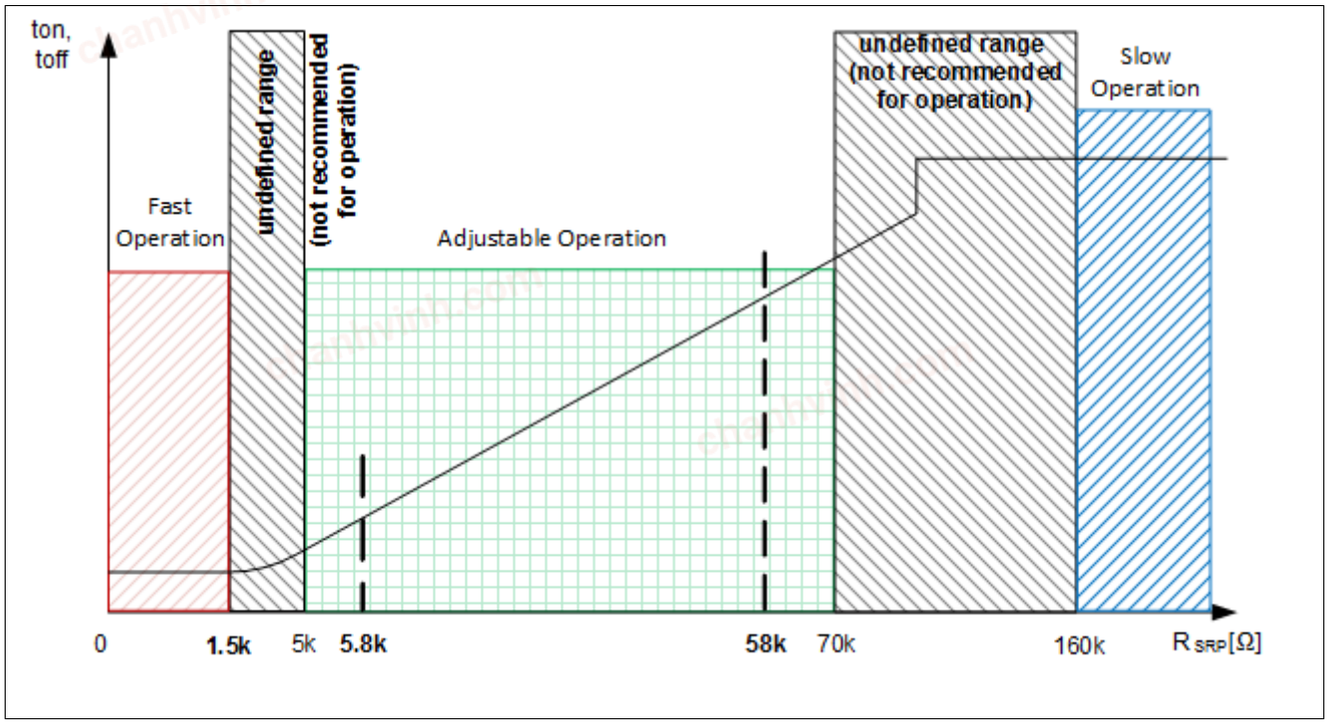


Figure 16 Typical simplified relation between switching time and R_{SRP} resistor values used on SRP pin

It is not recommended to change the slew rate resistance during switching (supplied device, $V_{DD} > V_{DD(UV_ON)}$. Undefined switching times can result.

If the SRP pin is externally pulled up above the normal SRP pin voltage V_{SRP} (e.g. to V_{DD}) the slowest slew rate settings apply.

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5.7 Inverse Current Capability

An inverse situation means the OUT pin is pulled below GND potential via the load and current flows in the Power DMOS intrinsic body diode.

In certain application cases (for example in use in a bridge or half-bridge configuration) the body diode is used for freewheeling of an inductive load. In this case the device is still supplied but the inverse current is flowing from GND to OUT(drain).

In inverse operation the body diode is dissipating power, which is defined by the driven current times the voltage drop on the body diode $-V_{DS}$.

In order to dissipate less power in inverse situation, a dedicated circuit has been implemented.

The BTF3050EJ includes an inverse current detection circuit that allows to turn ON the Power DMOS while inverse current is present (active freewheeling) and disables all protections, e.g. current limitation, temperature shutdown or over voltage clamping. To do active freewheeling, both ENABLE and IN pin must be set to logic high.

The timings are set to slow mode (open SRP pin), regardless of the SRP pin configuration.

During inverse current condition the quiescent current of the circuit is the same as in normal operation if ENABLE=high (see **Chapter 9.4**). If ENABLE=low and the device is still supplied, the standby supply current in inverse increases compared to standby supply current in normal output current condition (see **Table 8 “Electrical Characteristics: Supply and Input” on Page 35**).

The maximum admissible inverse current is $-I_{L(NOM)}$.

5.8 Characteristics

See **Table 9.1 “Power Stage” on Page 30** for electrical characteristics.

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6 Protection Functions

The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operation. Protection functions are not to be used for continuous or repetitive operation. Over temperature is indicated by a low active signal on the STATUS pin.

6.1 Over Voltage Clamping on OUT

The BTF3050EJ is equipped with a voltage clamp circuitry that keeps the drain-source voltage V_{DS} at a certain level $V_{OUT(CLAMP)}$. The over voltage clamping is overruling the other protection functions. Power dissipation has to be limited not to exceed the maximum allowed junction temperature.

This function is also used in terms of inductive clamping. See also **“Output Clamping” on Page 17** for more details.

6.2 Over Temperature Protection with Latched Fault Signal

The device is protected against over temperature due to overload and/or bad cooling conditions by an integrated temperature sensor. The over temperature protection is available if the device is active, i.e. IN=high and ENABLE=high.

The device incorporates an absolute ($T_{J(SD)}$) and a dynamic temperature limitation ($\Delta T_{J(SW)}$). Triggering one of them will cause the output to switch off. The dynamic temperature limitation principle is developed in a separated Application Note for HITFET+.

The switch off will be done with the fastest possible slew rate. The BTF3050EJ has a thermal-restart function. If IN pin is still high the device will turn on again after the junction temperature has dropped below the thermal hysteresis (ΔT_{J_HYS}).

In case of detected overtemperature the fault signal will be set and the STATUS pin will be internally pulled down to $V_{STATUS(FAULT)}$.

This V_{STATUS} is independent from the IN signal, providing a stable fault signal (Logic “low”) to be read out by a micro controller.

The latched fault signal needs to be reset by a pull-up signal ($V_{STATUS} \geq V_{STATUS(RESET)}$) at the STATUS pin for a minimum duration of t_{RESET}, provided that the junction temperature has decreased at least from the thermal hysteresis in the meantime.

The latched fault signal can also be reset by setting ENABLE=low. See **Chapter 6.4** for an overview of reset conditions.

See **“Diagnostics” on Page 26** for details on the feedback and reset function.

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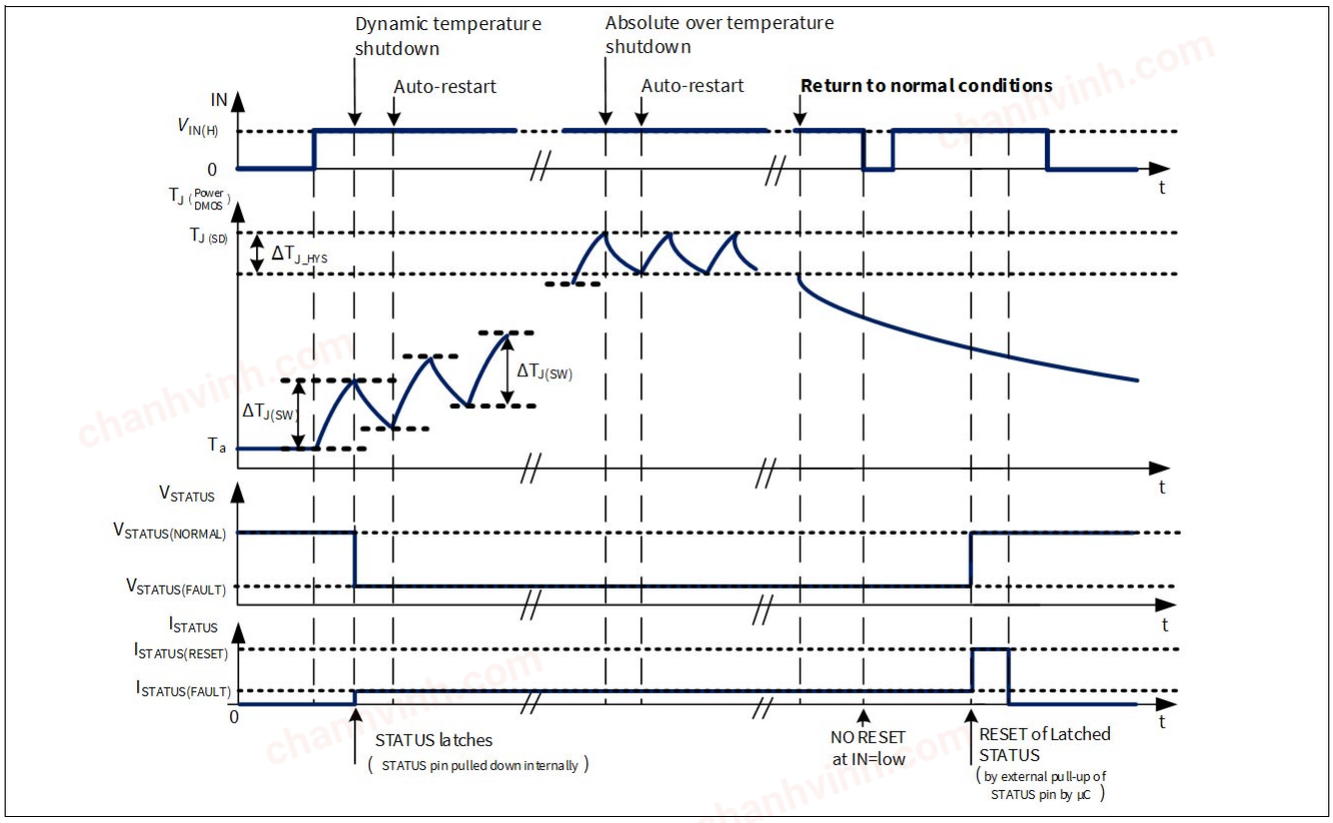


Figure 17 Thermal protective switch OFF scenario for case of overload or short circuit

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

6.3 Overcurrent Limitation / Short Circuit Behavior

BTF3050EJ provides a smart overcurrent limitation intended to protect against short circuit conditions while allowing also load inrush currents higher than the current limitation level. It has a current limitation level $I_{L(LIM)}$ which is triggered by a higher trigger level $I_{L(LIM)TRIGGER}$.

If the load current I_L reaches the current limitation trigger level $I_{L(LIM)TRIGGER}$, the internal current limitation will be activated and the device limits the current to a lower value $I_{L(LIM)}$.

The $I_{L(LIM)TRIGGER}$ function has a latch behaviour, it happens once and is disabled until it is reset.

Then, BTF3050EJ behaves as a normal auto-restart, current limiting device: It keeps heating up at $I_{L(LIM)}$ until the thermal shutdown temperature $T_{J(SD)}$ is reached, then it turns off.

Due to autorestart feature, the MOSFET turns on again after it drops in temperature below thermal hysteresis (ΔT_{J_HYS}). If fault situation is still present, the current will be limited to $I_{L(LIM)}$ as the trigger feature is now disabled. The time to over temperature switch off strongly depends on the cooling conditions.

To reset the $I_{L(LIM)TRIGGER}$ level feature, two conditions are necessary. The STATUS pin needs a pull-up signal ($V_{STATUS} \geq V_{STATUS(RESET)}$) for a minimum duration of t_{RESET}, and the IN pin must be in low state ($V_{IN} \leq V_{IN(L)}$) at the same time.

The $I_{L(LIM)TRIGGER}$ level feature can also be reset by setting ENABLE=low. See **Chapter 6.4** for an overview of reset conditions.

Figure 18 “Short circuit protection via current limitation and thermal switch off , with latched fault signal on STATUS” on Page 23 shows this behavior.

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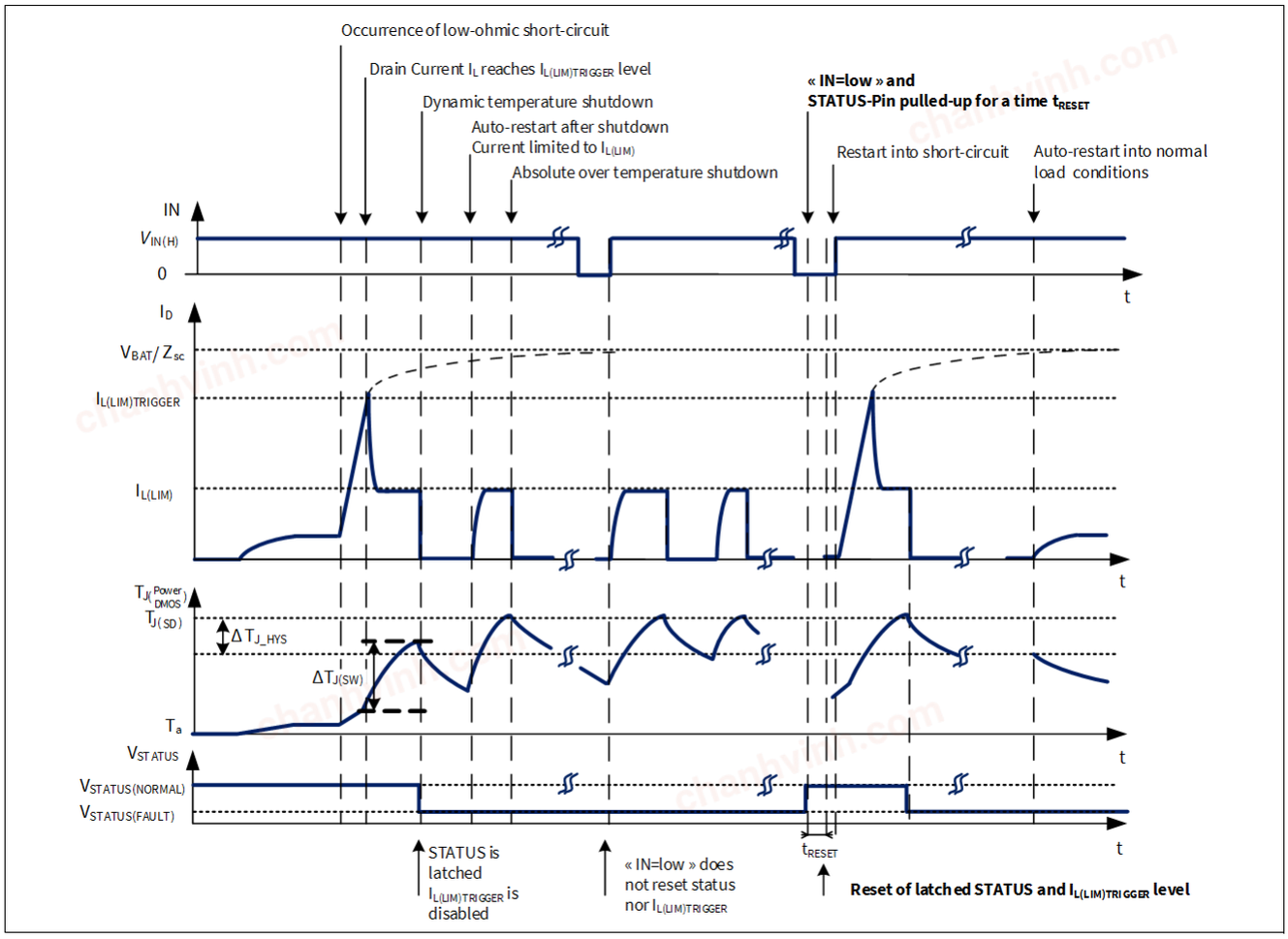


Figure 18 Short circuit protection via current limitation and thermal switch off , with latched fault signal on STATUS

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

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Behavior with overload current below current limitation trigger level

The lower current limitation level $I_{L(LIM)}$ is also triggered by any thermal shutdown. It can be the case when a still current, below the overcurrent limitation trigger level ($I_L < I_{L(LIM)TRIGGER}$), provokes an over temperature shutdown. Any over temperature shutdown disables the $I_{L(LIM)TRIGGER}$ function.

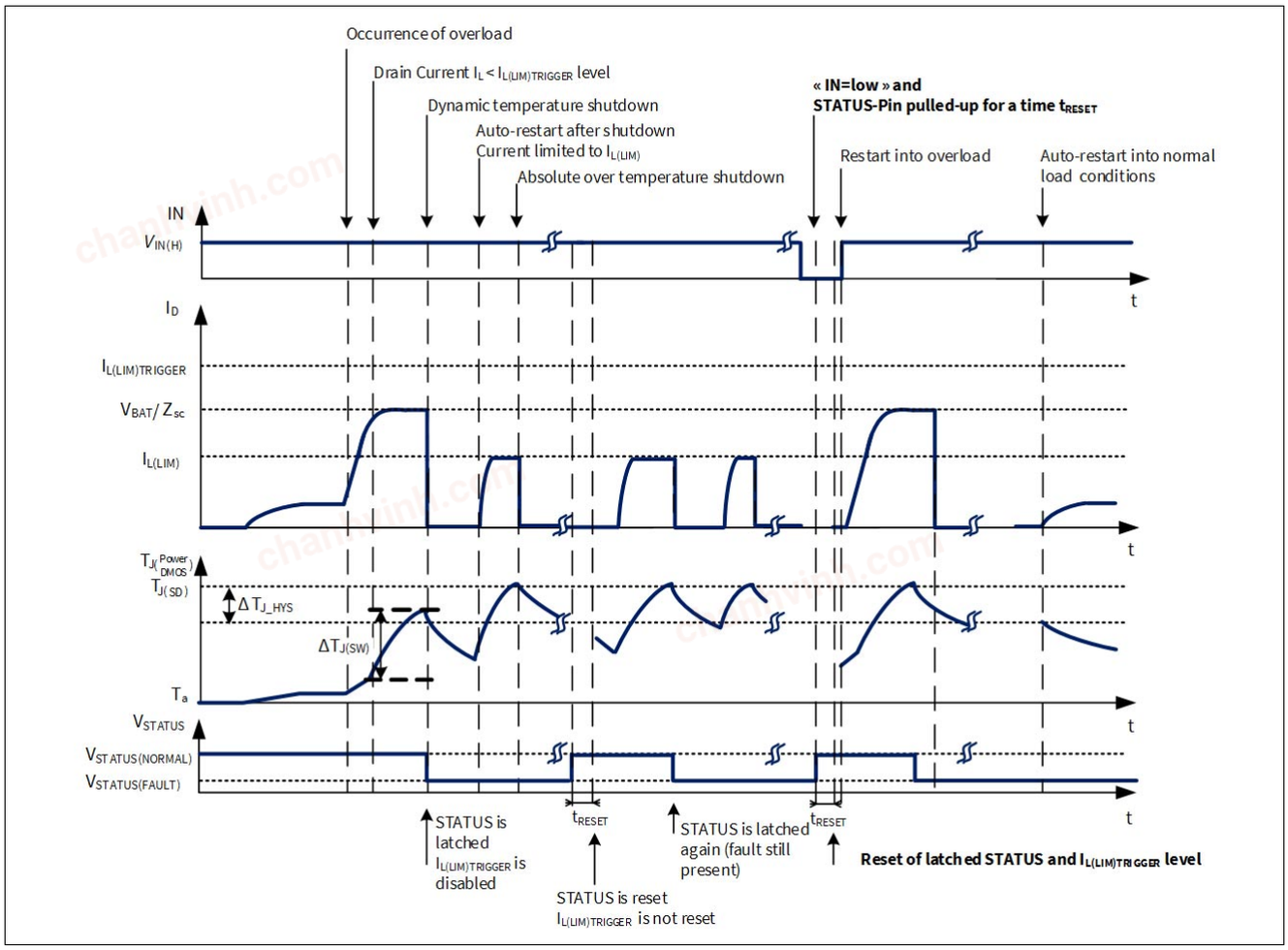


Figure 19 Example of overload behavior with thermal shutdown

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

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6.4 Reset conditions

The following table gives the reset conditions of the latched STATUS signal and the $I_{L(LIM)TRIGGER}$ function. Additionally, both functions are reset when ENABLE=low, regardless of STATUS and IN pin states.

	STATUS pin for a minimum time t_{RESET}	IN pin
Reset of Latched STATUS[1)]	Pull-up to V_{DD}	x[2)]
Reset of $I_{(LIM)TRIGGER}$ level[3)]	Pull-up to V_{DD}	low

[1)] Does not reset $I_{(LIM)TRIGGER}$ level if IN pin is high

[2)] Regardless of IN pin state, latched status is reset by STATUS pull-up for a minimum time t_{RESET}

[3)] Also reset latched STATUS

Figure 20 Reset conditions of latched STATUS signal and $I_{L(LIM)TRIGGER}$ function.

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7 Diagnostics

The BTF3050EJ provides a latched digital fault feedback signal on the STATUS pin triggered by an over temperature or dynamic temperature shutdown.

7.1 Functional Description of the STATUS pin

The BTF3xxxEJ series provides digital status information via the STATUS pin to give an alarm feedback to a possible connected micro controller. See **Figure 17 “Thermal protective switch OFF scenario for case of overload or short circuit” on Page 22**.

Normal operation mode

In normal operation (no fault is detected) the STATUS pin is logic “high”. It is pulled up via an external Resistor with a recommended value of 4.7kΩ. Internally it is connected to an open drain MOSFET via an internal Resistor.

Fault operation

In case of a temperature shutdown the internal MOSFET of the BTF3xxxEJ series pulls the STATUS pin down to approx 0.5V, which a connected microcontroller would accept as logic “low” level signal for a 4.7kΩ pull-up resistor. This mode stays active independent from the input pin state or internal auto-restarts until it is reset.

Reset Latch (external pull up)

To reset the latched STATUS signal, the STATUS pin has to be pulled-up to V_{DD}, for a minimum time of t_{RESET}. The IN pin state does not matter to reset the latched STATUS signal. See **Chapter 11** for an example of basic circuitry to use this digital feedback function.

Reset $I_{L(LIM)TRIGGER}$

See **Chapter 6.3** for detailed explanation on the function and **Chapter 6.4** for a quick overview of reset mechanism.

7.2 Characteristics

See **Table 9.3 “Diagnostics” on Page 34** for electrical characteristics.

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8 Supply and Input Stage

8.1 Supply Circuit

The supply pin V_{DD} is protected against ESD pulses as shown in **Figure 21**.

The device supply is not internally regulated but directly taken from a external supply. Therefore a reverse polarity protected and buffered (3.0V..5.5V) voltage supply is required. To achieve a reasonable $R_{DS(ON)}$ and the specified switching speed a 5V supply is required.

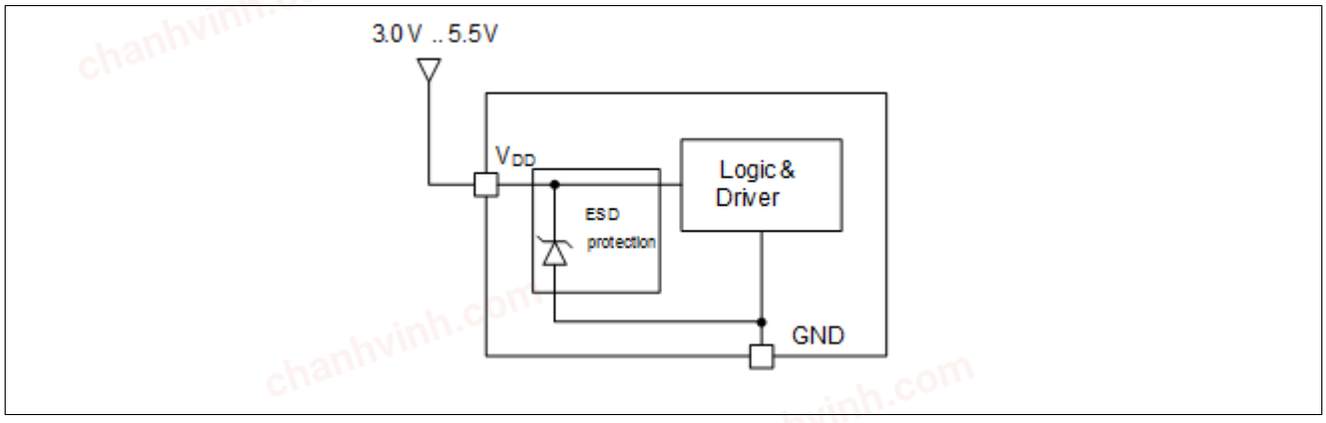


Figure 21 Supply Circuit

8.2 Undervoltage Shutdown

In order to ensure a stable and defined device behavior under all allowed conditions the supply voltage V_{DD} is monitored.

If the supply voltage V_{DD} drops below the switch-off threshold $V_{DD(TH)}$, the power DMOS switches off. In this case ENABLE pin is pulled to low state and both latched STATUS and $I_{L(LIM)TRIGGER}$ level are reset (See **Chapter 6.4**, Reset conditions). All device functions are only specified for supply voltages above the supply voltage threshold $V_{DD(TH)MAX}$. There is no fault feedback ensured for $V_{DD} < V_{DD(TH)}$.

8.3 Input/Enable Circuit

Figure 22 shows the IN pin circuit of the BTF3050EJ. Due to an internal pull-down it is ensured that the device switches off in case of open IN pin. A Zener structure protects the input circuit against ESD pulses.

This structure is also valid for ENABLE pin.

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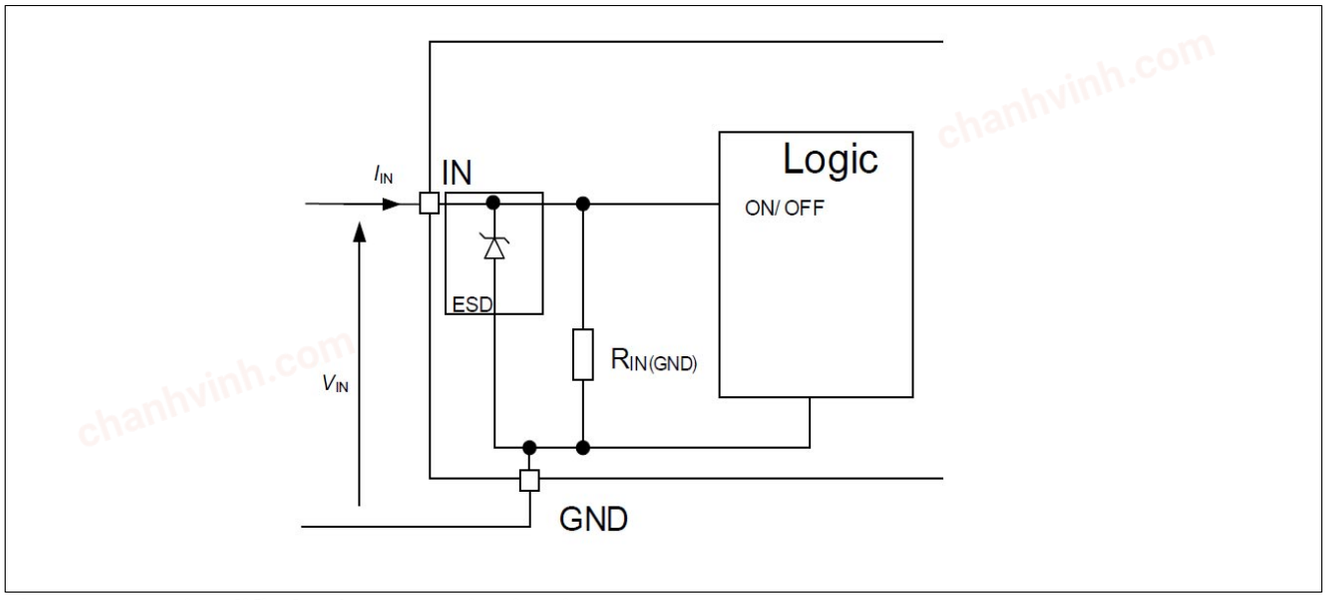


Figure 22 Simplified IN/ENABLE pin circuitry

8.4 Functional Description of the SRP Pin

The BTF3050EJ provides the possibility to adjust slewrate with an external resistor connected to the Slew-Rate-Preset pin (SRP). It defines the strength of the gate driver stage used to switch the power DMOS. The greater the resistor the lesser the current driven by the slew rate logic block to the gate driver block, which will result in a slower turn-on and turn-off. For details on this function please refer to **“Adjustable Switching Speed / Slew Rate” on Page 19**.

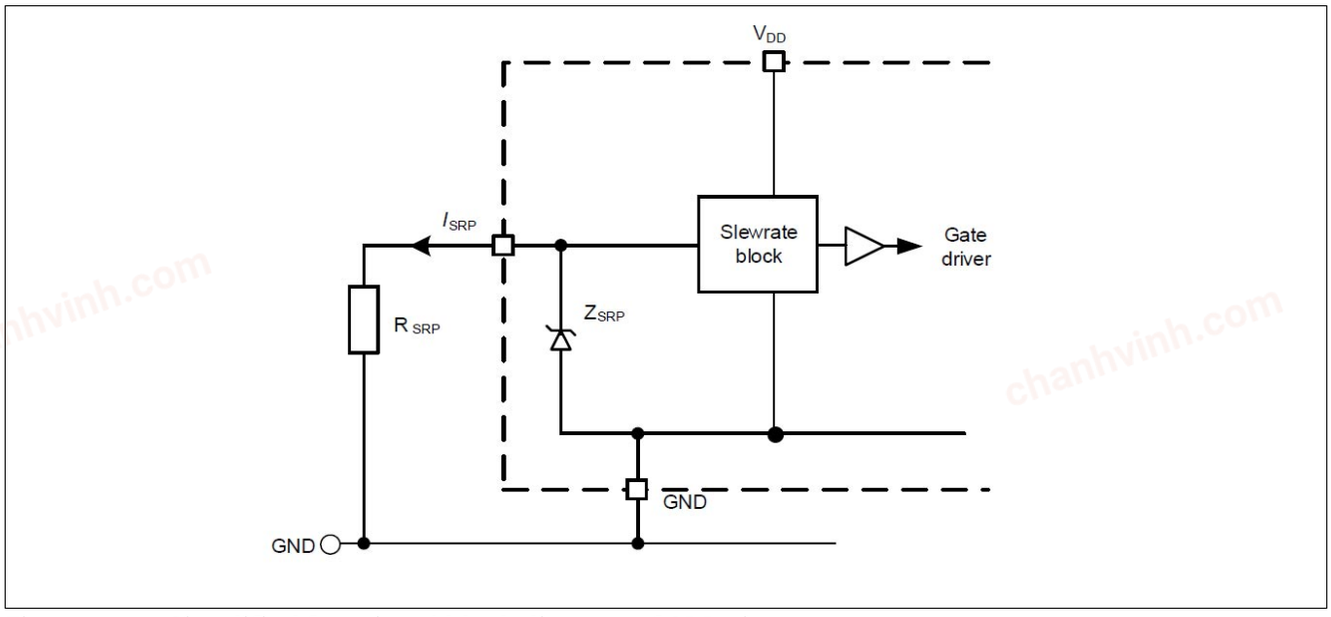


Figure 23 Simplified functional block diagram of SRP pin

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8.5 Characteristics

Please see **Table "INPUT" on Page 36**, **Table "ENABLE" on Page 36** for INPUT and ENABLE electrical characteristics.

The timings **Table** shows slew rate for specific resistor values, for the SRP pin electrical characteristics please see **Table "SRP" on Page 36**.

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9 Electrical Characteristics

Note: Characteristics show the deviation of parameter at given input voltage and junction temperature. Typical values show the typical parameters expected from manufacturing and in typical application condition.
All voltages and currents naming and polarity in accordance to
Figure 3 "Naming Definition of electrical parameters" on Page 7

9.1 Power Stage

See Chapter **"Power Stage" on Page 15** for parameters description and further details.

Table 5 Electrical Characteristics: Power Stage

T_J = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Stage - Static Characteristics							
On-State resistance	$R_{DS(ON)}$	–	45	–	mΩ	$I_L = I_{L(NOM)}$; V_{DD} = 5V; T_J = 25°C	P_9.1.3
On-State resistance	$R_{DS(ON)}$	–	87	100	mΩ	$I_L = I_{L(NOM)}$; V_{DD} = 5V; T_J = 150°C	P_9.1.8
Nominal load current	$I_{L(NOM)}$	–	4	–	A	[1] T_J < 150°C; V_{DD} = 5 V;	P_9.1.33
OFF state load current, Output leakage current	$I_{L(OFF)25}$	–	–	2	µA	[2] V_{BAT} = 13.5 V; V_{IN} = 0 V; V_{DD} = 5 V; $T_J \leq$ 85°C	P_9.1.38
OFF state load current, Output leakage current	$I_{L(OFF)150}$	–	1.2	4	µA	V_{BAT} = 18 V; V_{IN} = 0 V; V_{DD} = 5 V; T_J = 150°C	P_9.1.43
Reverse Diode							
Reverse diode forward voltage	$-V_{DS}$	–	0.8	1.5	V	$I_D = -I_{L(NOM)}$; V_{IN} = 0 V	P_9.1.50
Power Stage - Dynamic characteristics - switching time adjustment V_{BAT} = 13.5V, V_{DD} = 5 V; resistive load: R_L = 4.7Ω; $C_{SRP-GND}$ < 100 pF; see also Figure 12 "Definition of Power Output Timing for Resistive Load" on Page 16							
Turn-on time	$t_{ON(0)}$	0.45	1.35	2.8	µs	R_{SRP} = 0Ω [3]	P_9.1.51
Turn-off time	$t_{OFF(0)}$	0.8	2	4	µs	R_{SRP} = 0Ω [4]	P_9.1.55

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Table 5 Electrical Characteristics: Power Stage (cont'd)

T_J = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Turn-on delay time	$t_{DON(0)}$	0.15	0.35	0.8	µs	R_{SRP} = 0Ω	P_9.1.59
Turn-off delay time	$t_{DOFF(0)}$	0.5	1	2	µs	R_{SRP} = 0Ω	P_9.1.63
Turn-on output fall time	$t_{F(0)}$	0.3	1	2	µs	R_{SRP} = 0Ω	P_9.1.67
Turn-off output rise time	$t_{R(0)}$	0.3	1	2	µs	R_{SRP} = 0Ω	P_9.1.71
Turn-on Slew rate [5]	$-(DV/Dt)_{ON(0)}$	15	27	45	V/µs	R_{SRP} = 0Ω [5]	P_9.1.75
Turn-off Slew rate	$(DV/Dt)_{OFF(0)}$	15	27	45	V/µs	R_{SRP} = 0Ω [5]	P_9.1.79
Turn-on time	$t_{ON(5k8)}$	1.3	2.7	4.5	µs	R_{SRP} = 5.8kΩ [3]	P_9.1.52
Turn-off time	$t_{OFF(5k8)}$	2	4	6	µs	R_{SRP} = 5.8kΩ [4]	P_9.1.56
Turn-on delay time	$t_{DON(5k8)}$	0.3	0.75	1.5	µs	R_{SRP} = 5.8kΩ	P_9.1.60
Turn-off delay time	$t_{DOFF(5k8)}$	1	2	3	µs	R_{SRP} = 5.8kΩ	P_9.1.64
Turn-on output fall time	$t_{F(5k8)}$	1	2	3	µs	R_{SRP} = 5.8kΩ	P_9.1.68
Turn-off output rise time	$t_{R(5k8)}$	1	2	3	µs	R_{SRP} = 5.8kΩ	P_9.1.72
Turn-on Slew rate	$-(DV/Dt)_{ON(5k8)}$	7	13	21	V/µs	R_{SRP} = 5.8kΩ [5]	P_9.1.76
Turn-off Slew rate	$(DV/Dt)_{OFF(5k8)}$	7	13	21	V/µs	R_{SRP} = 5.8kΩ [5]	P_9.1.80
Turn-on time	$t_{ON(58k)}$	13	26	40	µs	R_{SRP} = 58kΩ [3]	P_9.1.53
Turn-off time	$t_{OFF(58k)}$	23	35	70	µs	R_{SRP} = 58kΩ [4]	P_9.1.57
Turn-on delay time	$t_{DON(58k)}$	3	6	10	µs	R_{SRP} = 58kΩ	P_9.1.61
Turn-off delay time	$t_{DOFF(58k)}$	7	15	35	µs	R_{SRP} = 58kΩ	P_9.1.65
Turn-on output fall time	$t_{F(58k)}$	10	20	30	µs	R_{SRP} = 58kΩ	P_9.1.69
Turn-off output rise time	$t_{R(58k)}$	10	20	30	µs	R_{SRP} = 58kΩ	P_9.1.73
Turn-on Slew rate	$-(DV/Dt)_{ON(58k)}$	0.7	1.4	2.1	V/µs	R_{SRP} = 58kΩ [5]	P_9.1.77
Turn-off Slew rate	$(DV/Dt)_{OFF(58k)}$	0.7	1.4	2.1	V/µs	R_{SRP} = 58kΩ [5]	P_9.1.81
Turn-on time	$t_{ON(open)}$	40	80	130	µs	R_{SRP} = 200kΩ(open) [3]	P_9.1.54
Turn-off time	$t_{OFF(open)}$	55	110	190	µs	R_{SRP} = 200kΩ(open) [4]	P_9.1.58
Turn-on delay time	$t_{DON(open)}$	10	20	40	µs	R_{SRP} = 200kΩ(open)	P_9.1.62

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Table 5 Electrical Characteristics: Power Stage (cont'd)

T_J = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Turn-off delay time	$t_{DOFF(open)}$	25	50	100	µs	R_{SRP} = 200kΩ(open)	P_9.1.66
Turn-on output fall time	$t_{F(open)}$	30	60	90	µs	R_{SRP} = 200kΩ(open)	P_9.1.70
Turn-off output rise time	$t_{R(open)}$	30	60	90	µs	R_{SRP} = 200kΩ(open)	P_9.1.74
Turn-on Slew rate	$-(DV/Dt)_{ON(open)}$	0.25	0.5	0.7	V/µs	R_{SRP} = 200kΩ(open) 5)	P_9.1.78
Turn-off Slew rate	$(DV/Dt)_{OFF(open)}$	0.25	0.5	0.7	V/µs	R_{SRP} = 200kΩ(open) 5)	P_9.1.82

1) Not subject to production test, calculated by R_{thJA} and $R_{DS(ON)}$.(JEDEC2S2P)
2) Not subject to production test, specified by design
3) Not subject to production test, calculated by (t_{DON} + t_F)
4) Not subject to production test, calculated by (t_{DOFF} + t_R)
5) Not subject to production test, calculated slew rate between 90% and 50%; see **Figure 12 "Definition of Power Output Timing for Resistive Load" on Page 16**

9.2 Protection

See Chapter **"Protection Functions" on Page 21** for parameter description and further details.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation

Table 6 Electrical characteristics: Protection

T_J = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V; V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal shut down 1)							
Thermal shut down junction temperature	$T_{J(SD)}$	150	175	200	°C	1)	P_9.2.1
Thermal hysteresis	ΔT_{J_HYS}	–	15	–	K	1)	P_9.2.3
Dynamic temperature limitation	$\Delta T_{J(SW)}$	–	70	–	K	1)	P_9.2.4
Over Voltage Protection / Clamping							
Drain clamp voltage	$V_{OUT(CLAMP)}$	40	–	–	V	V_{IN} = 0 V; I_L= 10 mA;	P_9.2.7

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Table 6 Electrical characteristics: Protection (cont'd)

T_J = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V; V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current limitation							
Current limitation trigger level	$I_{L(LIM)TRIGGER}$	29	43	58	A	V_{IN} = 5V; V_{DD} = 5V; V_{EN}=5V	P_9.2.10
Current limitation level	$I_{L(LIM)}$	10	-	20	A	V_{IN} = 5V; V_{DD} = 5V; V_{EN}=5V settled value	P_9.2.15

1) Not subject to production test, specified by design.

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9.3 Diagnostics

See Chapter “Diagnostics” on Page 26 for description and further details.

Table 7 Electrical Characteristics: Diagnostics

T_J = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Feedback pin							
STATUS pin voltage operation range	V_{STATUS}	-0.3	–	5.5	V		
STATUS Pin voltage drop Fault	$V_{STATUS(FAULT)}$	–	0.5	0.8	V	$I_{STATUS(FAULT)}$=1mA	P_9.3.2
STATUS Pin reset current	$I_{STATUS(RESET)}$	5	–	7	mA	–	P_9.3.3
STATUS Pin reset threshold voltage	$V_{STATUS(RESET)}$	0.9	2.0	2.5	V	–	P_9.3.6
STATUS Pin leakage current (85°C)	$I_{STATUS(85)}$		1.5	6	µA	$V_{STATUS} \leq 5.5V$ $T_J \leq 85°C$ 1)	P_9.3.4
STATUS Pin leakage current (150°C)	$I_{STATUS(150)}$		6	12	µA	$V_{STATUS} \leq 5V$ $T_J = 150°C$	P_9.3.5
Fault feedback reset time	t_{RESET}	20	–	–	µs	$V_{STATUS} > V_{STATUS(RESET)}$	P_9.3.7

1) Not subject to production test, specified by design.

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9.4 Supply and Input Stage

See Chapter **"Supply and Input Stage" on Page 27** for description and further details.

Table 8 Electrical Characteristics: Supply and Input

T_J = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply							
Nominal supply voltage	$V_{DD(NOM)}$	3.0	5.0	5.5	V	–	P_9.4.1
Supply ON/OFF threshold voltage	$V_{DD(TH)}$	1.3	2.4	3.0	V	V_{IN} = 5.0V; V_{BAT}=13.5V; V_{EN}= 5V; V_{IN}= 5V;	P_9.4.2
Supply current, continuous ON operation	$I_{DD(ON)}$	–	1.3	2.5	mA	V_{DD} = 5.0V; R_{SRP} = 0Ω; V_{EN}= 5V; $I_{OUT(0)}$ = $I_{OUT(NOM)}$	P_9.4.5
Supply current, inverse condition on OUT to GND, ON mode	$I_{DD_ON(-VOUT)}$	–	0.7	2.5	mA	V_{OUT} < -0.3V; V_{DD} = 5.5V; V_{EN}= 5V; V_{IN}= 5V; I_L =-$I_{L(NOM)}$	P_9.4.9
Supply current, inverse condition on OUT to GND, OFF mode	$I_{DD_OFF(-VOUT)}$	–	–	200	µA	V_{OUT} < -0.3V; V_{DD}= 5.5V; V_{EN}= 5V; V_{IN}= 0V; I_L =-$I_{L(NOM)}$	P_9.4.10
Standby supply current	$I_{DD(OFF)}$	–	1.5	6	µA	[1)] V_{IN} = 0V; V_{DD} = 5.0V; R_{SRP} = 0Ω; V_{EN}= 0V; T_J ≤ 85°C	P_9.4.11
Standby supply current, maximum at 150°C	$I_{DD(OFF)_150}$	–	6	14	µA	V_{IN} = 0V; V_{DD} = 5.0V; R_{SRP} = 0Ω; V_{EN}= 0V; T_J = 150°C	P_9.4.12

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Table 8 Electrical Characteristics: Supply and Input (cont'd)

T_J = -40°C to +150°C, V_{DD} = 3.0 V to 5.5 V, V_{BAT} = 6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
INPUT							
Input Voltage	V_{IN}	-0.3	–	5.5	V	–	
Low level input voltage	$V_{IN(L)}$	-0.3	–	0.8	V	–	P_9.4.14
High level input voltage	$V_{IN(H)}$	2.0	–	V_{DD}	V	–	P_9.4.15
Input voltage hysteresis	$V_{IN(HYS)}$	–	200	–	mV	–	P_9.4.16
Input pull down current	I_{IN}	–	–	160	µA	2.7V < V_{IN} < 5.5V -0.3V < V_{DD} < 5.5V	P_9.4.17
Internal Input pull down resistor	$R_{IN(GND)}$	25	50	100	kΩ	–	P_9.4.18
ENABLE							
ENABLE Voltage	V_{ENABLE}	-0.3	–	5.5	V	–	
Low level ENABLE voltage	$V_{ENABLE(L)}$	-0.3	–	0.8	V	–	P_9.4.20
High level ENABLEvoltage	$V_{ENABLE(H)}$	2.0	–	V_{DD}	V	–	P_9.4.21
ENABLE voltage hysteresis	$V_{ENABLE(HYS)}$	–	200	–	mV	–	P_9.4.22
ENABLE pull down current	I_{ENABLE}	–	–	160	µA	2.7V < V_{IN} < 5.5V -0.3V < V_{DD} < 5.5V	P_9.4.23
Internal ENABLE pull down resistor	$R_{ENABLE(GND)}$	25	50	100	kΩ	–	P_9.4.24
ENABLE masking time	$t_{ENABLE(MASKING)}$	4	8	16	µs	–	P_9.4.25
SRP							
SRP resistor range for adjustable operation	$R_{SRP(NOR)}$	5	–	70	KΩ	1)	P_9.4.26
SRP resistor range for fast operation	$R_{SRP(EXTF)}$	0	–	1.5	KΩ	1)	P_9.4.27
SRP resistor range for slow operation	$R_{SRP(EXTS)}$	160	–	–	KΩ	1)	P_9.4.28

1) Not subject to production test, specified by design.

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10 Characterization Results

10.1 Power Stage

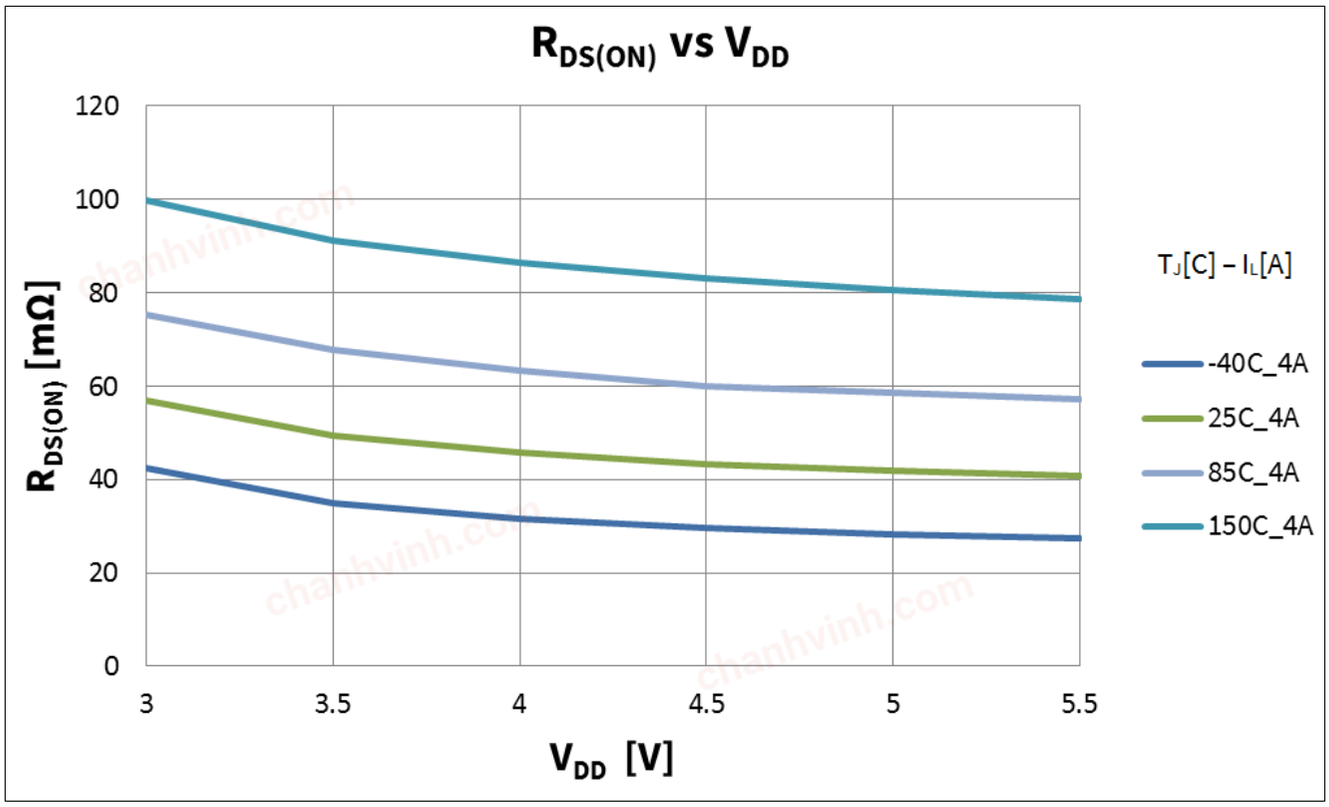


Figure 24 $R_{DS(ON)}$ vs. V_{DD} @ T_J=-40, 25, 85, 150°C, I_L=$I_{L(NOM)}$; V_{IN}= V_{ENABLE}= 5V; V_{DD}= *3...5.5V;* R_{SRP}= 0Ω

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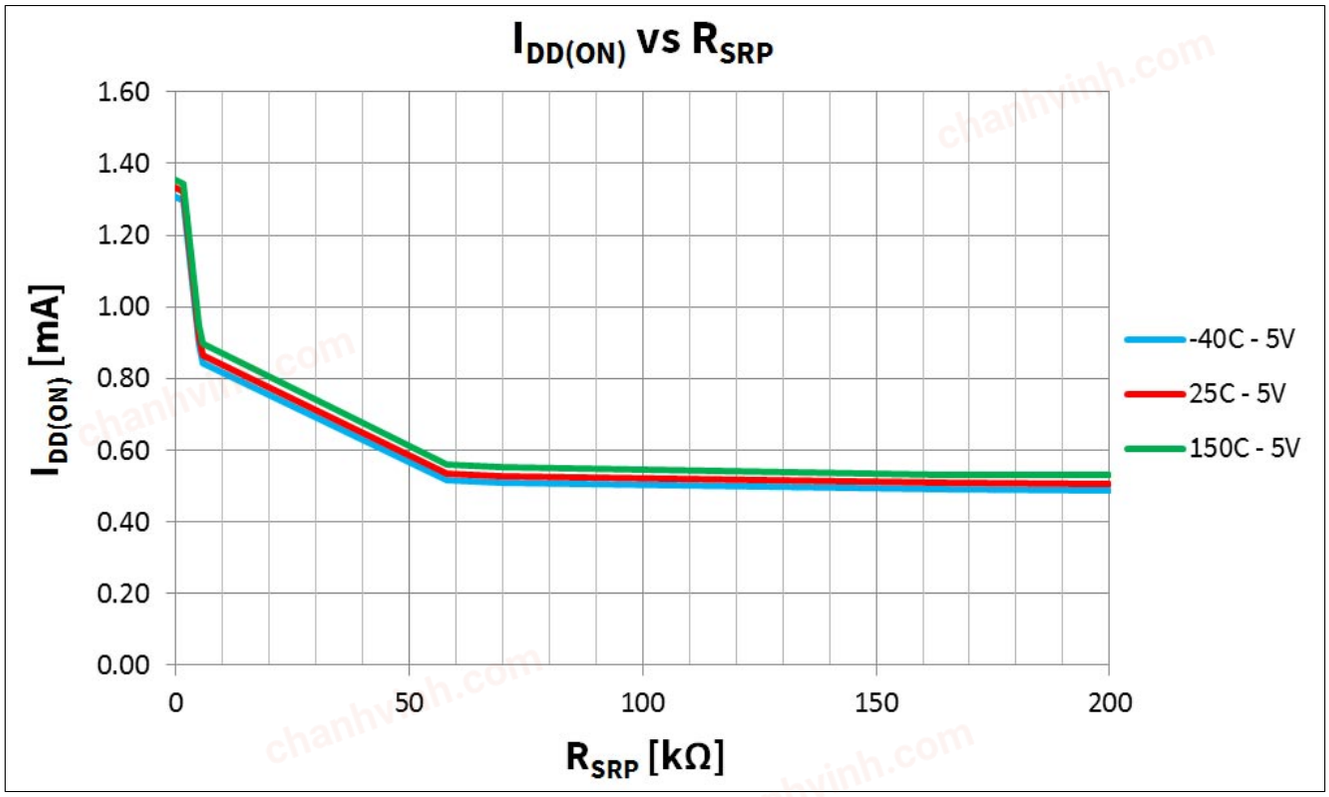


Figure 25 $I_{DD(ON)}$ **vs.** R_{SRP} **@** T_J**=-40, 25, 150°C,** I_L**=**$I_{L(NOM)}$**;** V_{IN} **=** V_{ENABLE}**=** V_{DD}**= 5V**

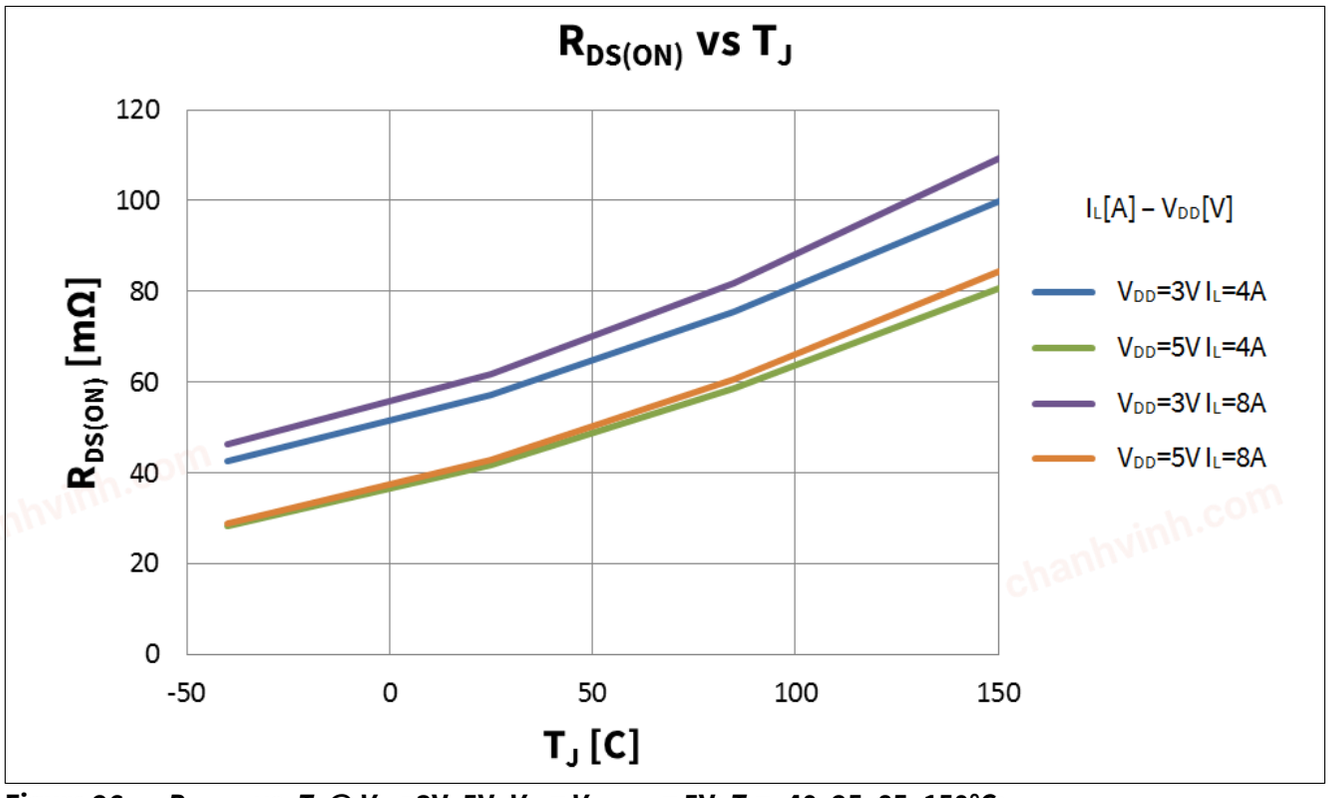


Figure 26 $R_{DS(ON)}$ **vs.** T_J **@** V_{DD}**=3V, 5V;** V_{IN} **=** V_{ENABLE} **= 5V;** T_J**= -40, 25, 85, 150°C;**

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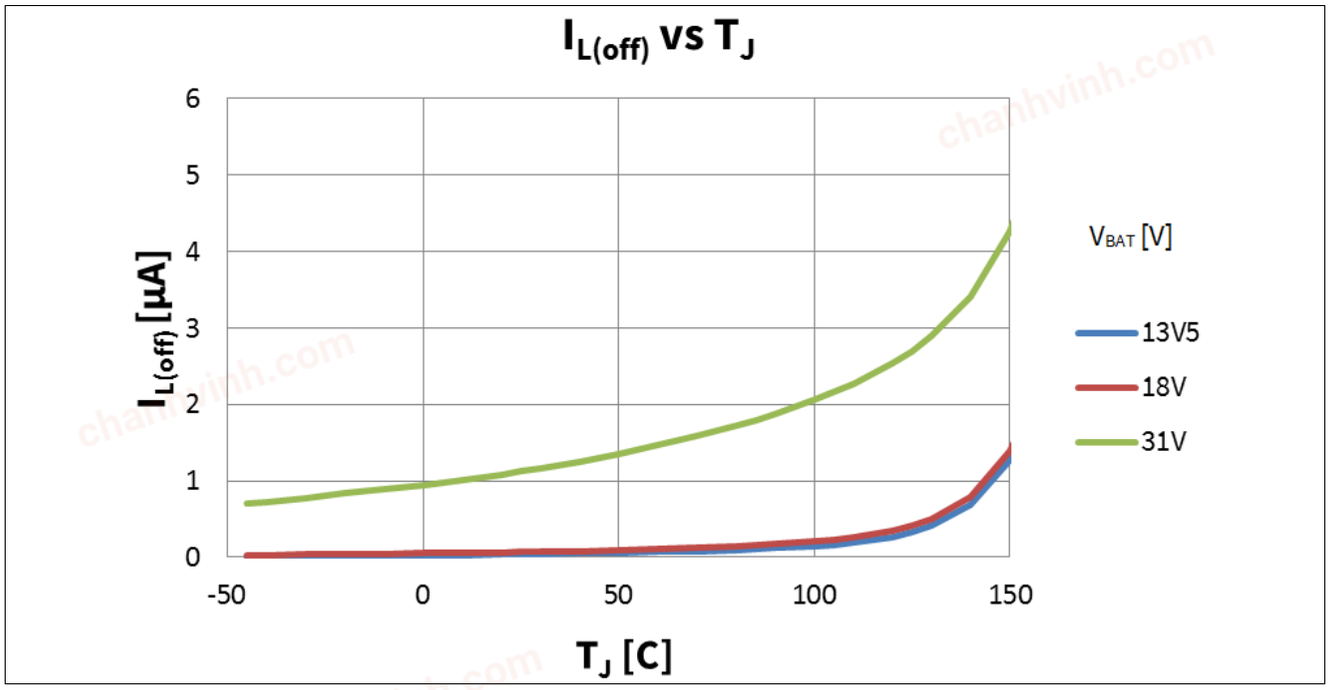


Figure 27 $I_{L(OFF)}$ vs. T_J @ V_{IN} = 0V; V_{ENABLE}= V_{DD}= 5V; T_J= -40, -20, 0, 25, 50, 85, 105, 125, 150°C; V_{BAT} = 13.5V, 18V, 31V

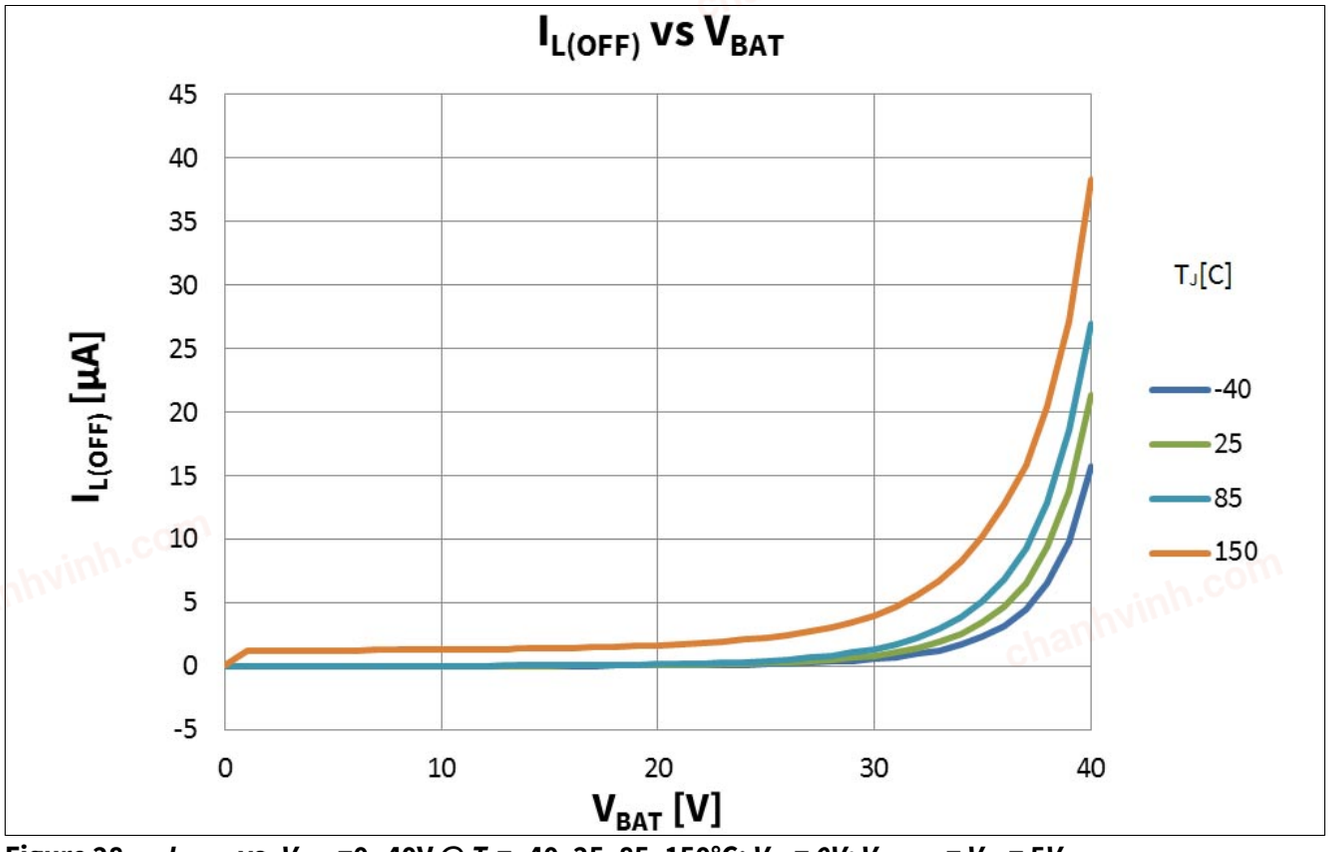


Figure 28 $I_{L(OFF)}$ vs. V_{BAT} =0..40V @ T_J= -40, 25, 85, 150°C; V_{IN} = 0V; V_{ENABLE}= V_{DD}= 5V

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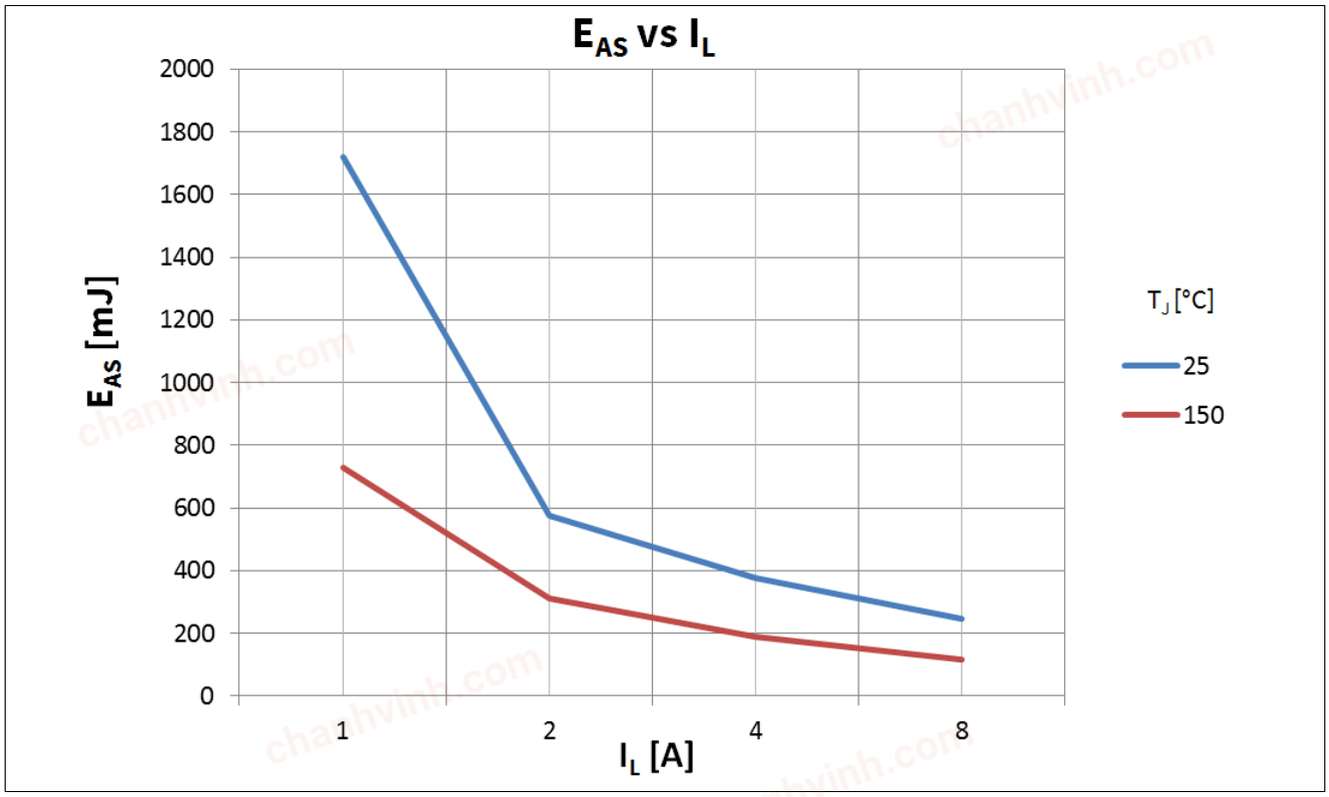


Figure 29 E_{AS} vs. I_L @ $T_{J(0)}$=25°C, 150°C, V_{BAT}=13.5V; V_{IN} = V_{ENABLE} = V_{DD}= open; I_L=$I_{L(NOM)}$ /4, $I_{L(NOM)}$/2, $I_{L(NOM)}$, 2*$I_{L(NOM)}$

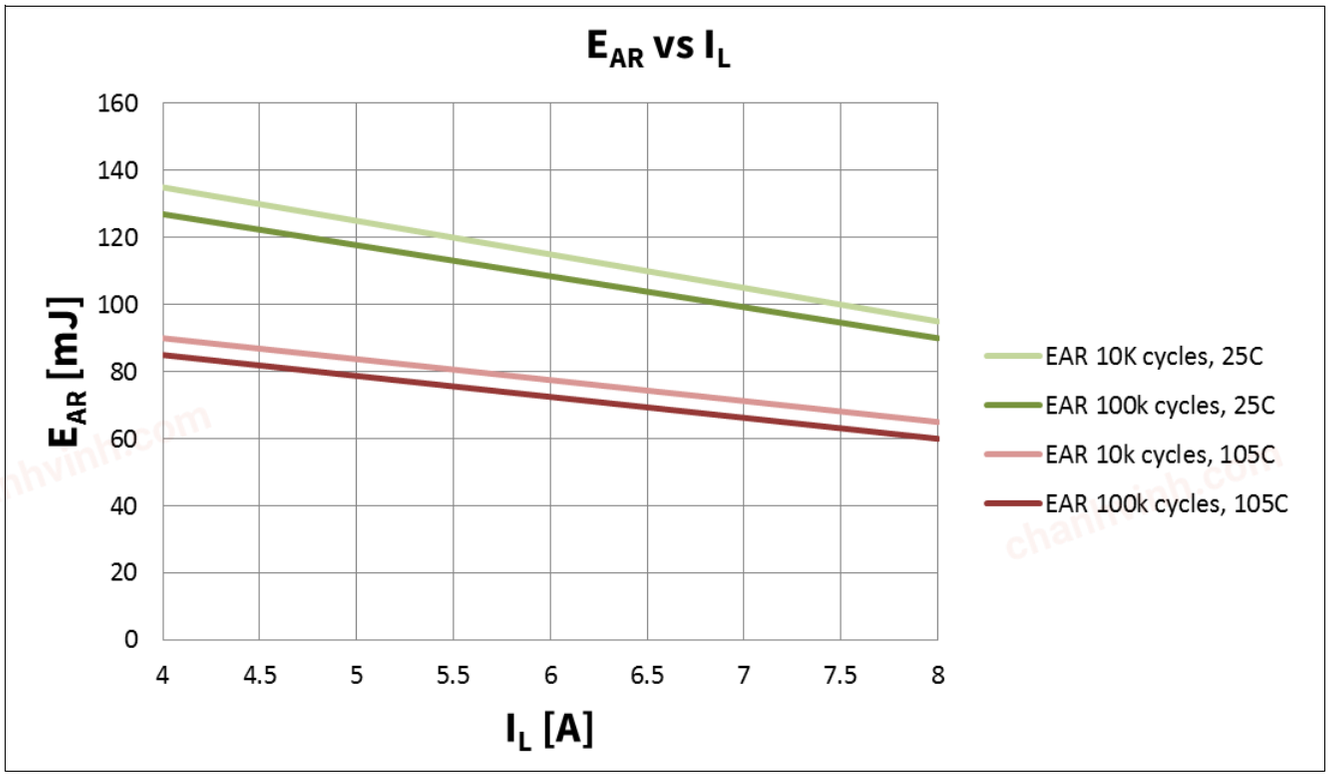


Figure 30 $E_{AR_10k, _100k}$ vs. I_L @ $T_{J(0)}$=25°C, 105°C, V_{BAT}= 13.5V; V_{IN} = V_{ENABLE} = V_{DD}= 5V; I_L =$I_{L(NOM)}$, 2*$I_{L(NOM)}$

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Characterization Results

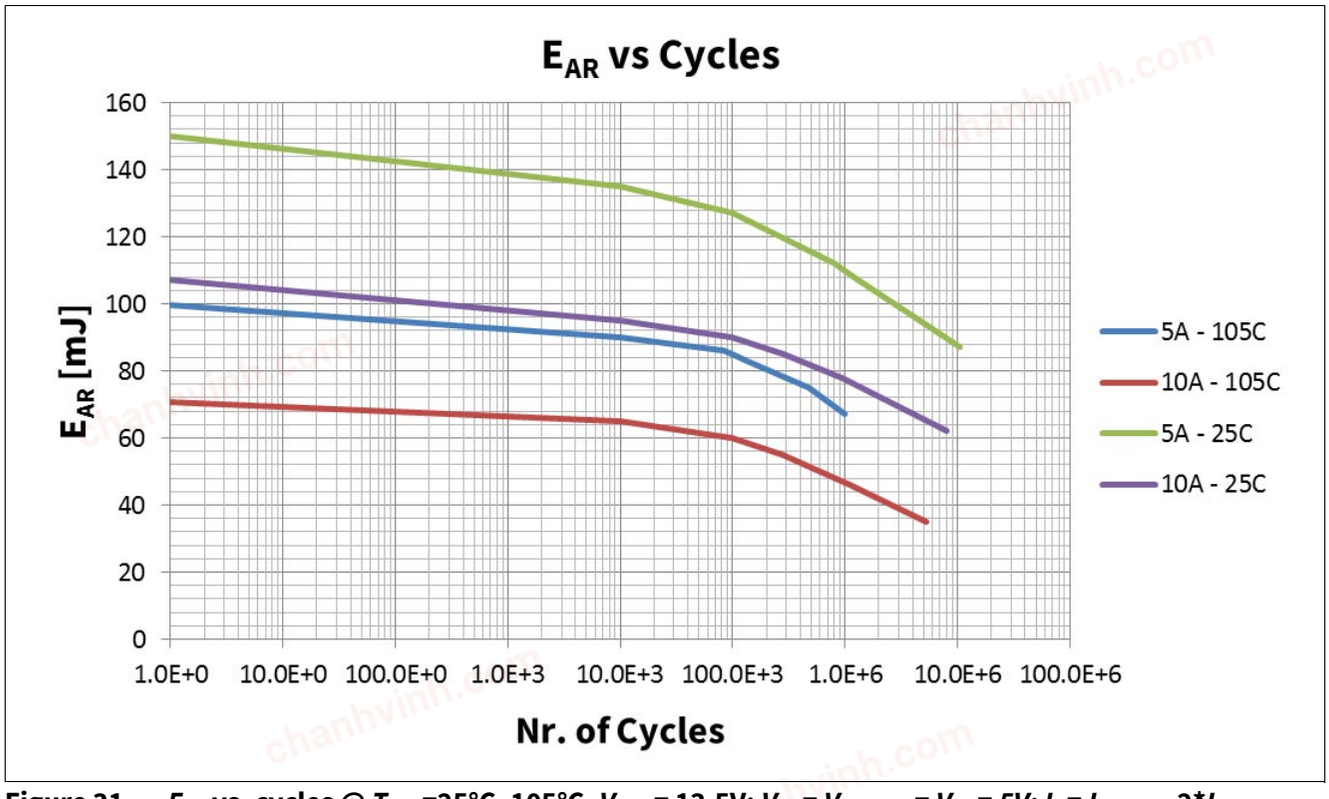


Figure 31 E_{AR} **vs. cycles @** $T_{J(0)}$**=25°C, 105°C,** V_{BAT} **= 13.5V;** $V_{IN} = V_{ENABLE} = V_{DD}$ **= 5V;** $I_L = I_{L(NOM)}$**,** $2*I_{L(NOM)}$

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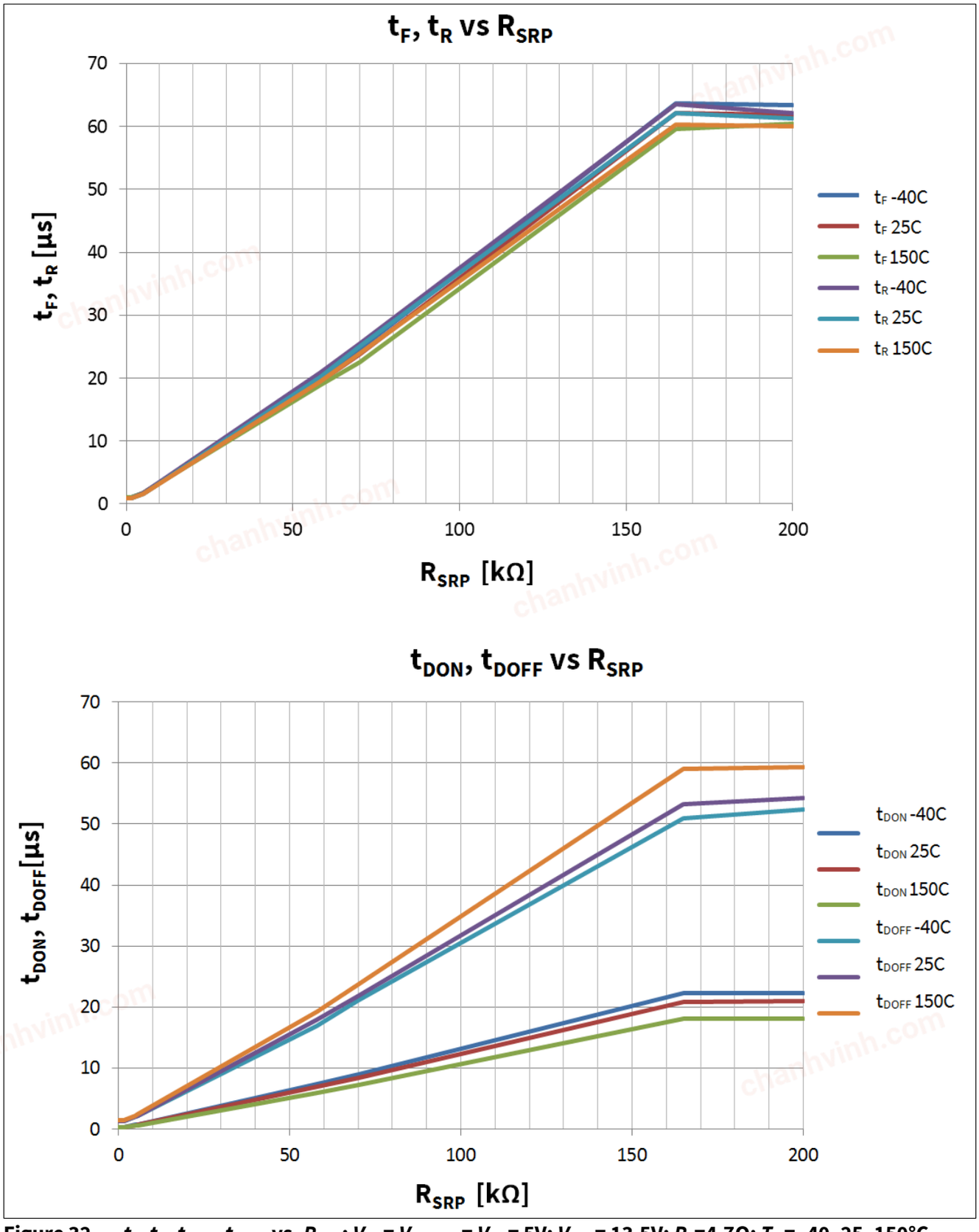


Figure 32 t_F, t_R, t_{DON}, t_{DOFF} vs. R_{SRP}; V_{IN} = V_{ENABLE}= V_{DD}= 5V; V_{BAT}= 13.5V; R_L=4.7Ω; T_J = -40, 25, 150°C

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Characterization Results

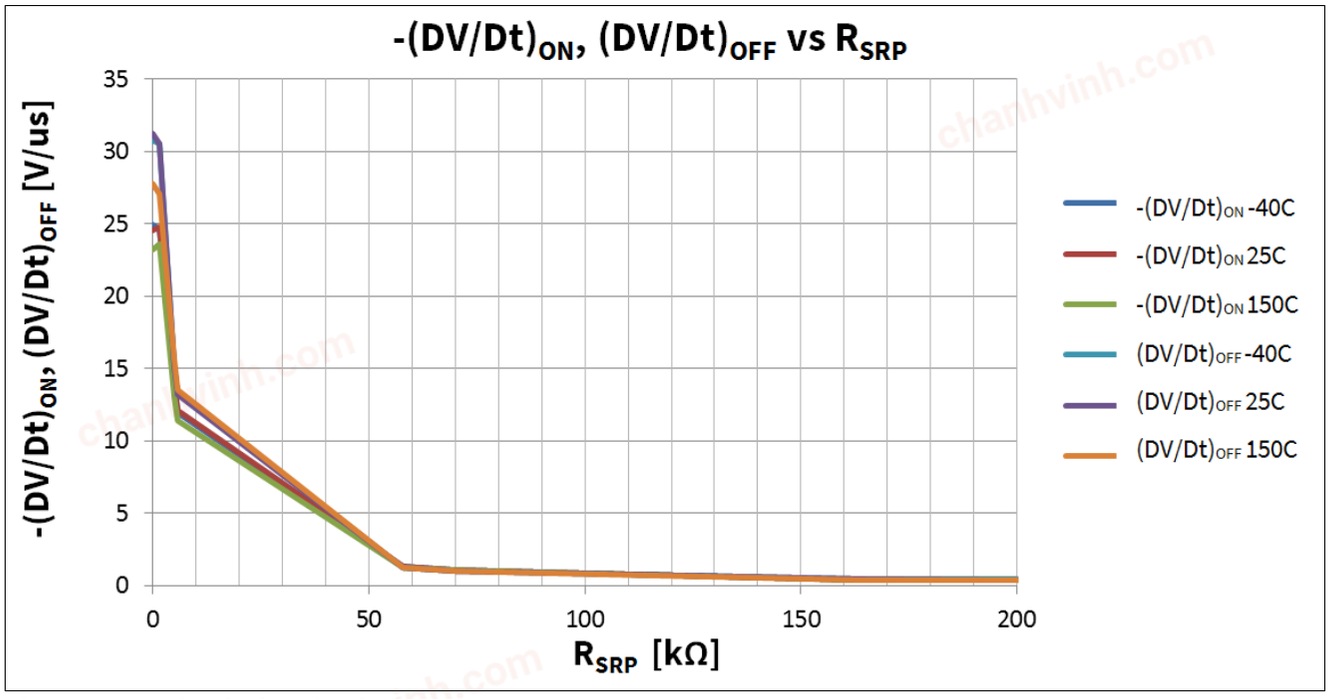


Figure 33 $-(\Delta V/\Delta t)_{ON}$, $(\Delta V/\Delta t)_{OFF}$ vs. R_{SRP}; $V_{IN} = V_{ENABLE} = V_{DD} = 5V$; $V_{BAT} = 13.5V$; $R_L = 4.7\Omega$; $T_J = -40, 25, 150°C$

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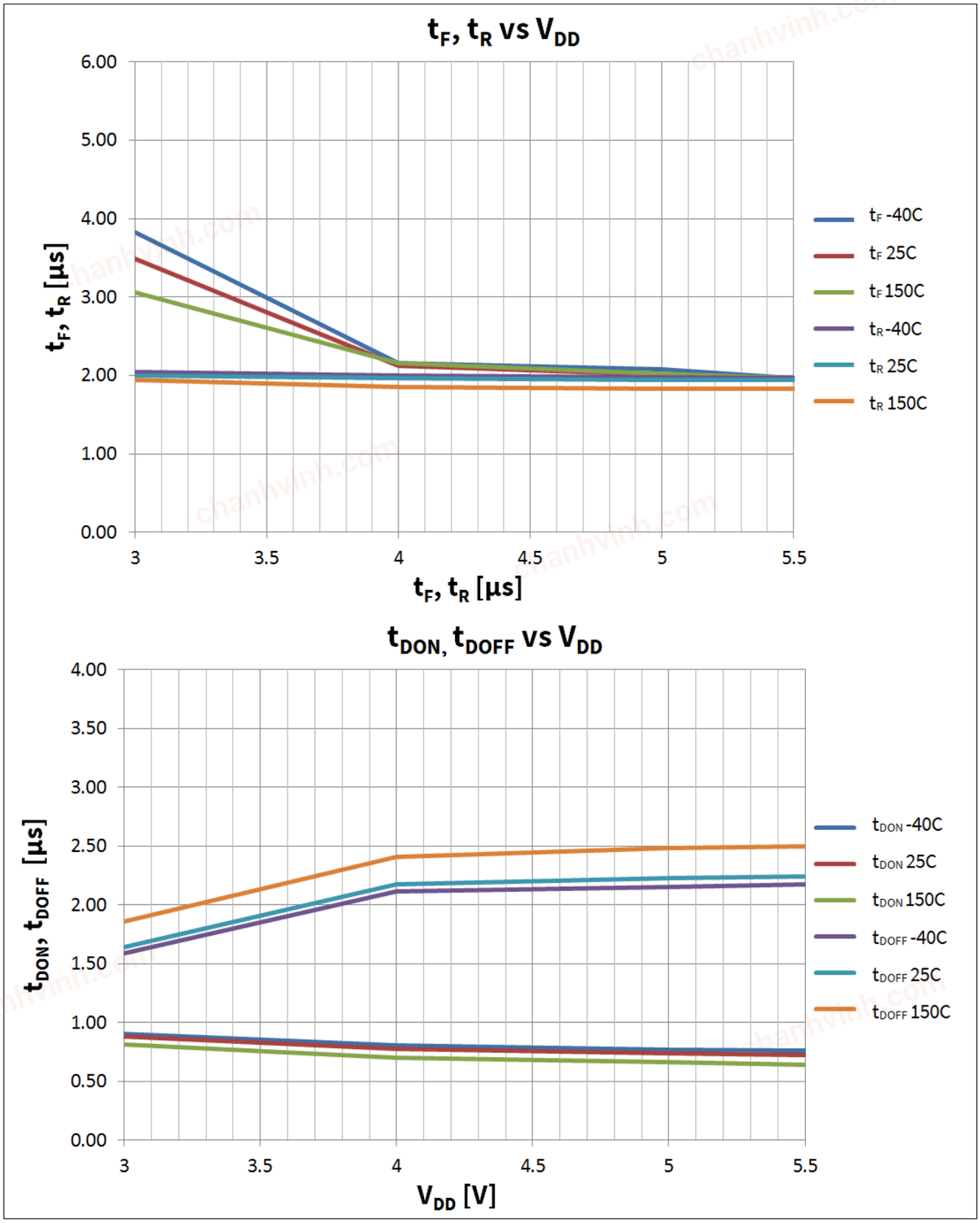


Figure 34 t_F, t_R, t_{DON}, t_{DOFF} vs. V_{DD}=3..5.5V @ V_{BAT}=13.5V; T_J= -40, 25, 150°C; R_{SRP} = 5.8kΩ; V_{IN} = V_{ENABLE} = 5V; R_L=4.7Ω;

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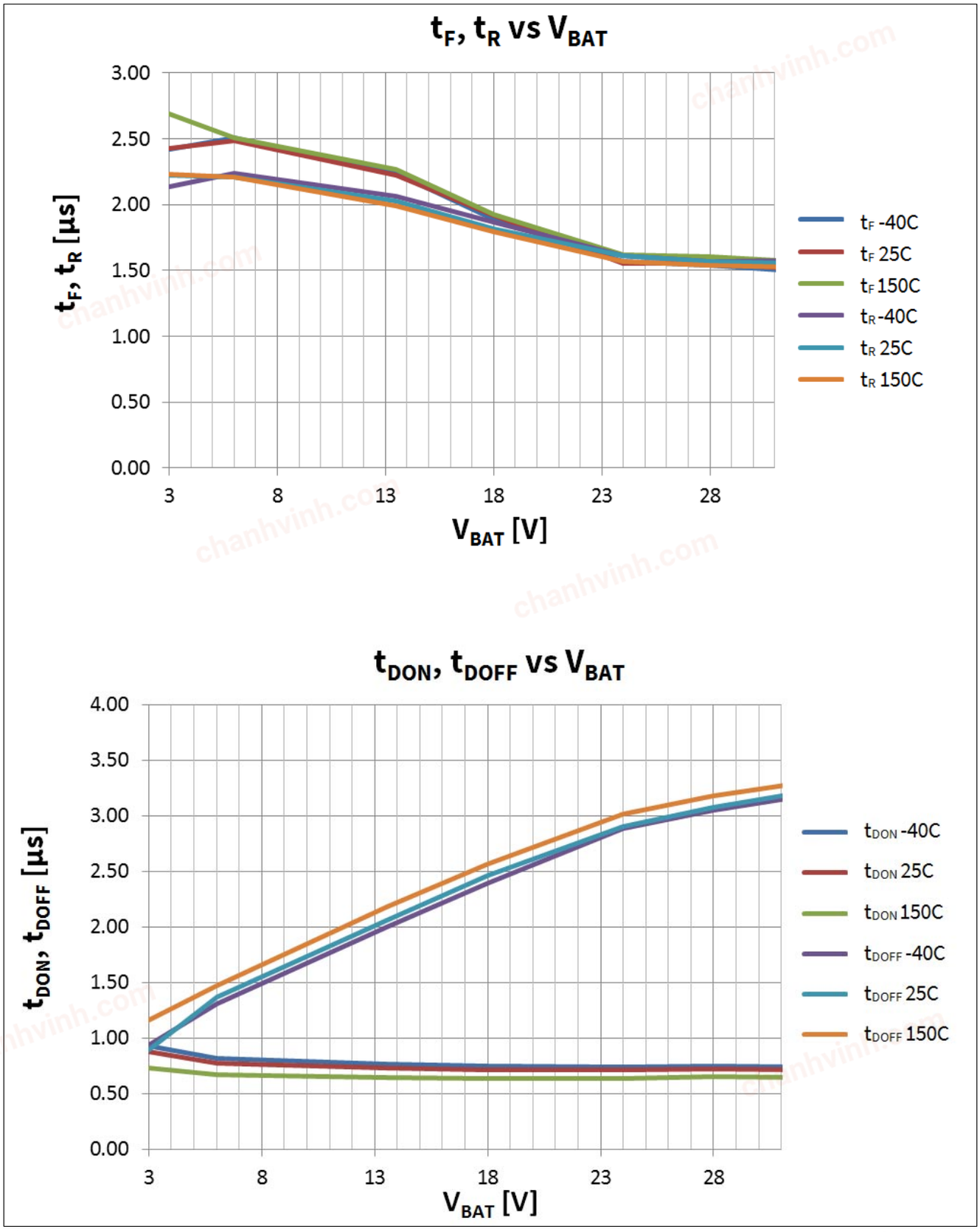


Figure 35 t_F, t_R, t_{DON}, t_{DOFF} vs. V_{BAT}=3..31V @ V_{DD}=5V; V_{IN} = V_{ENABLE}= V_{DD} = 5V; R_L = 4.7Ω; R_{SRP}=5.8kΩ, open; T_J= -40, 25, 150°C

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Characterization Results

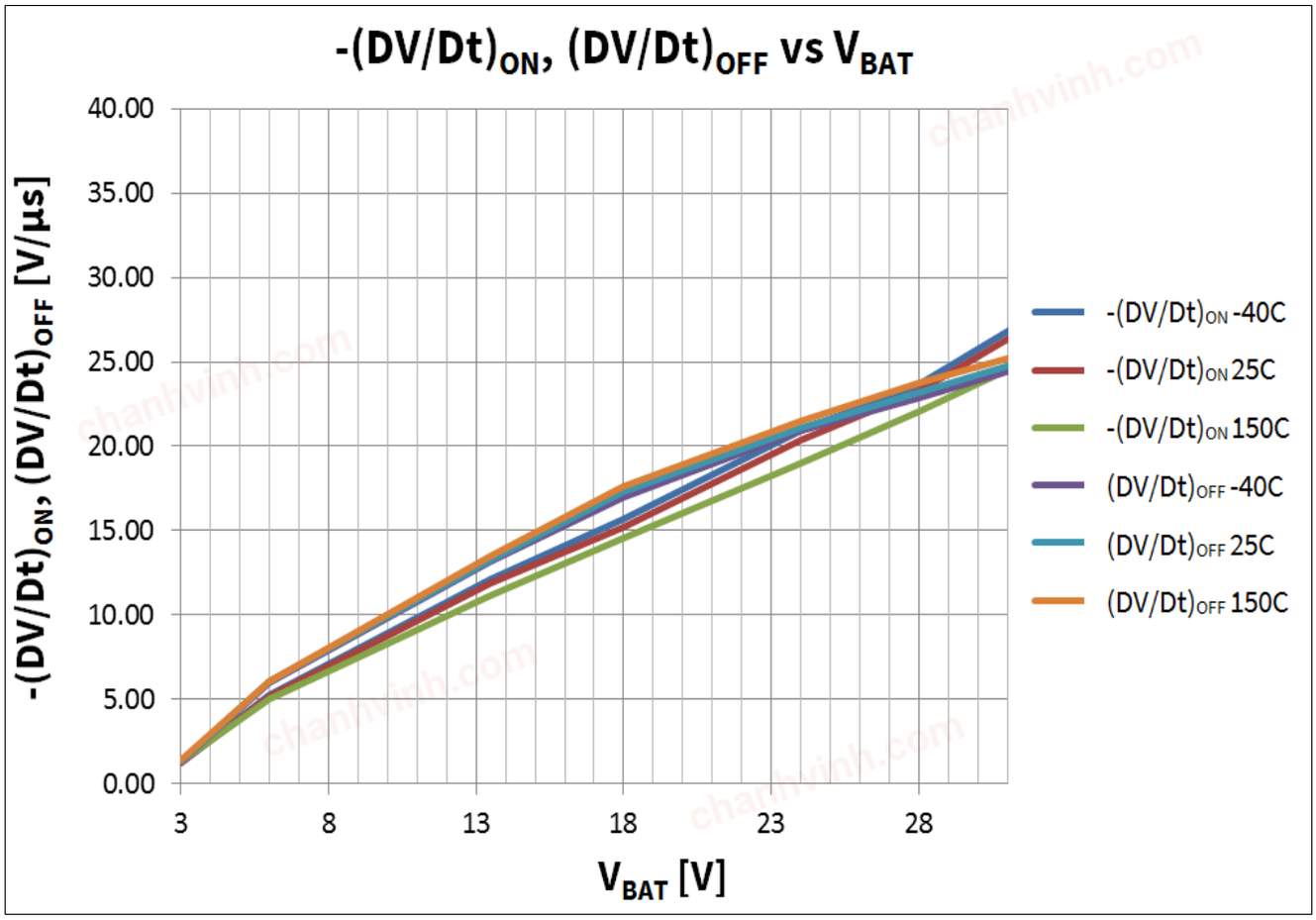


Figure 36 Slewrates ($-(\Delta V/\Delta t)_{ON}$, $(\Delta V/\Delta t)_{OFF}$ vs. V_{BAT} @ T_J = -40, 25, 150°C; R_L=4.7Ω; R_{SRP}= 5.8kΩ; V_{IN} = V_{DD} = V_{ENABLE}= 5V; V_{BAT} = 3..31V

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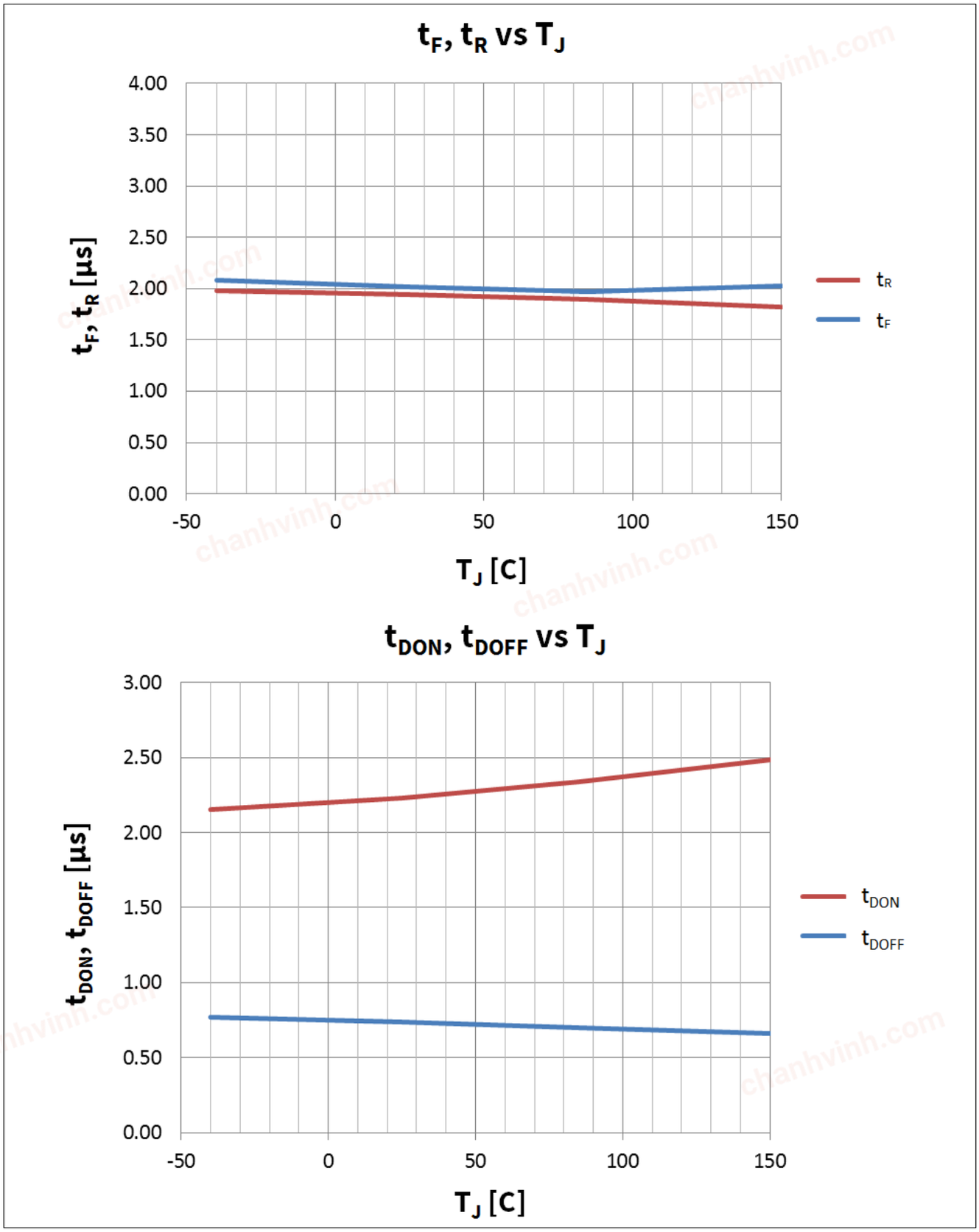


Figure 37 t_F, t_R, t_{DON}, t_{DOFF} vs. T_J= -40; 25; 150°C @ R_{SRP}= 5.8kΩ; V_{IN}= V_{ENABLE} = V_{DD} = 5V; V_{BAT} = 13.5V; R_L= 4.7Ω

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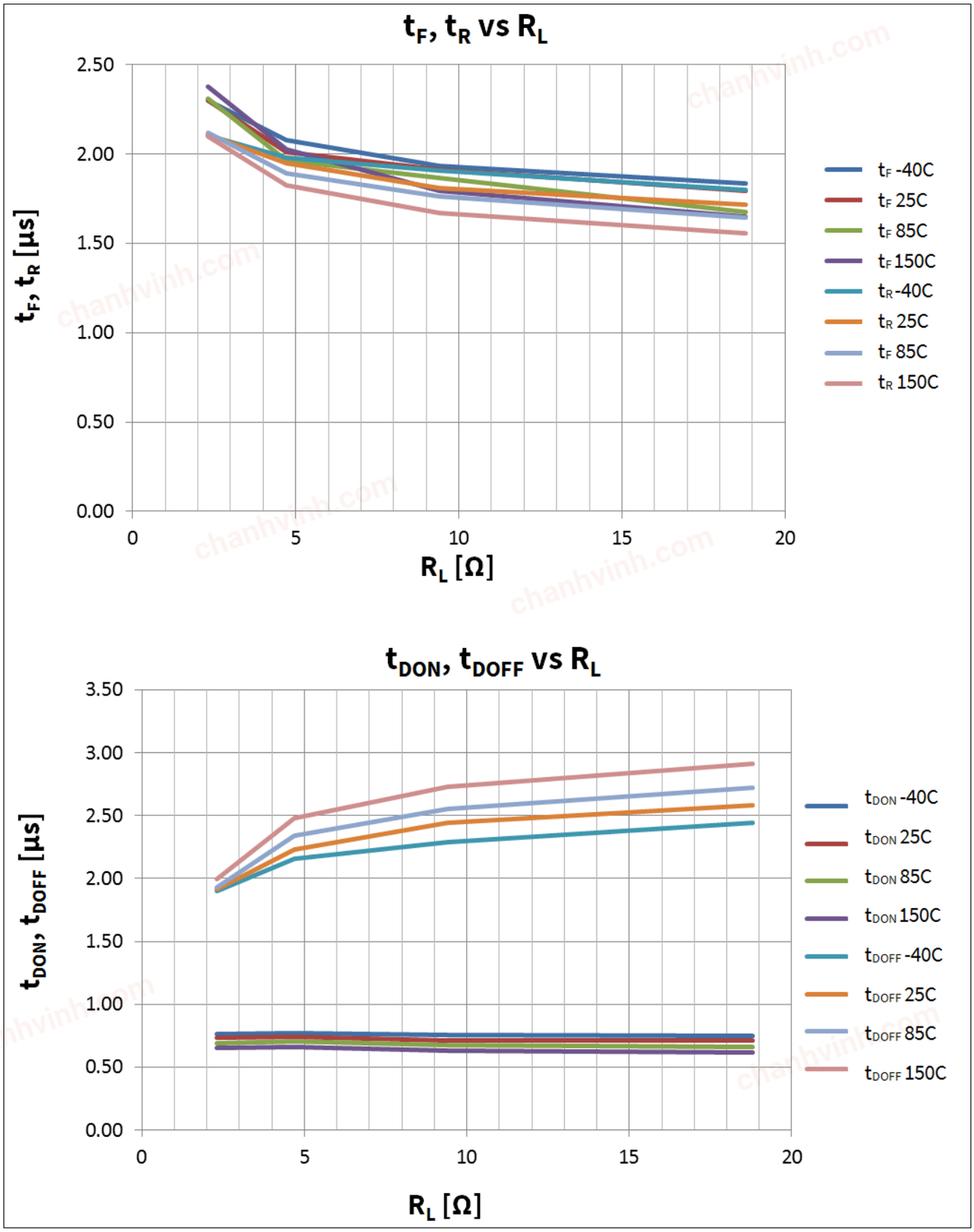


Figure 38 t_F, t_R, t_{DON}, t_{DOFF} vs. R_L @ R_{SRP}= 5.8kΩ; V_{IN}= V_{ENABLE}= V_{DD}= 5V; V_{BAT} = 13.5V; T_J = -40, 25, 150°C

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10.2 Protection

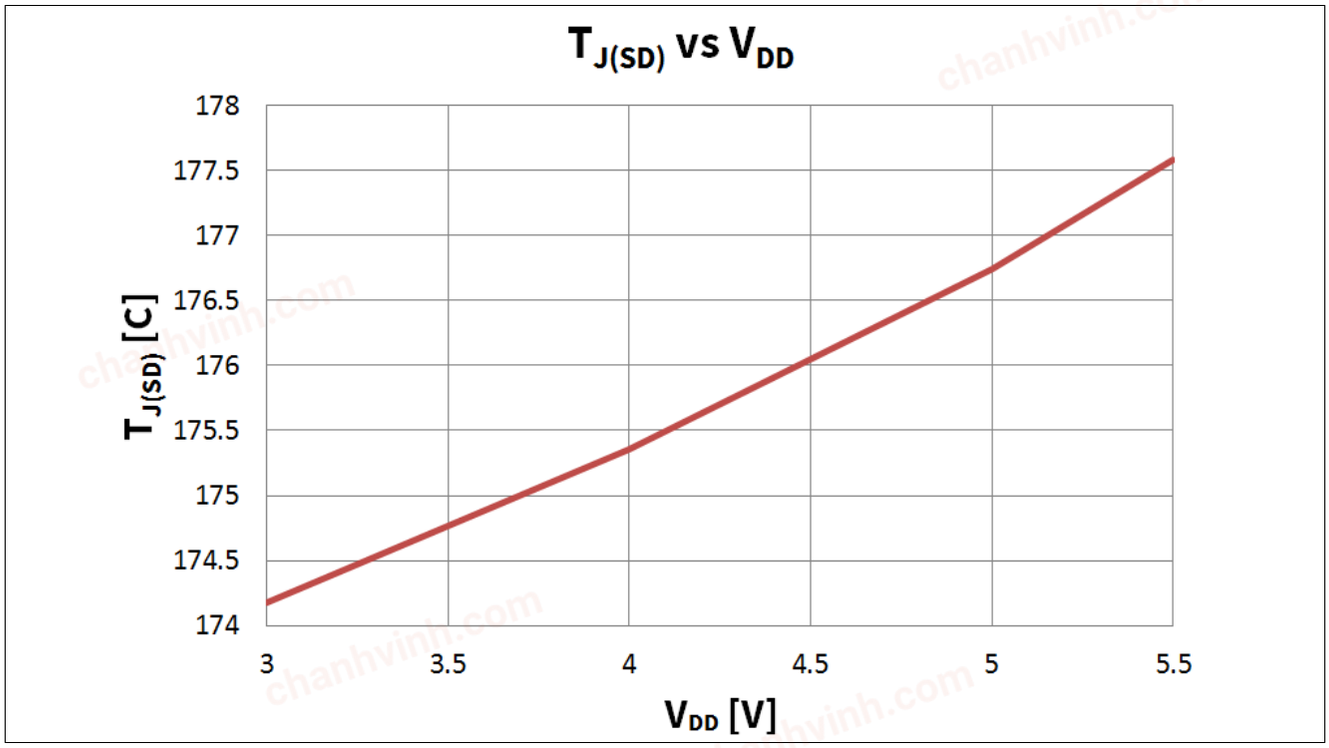


Figure 39 $T_{J(SD)}$ vs. V_{DD}; V_{IN}=V_{ENABLE}= 5V; V_{DD}= 3V...5.5V; I_L= 10mA

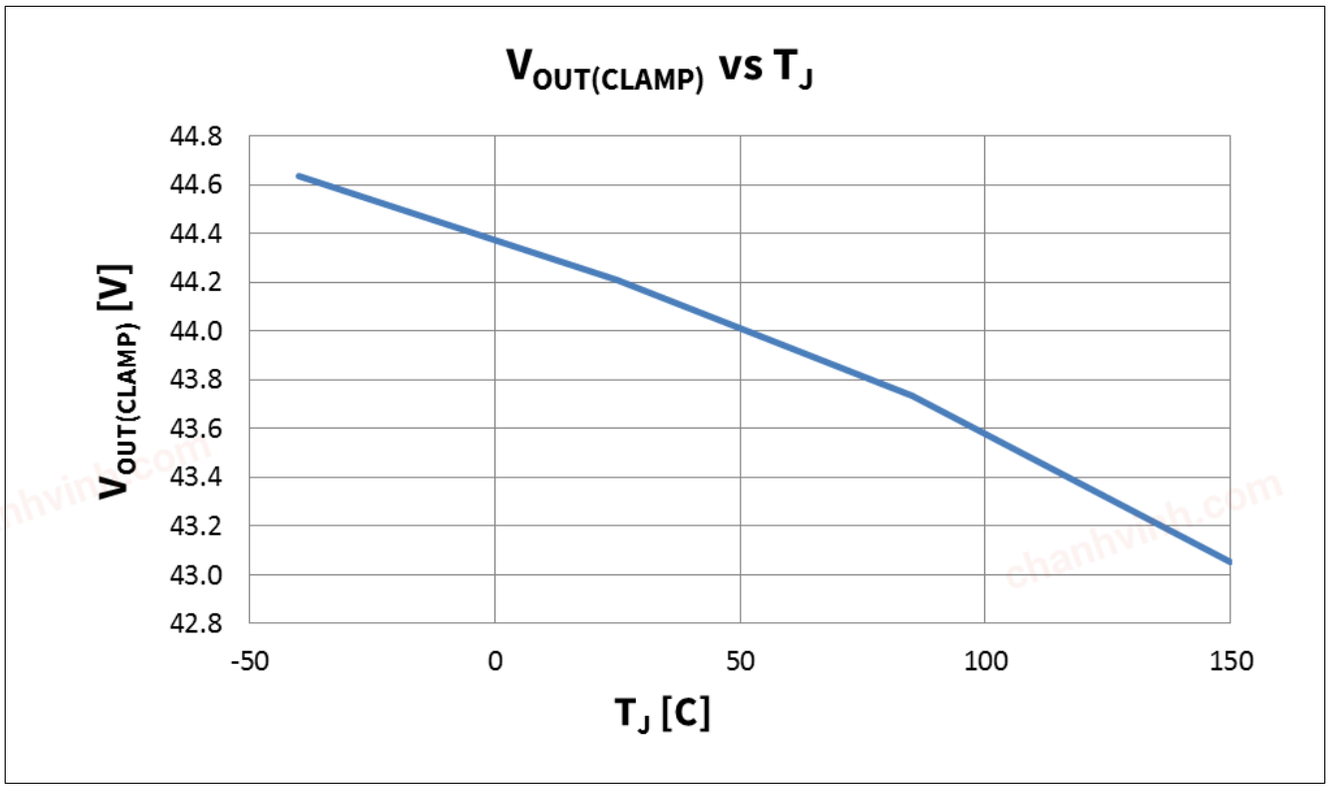


Figure 40 $V_{OUT(clamp)}$ vs. T_J; V_{IN}= 0V;V_{ENABLE}= V_{DD}= 5V; I_L= 10mA

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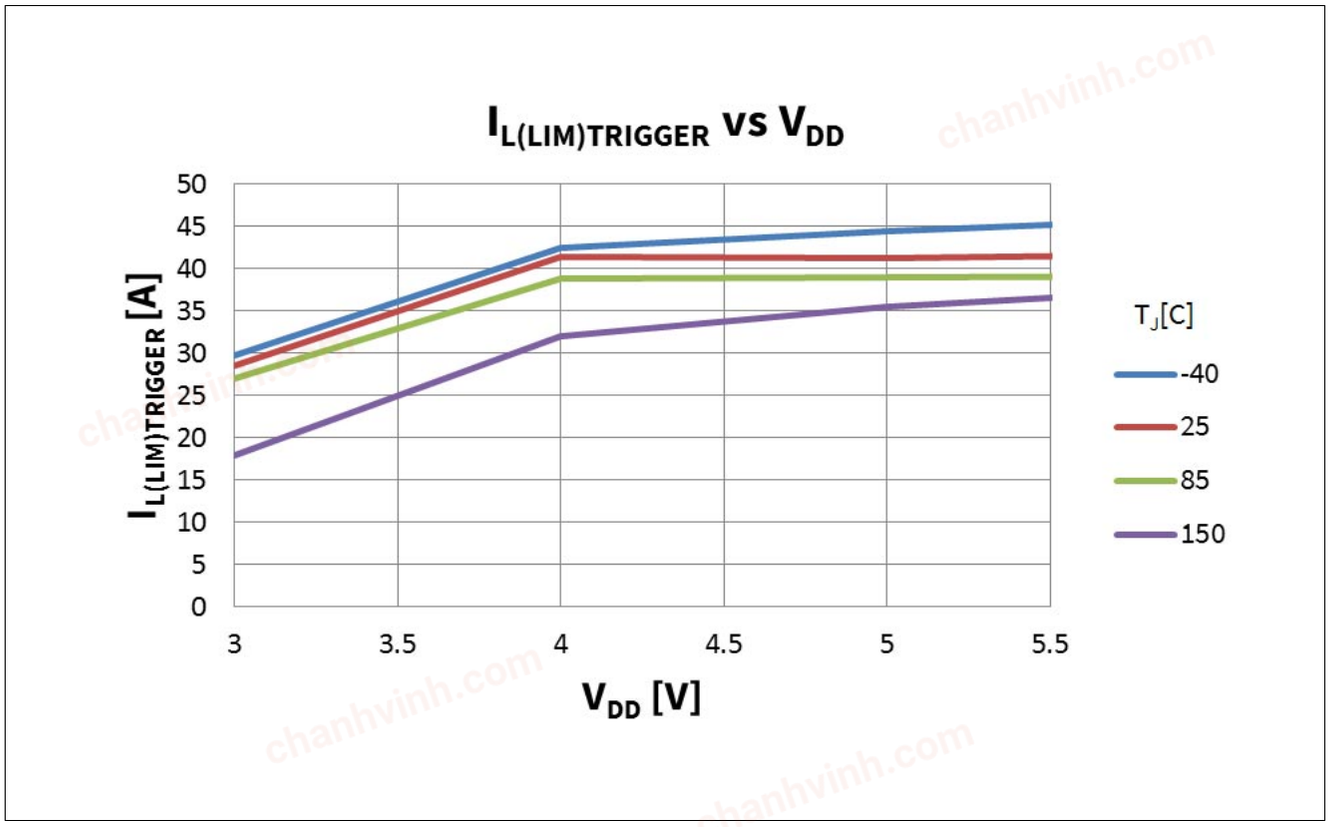


Figure 41 $I_{L(LIM)TRIGGER}$ peak vs. V_{DD}=3...5.5V@ T_J= -40, 25, 85, 150°C; V_{IN}= PWM 5V in SOA; V_{ENABLE}= 5V; V_{BAT}= 13.5V; R_L= 4.7Ω

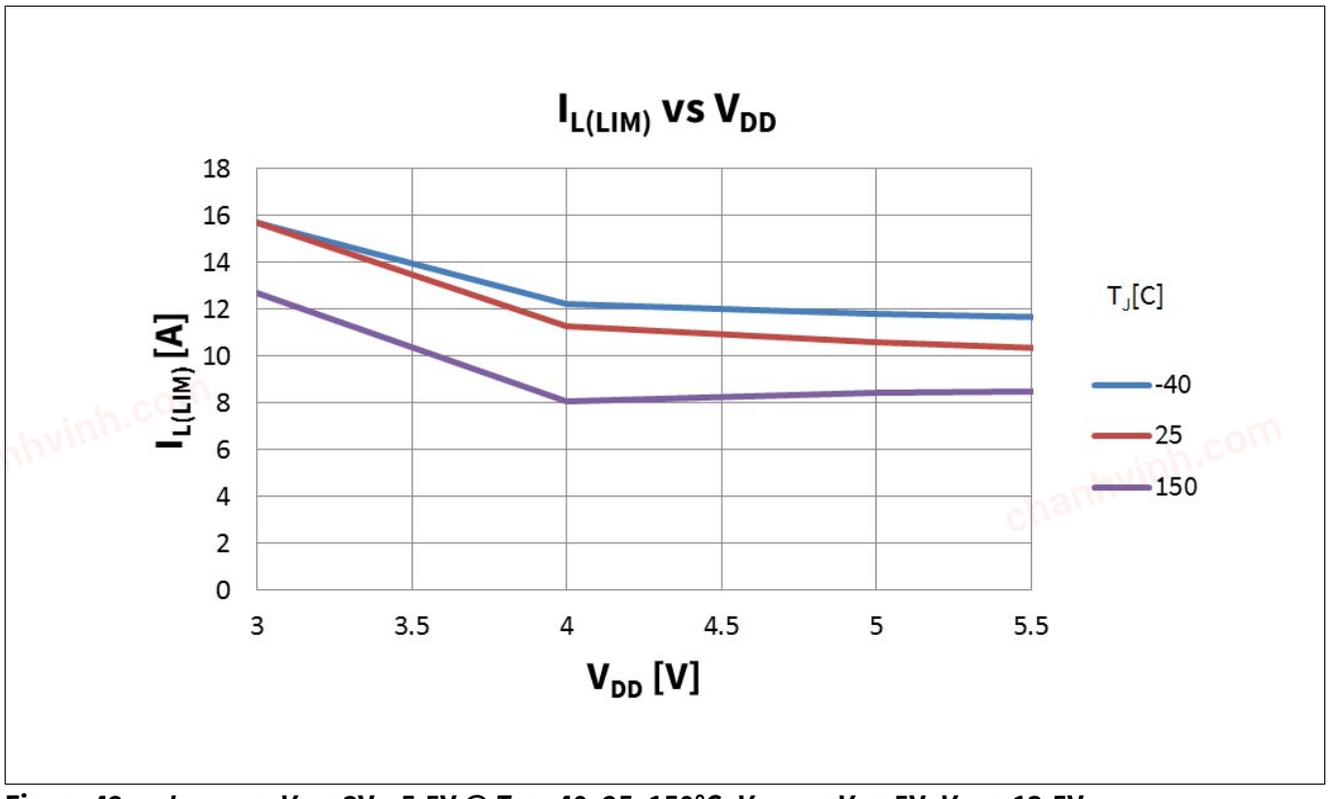


Figure 42 $I_{L(LIM)}$ vs. V_{DD}= 3V...5.5V @ T_J = -40, 25, 150°C; V_{ENABLE}=V_{IN}= 5V; V_{BAT}= 13.5V

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10.3 Diagnostics

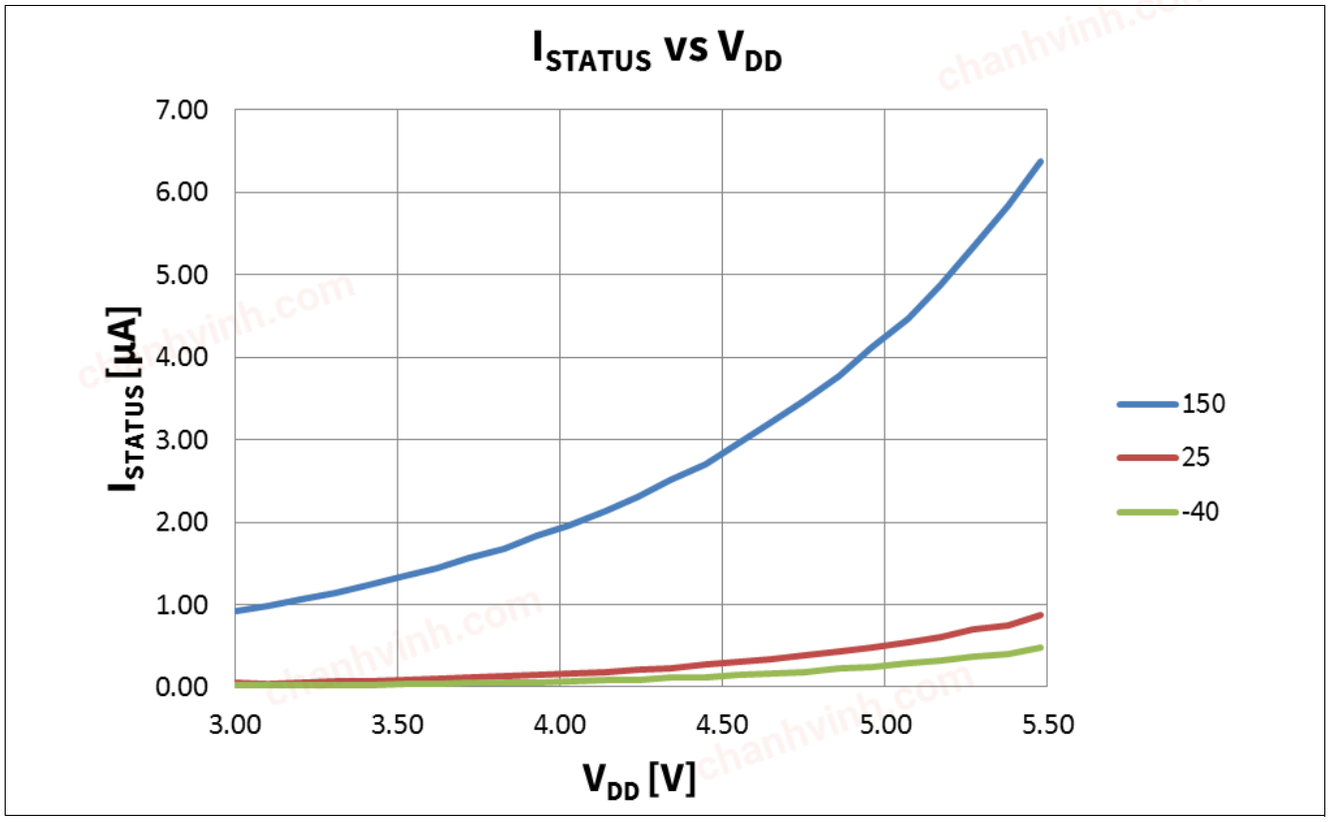


Figure 43 I_{STATUS} vs. V_{DD} = 3V...5.5V@ T_J= -40, 25, 150°C; V_{ENABLE}= V_{IN}= 5V; V_{BAT}= 13.5V;

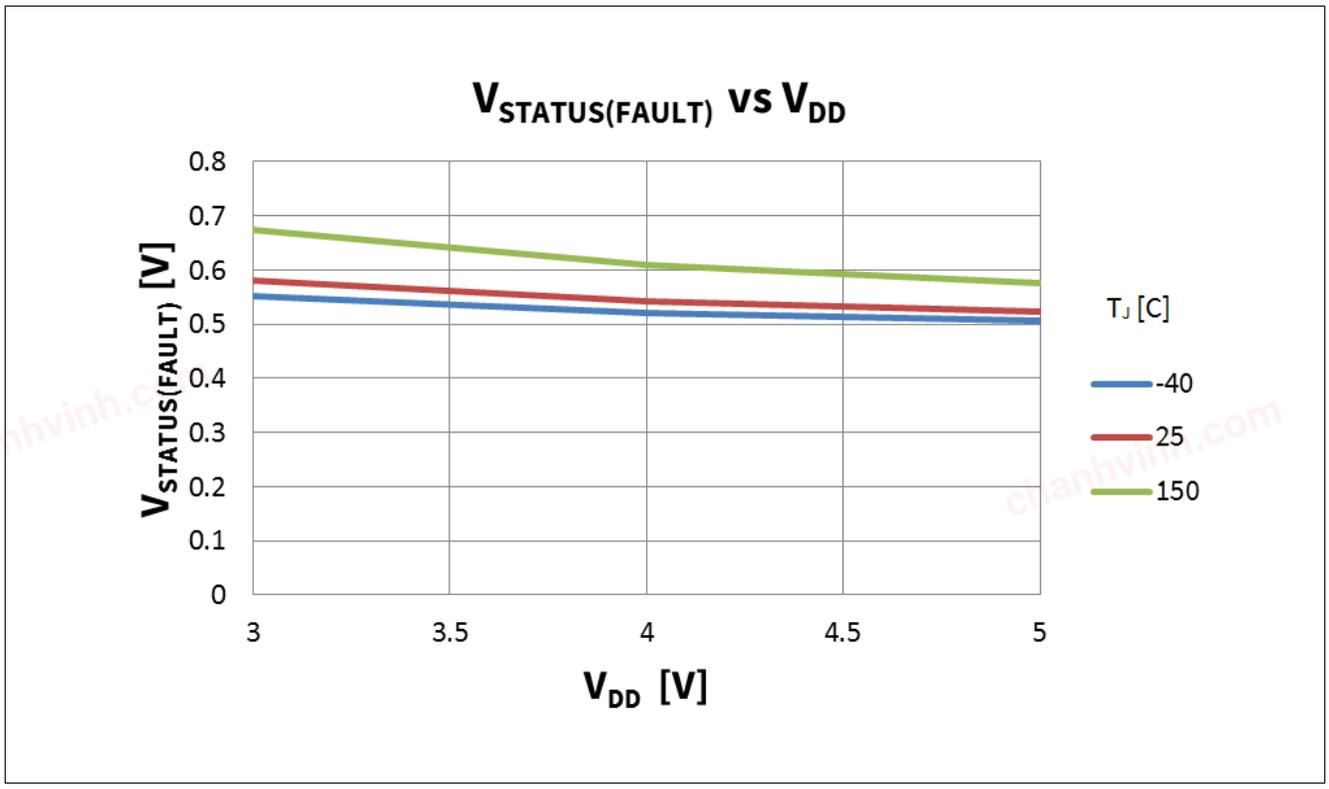


Figure 44 V_{STATUS} in fault mode vs. V_{DD} = 3V...5V@ T_J = -40, 25, 150°C; V_{IN} = V_{ENABLE}= 5V; V_{BAT}= 13.5V;

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10.4 Supply and Input Stage

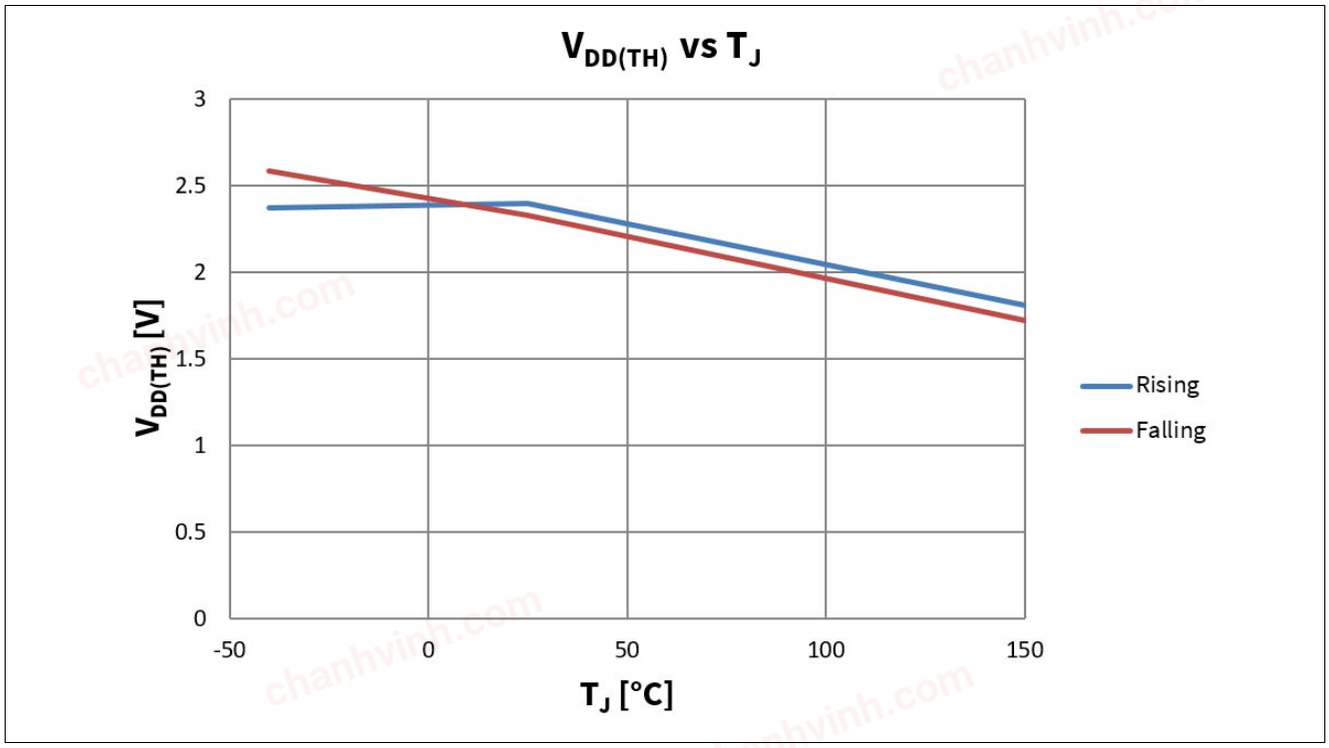


Figure 45 $V_{DD(TH)}$ vs. T_J = -40, 25, 150°C; V_{IN}=V_{ENABLE}= 5V; R_L= 4.7Ω; V_{BAT}= 13.5V; R_{SRP}= 0Ω

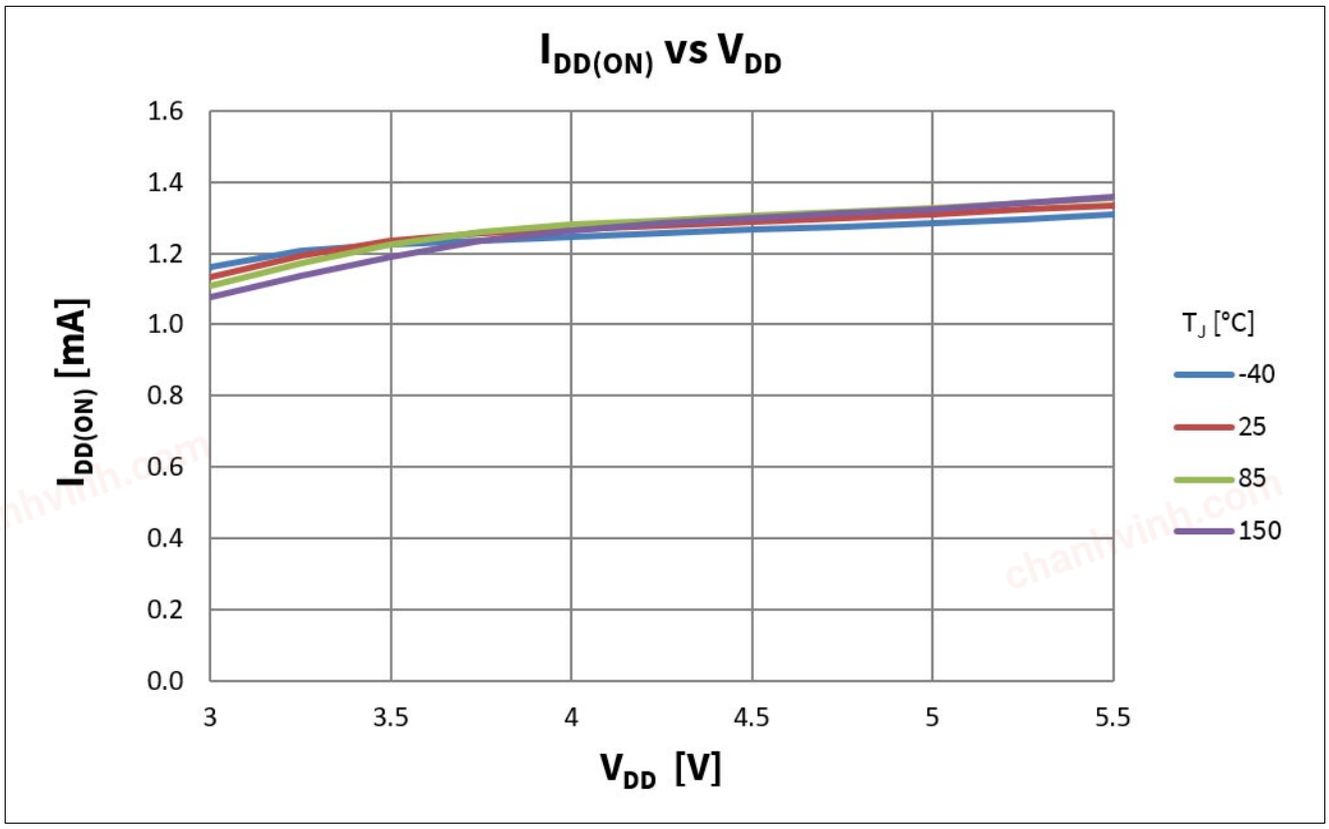


Figure 46 $I_{DD(ON)}$ vs. V_{DD} = 3V...5.5V@ T_J = -40, 25, 85, 150°C; V_{IN} = V_{ENABLE} = 5V; R_{SRP}= 0Ω; V_{BAT} = 13.5V;

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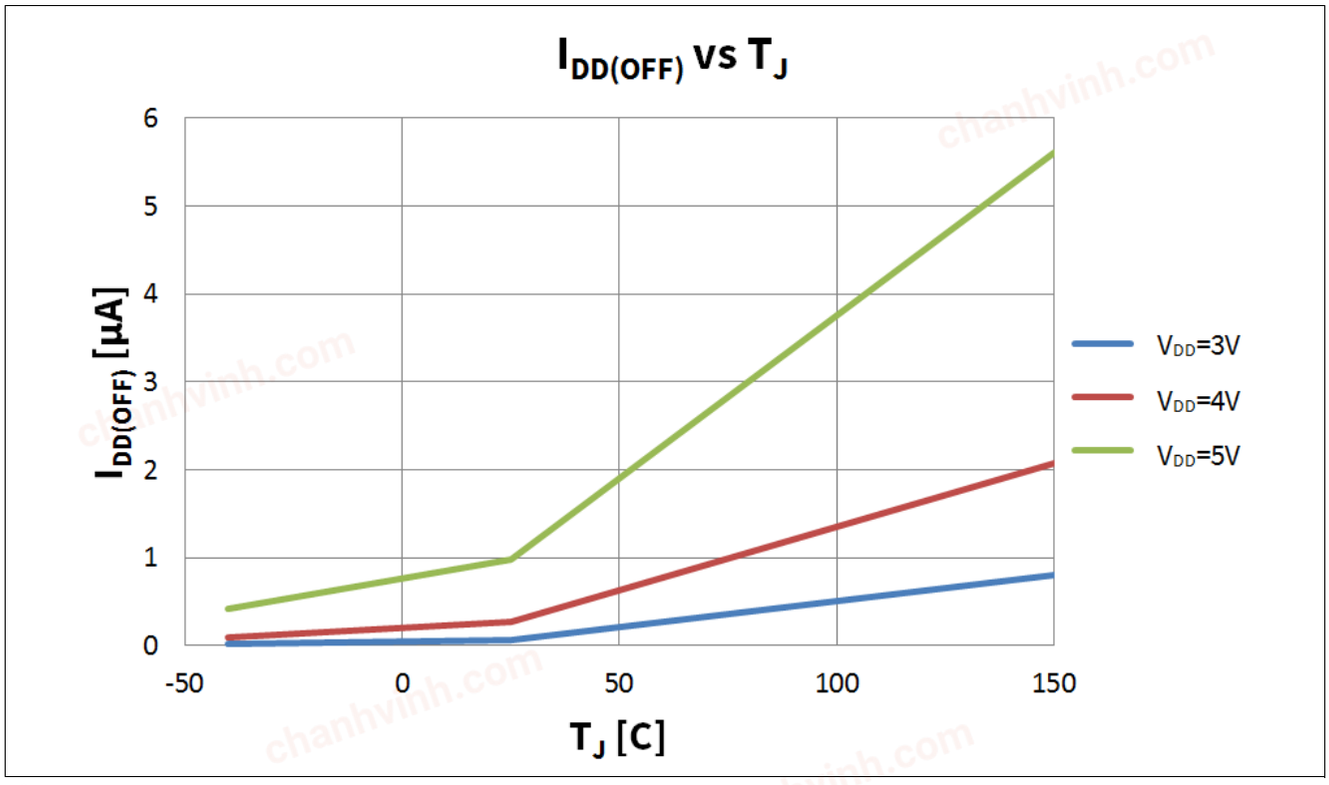


Figure 47 $I_{DD(OFF)}$ vs. T_J @ V_{DD} = 3, 4, 5V; V_{IN} = V_{ENABLE} = 0V;

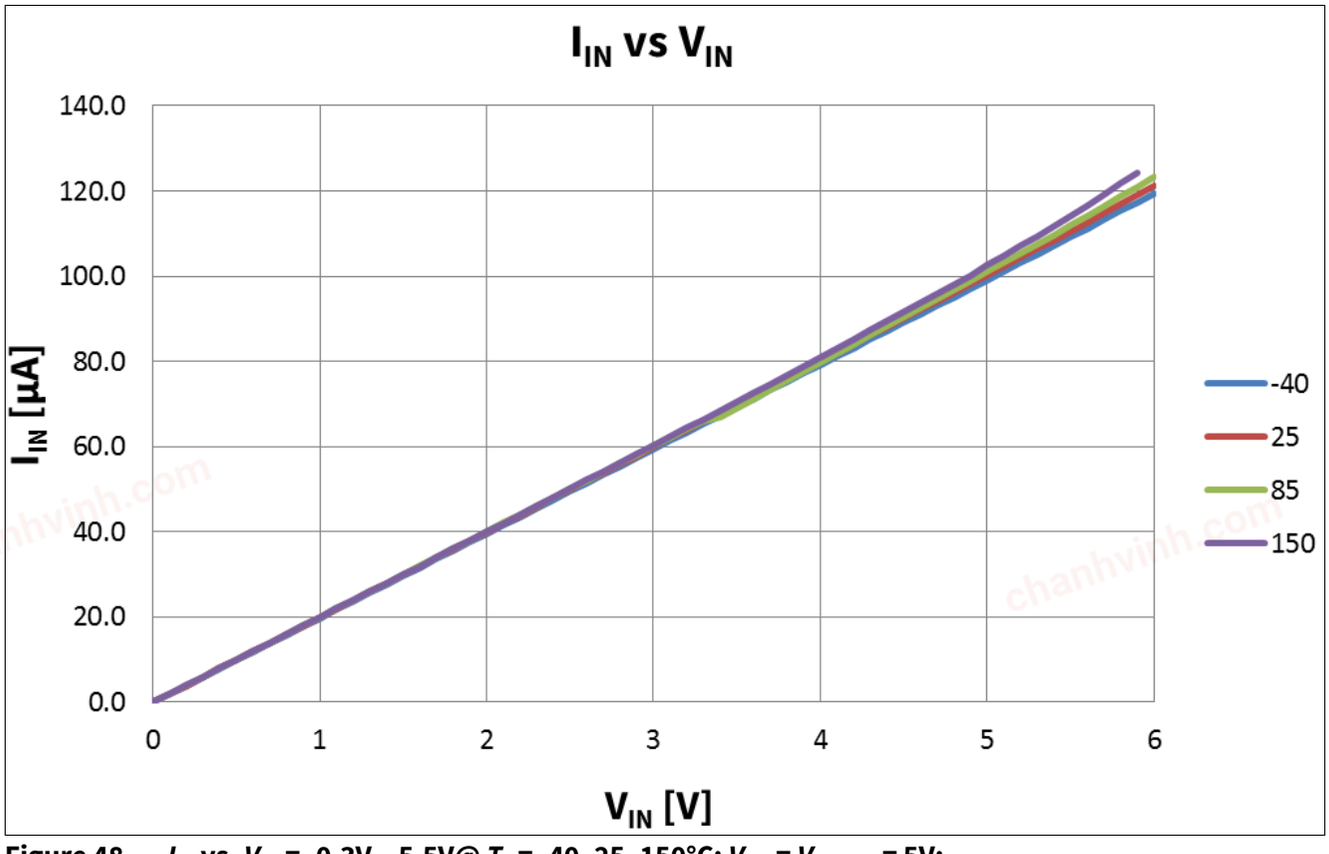


Figure 48 I_{IN} vs. V_{IN} = -0.3V...5.5V@ T_J = -40, 25, 150°C; V_{DD} = V_{ENABLE}= 5V;

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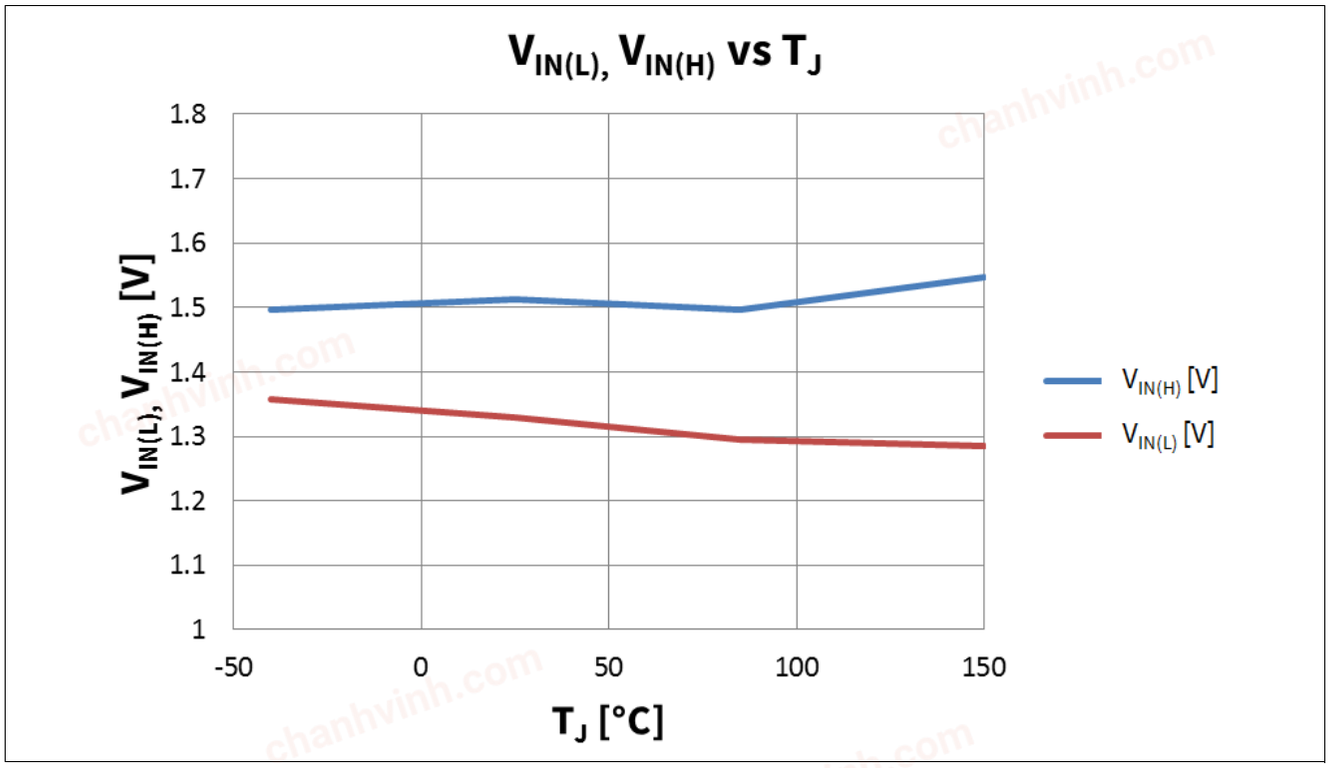


Figure 49 $V_{IN(L)}$, $V_{IN(H)}$ vs. T_J @ V_{DD} = 5V; V_{ENABLE}= 5V; I_L= *1.4 mA*; R_{SRP}= 0Ω; V_{IN}= 0V...5.5V; V_{BAT}= 13.5V;

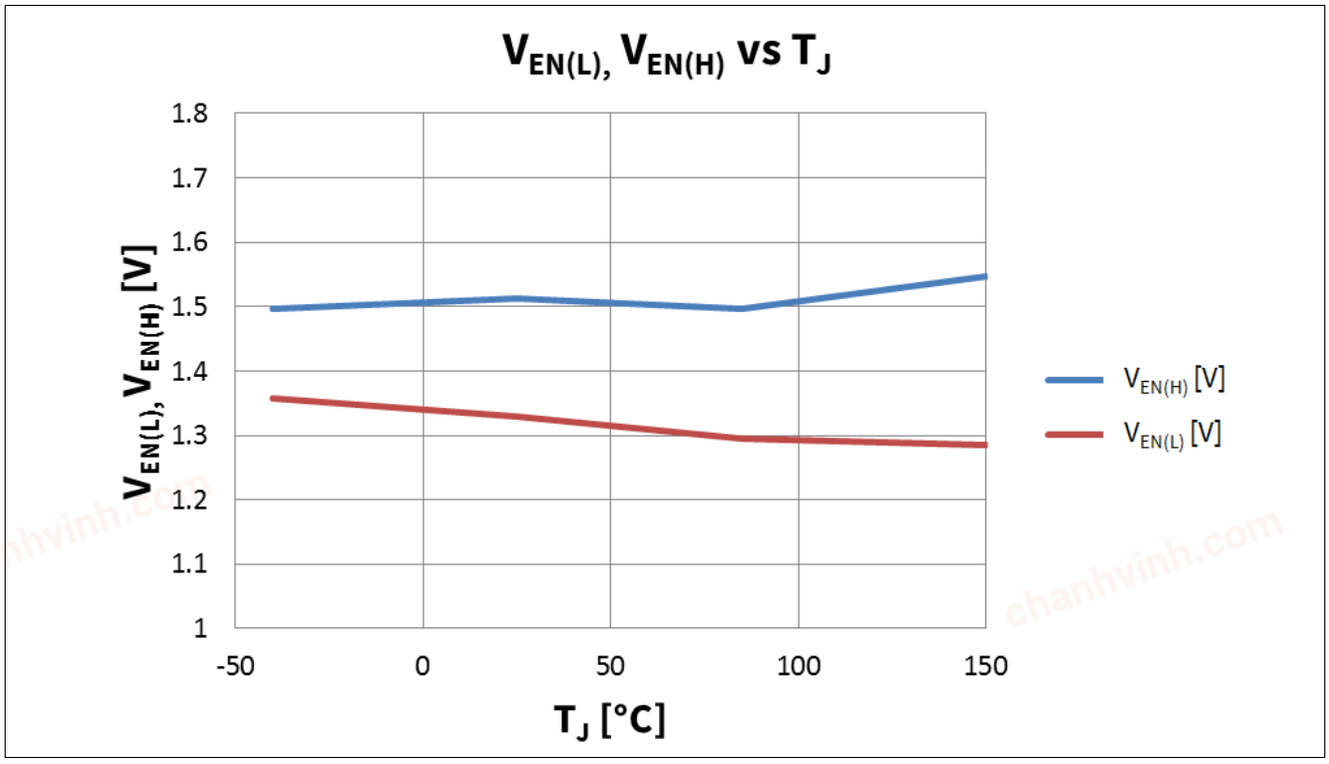


Figure 50 $V_{EN(L)}$, $V_{EN(H)}$ vs. T_J @ V_{DD} = 5V; V_{BAT}= 13.5V; I_L= 1.4mA; R_{SRP}= 0Ω; V_{EN}= 0V...5.5V; V_{BAT}= 13.5V;

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11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Application Diagram

An application example with the BTF3050EJ is shown below.

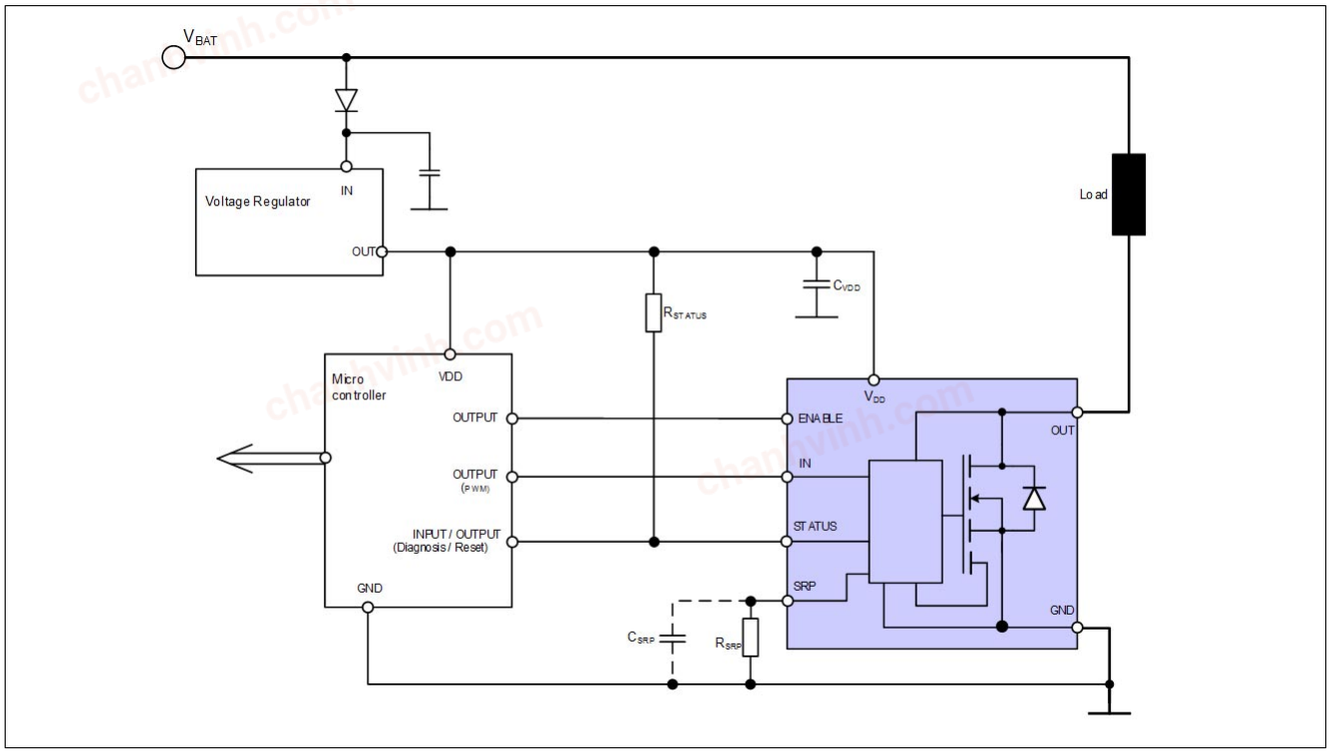


Figure 51 Simplified application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 9 Pin description for simplified application diagram

Reference	Value	Purpose
R_{STATUS}	4.7kΩ	Pulls-up the STATUS pin
R_{SRP}	kΩ	SRP resistor
$C_{SRP-GND}$	< 100pF	maximum permitted parasitic capacitance at the SRP pin
C_{VDD}	100nF	Filter capacitor on supply pin

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11.1 Design and Layout Recommendations/Considerations

As consequence of the fast switching times for high currents, special care has to be taken to the PCB layout. Stray inductances have to be minimized. The BTF3050EJ has no separate pin for power ground and logic ground. Therefore it is recommended to assure that the offset between the ground connection of the slew rate resistor and ground pin of the device (GND/SOURCE) is minimized. The resistor R_{SRP} should be placed near to the device and directly connected to the GND pin of the device to avoid any influence of GND shift to the functionality of the SRP pin.

In order to avoid influence on SRP functionality (e.g. switching times..) the maximum capacitance on SRP pin to GND ($C_{SRP-GND}$) has to be less than 100pF. This has to be considered by a proper layout also taking into account of parasitic capacitors.

It is recommended not to let the SRP pin floating. A maximum resistor of 200 kOhm to GND is recommended.

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12 Package information

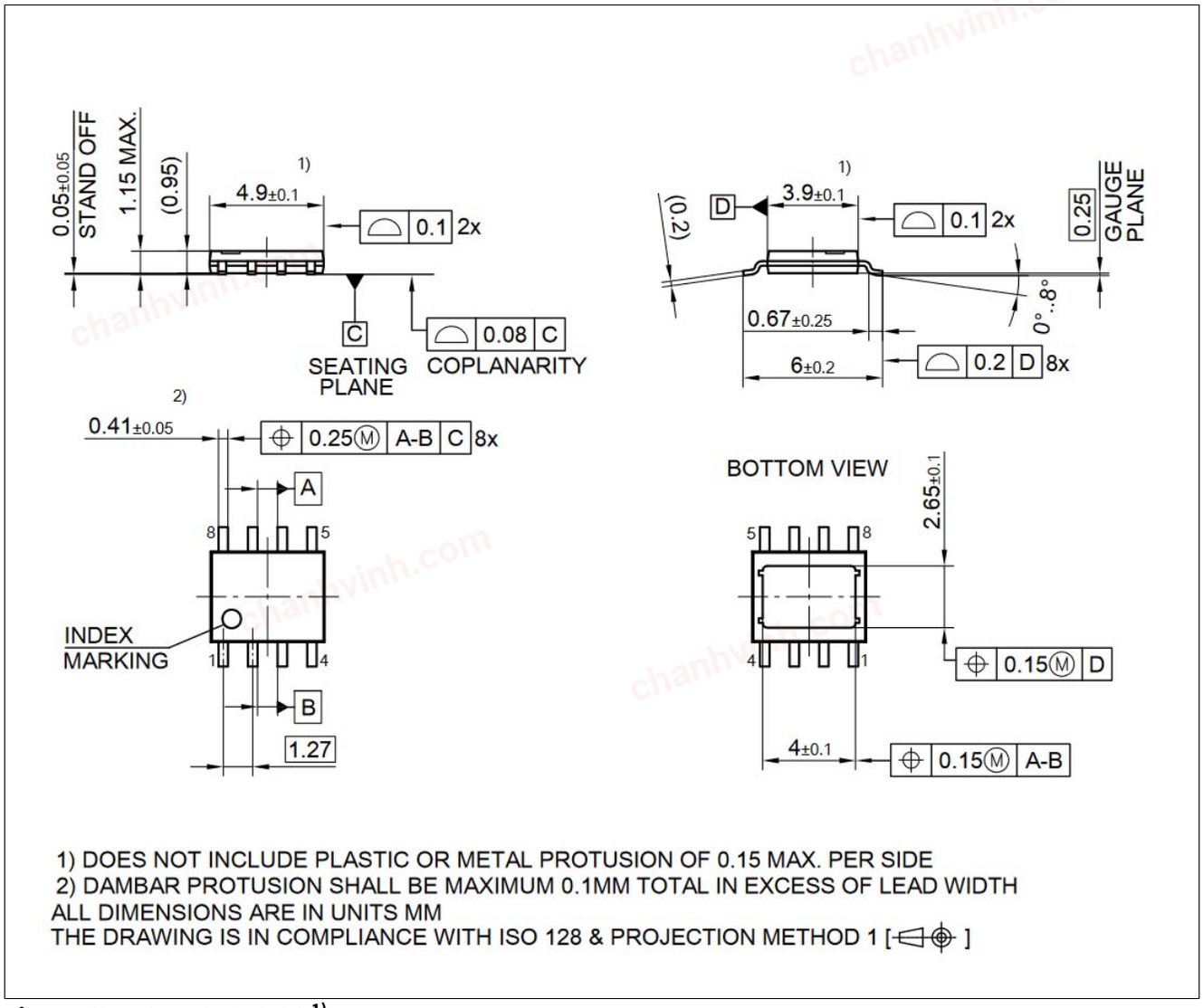


Figure 52 PG-TDSO-8-31 [1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimension in mm

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13 Revision History

Revision	Date	Changes
Rev. 1.0	2018-08-08	First Release

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