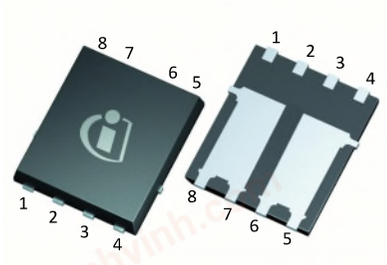
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MOSFET

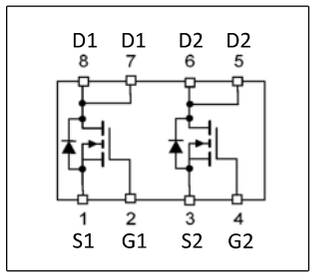
OptiMOS™-T2 Power Transistor, 60 V

TDSON-8-4 (SSO8 dual)



Features

· Dual N-channel,Normal Level
· Fast switching MOSFETs
· 175°C operating temperature
· Green product (RoHS compliant)
· 100% Avalanche tested
· Optimized technology for drives applications
· Halogen-free according to IEC61249-2-21
· Superior thermal resistance



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	15.5	mΩ
I_D	42	A

Type / Ordering Code	Package	Marking	Related Links
BSC155N06ND	PG-TDSON-8-4	155N06ND	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified, one transistor active

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	-	-	42	A	V_{GS}=10 V, T_C=25 °C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	168	A	T_A=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	40	mJ	I_D=10 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	50	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	3	°C/W	-
Device on PCB, 6 cm² cooling area[4]	R_{thJA}	-	-	60	°C/W	-
Device on PCB, minimal footprint[5]	R_{thJA}	-	-	100	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information
[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[5] device mounted on a minimum pad (one layer, 70 µm thick)

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3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V_{DS}=V_{GS}, I_D=20 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	12.9	15.5	mΩ	V_{GS}=10 V, I_D=17 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1730	2250	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	380	490	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	15	30	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω
Rise time	t_r	-	2	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω
Turn-off delay time	$t_{d(off)}$	-	19	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω
Fall time	t_f	-	9	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge[1)]	Q_{gs}	-	9	12	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate to drain charge[1)]	Q_{gd}	-	2.0	4	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total[1)]	Q_g	-	21	29	nC	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V

[1)] Defined by design. Not subject to production test.
[2)] See "Gate charge waveforms" for parameter definition

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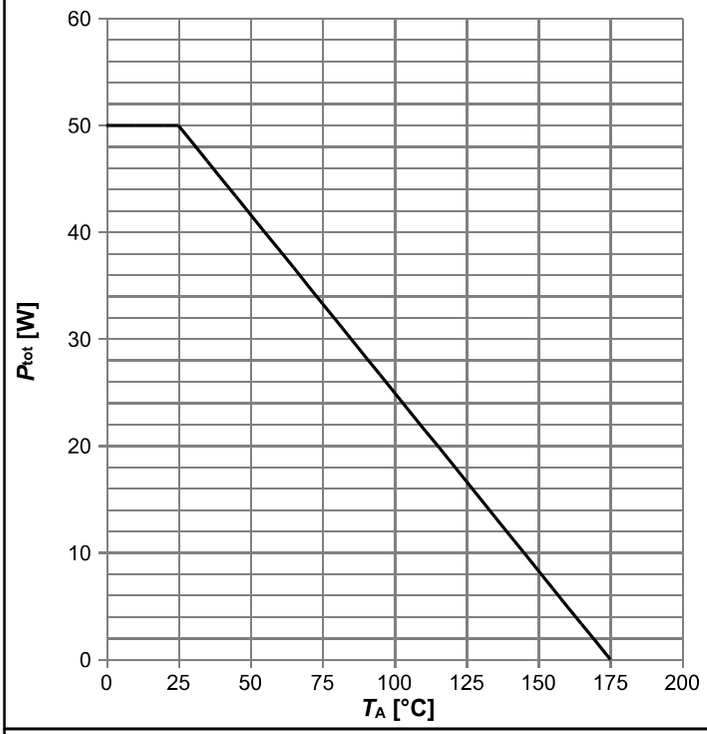
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	34	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	168	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.91	1.1	V	V_{GS}=0 V, I_F=17 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	35	-	ns	V_R=15 V, I_F=9 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	35	-	nC	V_R=15 V, I_F=9 A, di_F/dt=100 A/µs

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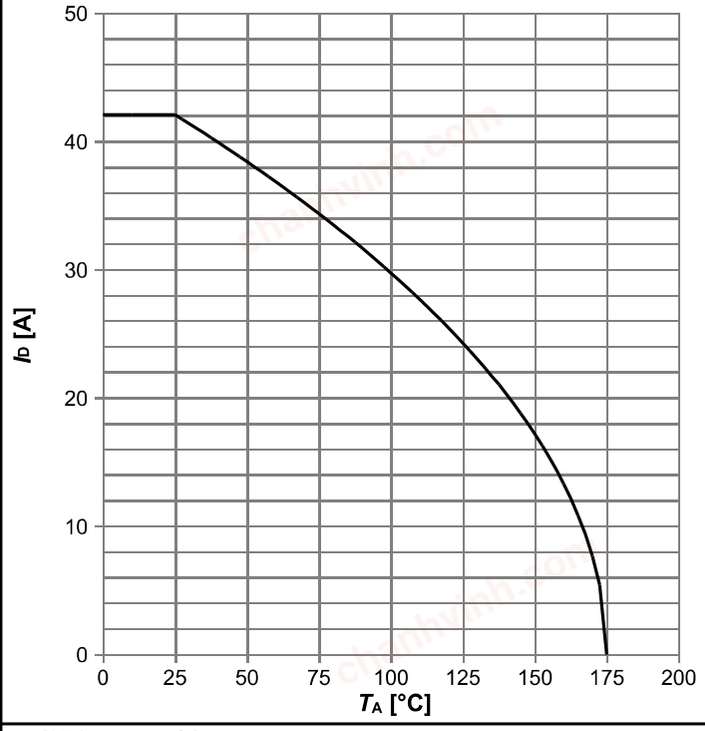
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



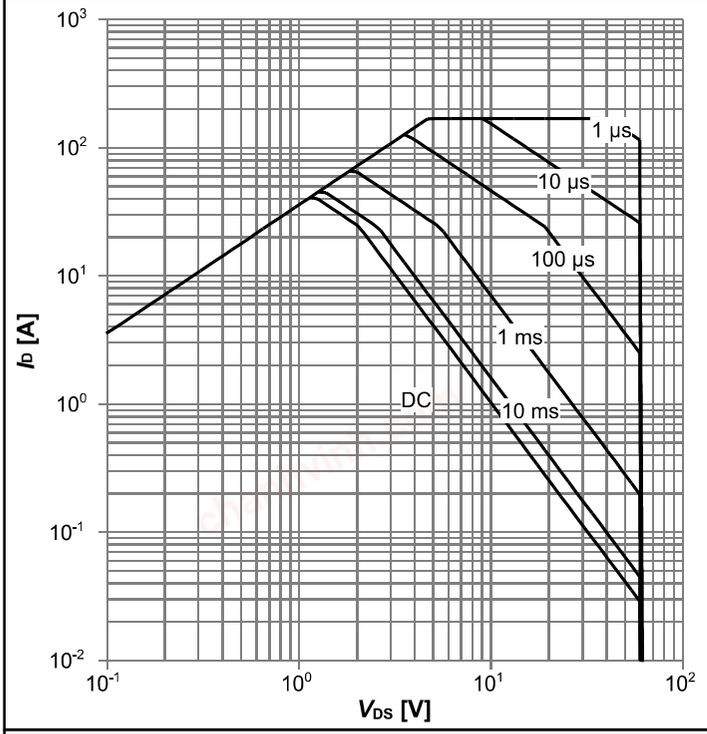
$P_{tot}=f(T_A)$, minimal footpint

Diagram 2: Drain current



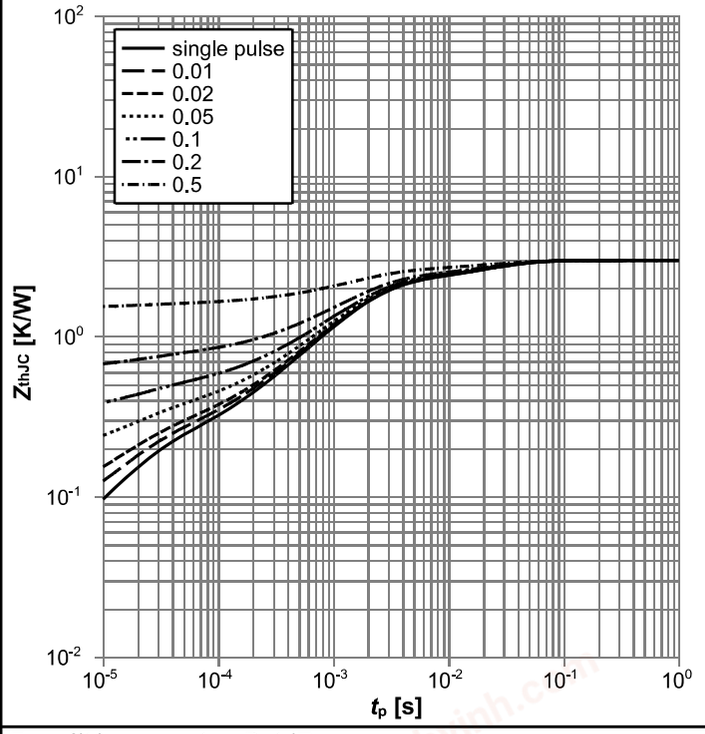
$I_D=f(T_A)$; minimal footpint

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

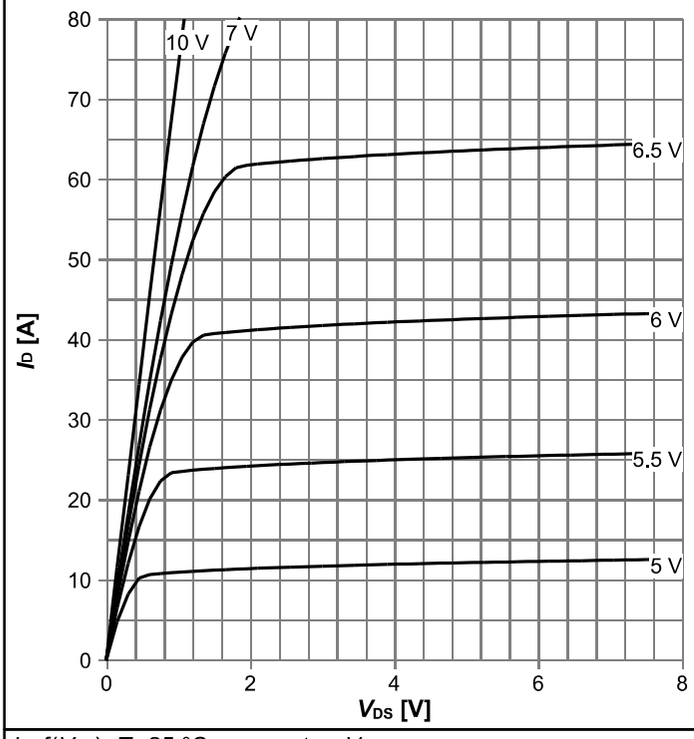
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

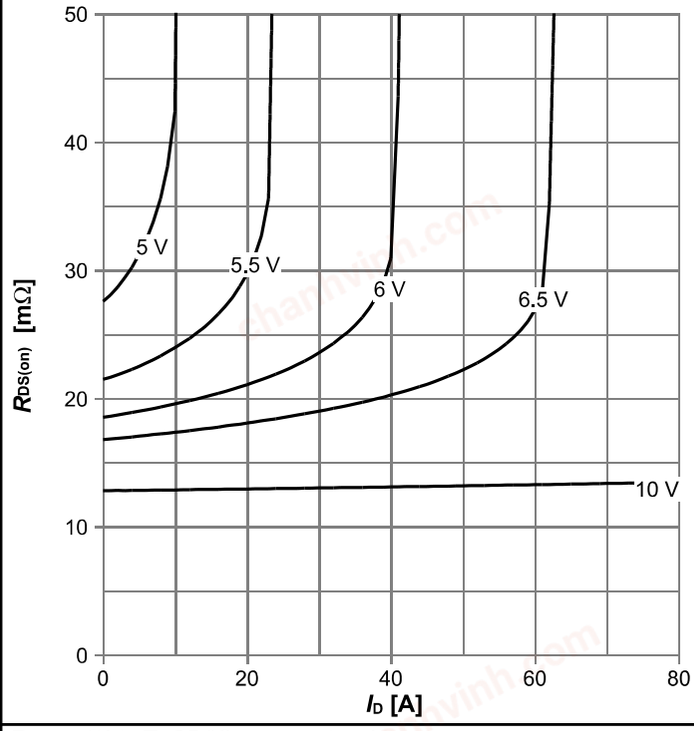
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Diagram 5: Typ. output characteristics



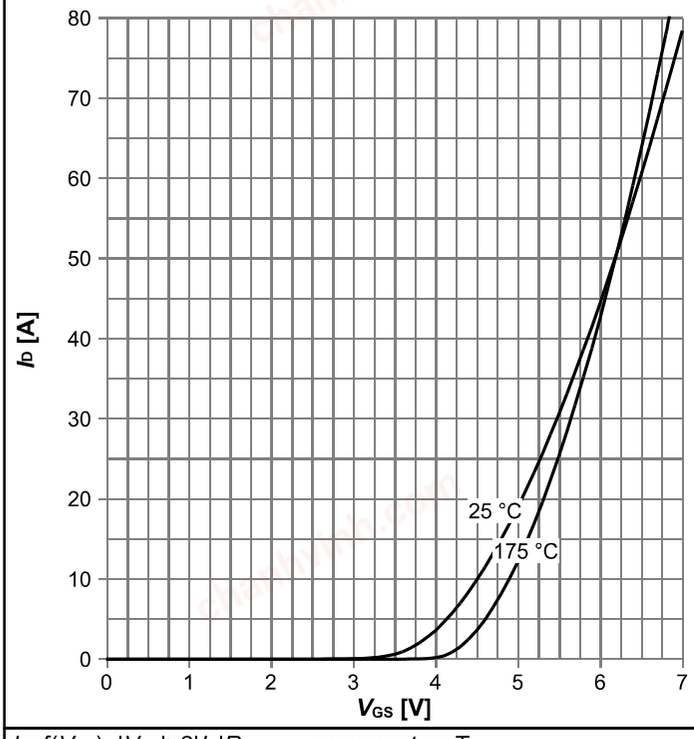
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



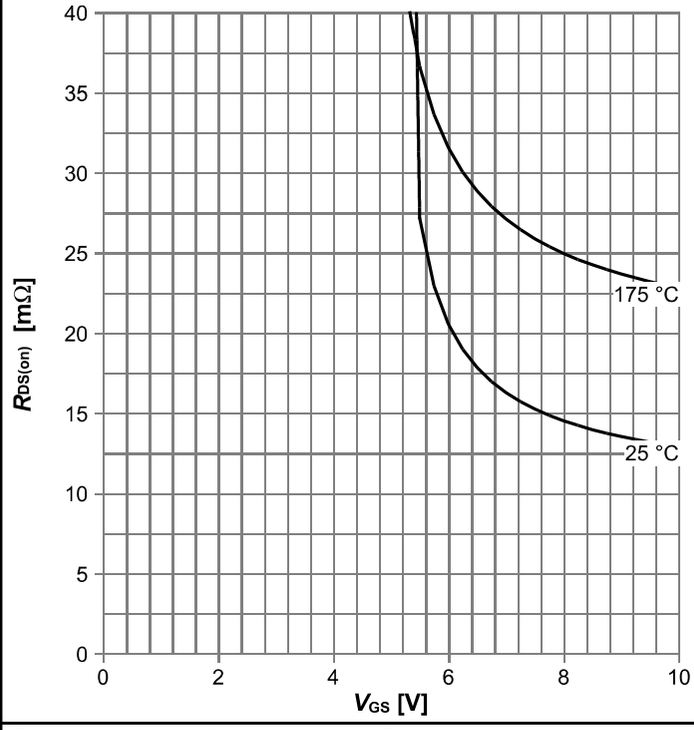
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

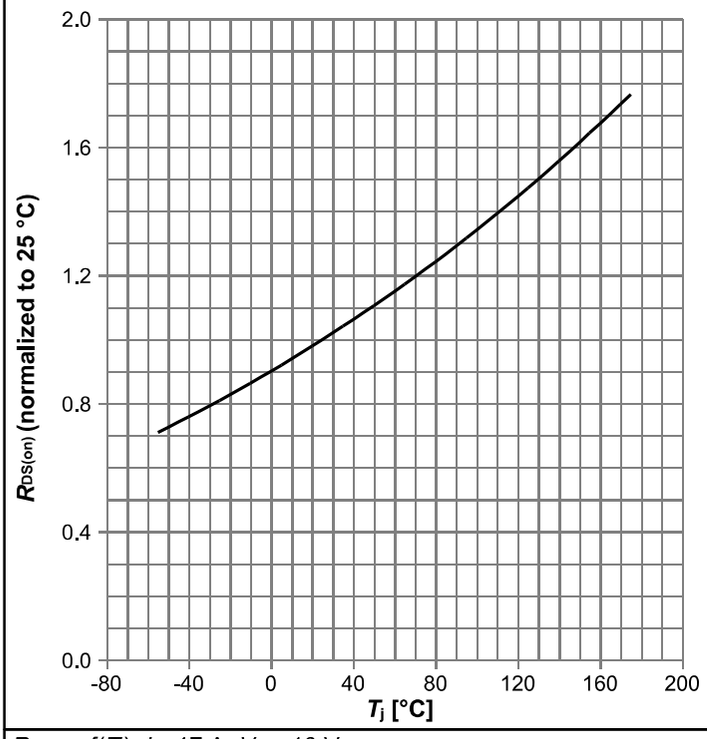
Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}=f(V_{GS})$, $I_D=17$ A; parameter: T_j

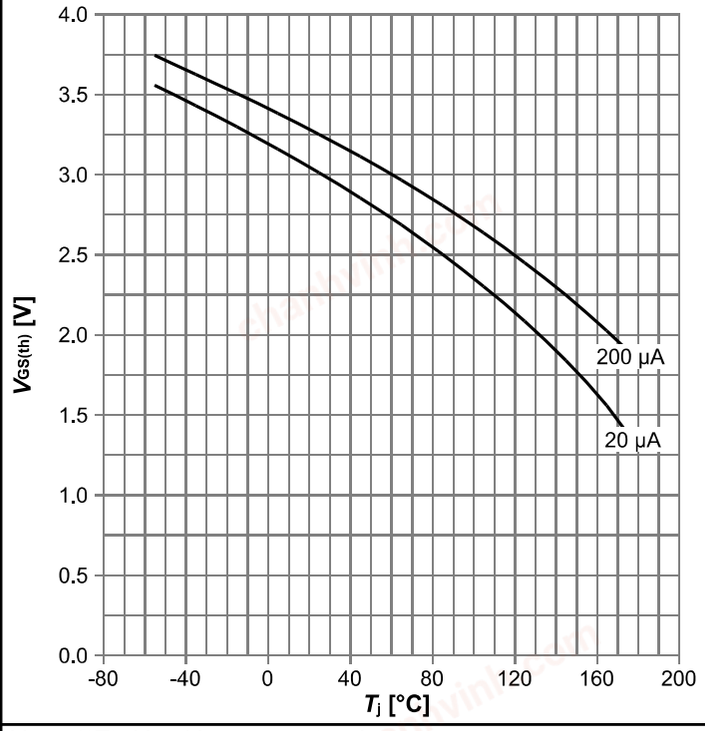
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Diagram 9: Normalized drain-source on resistance



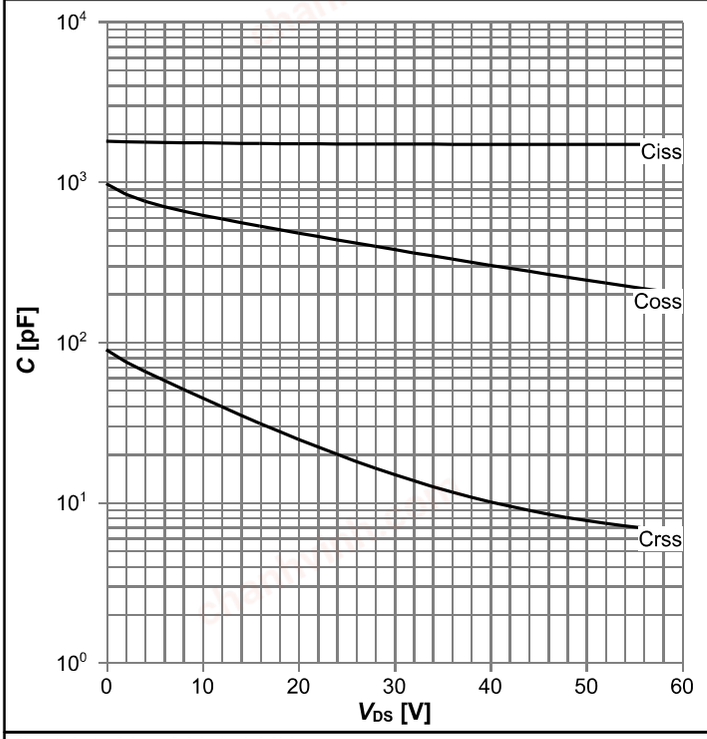
$R_{DS(on)}$=f(T_j), I_D=17 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



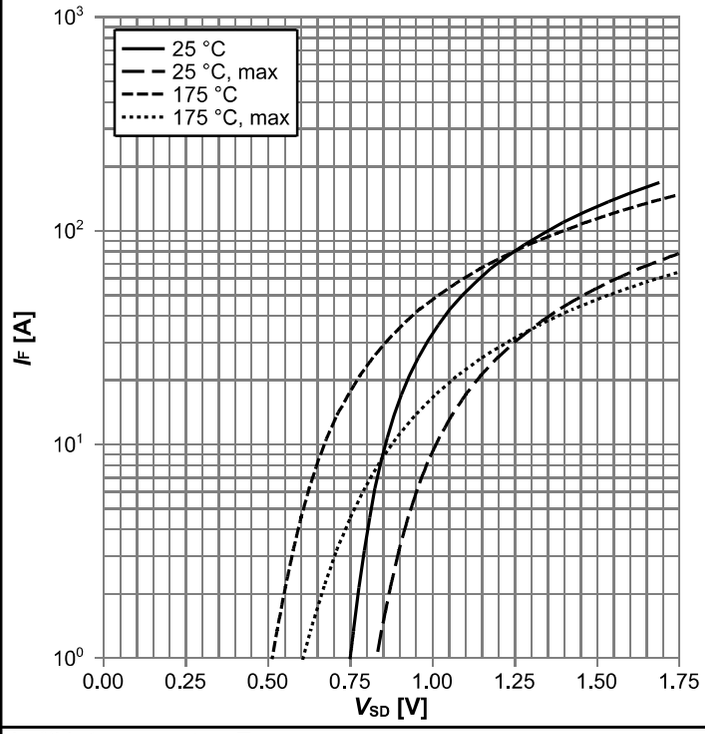
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

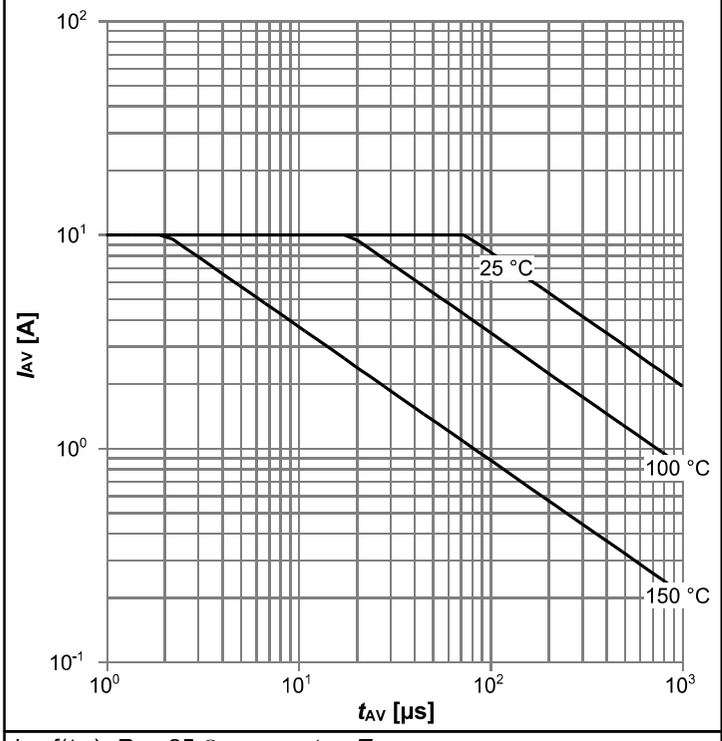
Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

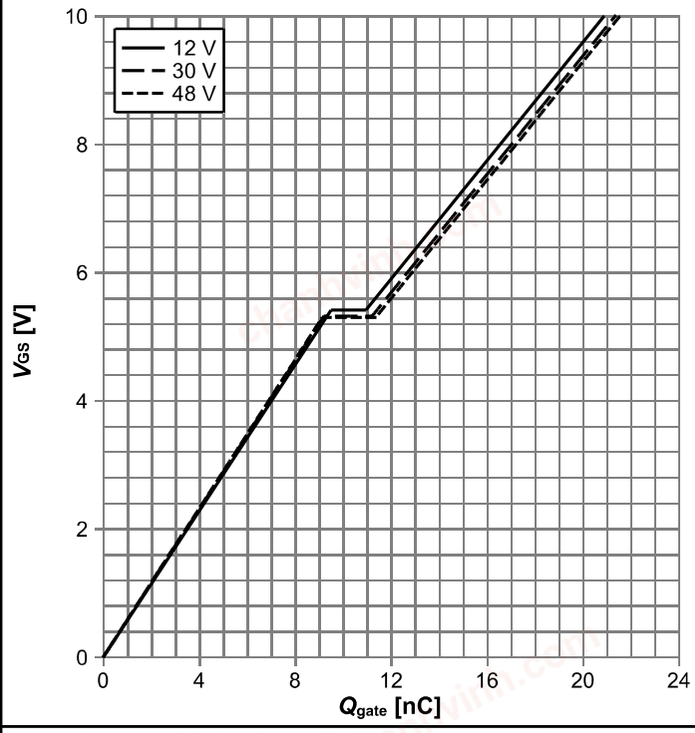
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Diagram 13: Avalanche characteristics



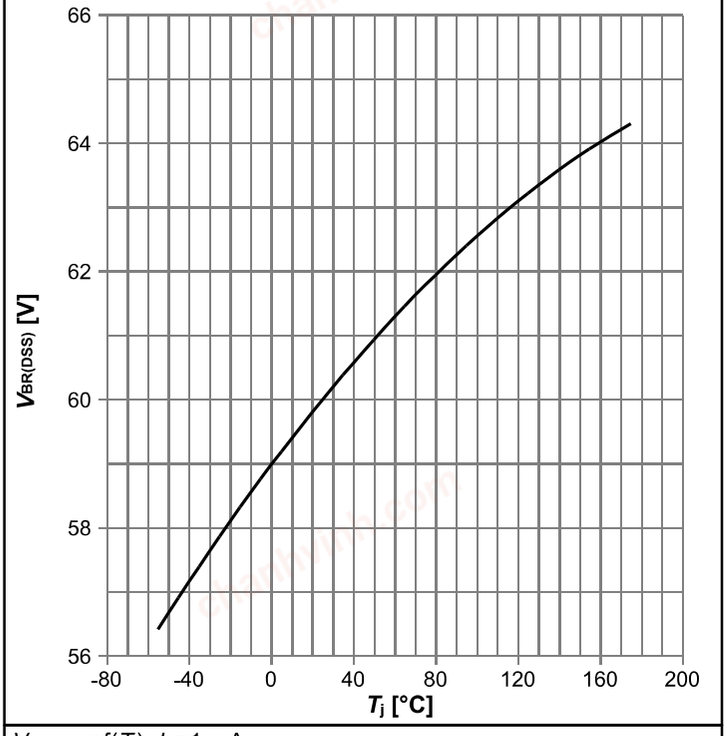
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



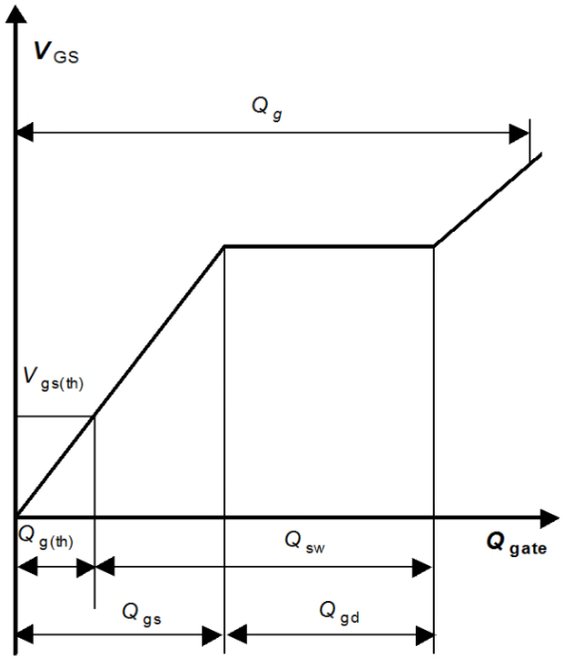
$V_{GS}=f(Q_{gate})$, $I_D=20$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



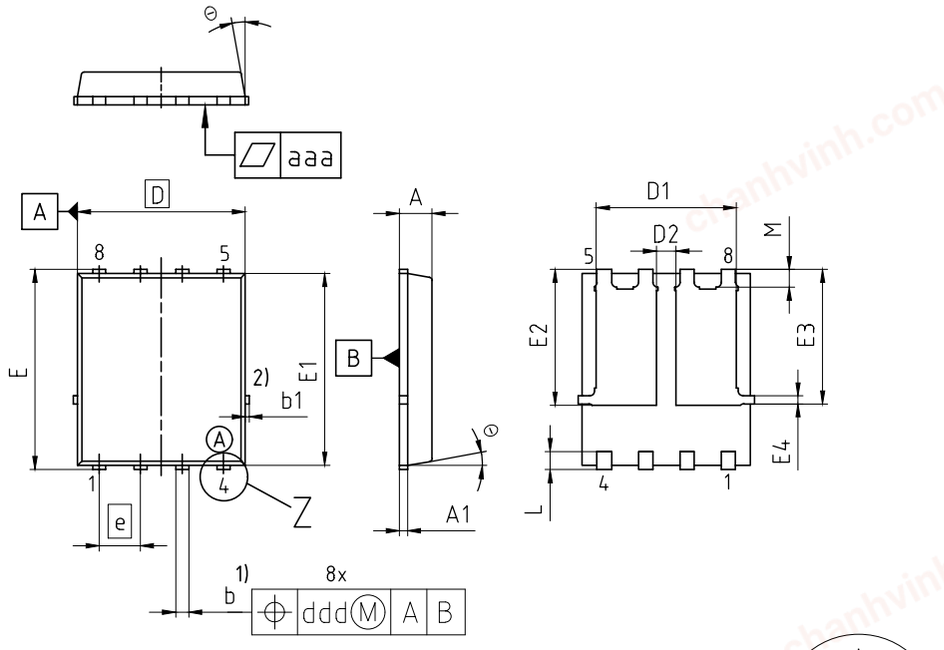
$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

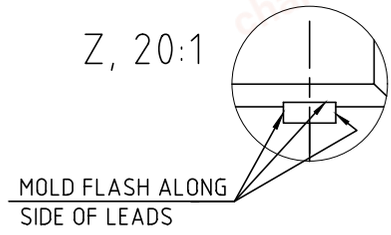
Diagram Gate charge waveforms



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5 Package Outlines





1) EXCLUDE MOLD FLASH

2) REMOVAL ON MOLD GATE, INTRUSION 0.1 mm
PROTRUSION 0.1 mm

ALL METAL SURFACES ARE PLATED EXCEPT AREA OF CUT

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
A1	0.15	0.35
b	0.34	0.54
b1	0.02	0.22
D	4.95	5.35
D1	4.20	4.40
D2	0.50	0.70
E	5.95	6.35
E1	5.70	6.10
E2	4.075	4.275
E3	4.035	4.235
E4	0.15	0.35
e	1.27	
L	0.45	0.65
M	0.45	0.65
⊖	8.5°	11.5°
aaa	0.05	
ddd	0.10	

DOCUMENT NO. Z8B00189767
REVISION 01
SCALE 5:1 0 1 2 3 4mm
EUROPEAN PROJECTION
ISSUE DATE 31.07.2018

Figure 1 Outline PG-TDSON-8-4, dimensions in mm

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Revision History

BSC155N06ND

Revision: 2021-06-28, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-12-11	Release of final version
2.1	2021-06-28	Update current rating and footnotes

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