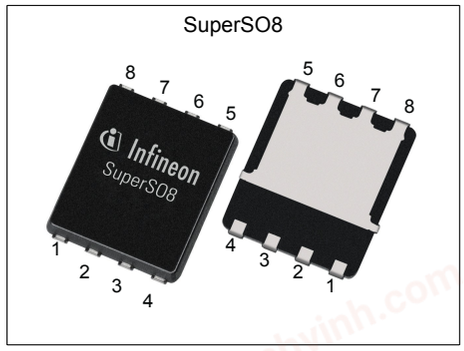
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# MOSFET

## OptiMOS™ 5 Power-Transistor, 100 V

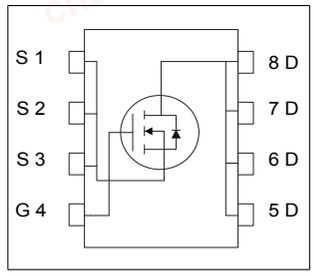



### Features

- Optimized for high performance SMPS, e.g. sync. Rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product validation

Qualified according to JEDEC Standard




### Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 100 | V |
| $R_{DS(on),max}$ | 14.6 | mΩ |
| $I_D$ | 44 | A |
| $Q_{oss}$ | 20 | nC |
| $Q_G$(0V..4.5V) | 7.6 | nC |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| BSC0803LS | PG-TDSON-8 | 0803LS | - |

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# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current | $I_D$ | -<br>-<br>- | -<br>-<br>- | 44<br>28<br>10 | A | $V_{GS}$=10 V, $T_C$=25 °C<br>$V_{GS}$=10 V, $T_C$=100 °C<br>$V_{GS}$=10 V, $T_A$=25 °C, $R_{THJA}$=50 °C/W[1] |
| Pulsed drain current[2] | $I_{D,pulse}$ | - | - | 176 | A | $T_A$=25 °C |
| Avalanche energy, single pulse[3] | $E_{AS}$ | - | - | 30 | mJ | $I_D$=20 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | -<br>- | -<br>- | 52<br>2.5 | W | $T_C$=25 °C<br>$T_A$=25 °C, $R_{THJA}$=50 °C/W[2] |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 150 | °C | IEC climatic category; DIN IEC 68-1: 55/150/56 |

# 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | 1.4 | 2.4 | °C/W | - |
| Device on PCB, 6 cm² cooling area[1] | $R_{thJA}$ | - | - | 50 | °C/W | - |

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information

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# 3 Electrical characteristics

at $T_j$=25 °C, unless otherwise specified

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 100 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 1.1 | 1.7 | 2.3 | V | $V_{DS}$=$V_{GS}$, $I_D$=23 µA |
| Zero gate voltage drain current | $I_{DSS}$ | -<br>- | 0.1<br>10 | 1<br>100 | µA | $V_{DS}$=100 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=100 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 10 | 100 | nA | $V_{GS}$=20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | -<br>- | 12.2<br>15.8 | 14.6<br>20.8 | mΩ | $V_{GS}$=10 V, $I_D$=22 A<br>$V_{GS}$=4.5 V, $I_D$=11 A |
| Gate resistance[1)] | $R_G$ | - | 1 | 1.5 | Ω | - |
| Transconductance | $g_{fs}$ | 19 | 38 | - | S | $\lvert V_{DS}\rvert \geq 2 \lvert I_D\rvert R_{DS(on)max}$, $I_D$=22 A |

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance[1)] | $C_{iss}$ | - | 1000 | 1300 | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Output capacitance[1)] | $C_{oss}$ | - | 170 | 220 | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Reverse transfer capacitance[1)] | $C_{rss}$ | - | 9 | 15 | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 5 | - | ns | $V_{DD}$=50 V, $V_{GS}$=10 V, $I_D$=22 A, $R_{G,ext}$=3 Ω |
| Rise time | $t_r$ | - | 3 | - | ns | $V_{DD}$=50 V, $V_{GS}$=10 V, $I_D$=22 A, $R_{G,ext}$=3 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 14 | - | ns | $V_{DD}$=50 V, $V_{GS}$=10 V, $I_D$=22 A, $R_{G,ext}$=3 Ω |
| Fall time | $t_f$ | - | 3 | - | ns | $V_{DD}$=50 V, $V_{GS}$=10 V, $I_D$=22 A, $R_{G,ext}$=3 Ω |

## Table 6 Gate charge characteristics[2)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 3.3 | - | nC | $V_{DD}$=50 V, $I_D$=22 A, $V_{GS}$=0 to 4.5 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | 1.7 | - | nC | $V_{DD}$=50 V, $I_D$=22 A, $V_{GS}$=0 to 4.5 V |
| Gate to drain charge[1)] | $Q_{gd}$ | - | 2.8 | 4.2 | nC | $V_{DD}$=50 V, $I_D$=22 A, $V_{GS}$=0 to 4.5 V |
| Switching charge | $Q_{sw}$ | - | 4.4 | - | nC | $V_{DD}$=50 V, $I_D$=22 A, $V_{GS}$=0 to 4.5 V |
| Gate charge total[1)] | $Q_g$ | - | 7.6 | 10 | nC | $V_{DD}$=50 V, $I_D$=22 A, $V_{GS}$=0 to 4.5 V |
| Gate plateau voltage | $V_{plateau}$ | - | 3.3 | - | V | $V_{DD}$=50 V, $I_D$=22 A, $V_{GS}$=0 to 4.5 V |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 13 | - | nC | $V_{DS}$=0.1 V, $V_{GS}$=0 to 10 V |
| Output charge[1)] | $Q_{oss}$ | - | 20 | 27 | nC | $V_{DS}$=50 V, $V_{GS}$=0 V |

[1)] Defined by design. Not subject to production test.
[2)] See "Gate charge waveforms" for parameter definition

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## Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | 47 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | - | - | 176 | A | $T_C$=25 °C |
| Diode forward voltage | $V_{SD}$ | - | 0.9 | 1.1 | V | $V_{GS}$=0 V, $I_F$=22 A, $T_j$=25 °C |
| Reverse recovery time[1)] | $t_{rr}$ | - | 26 | 52 | ns | $V_R$=50 V, $I_F$=22 A, d$i_F$/d$t$=100 A/µs |
| Reverse recovery charge[1)] | $Q_{rr}$ | - | 19 | 38 | nC | $V_R$=50 V, $I_F$=22 A, d$i_F$/d$t$=100 A/µs |

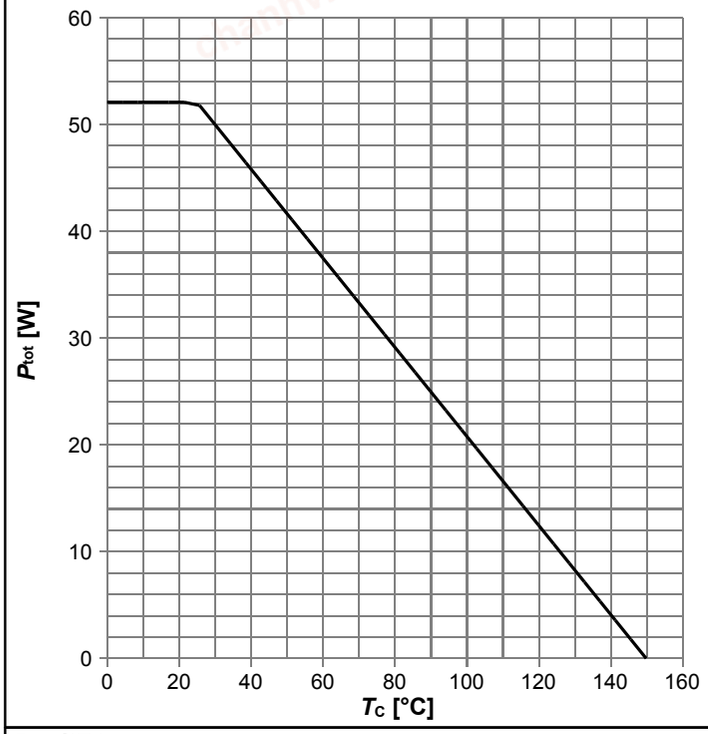
[1)] Defined by design. Not subject to production test.

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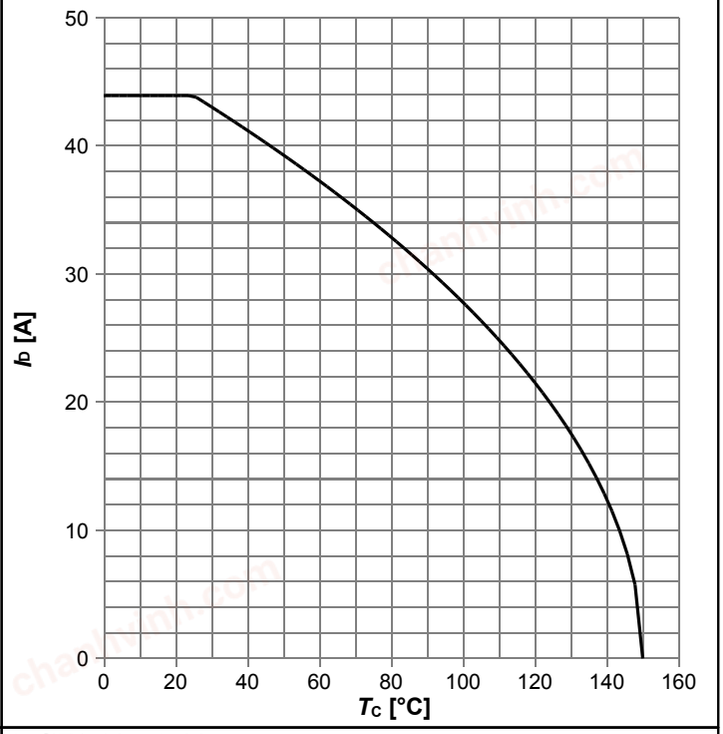
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



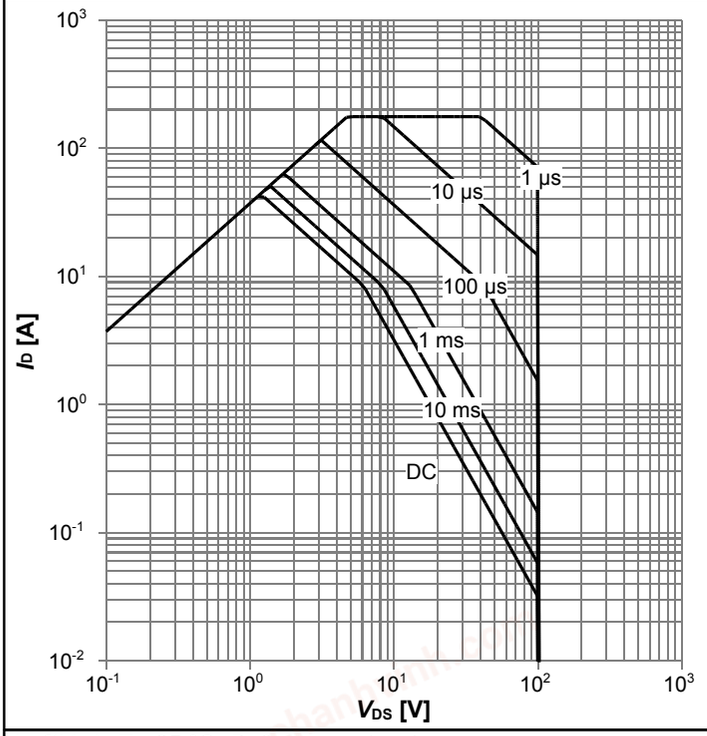

$P_{tot}=f(T_C)$

**Diagram 2: Drain current**



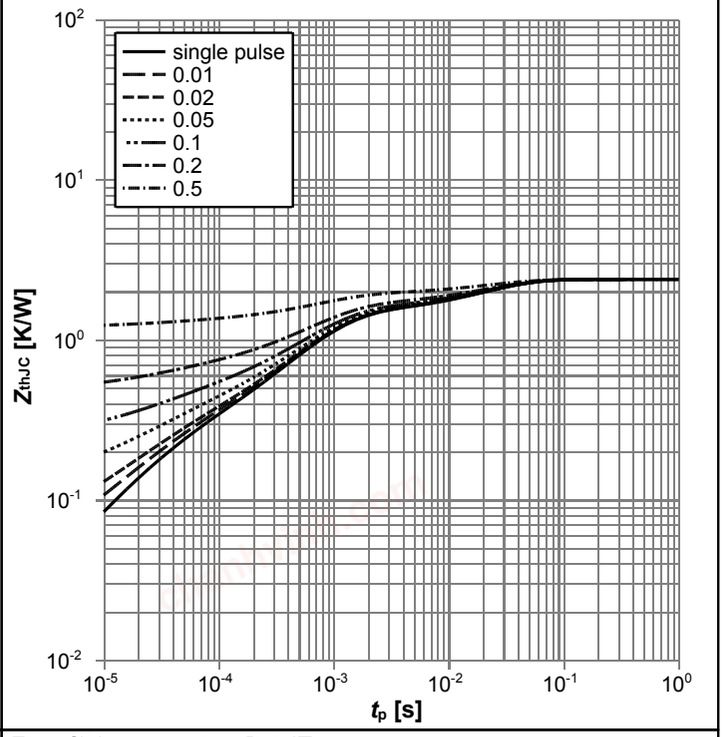

$I_D=f(T_C)$; $V_{GS}\geq 10$ V

**Diagram 3: Safe operating area**




$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**

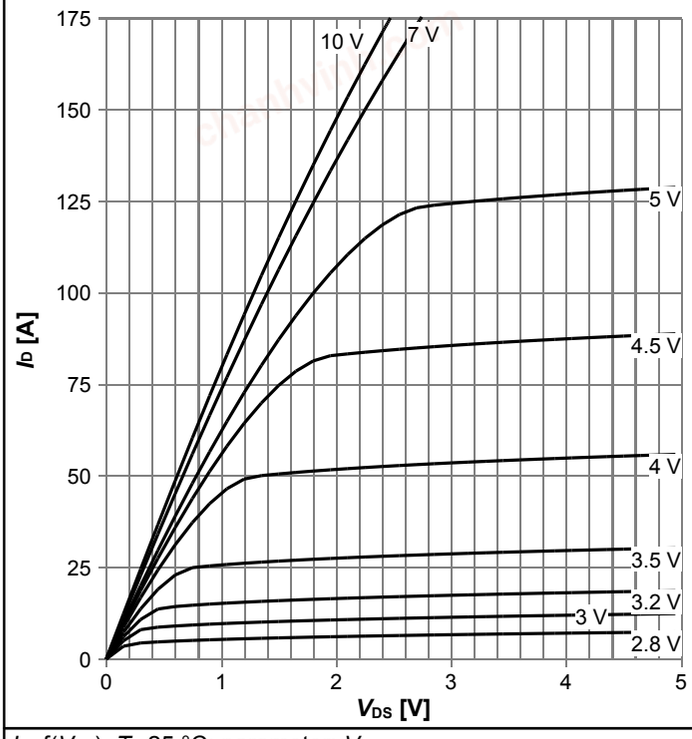



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

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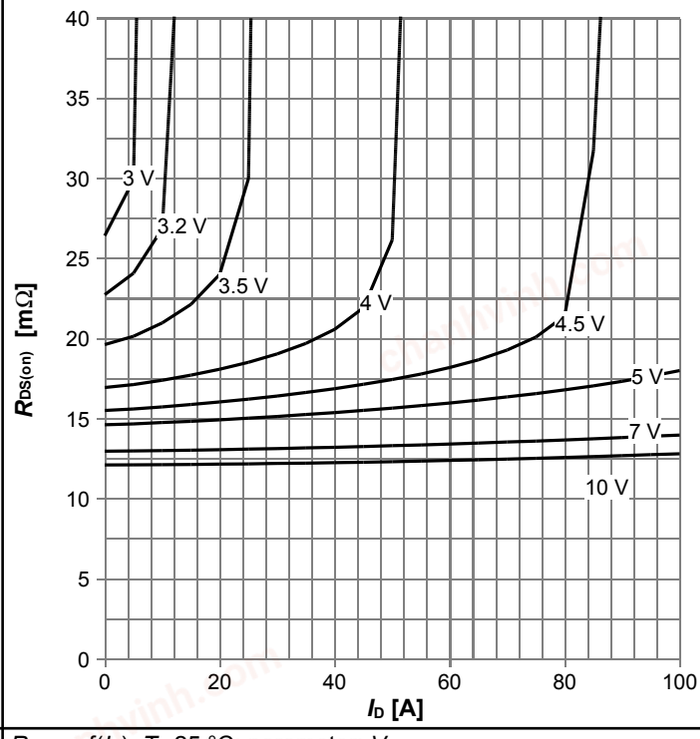


**Diagram 5: Typ. output characteristics**



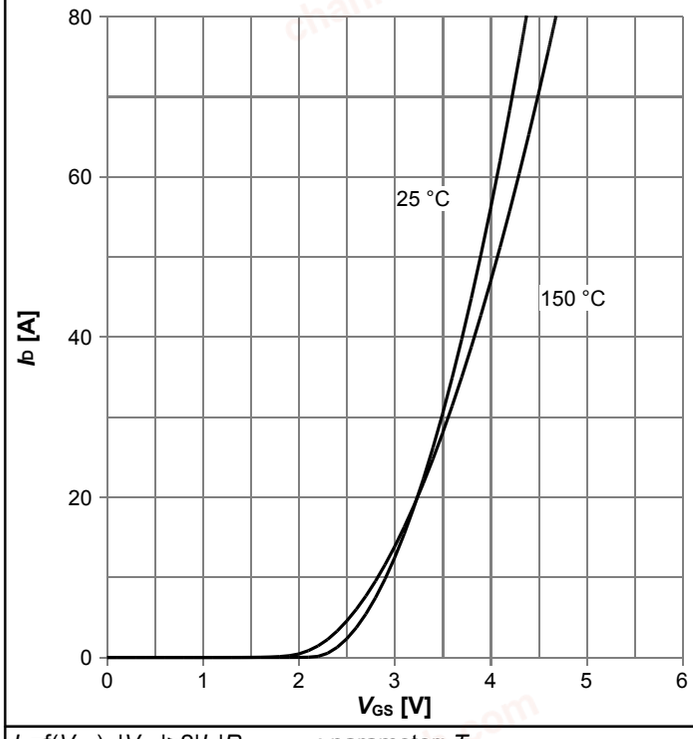

$I_D$=f($V_{DS}$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



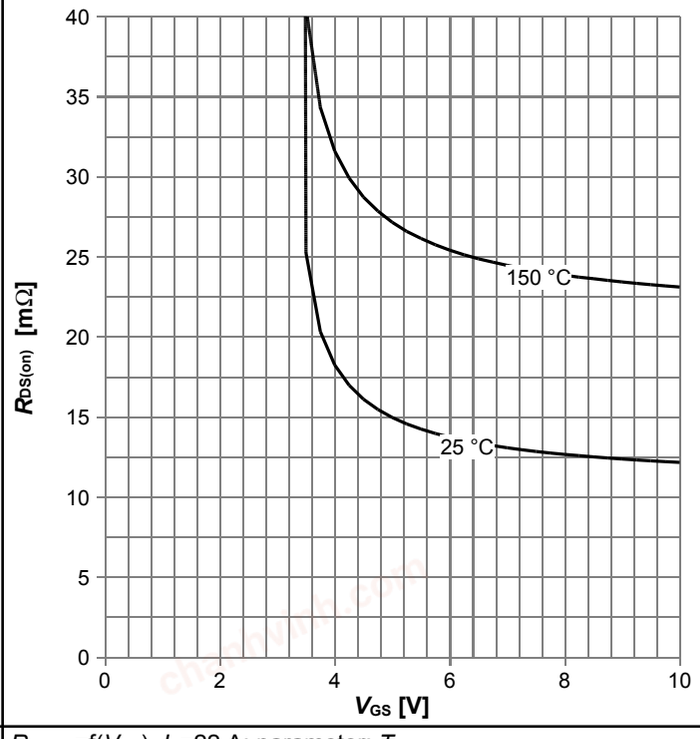

$R_{DS(on)}$=f($I_D$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**




$I_D$=f($V_{GS}$), |$V_{DS}$|>2|$I_D$|$R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. drain-source on resistance**

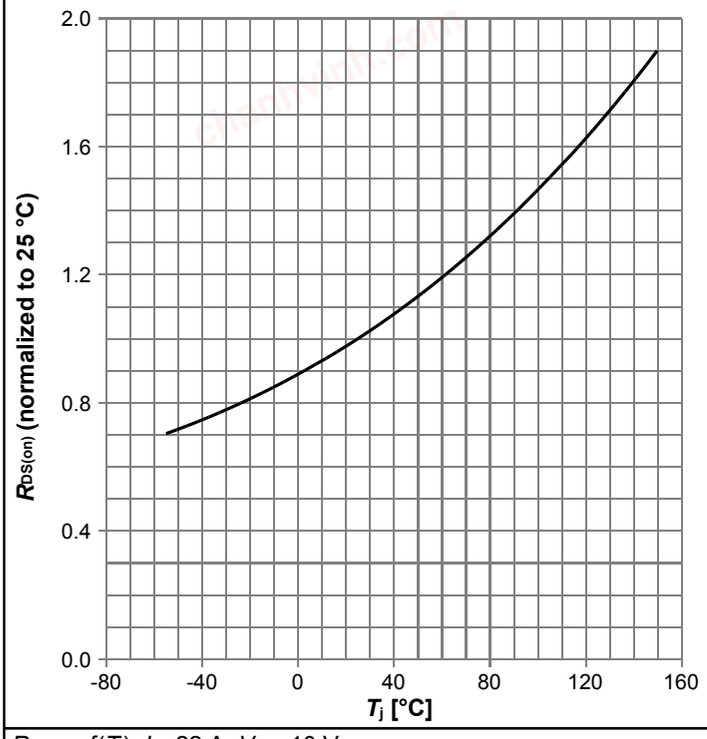



$R_{DS(on)}$=f($V_{GS}$), $I_D$=22 A; parameter: $T_j$

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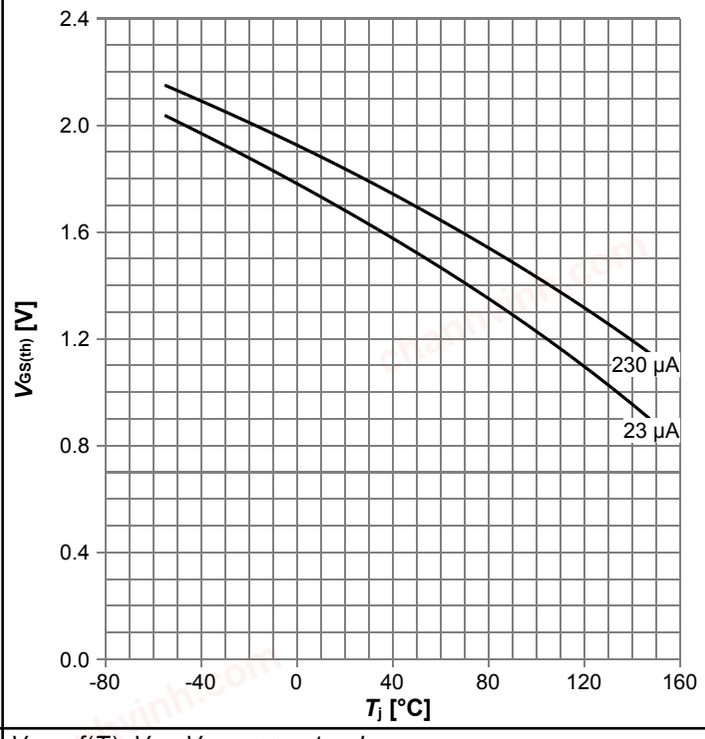


**Diagram 9: Normalized drain-source on resistance**



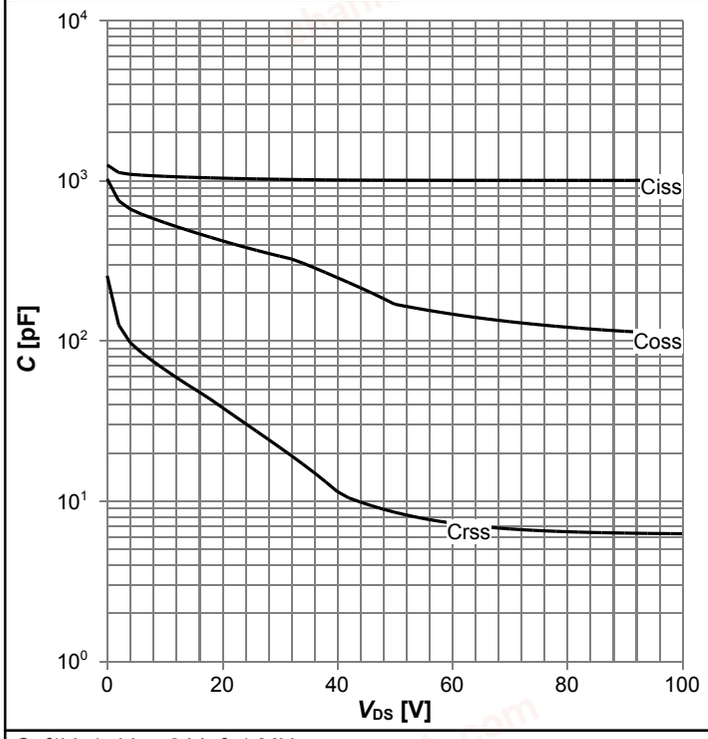

$R_{DS(on)}$=f($T_j$), $I_D$=22 A, $V_{GS}$=10 V

**Diagram 10: Typ. gate threshold voltage**



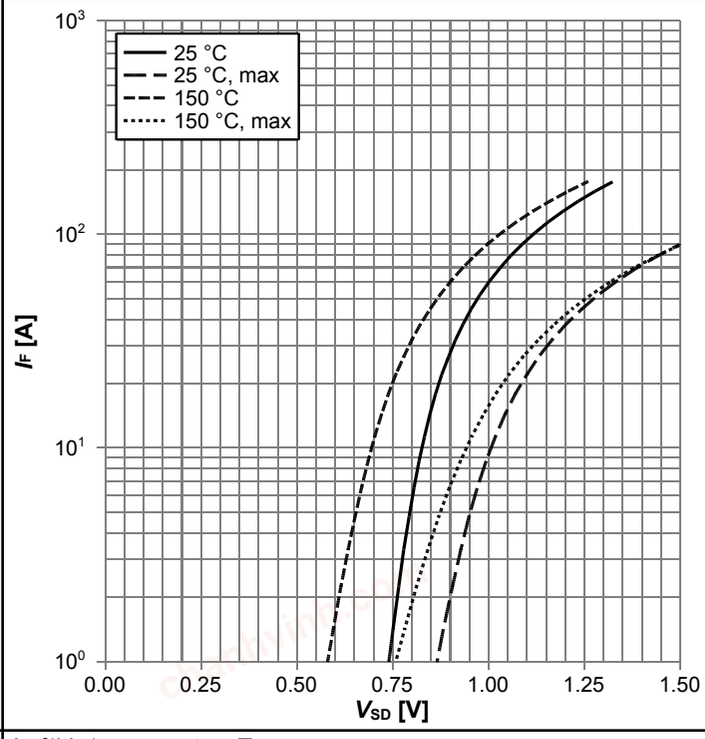

$V_{GS(th}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 11: Typ. capacitances**




$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Forward characteristics of reverse diode**

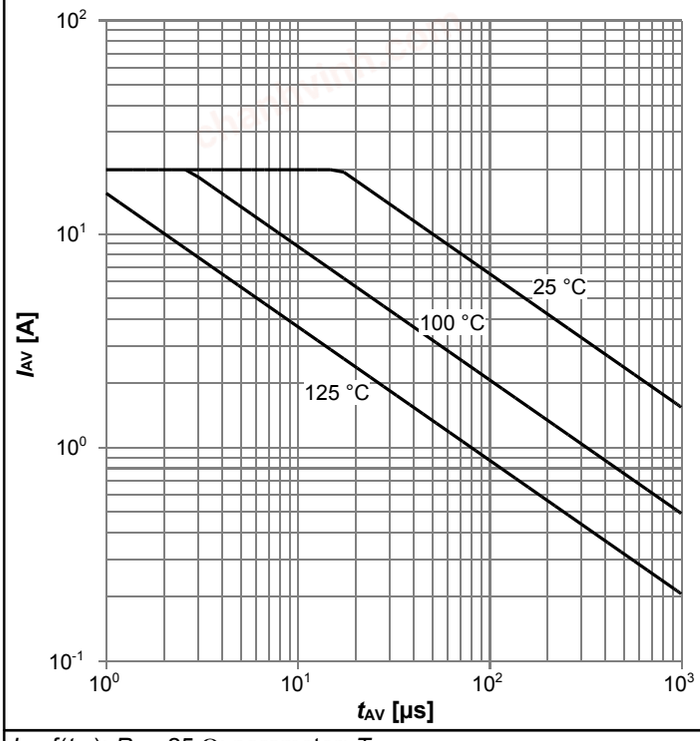



$I_F$=f($V_{SD}$); parameter: $T_j$

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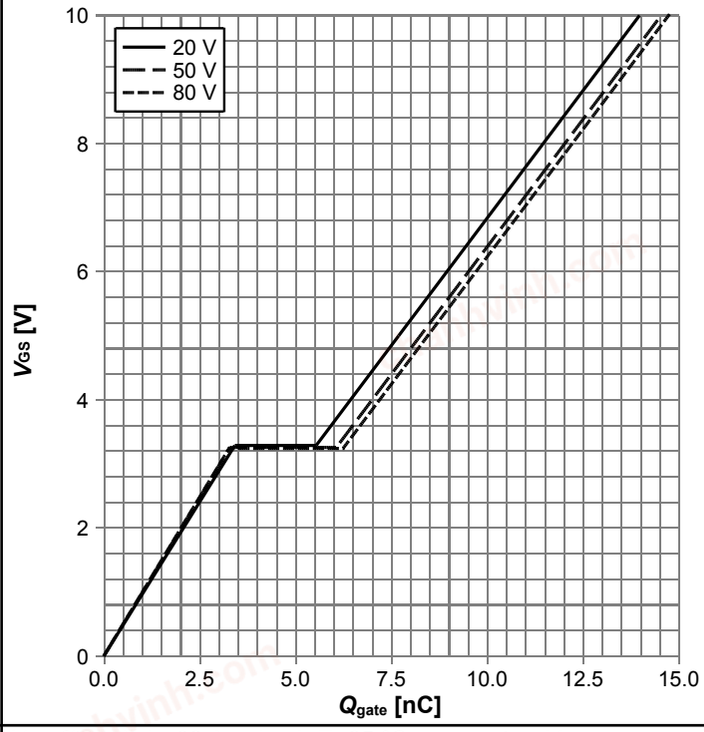


**Diagram 13: Avalanche characteristics**



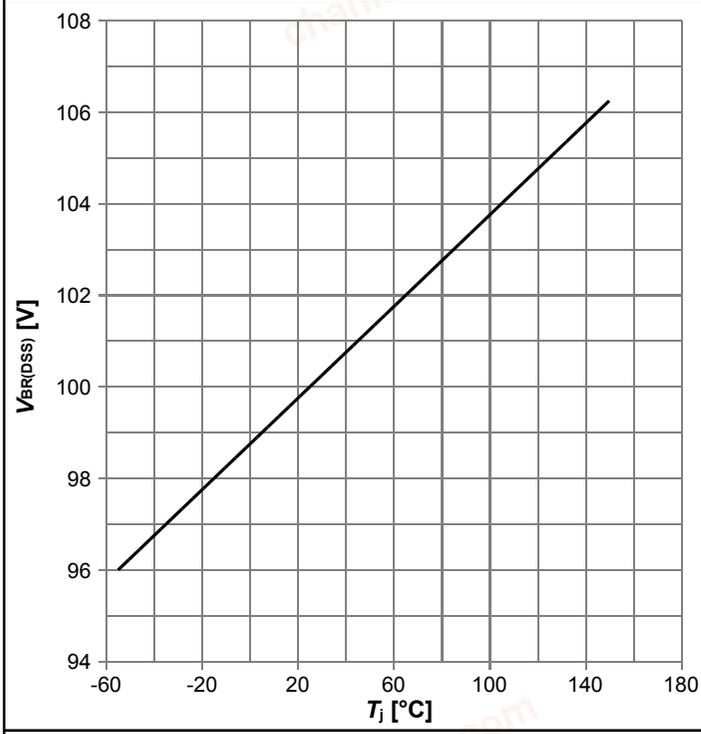

$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

**Diagram 14: Typ. gate charge**



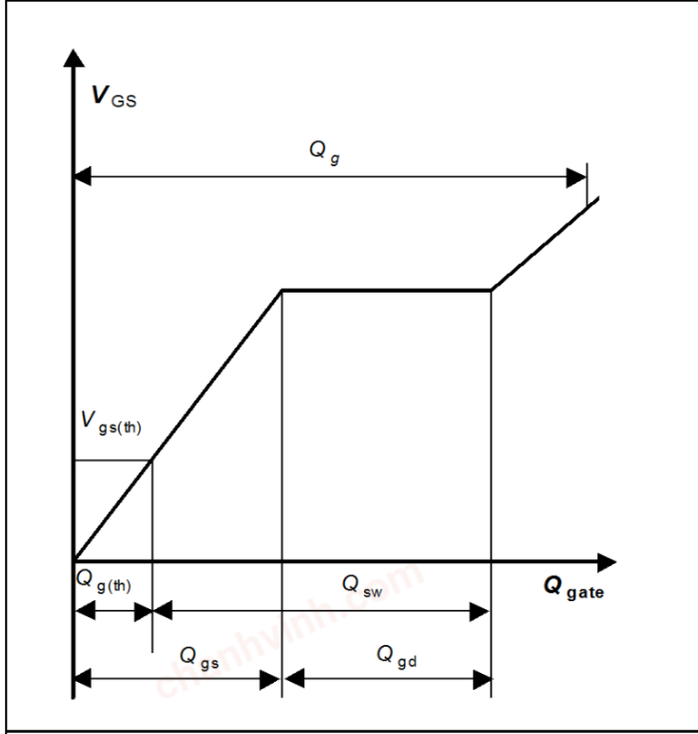

$V_{GS}=f(Q_{gate})$, $I_D=22$ A pulsed, $T_j=25$ °C; parameter: $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**




$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

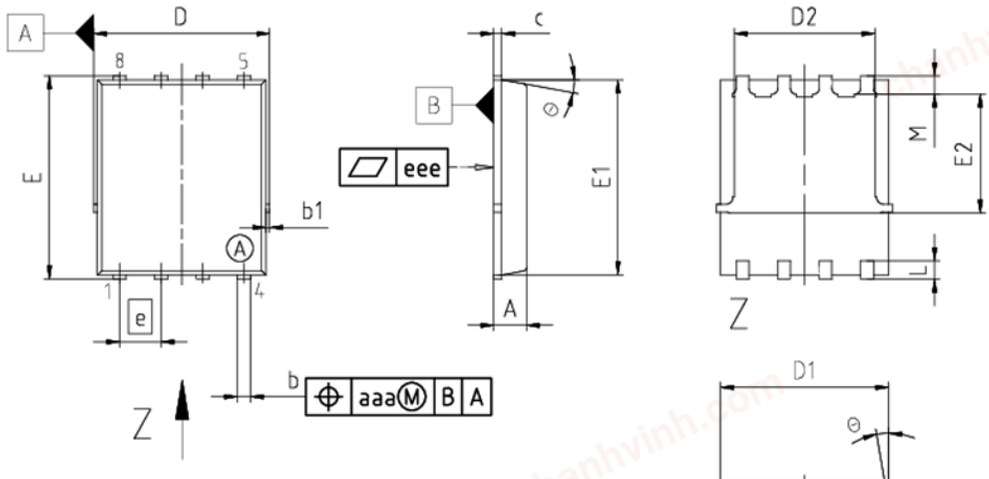
**Diagram Gate charge waveforms**



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## 5 Package Outlines




| DIM | MILLIMETERS | |
|---|---|---|
| | MIN | MAX |
| A | 0.90 | 1.10 |
| b | 0.31 | 0.54 |
| b1 | 0.02 | 0.22 |
| c | 0.15 | 0.35 |
| D | 5.15 | 5.49 |
| D1 | 4.95 | 5.35 |
| D2 | 3.70 | 4.40 |
| E | 5.95 | 6.35 |
| E1 | 5.70 | 6.10 |
| E2 | 3.40 | 3.80 |
| e | 1.27 | |
| N | 8 | |
| L | 0.45 | 0.71 |
| M | 0.45 | 0.75 |
| Θ | 8.5° | 12° |
| aaa | 0.25 | |
| eee | 0.08 | |

DOCUMENT NO.
Z8B00003332

SCALE 0 2 0 2 4mm

EUROPEAN PROJECTION

ISSUE DATE
10-04-2013

REVISION
04

**Figure 1 Outline PG-TDSON-8, dimensions in mm**

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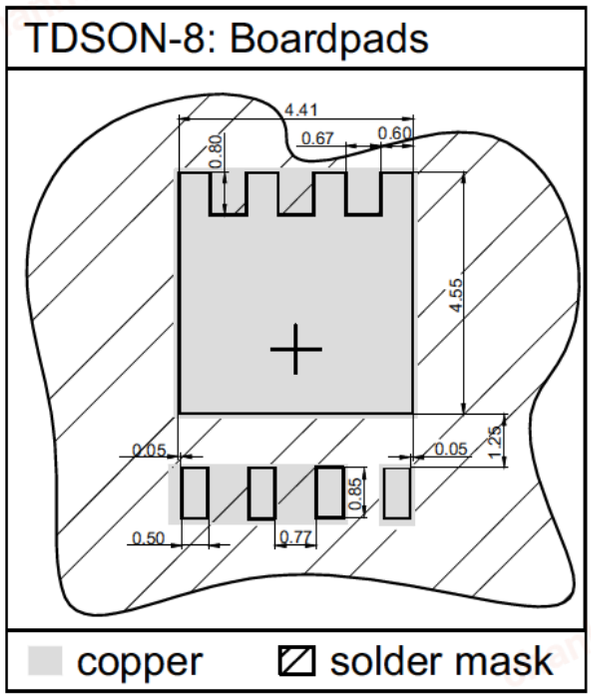



**Figure 2 Outline Footprint (TDSON-8)**

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## Revision History

BSC0803LS

**Revision: 2019-05-20, Rev. 2.1**

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 2.0 | 2016-09-30 | Release of final version |
| 2.1 | 2019-05-20 | Update Rg, trr, Qrr, Diagrams 5, 8 and 9 |

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