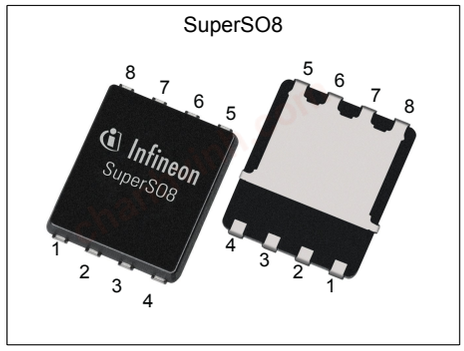
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MOSFET

OptiMOS™5 Power-Transistor, 80 V



Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

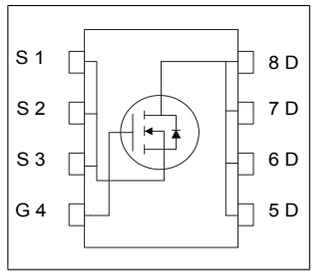


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	7.2	mΩ
I_D	74	A
Q_{oss}	29	nC
Q_G(0V..10V)	24	nC

Type / Ordering Code	Package	Marking	Related Links
BSC072N08NS5	PG-TDSON-8	072N08NS	-

[1] J-STD20 and JESD22

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1 Maximum ratings

at T_j = 25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	74 47 19	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_C=25 °C, R_{thJA} =50K/W[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	296	A	T_C=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	40	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	69 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[1]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.1	1.8	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm² cooling area[1]	R_{thJA}	-	-	50	K/W	-

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[2] See figure 3 for more detailed information
[3] See figure 13 for more detailed information

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3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=36 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	6.2 8.7	7.2 10.4	mΩ	V_{GS}=10 V, I_D=37 A V_{GS}=6 V, I_D=18.5 A
Gate resistance[1)]	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	31	62	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=37 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1600	2100	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	280	360	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	15	26	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=37 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	7	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=37 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	19	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=37 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	5	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=37 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8	-	nC	V_{DD}=40 V, I_D=37 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	5	-	nC	V_{DD}=40 V, I_D=37 A, V_{GS}=0 to 10 V
Gate to drain charge[1)]	Q_{gd}	-	5	8	nC	V_{DD}=40 V, I_D=37 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	9	-	nC	V_{DD}=40 V, I_D=37 A, V_{GS}=0 to 10 V
Gate charge total[1)]	Q_g	-	24	29	nC	V_{DD}=40 V, I_D=37 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	V_{DD}=40 V, I_D=37 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	20	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	29	39	nC	V_{DD}=40 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See ″Gate charge waveforms″ for parameter definition

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Table 7 Reverse diode

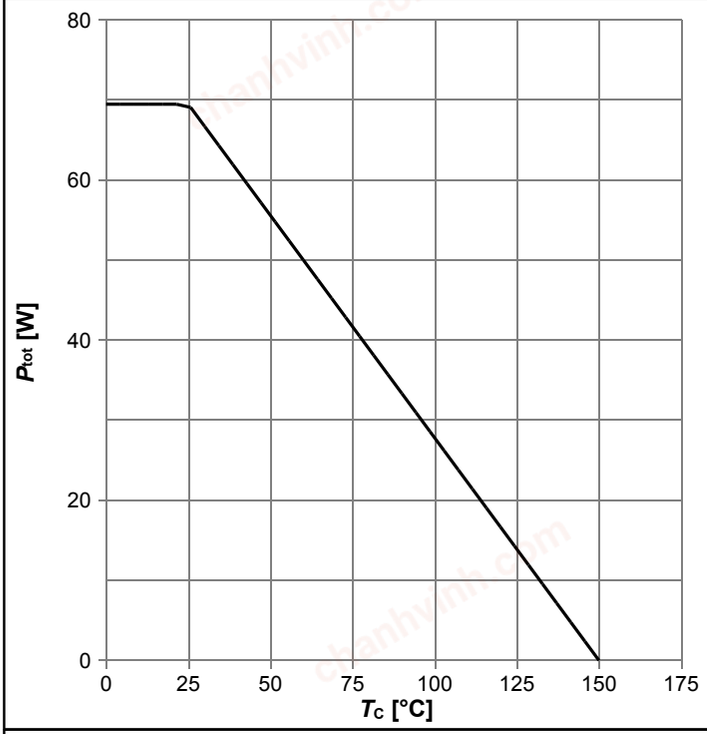
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	63	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	296	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.9	1.1	V	V_{GS}=0 V, I_F=37A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	36	72	ns	V_R=40 V, I_F=37A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	37	73	nC	V_R=40 V, I_F=37A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

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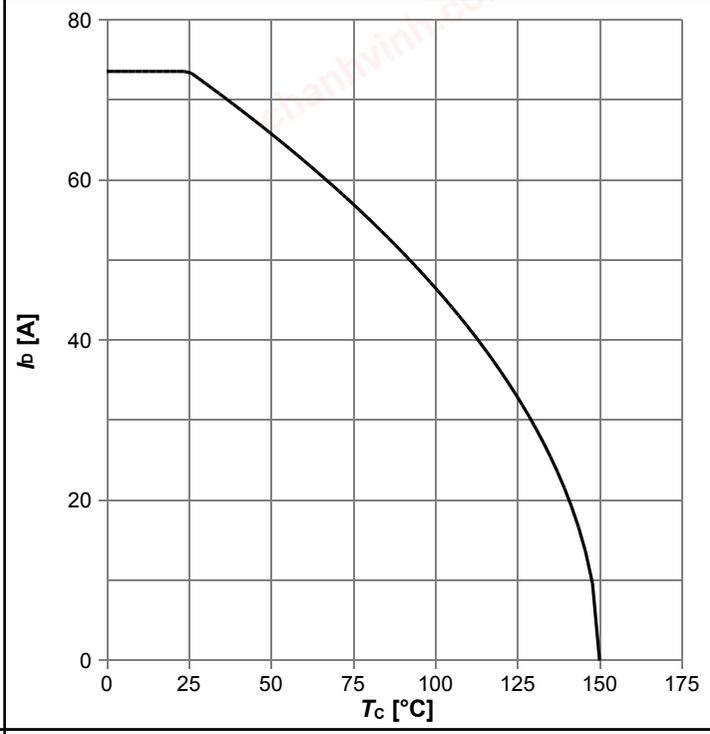
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



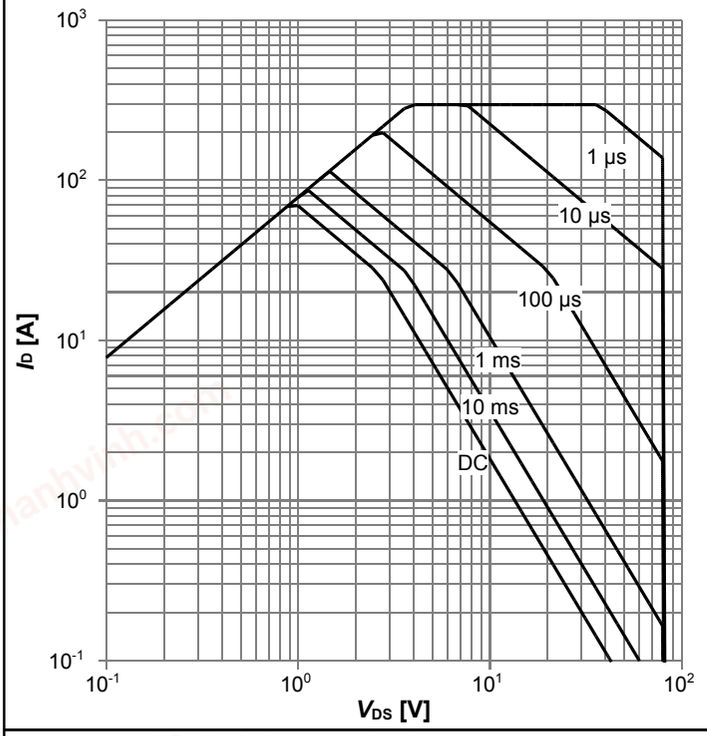
$P_{tot}=f(T_C)$

Diagram 2: Drain current



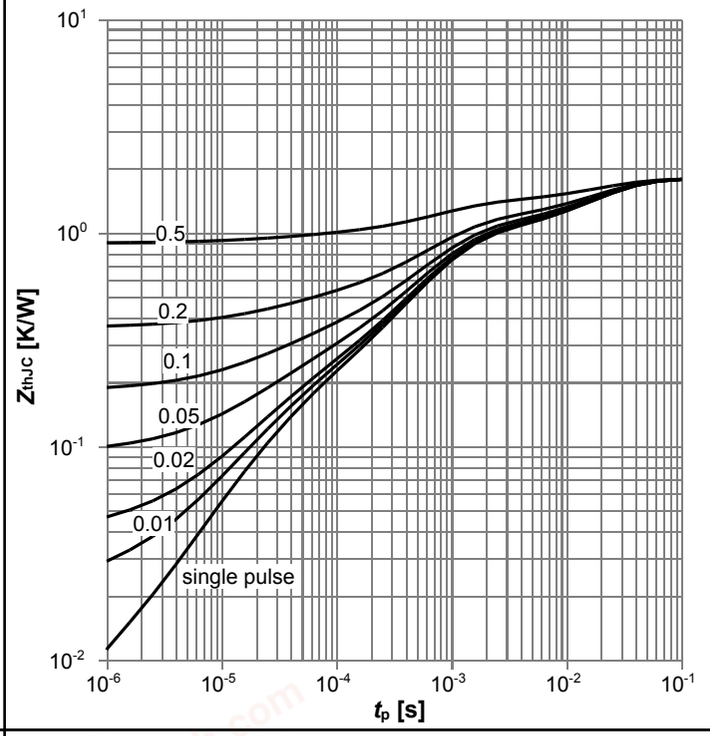
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

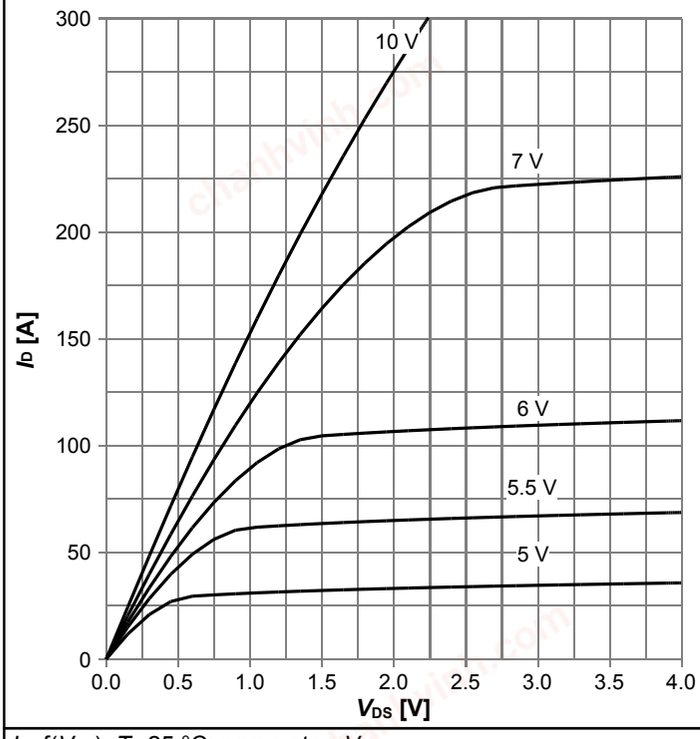
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

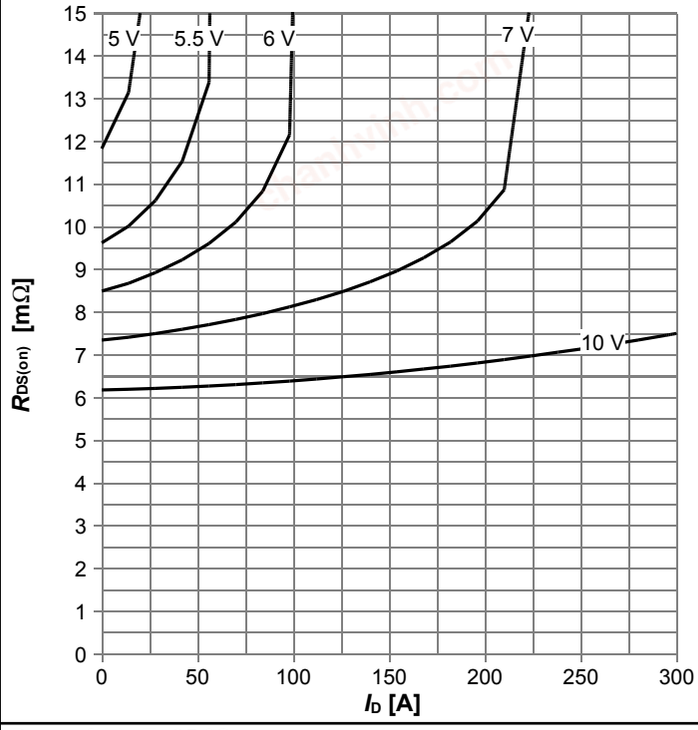
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Diagram 5: Typ. output characteristics



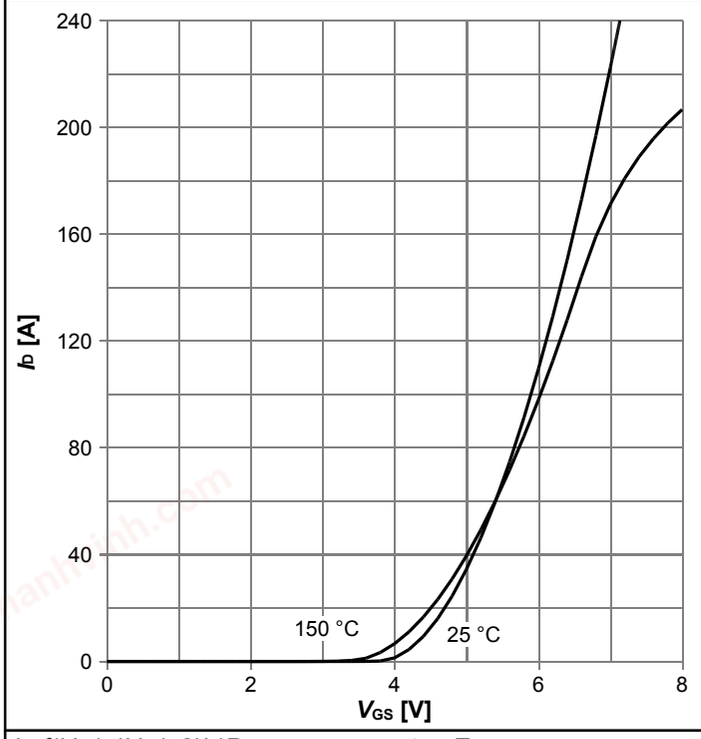
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



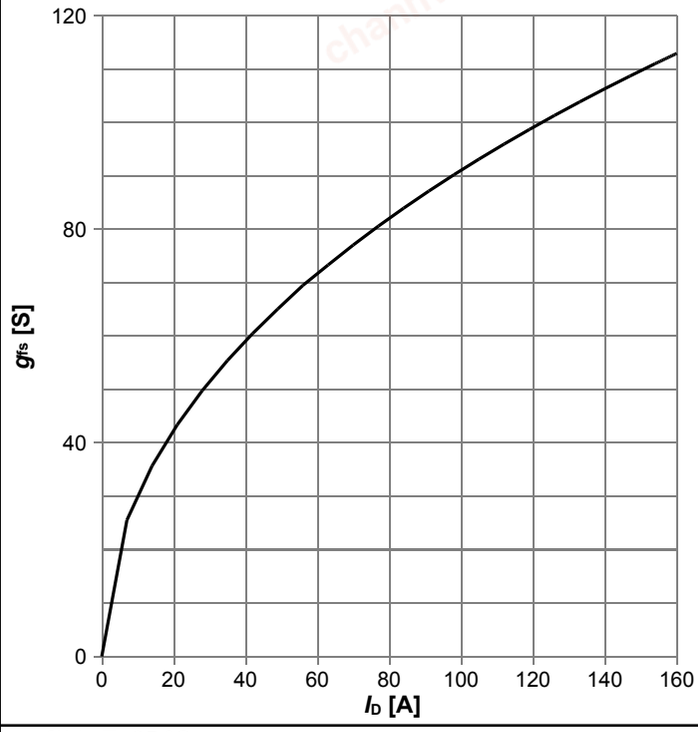
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

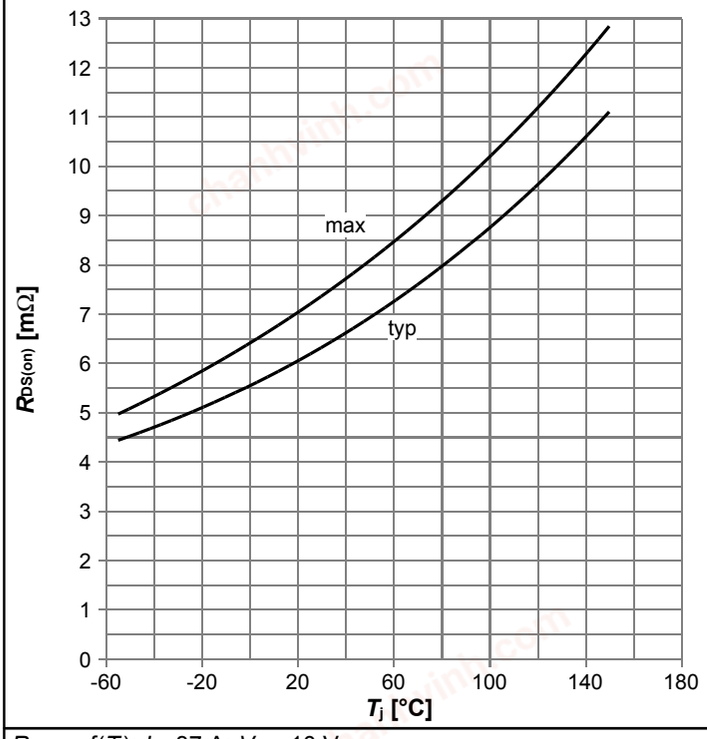
Diagram 8: Typ. forward transconductance



g_{fs}=f(I_D); T_j=25 °C

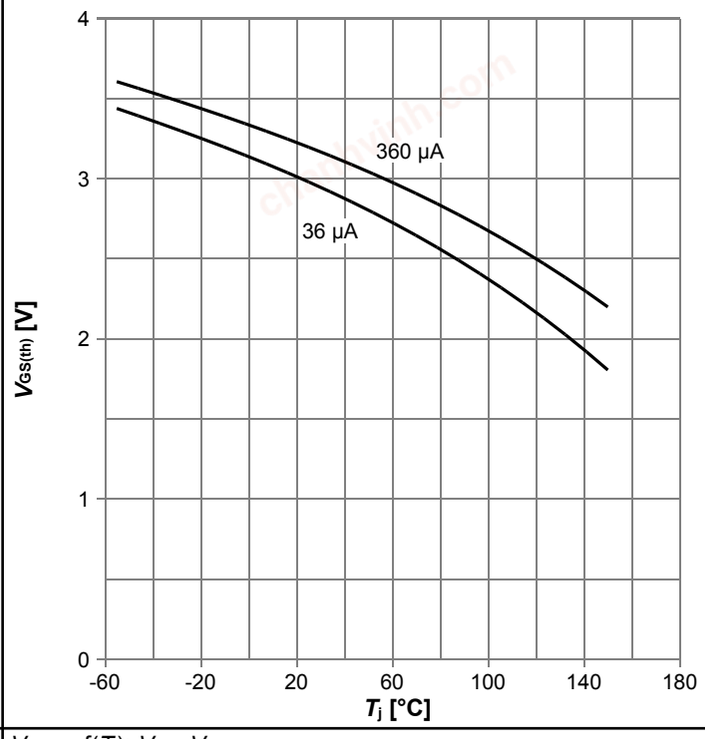
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Diagram 9: Drain-source on-state resistance



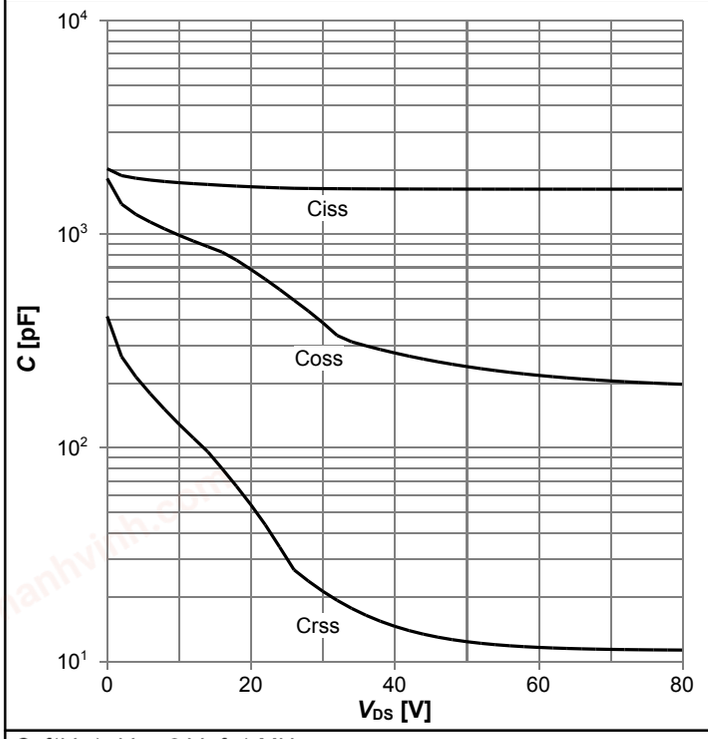
$R_{DS(on)}=f(T_j)$; I_D=37 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



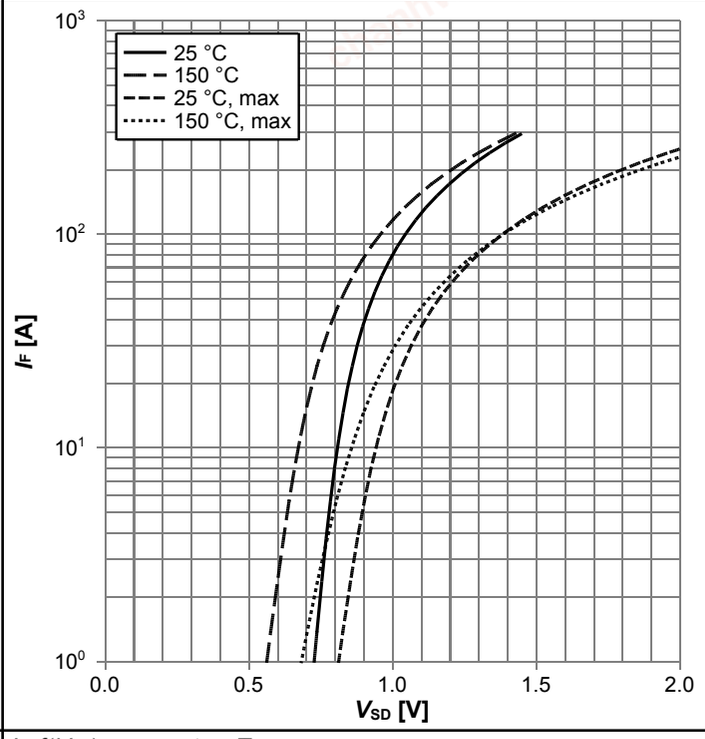
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz

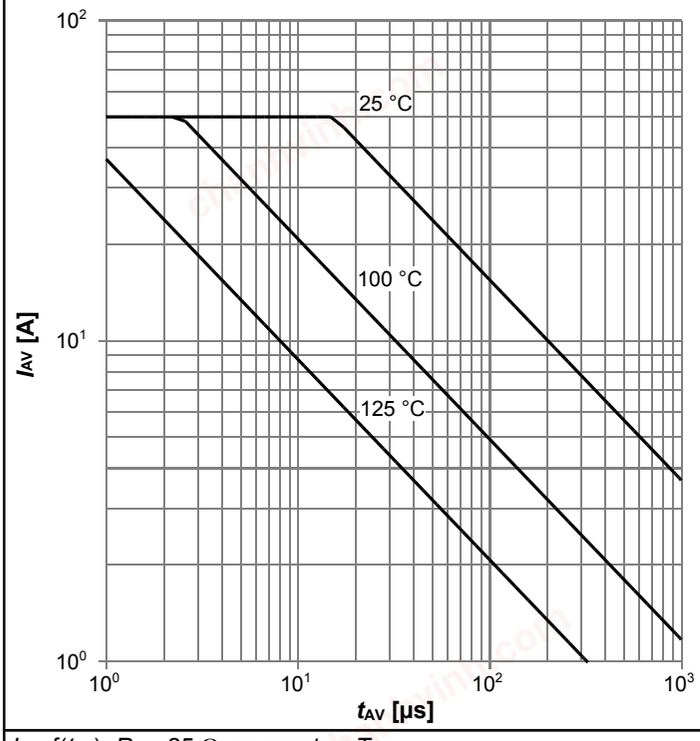
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$; parameter: T_j

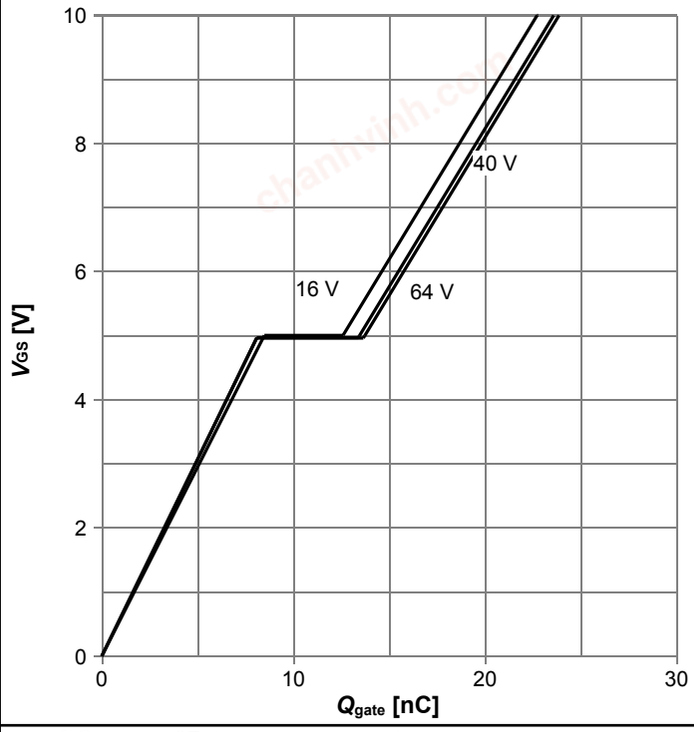
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Diagram 13: Avalanche characteristics



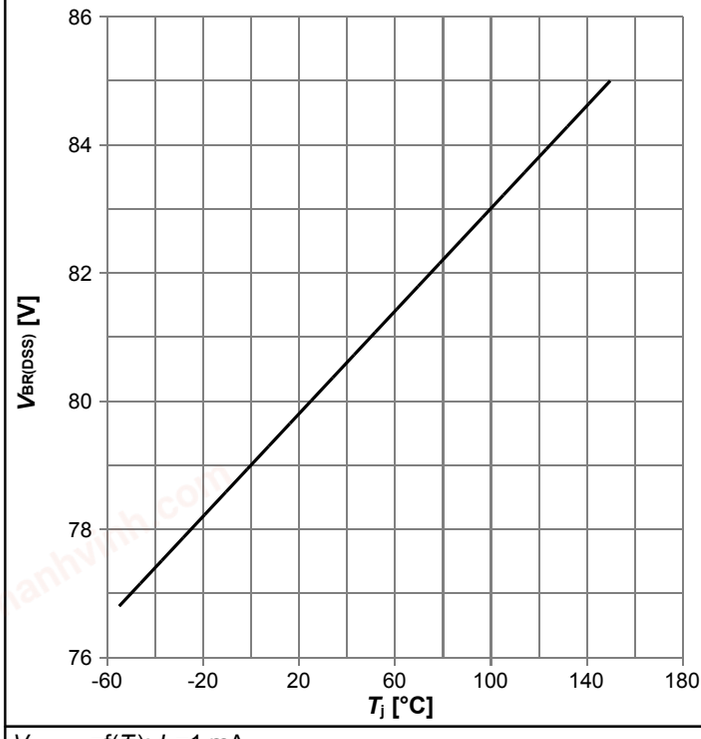
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



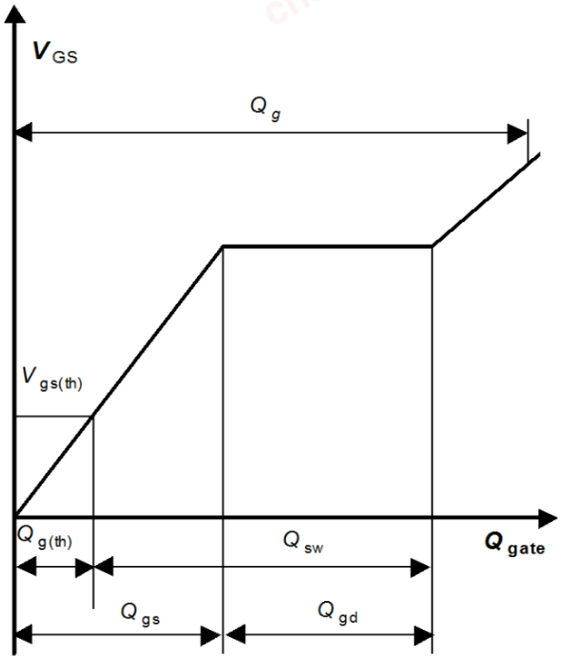
V_{GS}=f(Q_{gate}); I_D=37 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



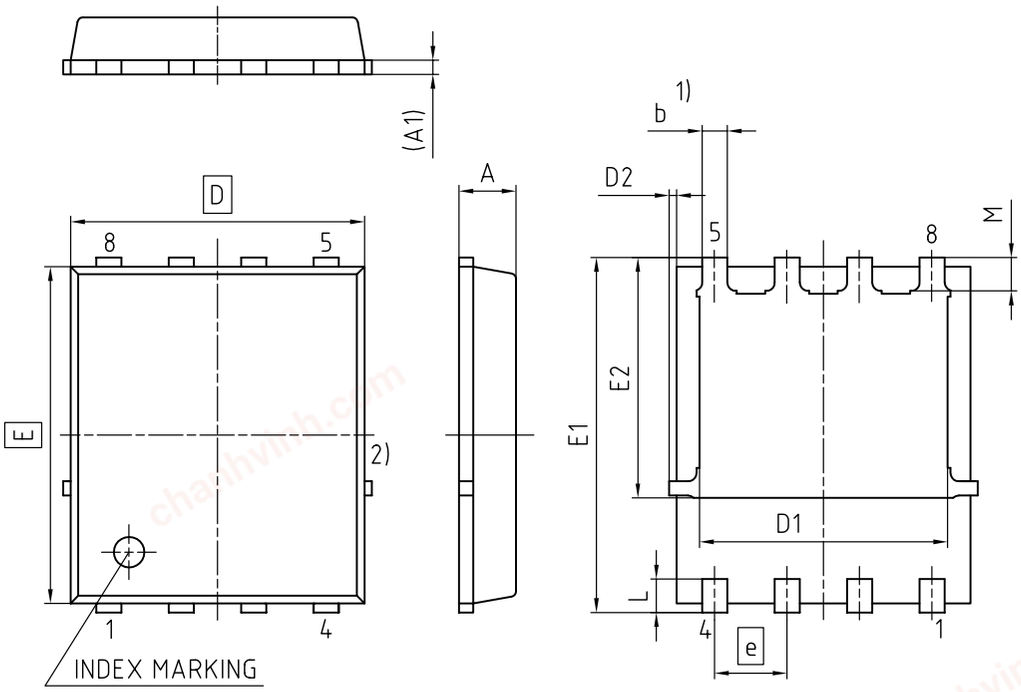
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



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5 Package Outlines



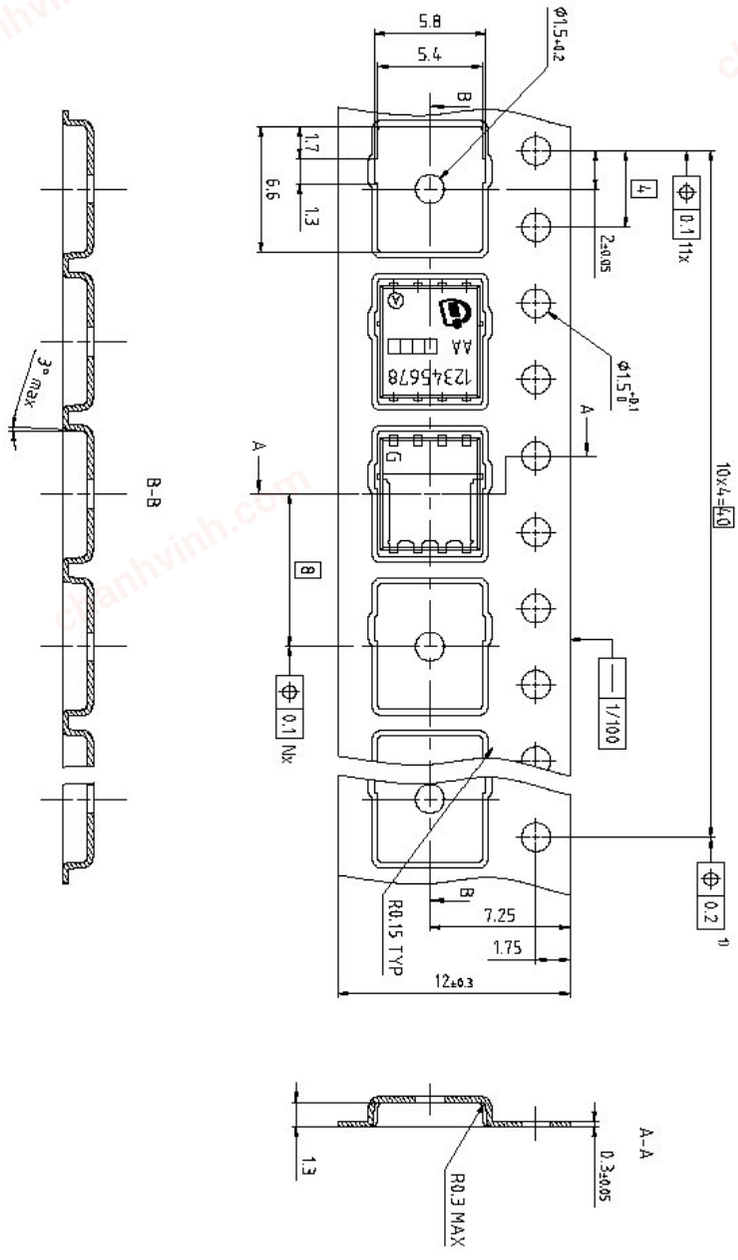
1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO. Z8B00003332
REVISION 07
SCALE 10:1 0 1 2 3mm
EUROPEAN PROJECTION
ISSUE DATE 06.06.2019

Figure 1 Outline PG-TDSON-8, dimensions in mm

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Dimension in mm

Figure 2 Outline Tape (TDSON-8)

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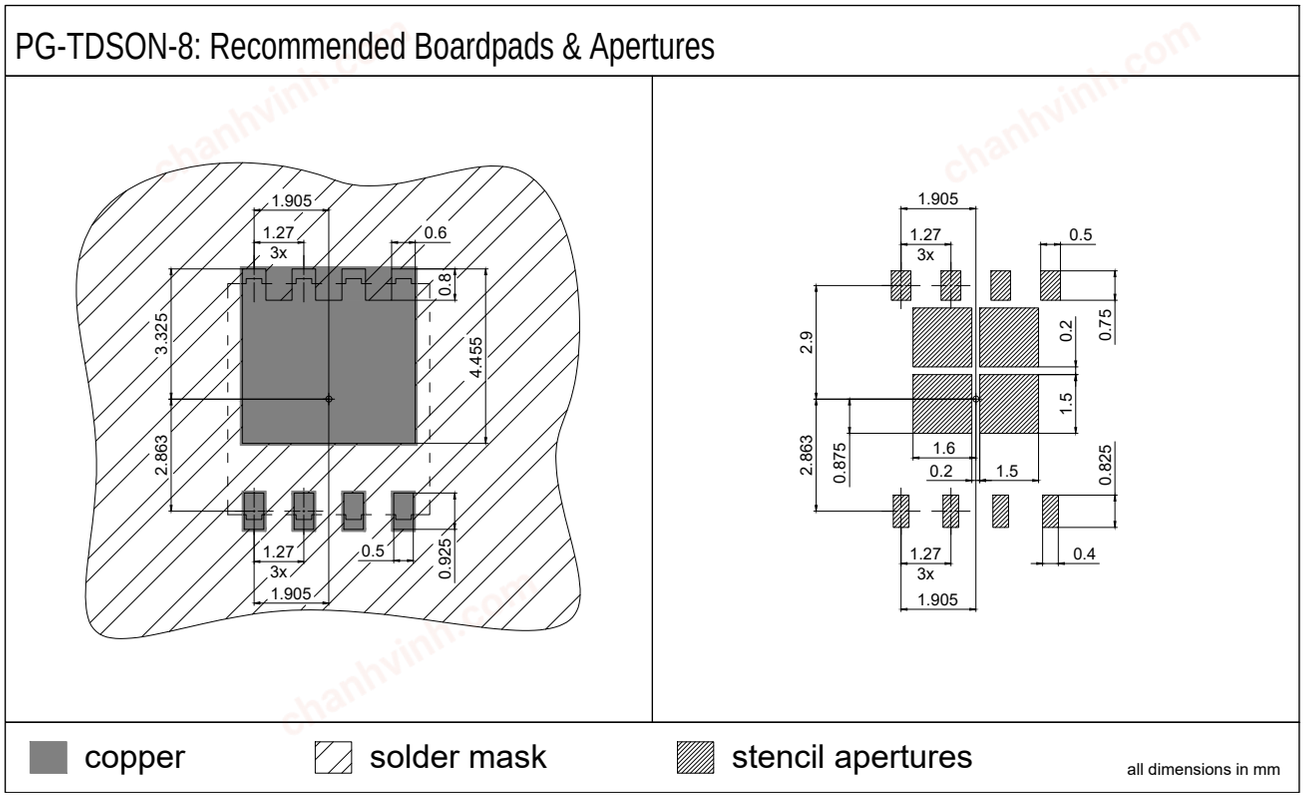


Figure 3 Outline Boardpads (TDSON-8), dimensions in mm

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Revision History

BSC072N08NS5

Revision: 2019-11-13, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-27	Release of final version
2.1	2019-11-13	Update package drawings

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