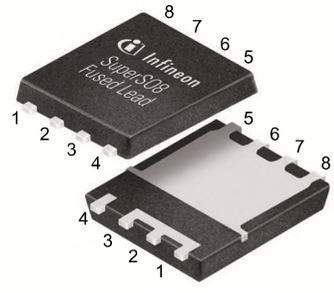
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MOSFET

OptiMOS™ 5 Power-Transistor, 30 V

TDSON-8 FL (enlarged source interconnection)



Features

- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- Optimized charges for fast switching
- Optimized QGD/QGS for induced turn on ruggedness
- Superior thermal resistance
- N-channel
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

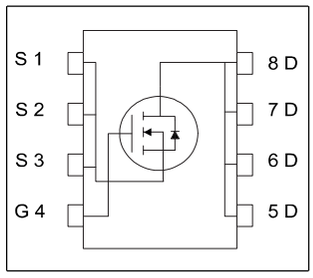


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	0.55	mΩ
I_D	433	A
Q_{oss}	70	nC
Q_G(0V..4.5V)	59	nC

Type / Ordering Code	Package	Marking	Related Links
BSC005N03LS5	PG-TDSON-8 FL	05N03LS5	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	433 306 42	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_A=25 °C, R_{THJA}=50 °C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	1731	A	T_A=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	900	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	188 3.0	W	T_C=25 °C T_A=25 °C, R_{THJA}=50 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.8	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Device on PCB, 6 cm² cooling area	R_{thJA}	-	-	50	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

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3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1	1.5	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.48 0.63	0.55 0.95	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=4.5 V, I_D=50 A
Gate resistance[1]	R_G	-	0.7	1.2	Ω	-
Transconductance	g_{fs}	-	300	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	8900	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance	C_{oss}	-	2700	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	300	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	21	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	20.7	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	48.4	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	16.2	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	21	-	nC	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	12	-	nC	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	14	-	nC	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	22	-	nC	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	59	-	nC	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.3	-	V	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	122	-	nC	V_{DD}=15 V, I_D=50 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	70	-	nC	V_{DS}=15 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

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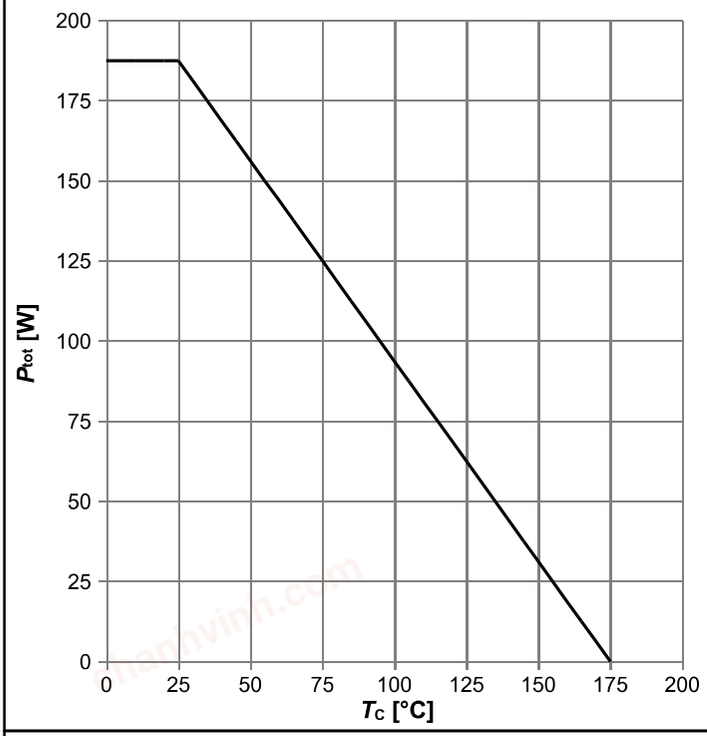
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	188	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1731	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.79	1	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	30	-	nC	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs

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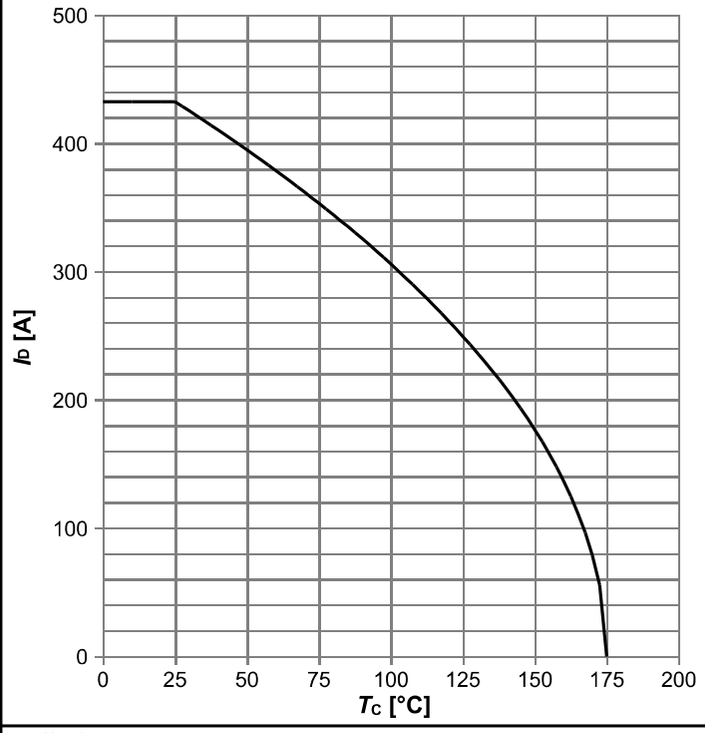
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



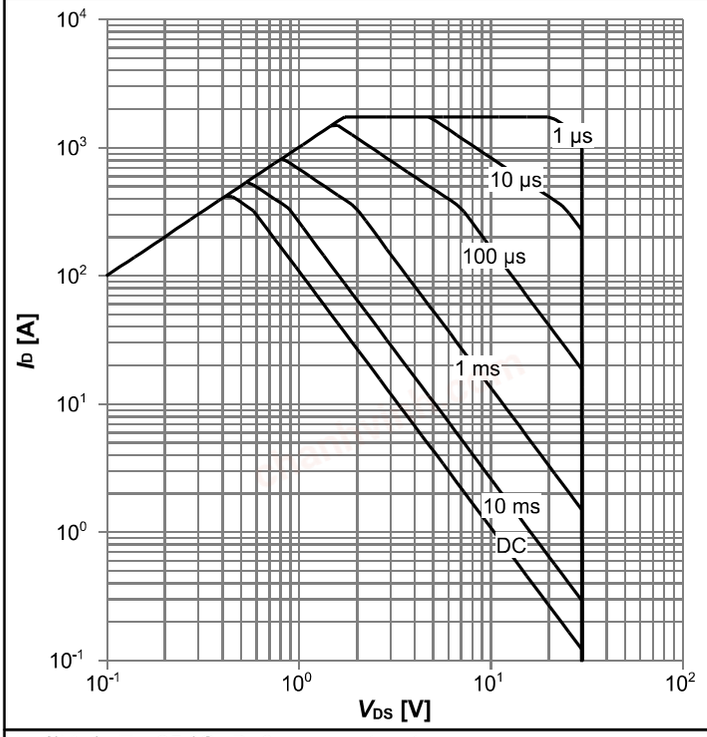
$P_{tot}=f(T_C)$

Diagram 2: Drain current



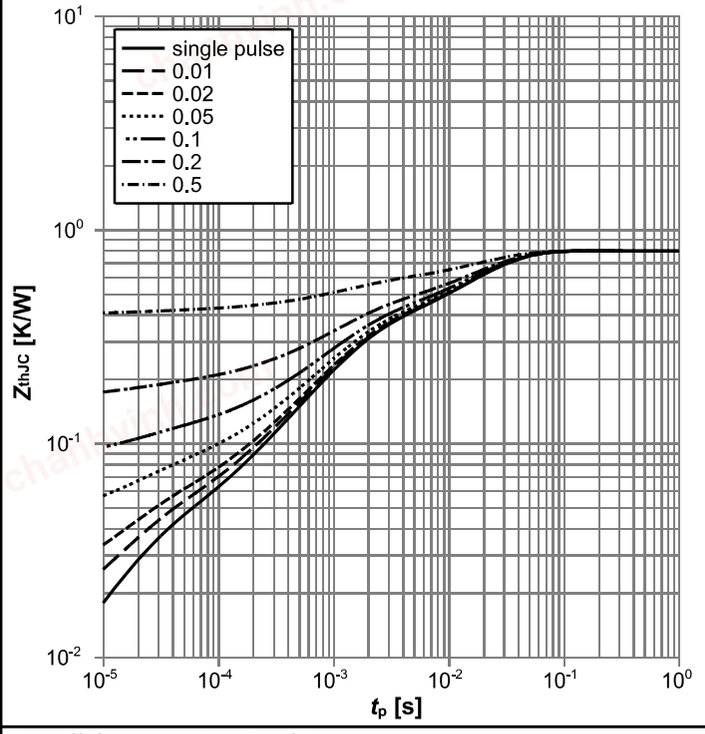
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

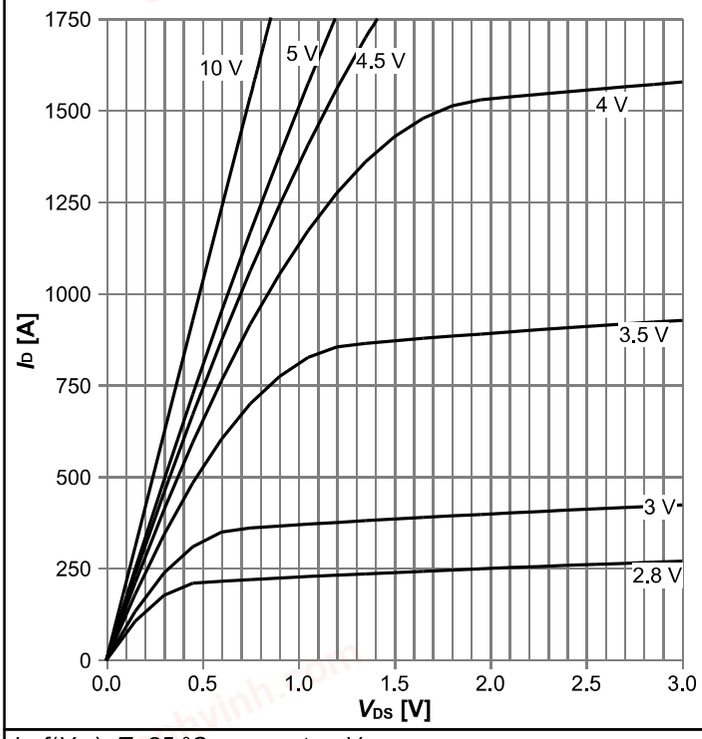
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

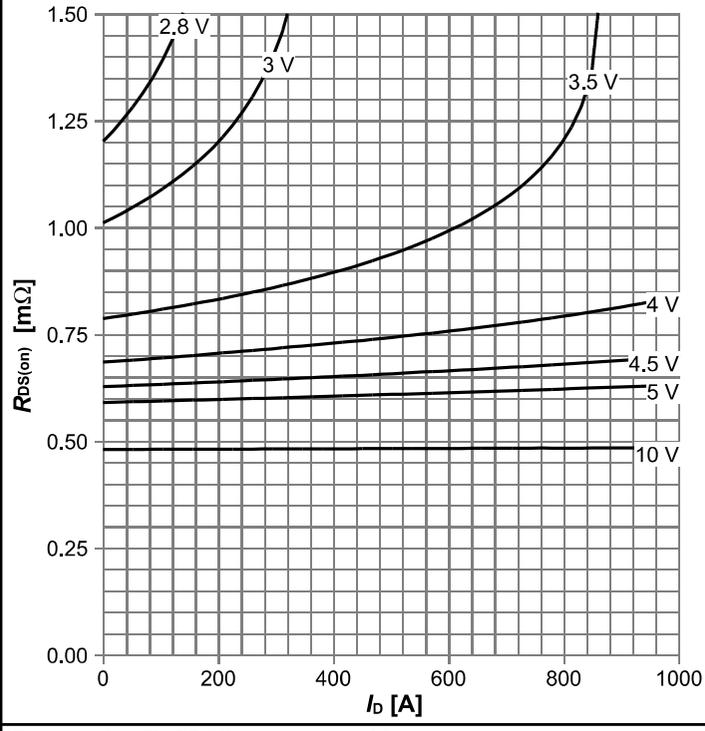
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Diagram 5: Typ. output characteristics



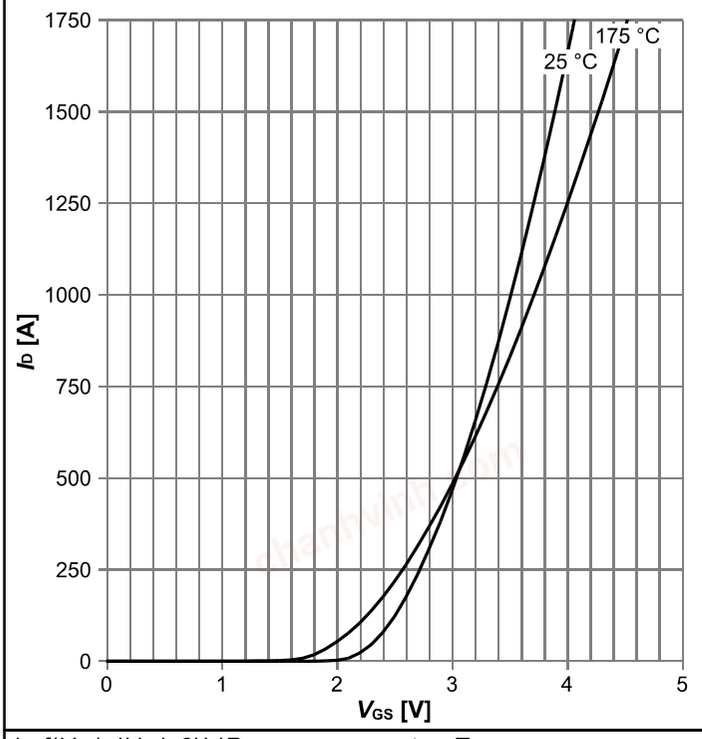
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



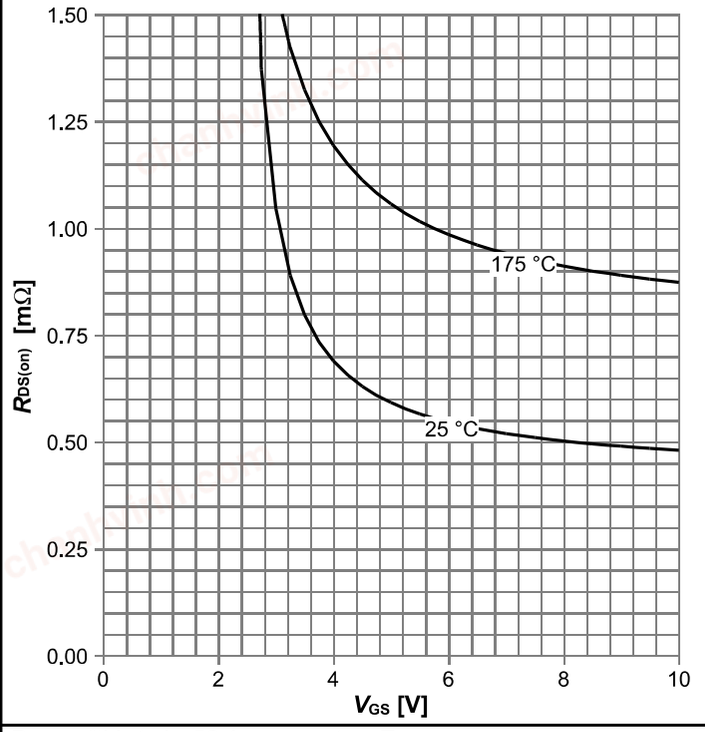
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

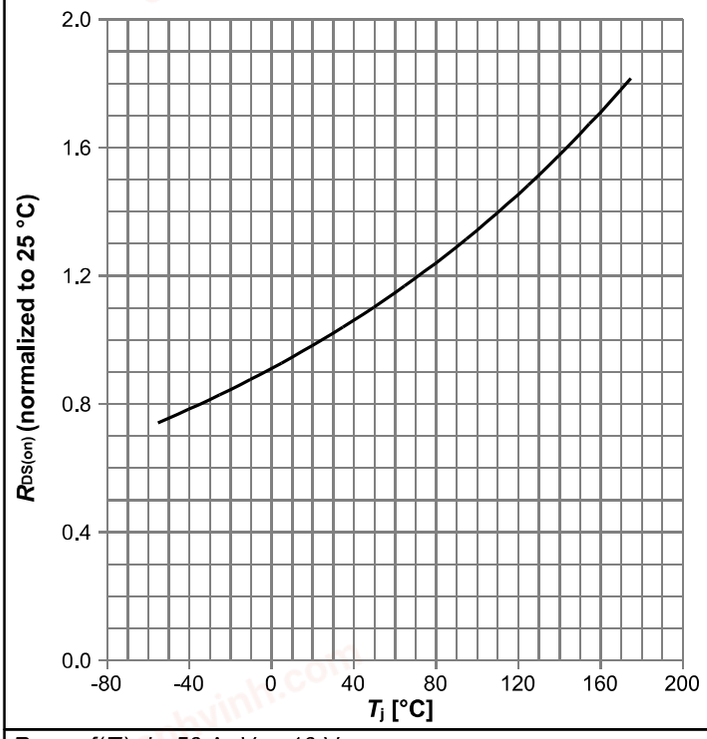
Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}=f(V_{GS})$, $I_D=50$ A; parameter: T_j

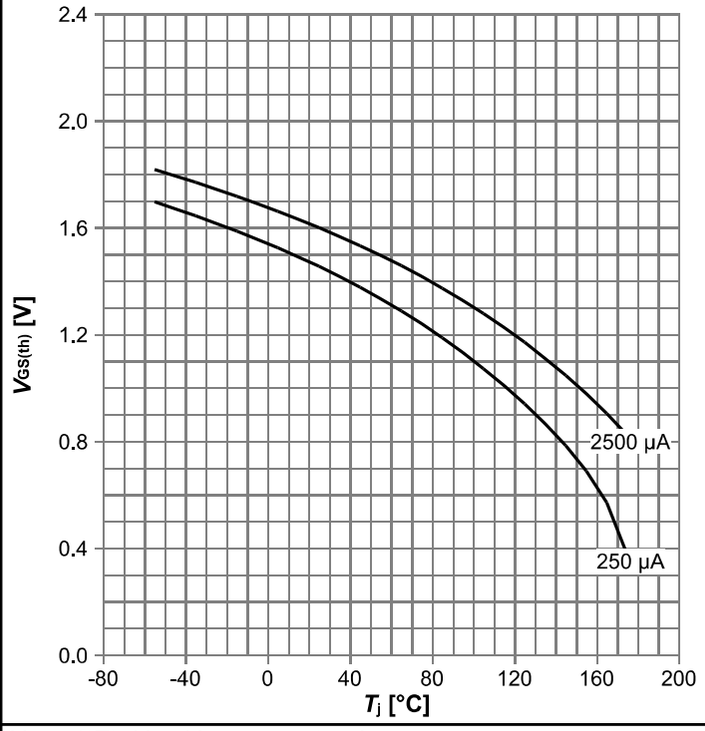
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Diagram 9: Normalized drain-source on resistance



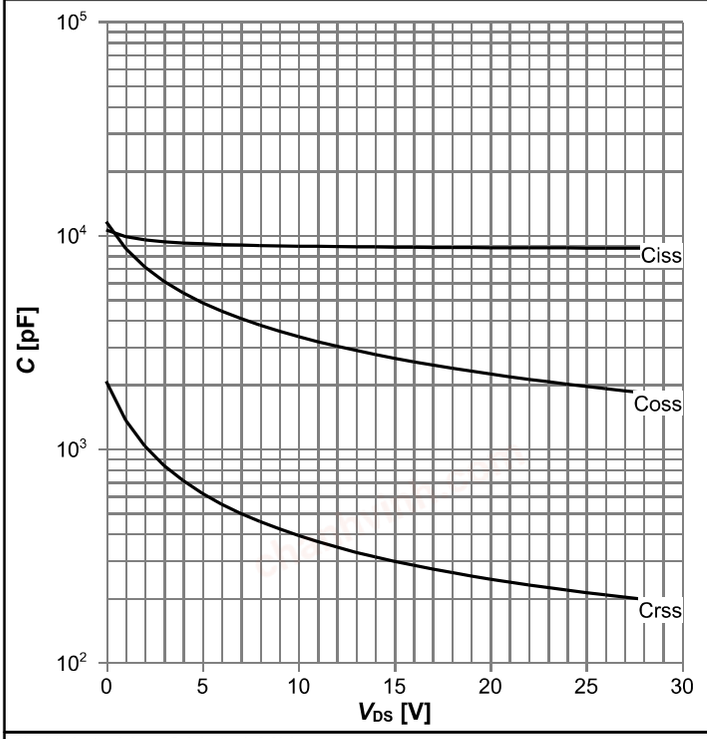
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



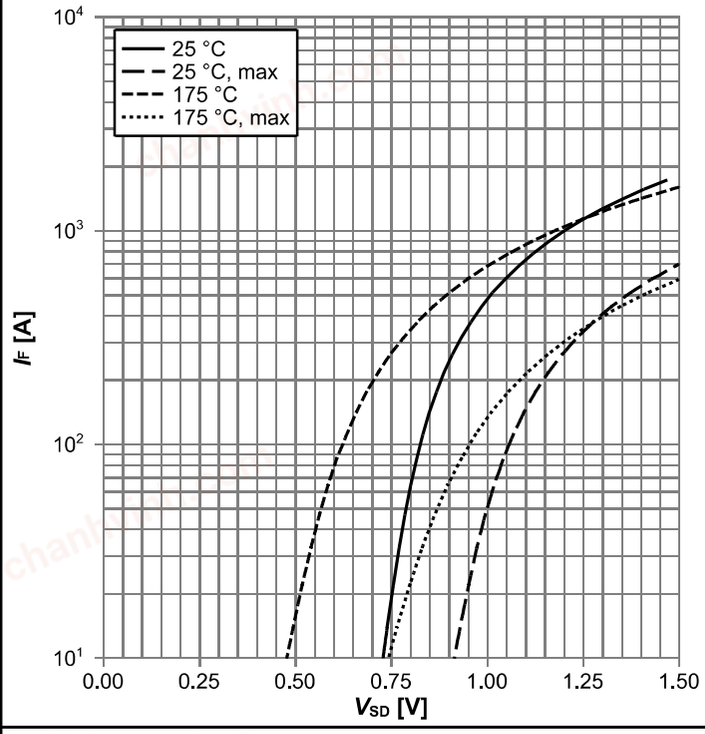
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

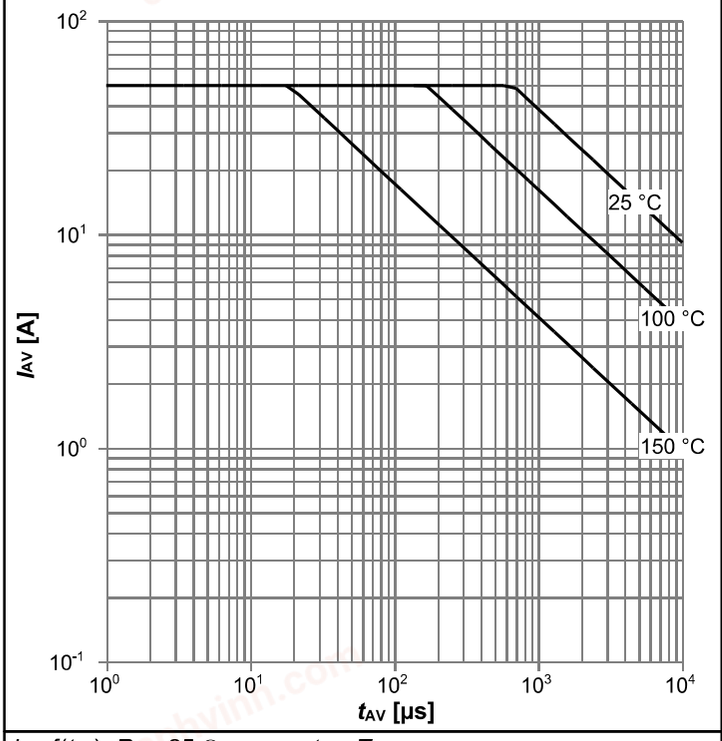
Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

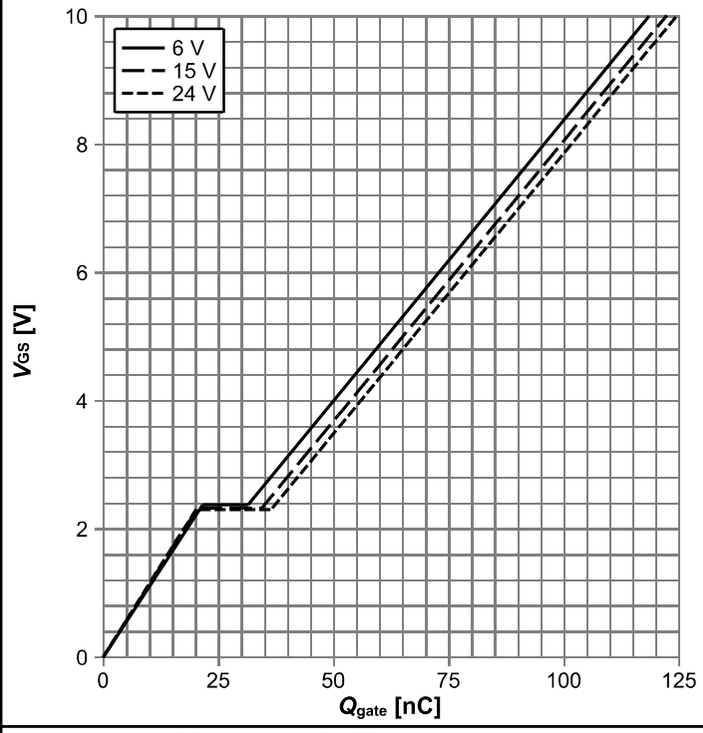
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Diagram 13: Avalanche characteristics



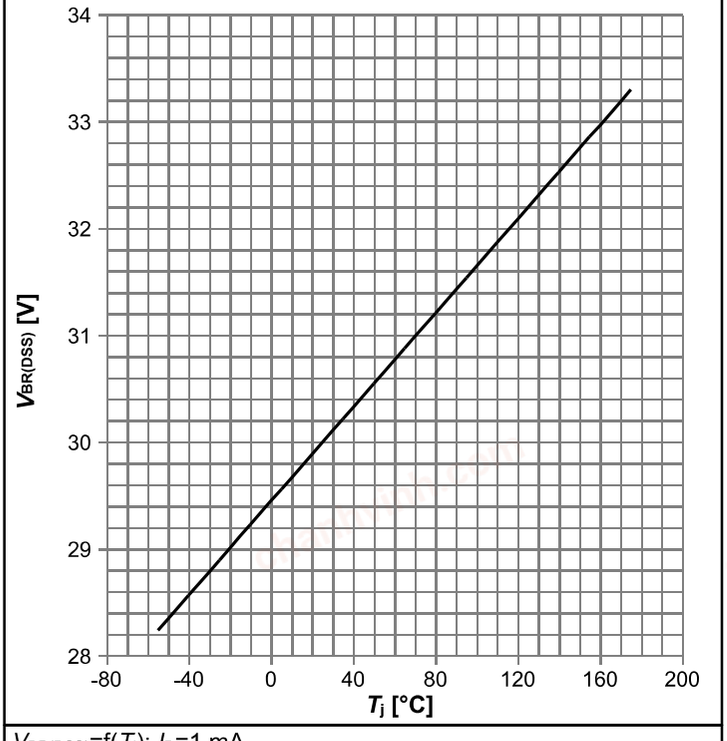
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



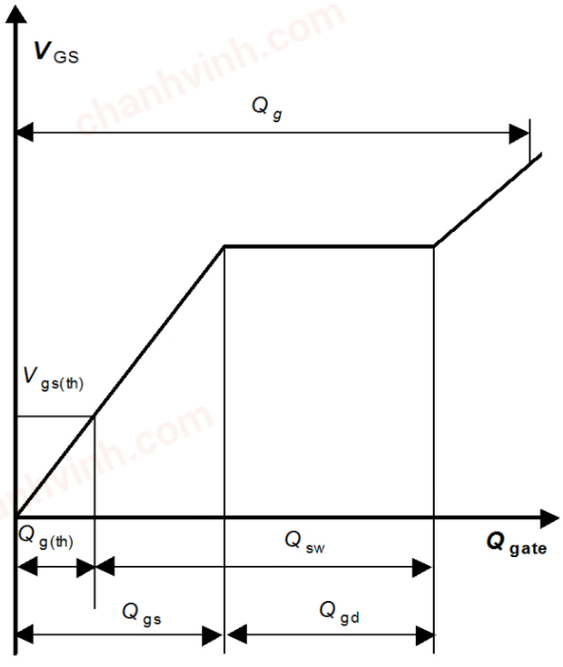
V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



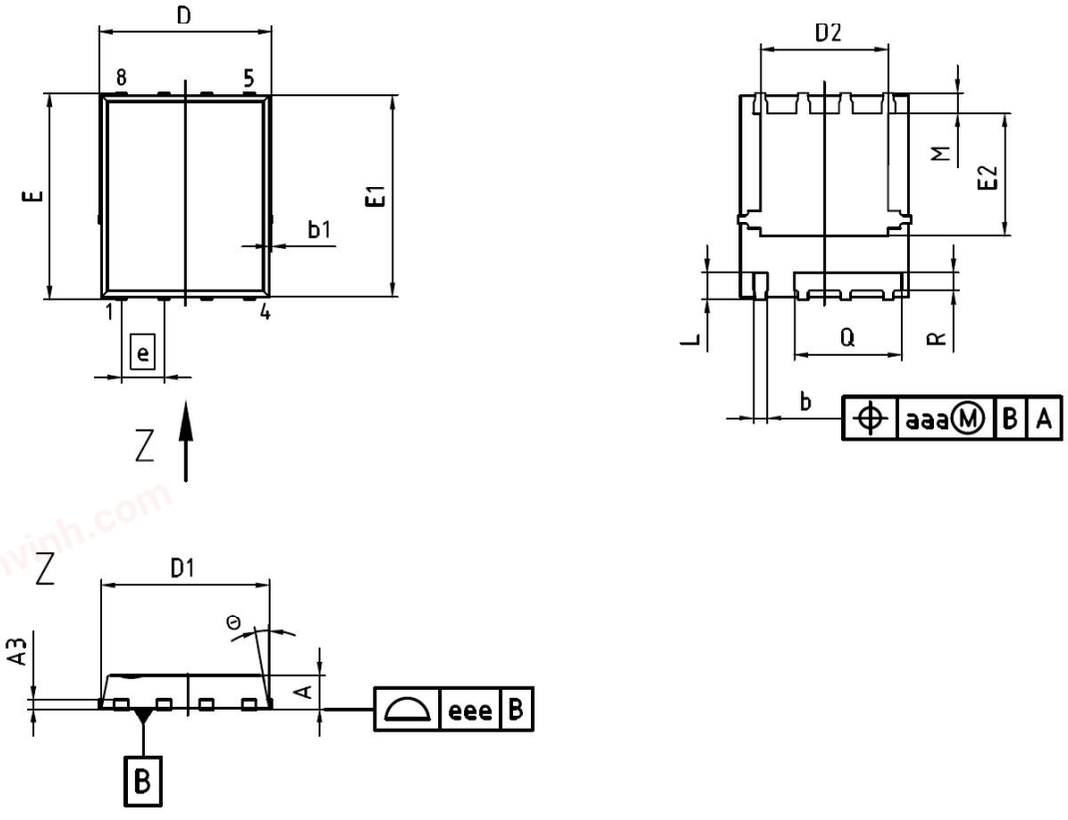
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



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5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
A3	0.25 (REF)		0.011 (REF)	
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.009
D	5.15 (BSC)		0.203 (BSC)	
D1	5.00 (BSC)		0.197 (BSC)	
D2	3.70	4.40	0.146	0.173
E	6.15 (BSC)		0.242 (BSC)	
E1	6.00 (BSC)		0.236 (BSC)	
E2	3.40	3.80	0.134	0.150
e	1.27 (BSC)		0.050 (BSC)	
N	8		8	
L	0.74	0.84	0.029	0.033
M	0.45	0.66	0.018	0.026
Θ	8.5°	12°	8.5°	12°
Q	3.15	3.25	0.124	0.128
R	0.48	0.58	0.019	0.023
aaa	0.25		0.010	
eee	0.08		0.003	

DOCUMENT NO.	Z8B00162237
SCALE	0 2.5 0 2.5 5mm
EUROPEAN PROJECTION	
ISSUE DATE	02-08-2011
REVISION	01

Figure 1 Outline PG-TDSON-8 FL, dimensions in mm/inches

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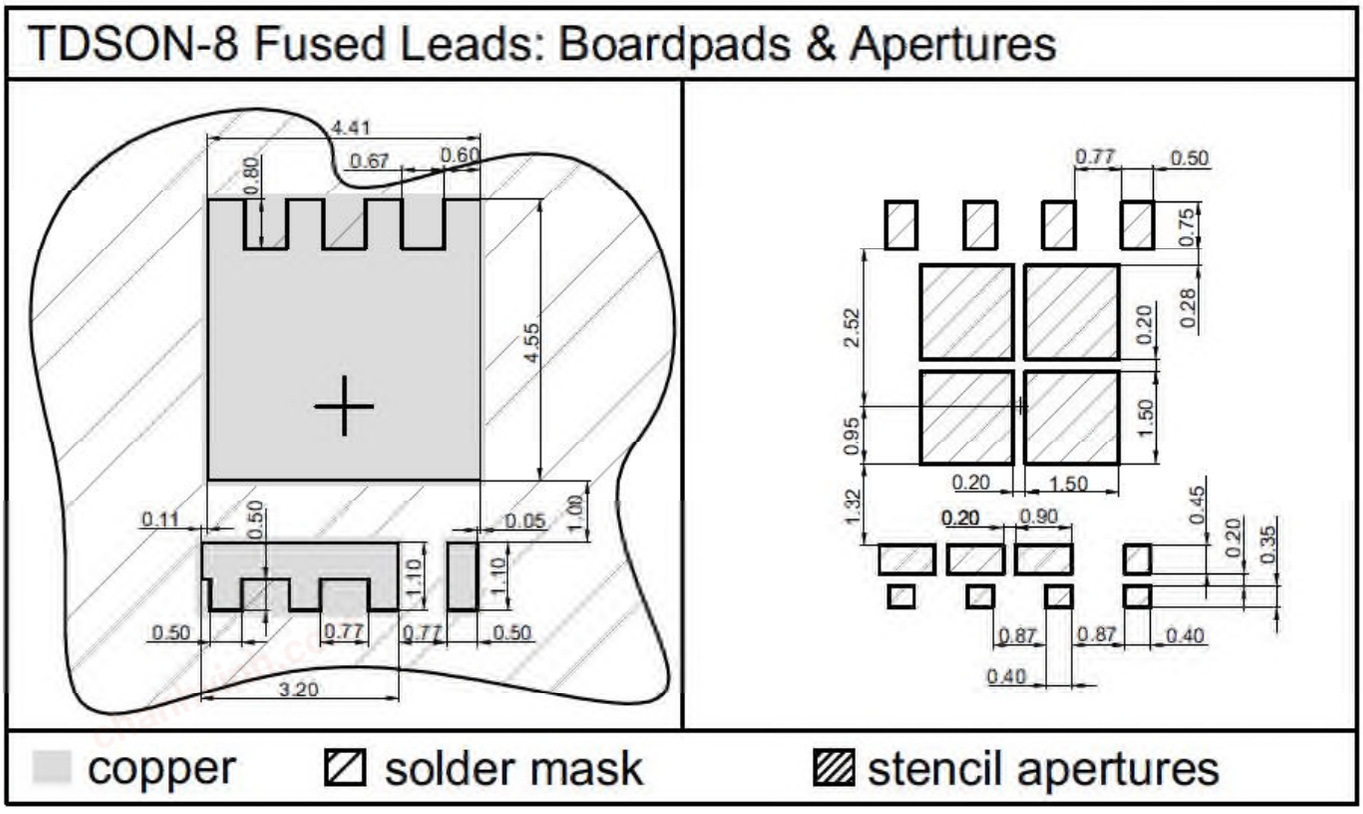


Figure 2 Outline Boardpads (TDSON-8 FL)

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Revision History

BSC005N03LS5

Revision: 2020-12-22, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2020-04-16	Release of final version
2.1	2020-12-22	Update Id for VGSTH

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