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International
IOR Rectifier

January 14, 2011

Automotive Grade AUIRS2301S

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 5V to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Lower di/dt gate driver for better noise immunity
- Leadfree, RoHS compliant
- Automotive qualified*

Typical Applications

- Automotive motor drives
- Servo drives
- Micro inverter drives
- General purpose three phase inverters

Product Summary

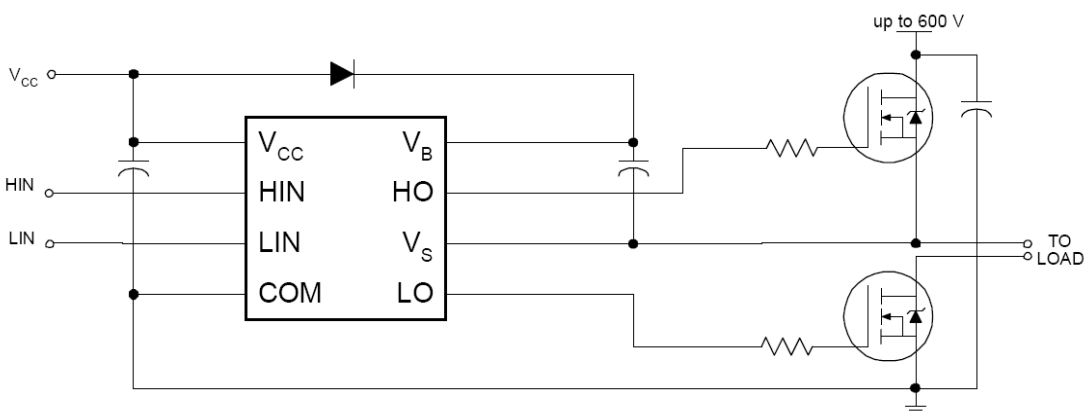
V_{OFFSET}	600V Max
V_{OUT}	5V – 20V
I_{o+} & I_{o-} (typical)	200mA / 350mA
t_{ON} & t_{OFF} (typical)	220ns / 200ns
Delay Matching	50ns

Package Options



8-Lead SOIC
AUIRS2301S

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only.
Please refer to our Application Notes and DesignTips for proper circuit board layout.

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Description

The AUIRS2301S is a high voltage, high speed power MOSFET and IGBT driver with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600V.

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Qualification Information†

Qualification Level		Automotive (per AEC-Q100††) Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.
Moisture Sensitivity Level		MSL3††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (Pass +/-200V) (per AEC-Q100-003)
	Human Body Model	Class H1C (Pass +/-2000V) (per AEC-Q100-002)
	Charged Device Model	Class C5 (Pass +/-1000V) (per AEC-Q100-011)
IC Latch-Up Test		Class II , Level B (per AEC-Q100-004)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/
†† Exceptions to AEC-Q100 requirements are noted in the qualification report.
††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	-0.3	625	V
V_S	High-side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low-side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	COM -0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	V_S + 5	V_S + 20	V
V_S	High-side floating supply offset voltage	† 1	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	5	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	COM	V_{CC}	
T_A	Ambient temperature	-40	125	°C

†: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to – V_{BS}. (Please refer to the Design Tip DT97 -3 for more details).

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Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}) = 15V. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads: HIN and LIN. The V_O, I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min	Typ	Max	Units	Test conditions
V_{IH}	Logic "1" input voltage	2.5	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	0.2	V	I_O = 2mA
V_{OL}	Low level output voltage, V_O	—	—	0.1		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	60	160	260		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	60	160	260		
I_{IN+}	Logic "1" input bias current	—	5	20		V_{IN} = 5V
I_{IN-}	Logic "0" input bias current	—	—	5		V_{IN} = 0V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	3.3	4.1	5	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	3	3.8	4.7		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.1	0.3	—		
I_{O+}	Output high short circuit pulsed current	—	200	—	mA	V_O = 0V, PW ≤ 10µs
I_{O-}	Output low short circuit pulsed current	—	350	—		V_O = 15V, PW ≤ 10µs

Dynamic Electrical Characteristics

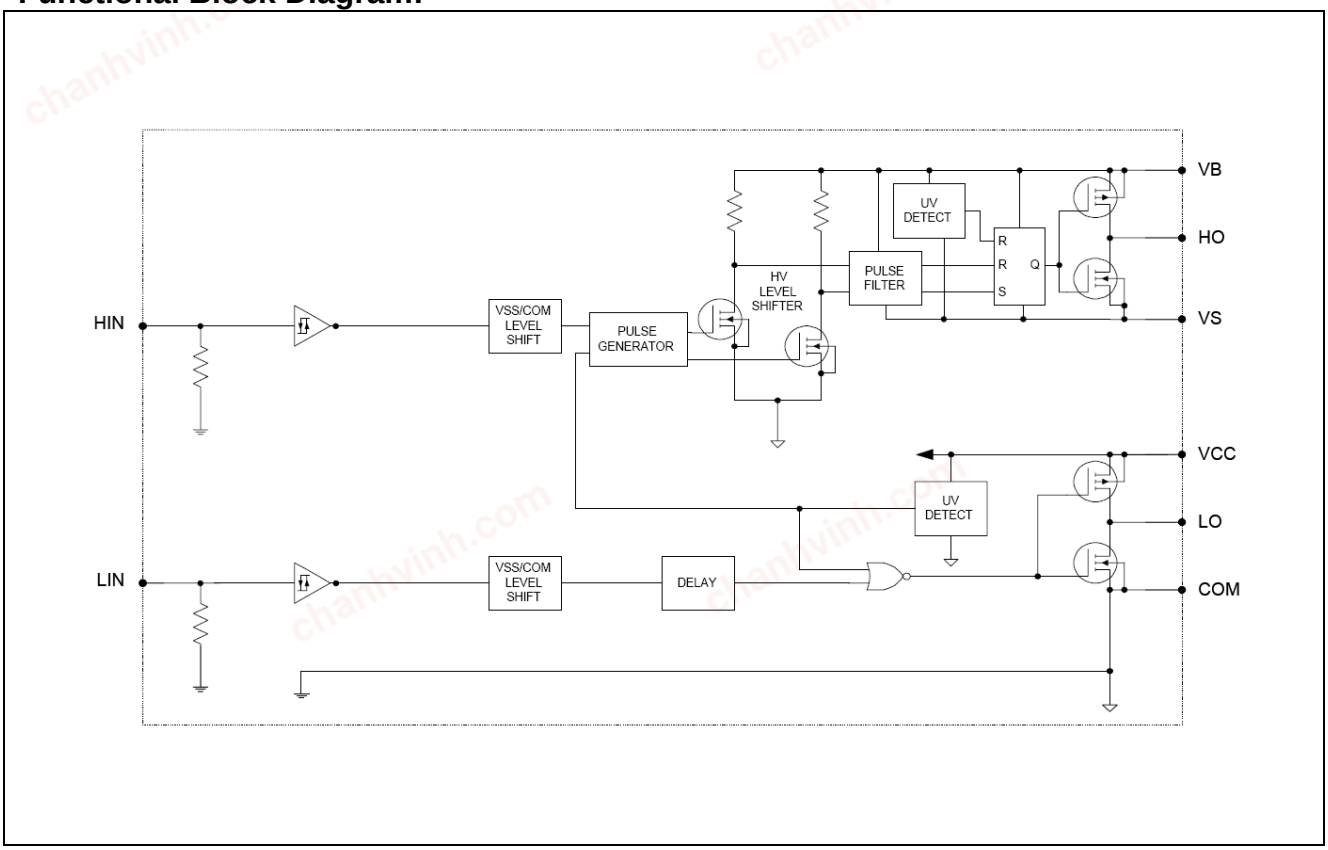
Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤125°C with bias conditions of V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF.

Symbol	Definition	Min	Typ	Max	Units	Test conditions
t_{on}	Turn-on propagation delay	—	220	300	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	130	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		

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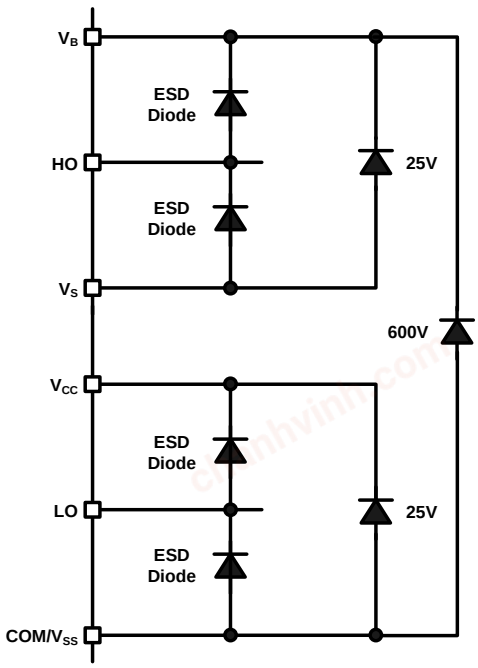
Functional Block Diagram:

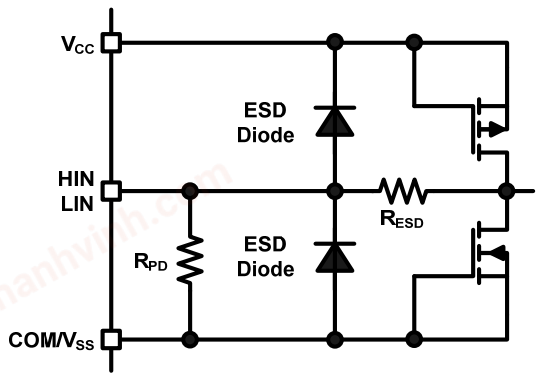


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Input/Output Pin Equivalent Circuit Diagrams:





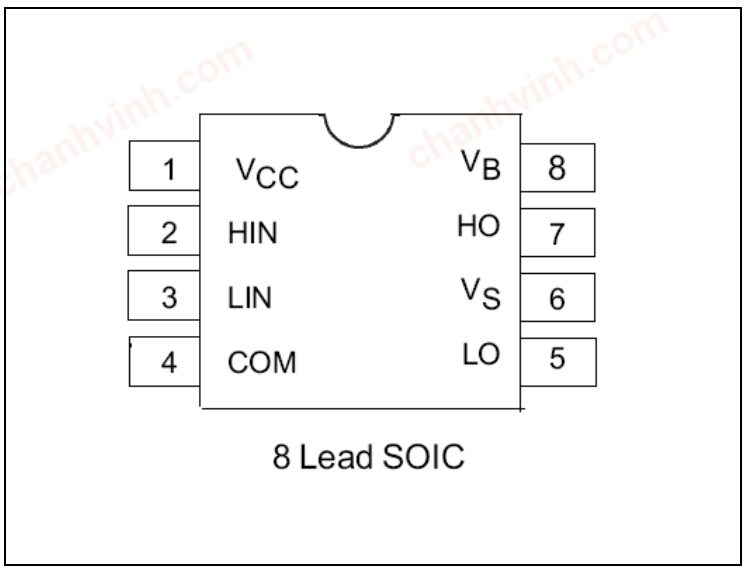
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Lead Definitions:

PIN#	Symbol	Description
1	V_{CC}	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver outputs (HO), in phase with HO
3	LIN	Logic input for low-side gate driver outputs (LO), in phase with LO
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

Lead Assignments



8 Lead SOIC

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Application Information and Additional Details

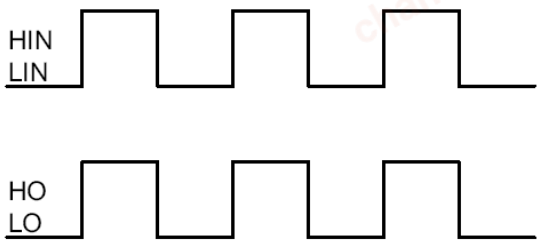


Figure 1: Input/Output Timing Diagram

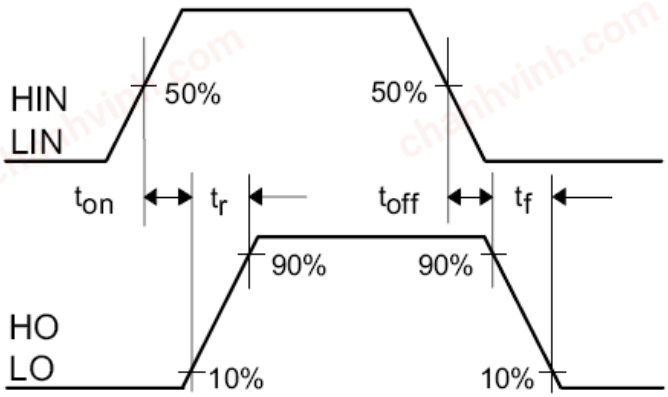


Figure 2: Switching Time Waveform Definitions

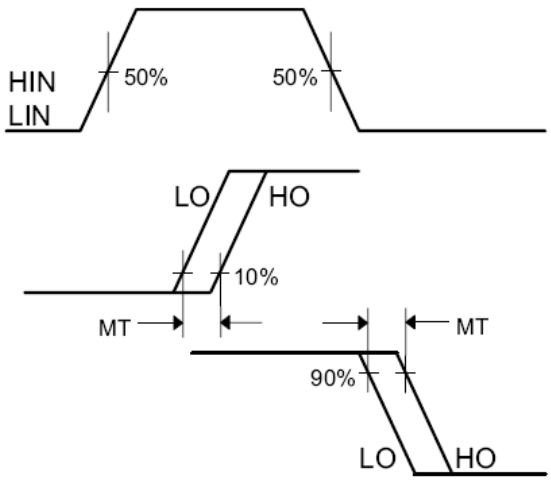


Figure 3: Delay Matching Waveform Definitions

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Tolerability to Negative VS Transients

The AUIRS2301S has been seen to withstand negative V_S transient conditions on the order of -25V for a period of 100 ns (V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C).
An illustration of the AUIRS2301S performance can be seen in Figure 4.
Even though the AUIRS2301S has been shown able to handle these negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

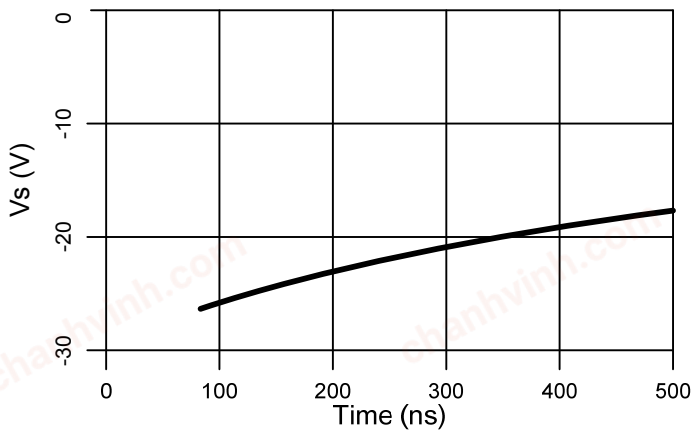


Figure 4: -Vs Transient results

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Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS2301S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

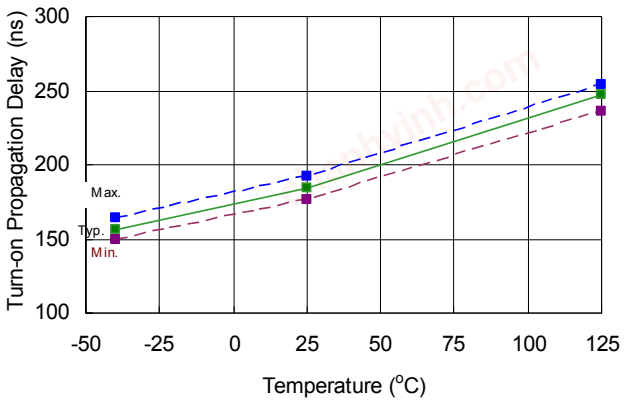


Figure 5: T_{ON} vs. temperature

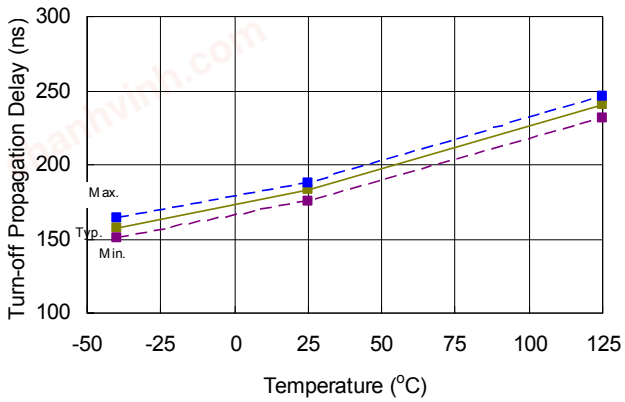


Figure 6: T_{OFF} vs. temperature

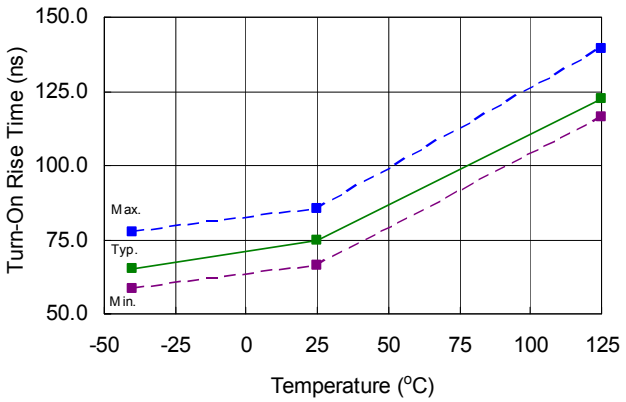


Figure 7: T_R vs. temperature

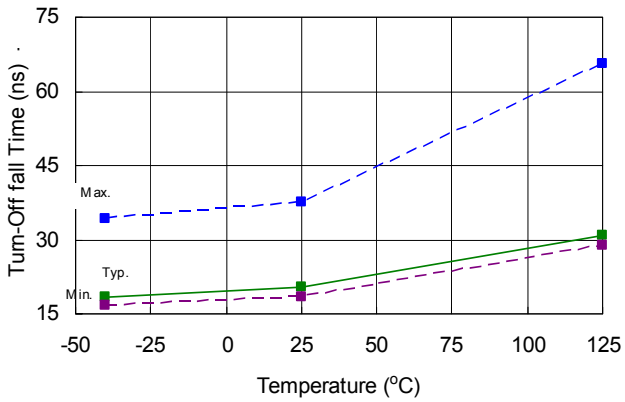


Figure 8: T_F vs. temperature

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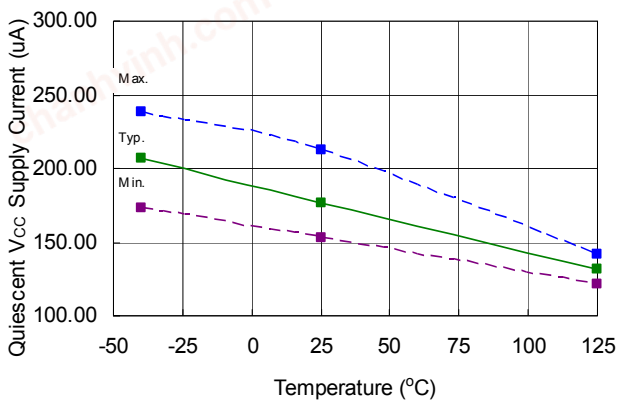


Figure 9: V_{CC} supply current vs. temperature

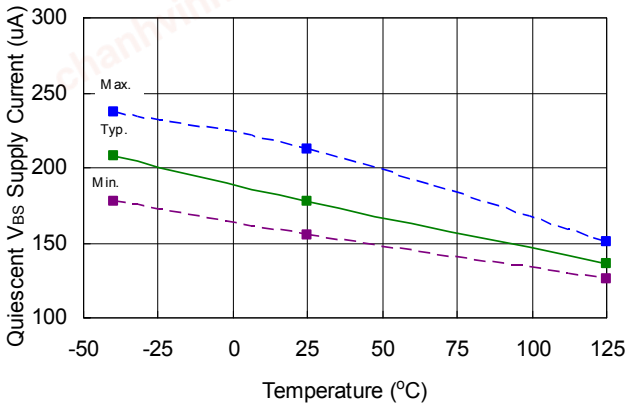


Figure 10: V_{BS} supply current vs. temperature

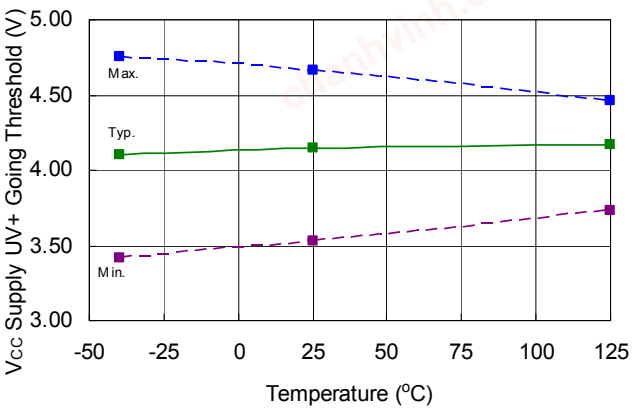


Figure 11: V_{CCUV+} vs. temperature

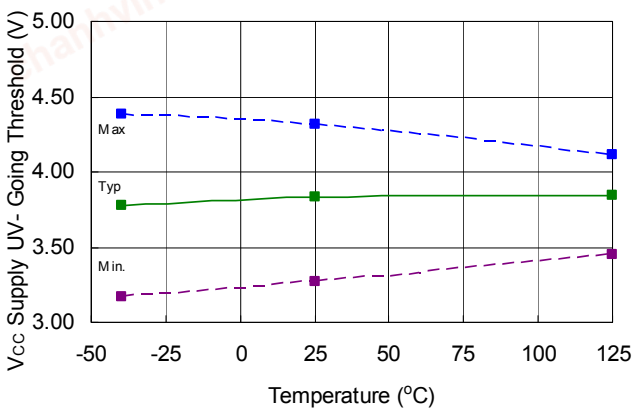


Figure 12: V_{CCUV-} vs. temperature

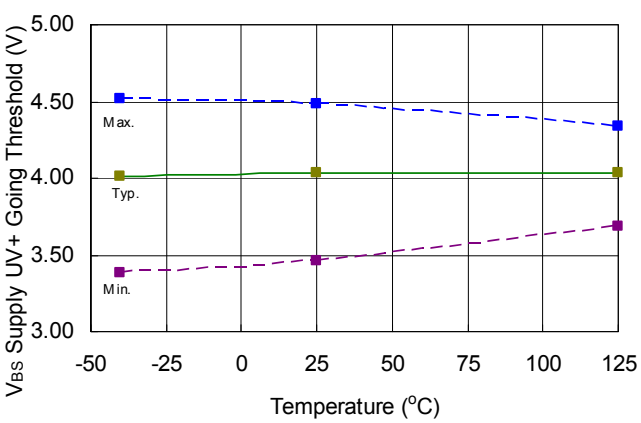


Figure 13: V_{BSUV+} vs. temperature

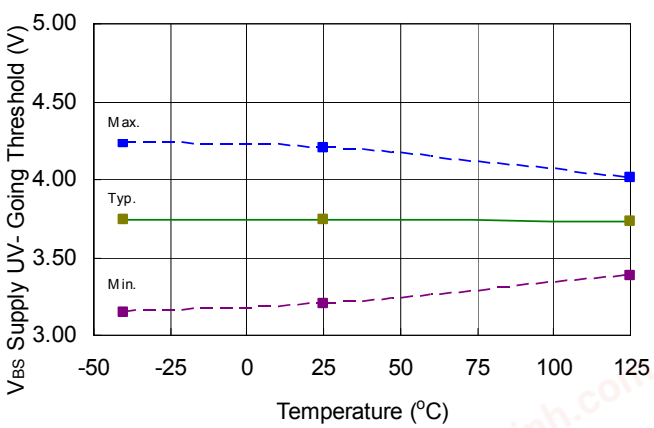


Figure 14: V_{BSUV-} vs. temperature

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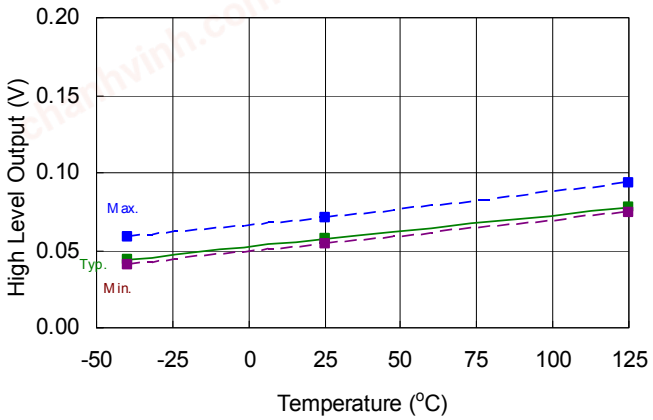


Figure 15: V_{OH} (I_O = 2mA) vs. temperature

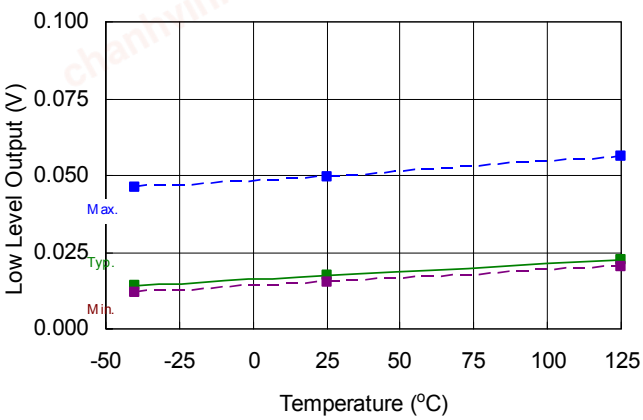


Figure 16: V_{OL} (I_O = 2mA) vs. temperature

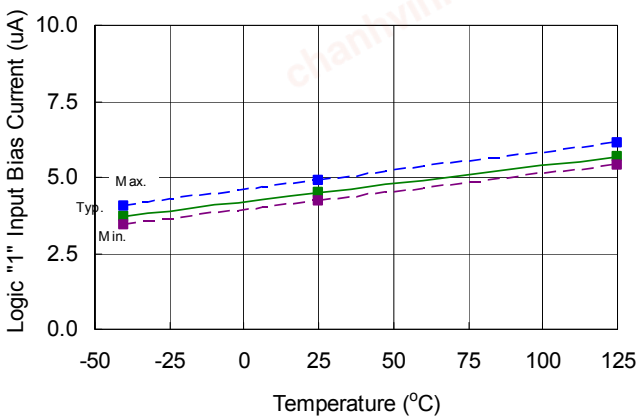


Figure 17: Logic “1” input Bias current vs. temperature

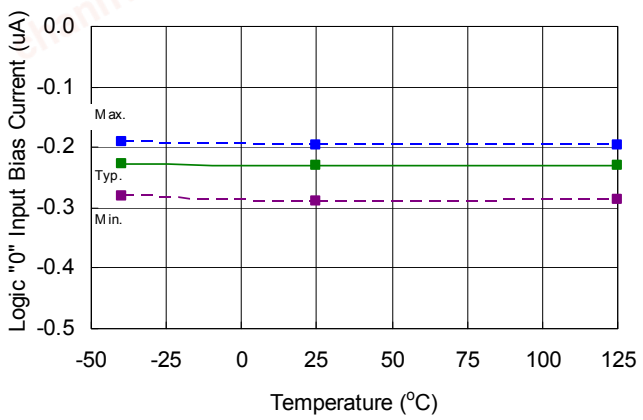


Figure 18: Logic “0” input bias current vs. temperature

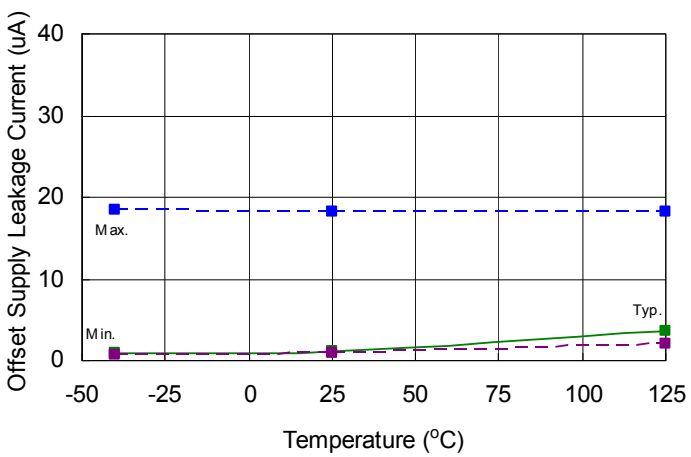
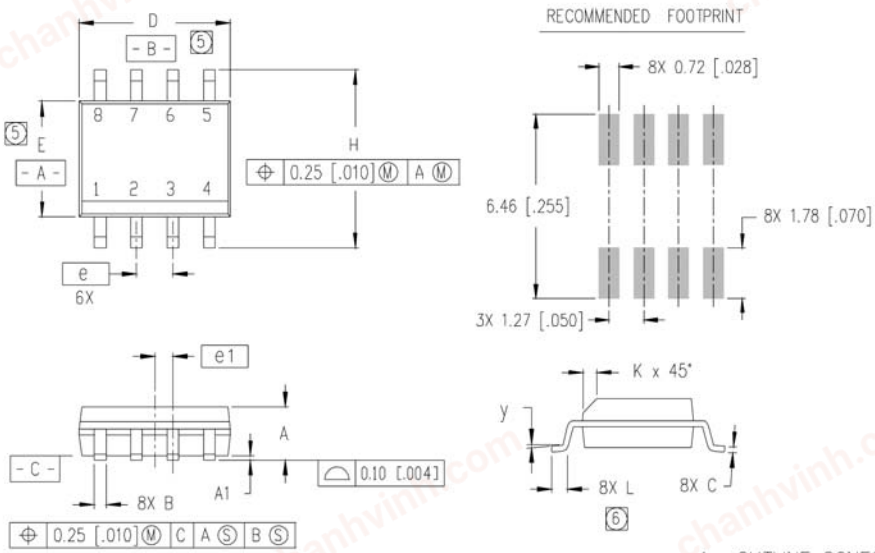


Figure 19: Offset leakage current vs. temperature

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Package Details



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

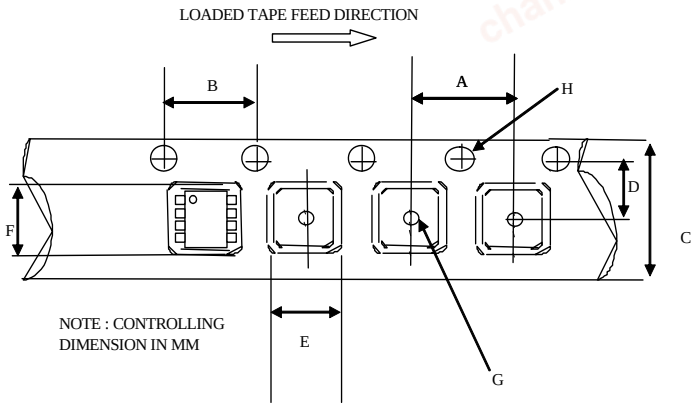
(6) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

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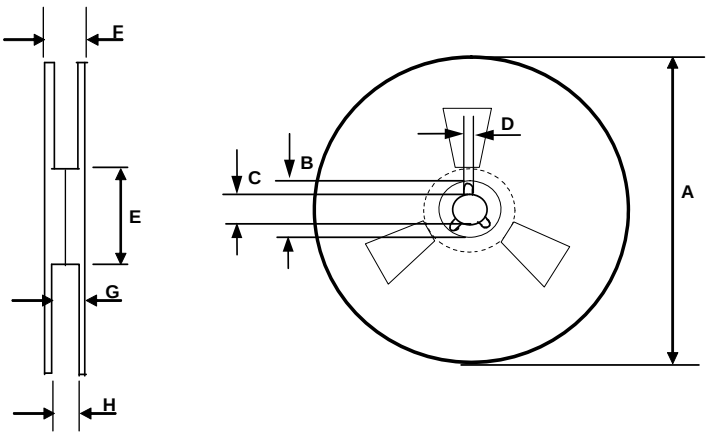
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Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



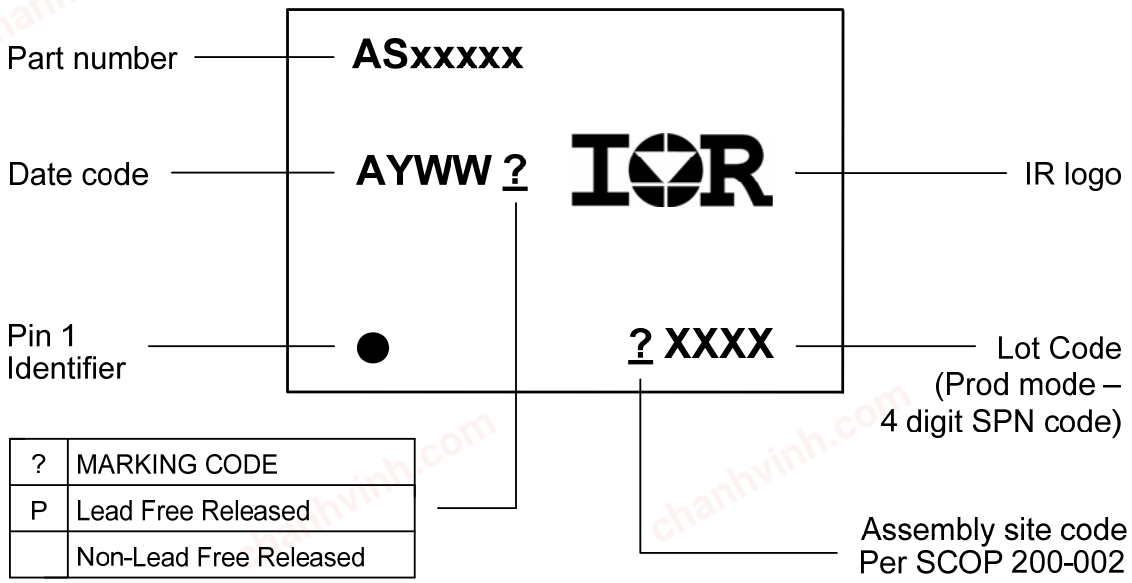
REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

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Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2301	SOIC8	Tube/Bulk	95	AUIRS2301S
		Tape and Reel	2500	AUIRS2301STR

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Revision History

Date	Comment
11/18/08	New template, standard pack quantity corrected
12/1/08	Removed Typical Applications section from the first page Changed I_{O+} & I_{O-} text from typ to min, min values were reported Updated all parameters to reflect the previously released Gen2 part, modifications can be made at a later date if need be Imported correct I/O diagrams
12/9/08	Added Pin# in lead assignment table and changed the order
2/6/09	Changed ESD/LU ratings to TBD pending data
3/3/9	Removed PDIP
3/4/09	Removed “Parameter Temp Trend” section (updated page number references as well) Modified page header to read “2301” in place of “2103” Changed IQCC from 50/120/190uA to 60/150/240uA Changed IQBS from 20/60/100uA to 60/150/240uA
6/2/09	Feature comparison removed on p3 Qual table updated
6/9/09	F front page: - HIGH AND LOW SIDE DRIVER in place of HALF BRIDGE DRIVER (no cross conduction prevention logic, no dead time). - “Logic and power ground ± 5V offset” sentence removed (only COM exists as ground pin). Page3: “designed for minimum driver cross-conduction” sentence erased. Page 11: added this page with section “Tolerability to Negative VS Transients” (APBU review)
7/2/09	Updated IQCC/IQBS UL to 260uA from 240uA
7/9/09	Changed the year to 2009 in footer Removed “( )” in the part number in the description and file name Removed rows for PDIP in the Absolute Maximum Ratings Removed min spec on Io+/Io- since we don’t test this parameter on ATE Deleted “SOIC8” from qual table
7/15/09	T_A max temp changed from 150 to 125
7/28/09	Remove preliminary sign (DR3 approved)
7/30/09	Application section added in front page
9/8/09	ESD class modified MM M2 (was M3 based on the incorrect ESD summary)
9/14/09	Added ESD passing voltages
1/13/11	Added parameter temperature trends, updated test condition to tri-temp and important notice
1/14/11	Revised Io+/- to be typical value on front page

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