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International
IOR Rectifier

AUTOMOTIVE GRADE

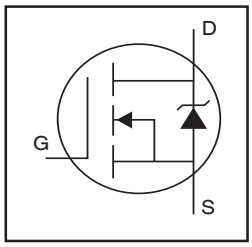
PD - 97676A

AUIRF1324WL

WIDELEAD HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 50% Lower Lead Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



$V_{(BR)DSS}$	24V
$R_{DS(on)}$ typ.	1.16mΩ
max.	1.30mΩ
$I_{D\ (Silicon\ Limited)}$	382A ①
$I_{D\ (Package\ Limited)}$	240A

Description

Specifically design for automotive applications this Widelead TO-262 package part has the advantage of having over 50% lower lead resistance and delivering over 20% lower Rds(on) when compared with a traditional TO-262 package housing the same silicon die. This greatly helps in reducing condition losses, achieving higher current levels or enabling a system to run cooler and have improved efficiency. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive and other applications.



TO-262 WideLead

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	382①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	270①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	240	
I_{DM}	Pulsed Drain Current ②	1530	
P_D @T_C = 25°C	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	530	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode Recovery ④	1.3	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.50	°C/W

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*Qualification standards can be found at http://www.irf.com/

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Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	24	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/°C	Reference to 25°C, I_D = 5mA ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.16	1.30	mΩ	V_{GS} = 10V, I_D = 195A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Transconductance	210	—	—	S	V_{DS} = 10V, I_D = 195A
R_G	Internal Gate Resistance	—	2.4	—	Ω	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 24V, V_{GS} = 0V
		—	—	250		V_{DS} = 19V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	120	180	nC	I_D = 195A
Q_{gs}	Gate-to-Source Charge	—	58	—		V_{DS} =12V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	36	—		V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	—	84	—		I_D = 195A, V_{DS} =0V, V_{GS} = 10V ⑤
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	V_{DD} = 16V
t_r	Rise Time	—	200	—		I_D = 195A
$t_{d(off)}$	Turn-Off Delay Time	—	75	—		R_G = 2.7Ω
t_f	Fall Time	—	110	—		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	—	7630	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	3390	—		V_{DS} = 19V
C_{rss}	Reverse Transfer Capacitance	—	1960	—		f = 1.0MHz, See Fig.5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	4660	—		V_{GS} = 0V, V_{DS} = 0V to 19V ⑦, See Fig.11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	—	4685	—		V_{GS} = 0V, V_{DS} = 0V to 19V ⑥

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	382①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	1530		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 195A, V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	—	46	69	ns	T_J = 25°C V_R = 20V,
		—	45	68		T_J = 125°C I_F = 195A
Q_{rr}	Reverse Recovery Charge	—	395	593	nC	T_J = 25°C di/dt = 100A/µs ⑤
		—	345	518		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	1.9	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.(Refer to AN-1140 http://www.irf.com/technical-info/appnotes/an-1140.pdf

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.028mH R_G = 50Ω, I_{AS} = 195A, V_{GS} =10V. Part not recommended for use above this value.

④ I_{SD} ≤ 195A, di/dt ≤ 600A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ R_θ is measured at T_J approximately 90°C.

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Qualification Information†

Qualification Level		Automotive (per AEC-Q101) ††	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		TO-262 WideLead	MSL1
ESD	Machine Model	Class M4 (+/- 425V)††† AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V)††† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V)††† AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

††† Highest passing voltage.

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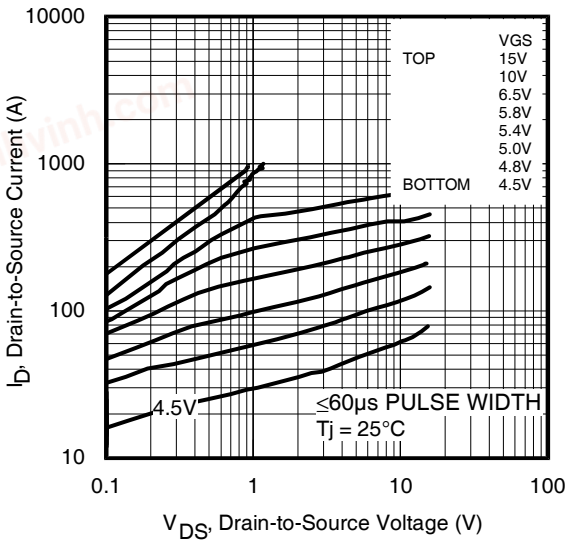


Fig 1. Typical Output Characteristics

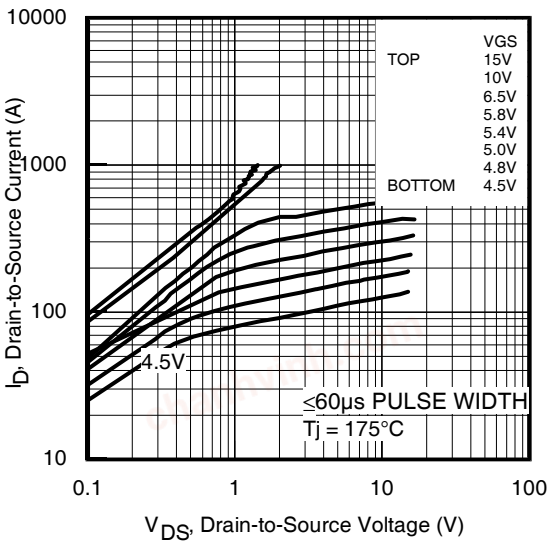


Fig 2. Typical Output Characteristics

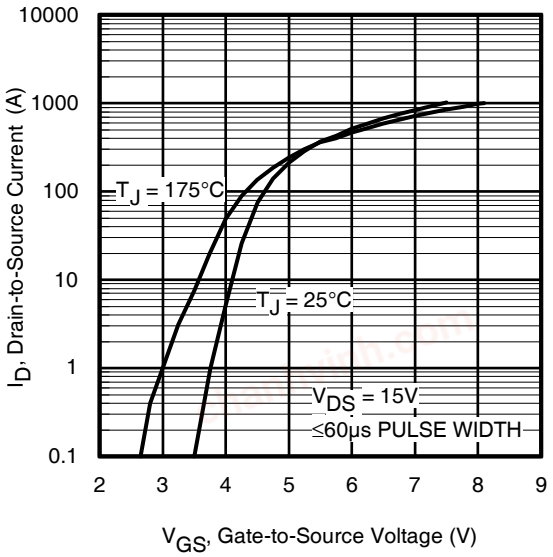


Fig 3. Typical Transfer Characteristics

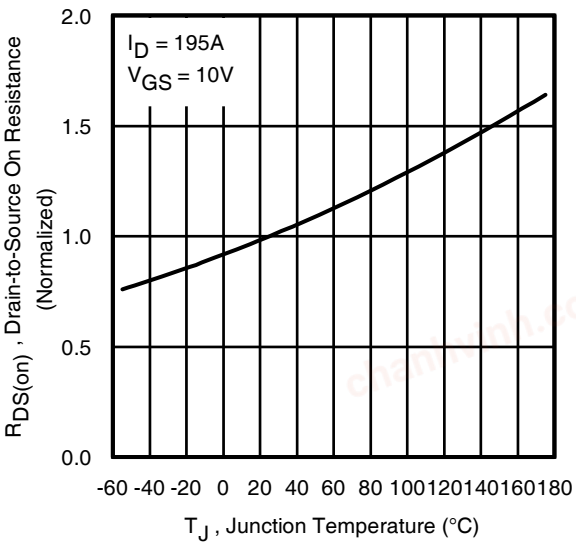


Fig 4. Normalized On-Resistance vs. Temperature

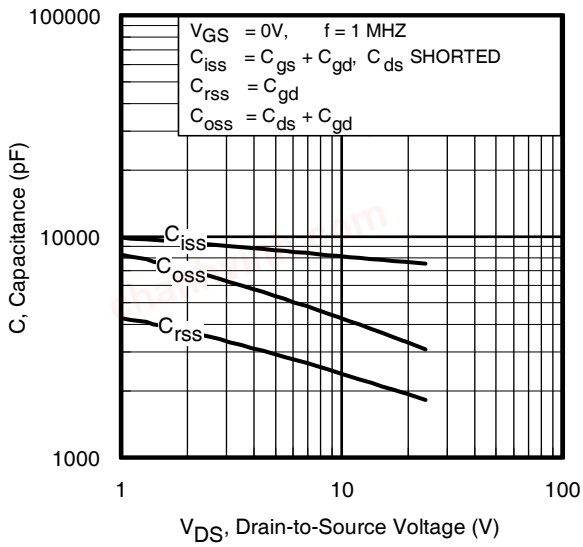


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

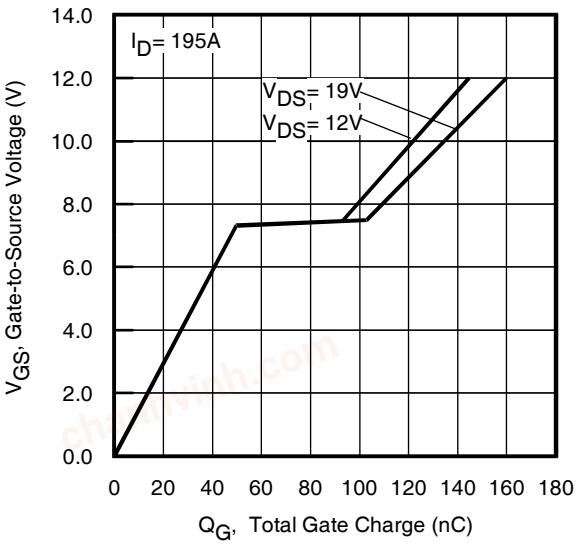


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

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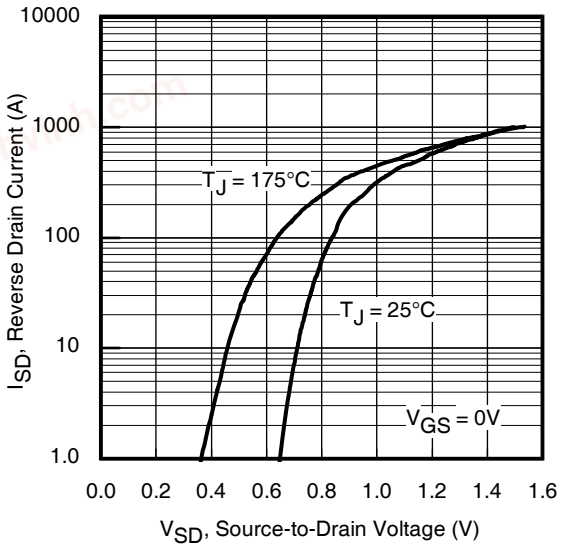


Fig 7. Typical Source-Drain Diode Forward Voltage

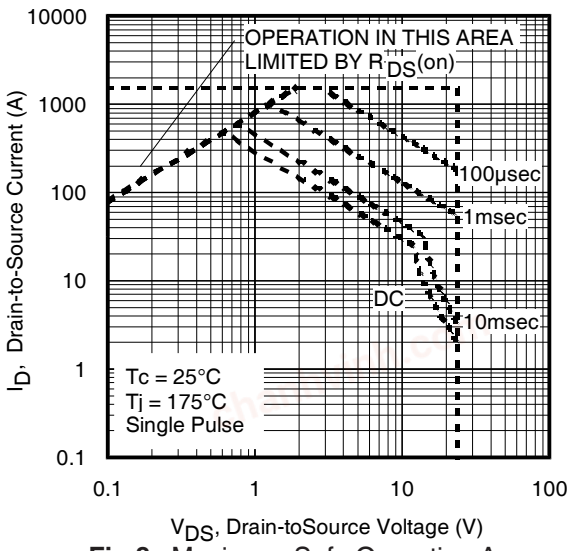


Fig 8. Maximum Safe Operating Area

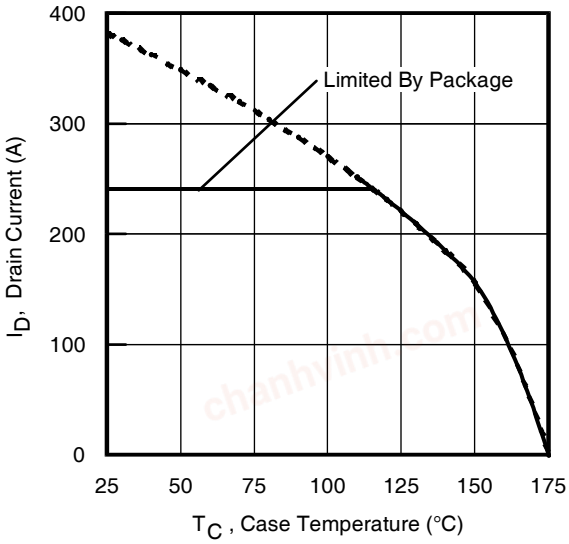


Fig 9. Maximum Drain Current vs. Case Temperature

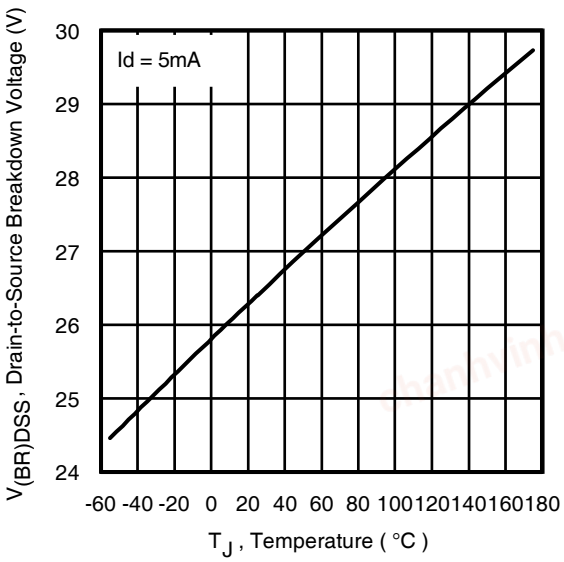


Fig 10. Drain-to-Source Breakdown Voltage

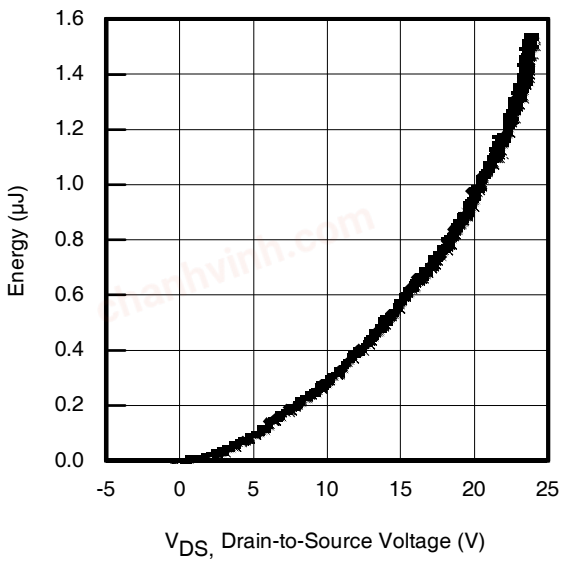


Fig 11. Typical C_{OSS} Stored Energy

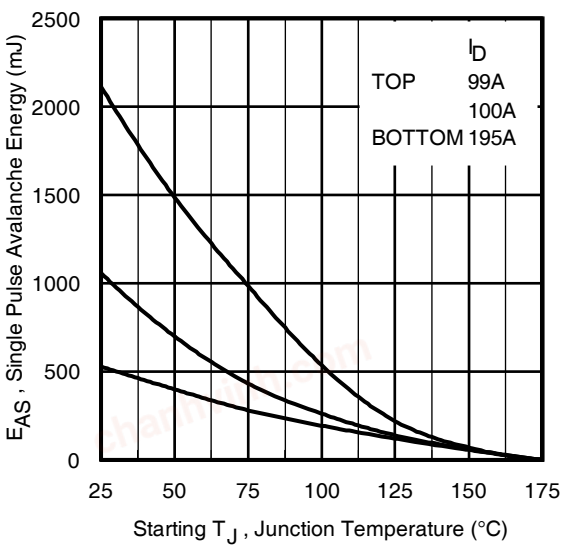


Fig 12. Maximum Avalanche Energy vs. DrainCurrent

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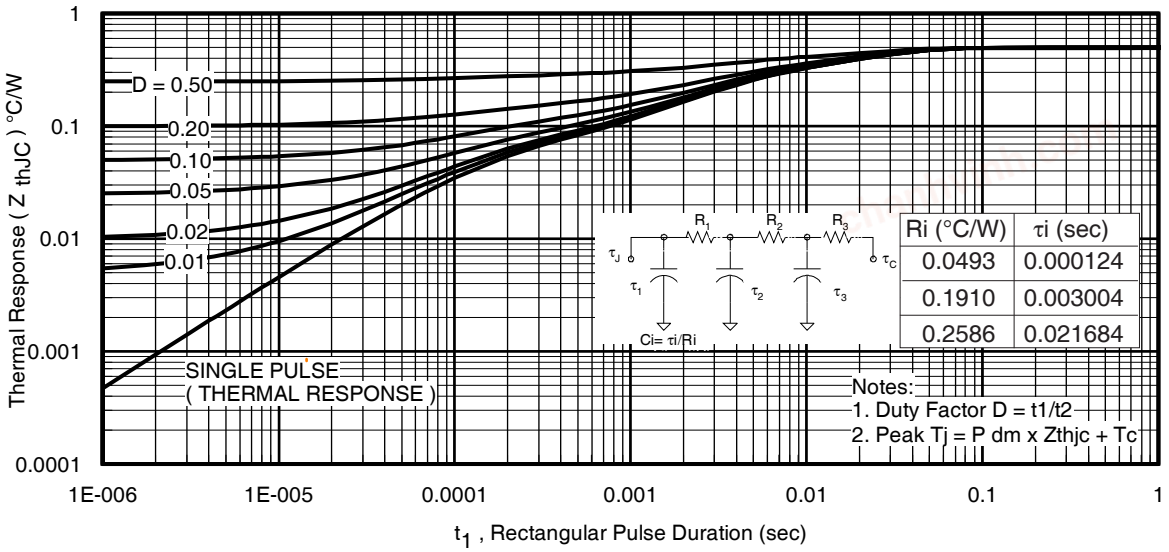


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

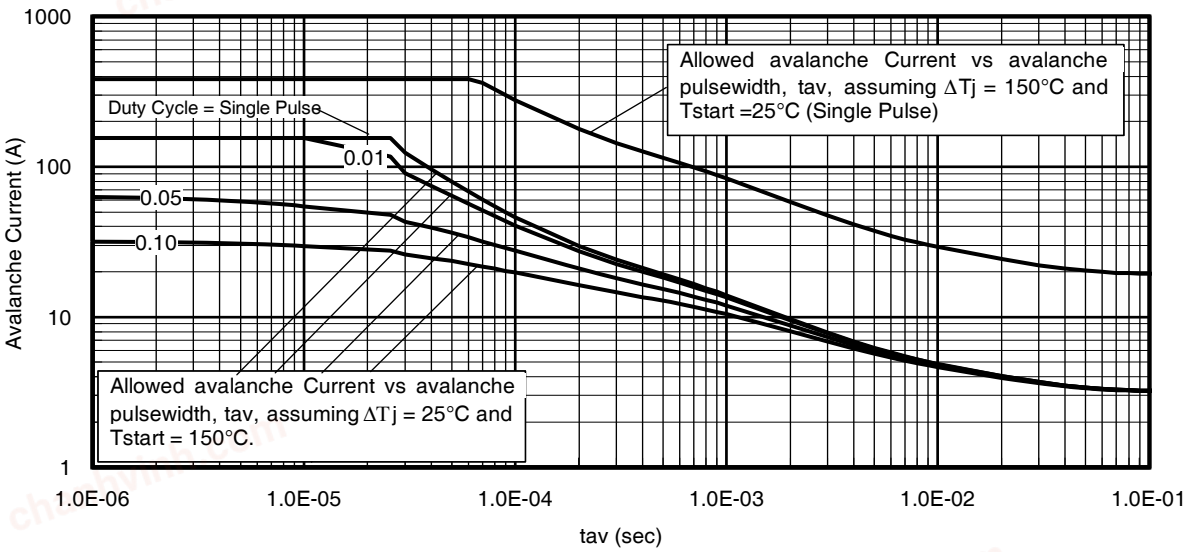


Fig 14. Typical Avalanche Current vs. Pulsewidth

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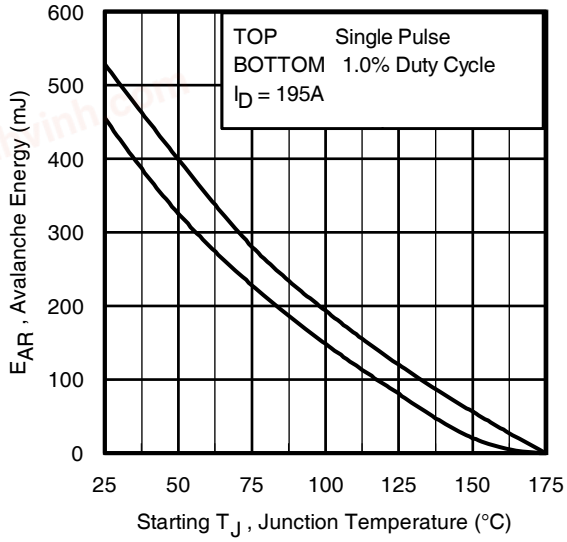


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figure 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

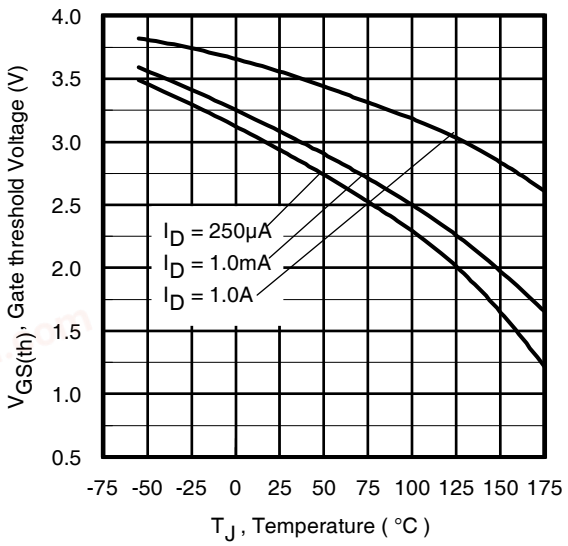


Fig 16. Threshold Voltage vs. Temperature

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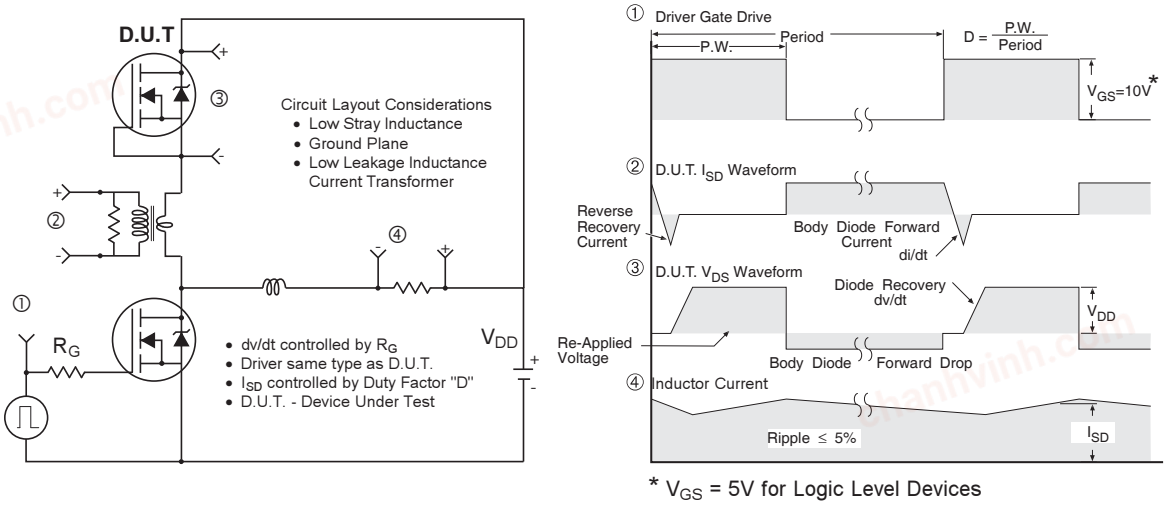


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

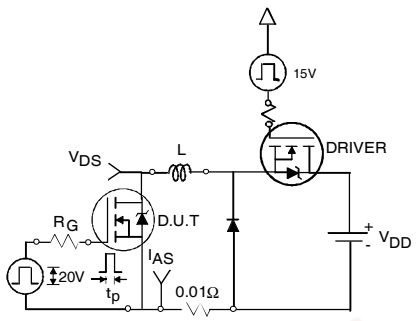


Fig 22a. Unclamped Inductive Test Circuit

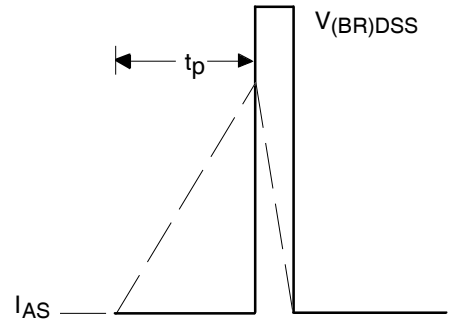


Fig 22b. Unclamped Inductive Waveforms

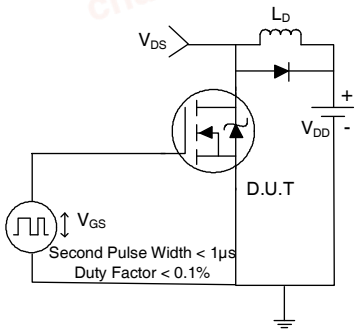


Fig 23a. Switching Time Test Circuit

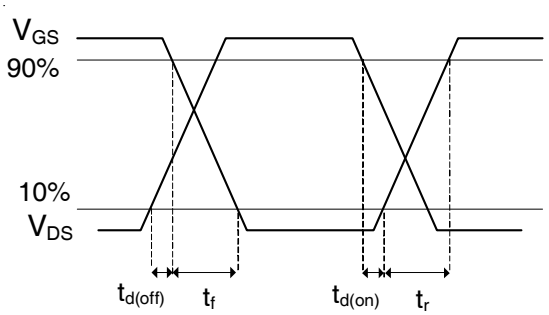


Fig 23b. Switching Time Waveforms

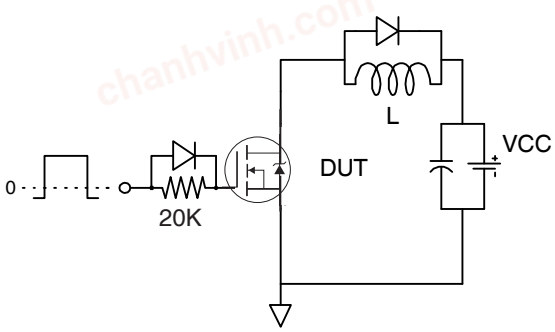


Fig 24a. Gate Charge Test Circuit

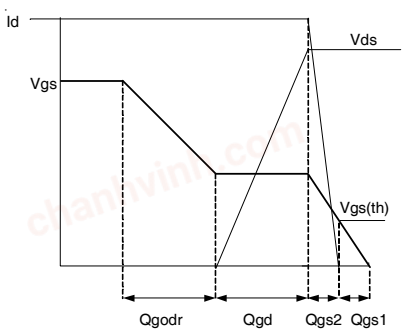
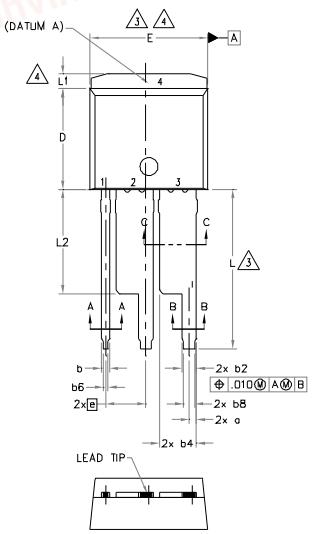


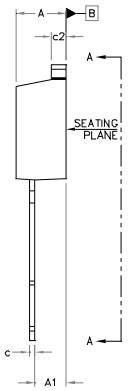
Fig 24b. Gate Charge Waveform

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TO-262 WideLead Package Outline

Dimensions are shown in millimeters (inches)





SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
a	0.20	0.51	.008	.020	
b	0.51	0.91	.020	.036	5
b1	0.51	0.81	.020	.032	
b2	1.07	1.47	0.42	.058	
b3	1.07	1.37	.042	.054	5
b4	3.05	3.45	.120	.136	
b5	3.05	3.35	.120	.132	5
b6	0.25	0.61	.010	.024	
b7	0.25	0.51	.010	.020	5
b8	0.76	1.17	.030	.046	
b9	0.76	1.07	.030	.022	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	8.48	.245	.334	4
e	3.81 BSC		.150 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	8.64	9.40	.340	.370	

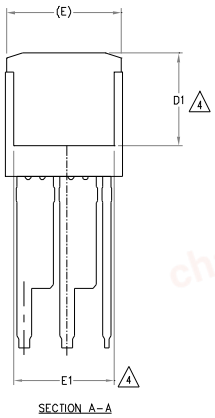
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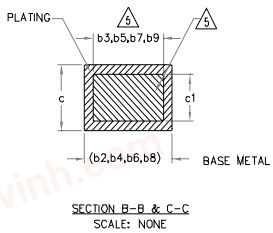
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b3, b5, b7, b9 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. – OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

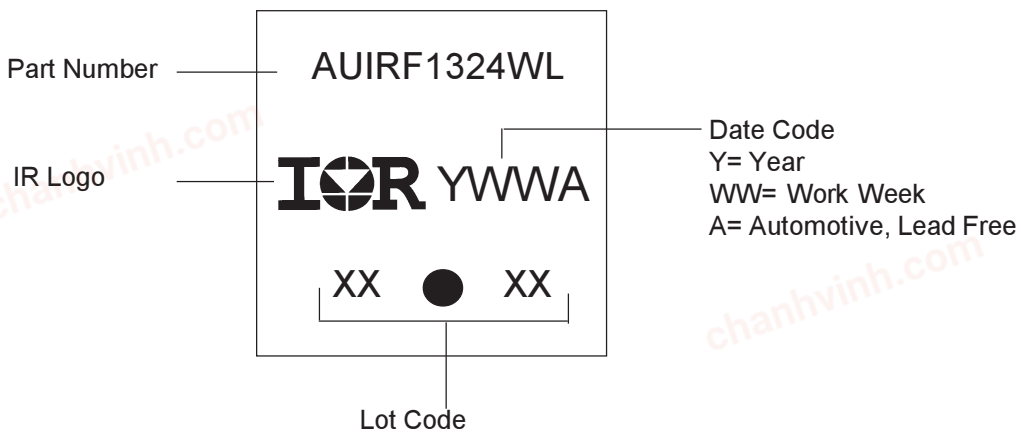
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE





TO-262 WideLead Part Marking Information



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF1324WL	TO-262 WideLead	Tube	50	AUIRF1324WL

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IMPORTANT NOTICE

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