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6ED2231S12T
1200 V Three Phase Gate Driver for IGBT/SiC with Integrated Bootstrap Diode and OCP

Features

- Infineon Thin-Film-SOI technology
- Fully operational to +1200 V
- Optimized for IGBT (insulated gate bipolar transistor) / SiC(Silicon carbide) MOSFET
- Integrated Ultra-fast Bootstrap Diode
- Floating channel designed for bootstrap operation
- Output source/sink current capability +0.35 A/-0.65 A
- Tolerant to negative transient voltage up to -100 V (Pulse width is up 700 ns) given by SOI-technology
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Over current protection with ±5% ITRIP threshold
- Fault reporting, automatic Fault clear and Enable function on the same pin (RFE)
- Matched propagation delay for all channels
- Integrated 460 ns deadtime protection
- Shoot-through (cross-conduction) protection
- V_{CC} support up to 25 V
- 2 kV HBM ESD

Product summary

V_{S_OFFSET}	≤ 1200 V
V_{CC}	= 13 V – 20 V
I_{O+} / I_{O-}(typ)	= + 0.35 A / - 0.65 A
t_{ON} / t_{OFF} (typ.)	= 700 ns/ 650 ns
Deadtime (typ.)	= 460 ns

Package



DSO-24 (DSO-28 with 4 pins removed)

Typical applications

- Industrial Drives
- Embedded inverters for Motor Control in Pumps, Fans
- Commercial Air Conditioning

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC78/20/22

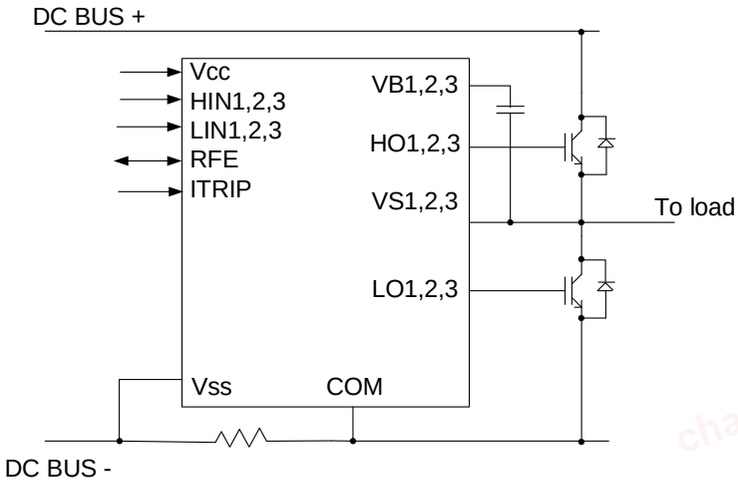
Ordering information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
6ED2231S12T	DSO-24	Tape and Reel	1000	6ED2231S12TXUMA1

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Description

The 6ED2231S12T is a high voltage, high speed power IGBT or SiC MOSFET gate driver with three independent high side and low side referenced output channels for three phase applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or TTL outputs, down to 3.3 V logic. An over-current protection (OCP) function which terminates all six outputs can also be derived from this resistor. An open drain FAULT signal is provided to indicate that an over-current or undervoltage shutdown has occurred. Fault conditions are cleared automatically after a delay programmed externally via an RC network. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive IGBTs or SiC MOSFETs in the high side configuration which operates up to 1200 V. Propagation delays are matched to simplify the HVIC's use in high frequency applications.



*(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to Application Notes & Design Tips for proper circuit board layout.

Figure 1 Typical application block diagram

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2 Electrical parameters

2.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 1 Absolute maximum ratings

Symbol	Definition	Min.	Max.	Units
V_{CC}	Low-side supply voltage	-0.3	25	
V_{IN}	Logic input voltage (LIN, HIN, RFE, ITRIP)	V_{SS} – 5	V_{CC} + 0.3	V
$V_{B\,1,2,3}$	High-side floating well supply voltage	-0.3	1225	
$V_{S\,1,2,3}$	High-side floating well supply return voltage [1]	$V_{B\,1,2,3}$ – 25	$V_{B\,1,2,3}$ + 0.3	
$V_{HO\,1,2,3}$	Floating gate drive output voltage	$V_{S\,1,2,3}$ – 0.3	$V_{B\,1,2,3}$ + 0.3	
$V_{LO\,1,2,3}$	Low-side output voltage	–0.3	V_{CC} + 0.3	
V_{SS}	Logic ground	V_{CC} -25	V_{CC}+ 0.3	
dV_S/dt	Allowable V_S offset supply transient relative to COM	—	50	V / ns
P_D	Package power dissipation @ $T_A \leq +25°C$		1.3	W
Rth_{JA}	Thermal resistance, junction to ambient		75	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

2.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. Recommended operating conditions

Table 2 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_{CC}	Low-side supply voltage	13	20	
V_{IN}	Logic input voltage (LIN, HIN, ITRIP)	V_{SS}	V_{SS} + 5	
V_{RFE}	RFE logic input voltage	V_{SS}	V_{CC}	
$V_{B1,2,3}$	High-side floating well supply voltage	$V_{S1,2,3}$ + 12	$V_{S1,2,3}$ + 20	
$V_{S1,2,3}$	High-side floating well supply offset voltage [1]	COM – 8	1200	
V_{St}	Transient High-side floating well supply offset voltage [2]	- 100	1200	
$V_{HO1,2,3}$	Floating gate drive output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low-side output voltage	0	V_{CC}	
V_{SS}	Logic ground	- 5	5	
T_A	Ambient temperature	-40	125	°C

1: Logic operational for V_S of -8V to +1200 V. Logic state held for V_S of -8V to -V_{BS}

2: In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins V_{CC} and V_{Bx}. Insensitivity of bridge output to negative transient voltage up to –100 V is not subject to production test – verified by design / characterization.

2.3 Static electrical characteristics

(V_{CC} - COM) = (V_B - V_S) = 15 V, V_{SS} = COM. T_A = 25 °C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads H_O or L_O. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

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Table 3 Static electrical characteristic

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	VBS supply under voltage positive threshold	11.5	12.2	12.9	V	
V_{BSUV-}	VBS supply under voltage negative threshold	10.6	11.3	12		
V_{BSUVHY}	VBS supply under voltage hysteresis	0.5	0.9	—		
V_{CCUV+}	VCC supply under voltage positive threshold	11.5	12.2	12.9		
V_{CCUV-}	VCC supply under voltage negative threshold	10.6	11.3	12		
V_{CCUVHY}	VCC supply under voltage hysteresis	0.5	0.9	—		
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	—	0.35	—		I_o = 20 mA
V_{OL}	Low level output voltage drop, V_O	—	0.15	—		
V_{IH}	Logic “1” input voltage	2.3	—	—		
V_{IL}	Logic “0” input voltage	—	—	0.7		
V_{RFE+}	RFE positive going threshold	1.7	1.9	2.3		
V_{RFE-}	RFE negative going threshold	0.7	0.9	1.1		
V_{ITRIP+}	ITRIP positive going threshold	0.475	0.500	0.525		
V_{ITRIP-}	ITRIP negative going threshold	0.425	0.450	0.475		
$V_{ITRIP\ HYS}$	ITRIP hysteresis	—	0.050	—		
I_{LK}	High-side floating well offset supply leakage	—	—	50	uA	V_B = V_S = 1200 V
I_{QBS}	Quiescent VBS supply current	—	175	250		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent VCC supply current	—	1000	1500		V_{IN} = 0 V or 5 V
$I_{O+\ mean}$	Mean output current for load capacity charging from 3 V (20%) to 6 V (40%)	200	300	—	mA	C = 22 nF
$I_{O-\ mean}$	Mean output current for load capacity discharging from 10.5 V (70%) to 7.5 V (50%)	400	600	—		C = 22 nF
I_{O+}	Output high short circuit pulsed current	—	350	—		V_O = 0 V PW ≤ 1 us
I_{O-}	Output low short circuit pulsed current	—	650	—		V_O = 15 V PW ≤ 1 us
I_{RFE+}	Logic “1” Input bias current (RFE)	—	0	1	uA	V_{RFE} = 3.3 V
I_{RFE-}	Logic “0” Input bias current (RFE)	1	0	—		V_{RFE} = 0 V
I_{IN+}	Logic “1” Input bias current (LIN, HIN)	—	1000	1250		V_{IN} = 5 V
I_{IN-}	Logic “0” Input bias current (LIN, HIN)	—	—	1		V_{IN} = 0 V
I_{ITRIP+}	Logic “1” Input bias current (ITRIP)	—	15	25		V_{IN} = 1 V
I_{ITRIP-}	Logic “0” Input bias current (ITRIP)	—	—	1		V_{IN} = 0 V
R_{BS}	Bootstrap diode on resistance	—	120	150	Ω	—
V_{FBSD}	Bootstrap diode forward voltage drop	—	0.9	—	V	I_o = 300 mA
$R_{ON,\ RFE}$	RFE mos resistance	—	40	60	Ω	—

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2.4 Dynamic electrical characteristics

V_{CC} = V_{BS}= 15 V, V_{SS} = COM, T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

Table 4 Dynamic electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	500	700	900	ns	V_S =0 V or 1200 V
t_{OFF}	Turn-off propagation delay	450	650	850		
t_R	Turn-on rise time	—	35	—		V_S =0 V
t_F	Turn-off fall time	—	20	—		
MT	Delay matching time (HS & LS turn-on/off)	—	—	130		V_S =0 V
DT	Deadtime: LO Turn-off to HO Turn-on & HO Turn-off to LO turn-on	300	460	700		V_S =0 V
$T_{FIL,IN}$	Input noise filter time	200	350	500		
t_{EN}	Enable low to output shutdown propagation delay	—	600	—		V_S =0 V or 1200 V
T_{ITRIP}	ITRIP to output shutdown propagation delay	—	750	1250		V_{ITRIP} = 1 V
T_{BL}	ITRIP blanking time	—	500	—		
T_{FLT}	ITRIP to FAULT propagation delay	450	650	900		
T_{FLTCLR}	FAULT clear time (R = 2 MΩ, C = 1 nF)	—	1.9	—	ms	VDD = 3.3 V

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3 Block diagram

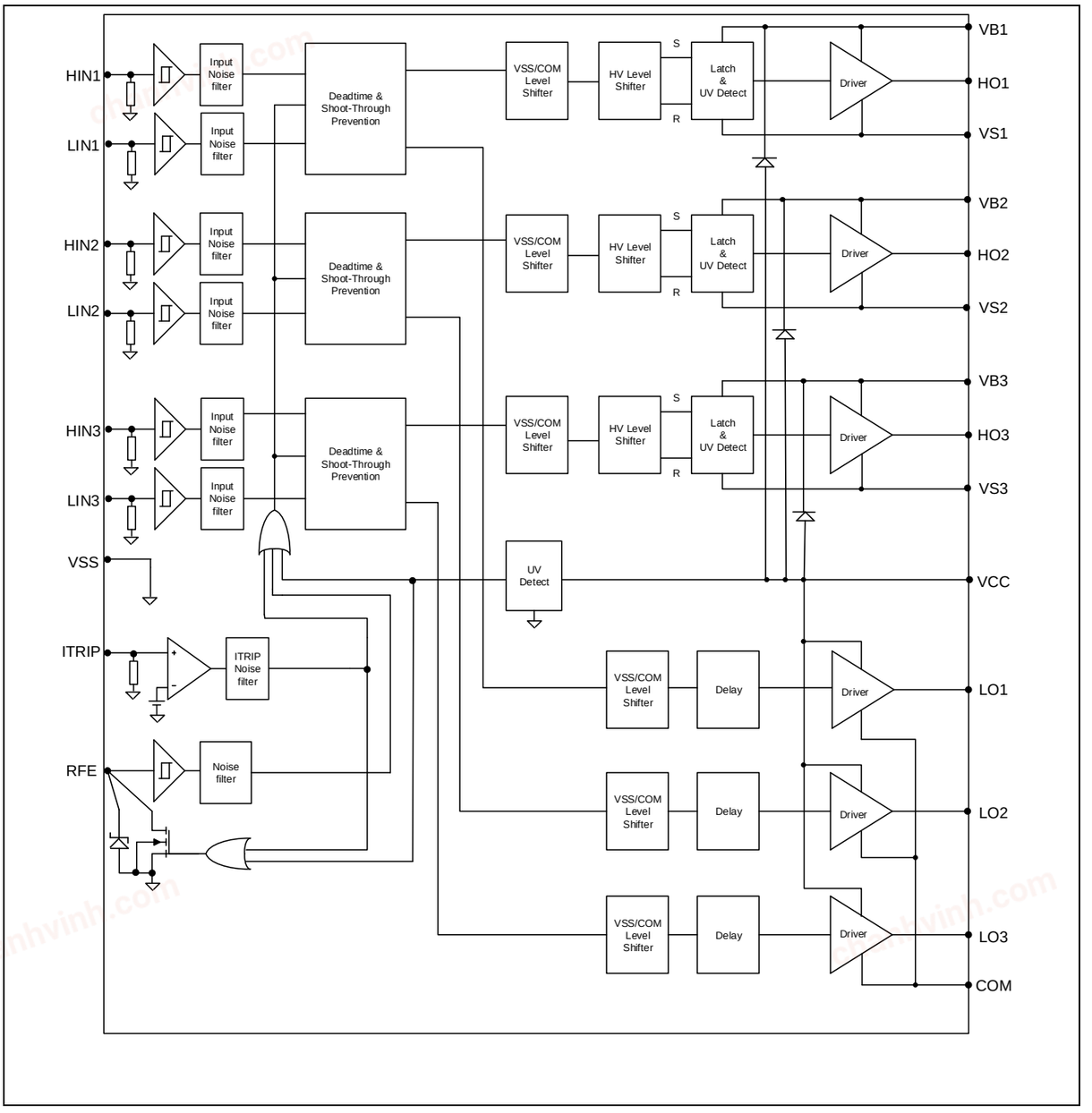


Figure 2 Functional block diagram

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4 Pin configuration and functionality

4.1 Pin configuration

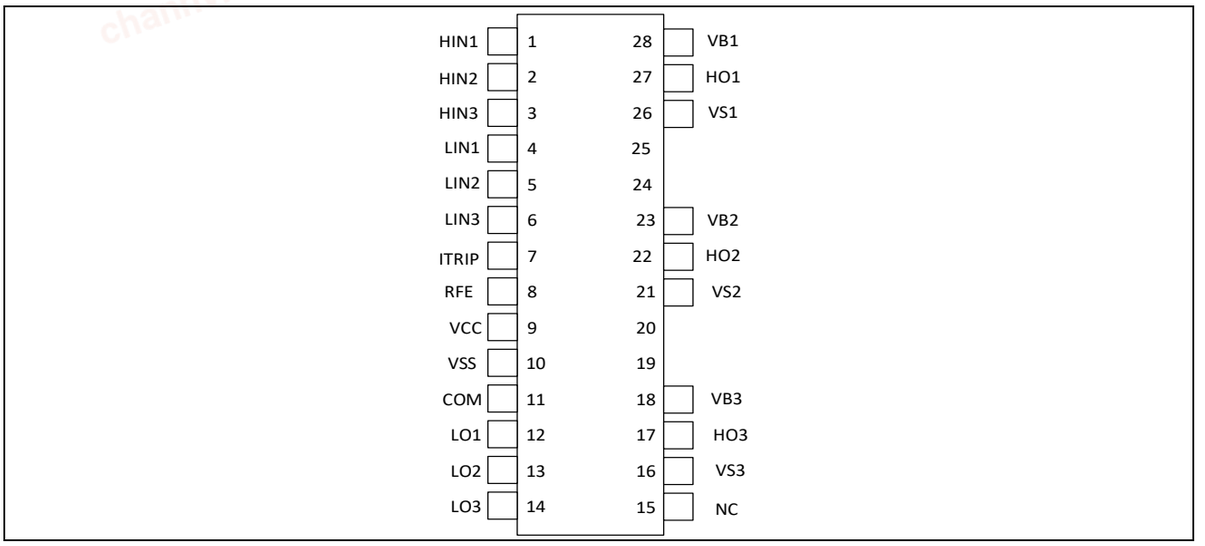


Figure 3 6ED2231S12T pin assignments (top view

4.2 Pin functionality

Table 5

Symbol	Description
HIN1,2,3	Logic input for high side gate driver output (HO), in phase
LIN1,2,3	Logic input for low side gate driver output (LO), in phase
$V_{B1,2,3}$	High side floating supply
HO1,2,3	High side gate drive output
$V_{S1,2,3}$	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return
V_{SS}	Logic ground
ITRIP	Analog input for over-current shutdown. When active, ITRIP shuts down outputs and activates RFE low. When ITRIP becomes inactive, RFE stays active low for an externally set time tFLTCLR, then automatically becomes inactive (open-drain high impedance).
RFE	Integrated fault reporting function like over-current (ITRIP), or low-side undervoltage lockout and the fault clear timer. This pin has negative logic and an open-drain output. The use of over-current protection requires the use of external components.

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5 Application information and additional details

Information regarding the following topics are included as subsections within this section of the datasheet.

- IGBT or SiC MOSFET gate drive
- Switching and timing relationships
- Deadtime
- Matched propagation delays
- Input logic compatibility
- Undervoltage lockout protection
- Shoot-Through protection
- Enable input
- Fault reporting and programmable fault clear timer
- Over-Current protection
- Truth table: Undervoltage lockout, ITRIP, and ENABLE
- Advanced input filter
- Short-Pulse / Noise rejection
- Ultra fast, Integrated bootstrap diodes
- Negative Vs transient SOA
- PCB layout tips
- Additional documentation

5.1 IGBT or SiC MOSFET gate drive

The 6ED2231S12T HVICs are designed to drive IGBT or SiC MOSFET power devices. ***Figure 4*** and ***Figure 5*** illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as IO. The voltage that drives the gate of the external power switch is defined as V_{OUT}.

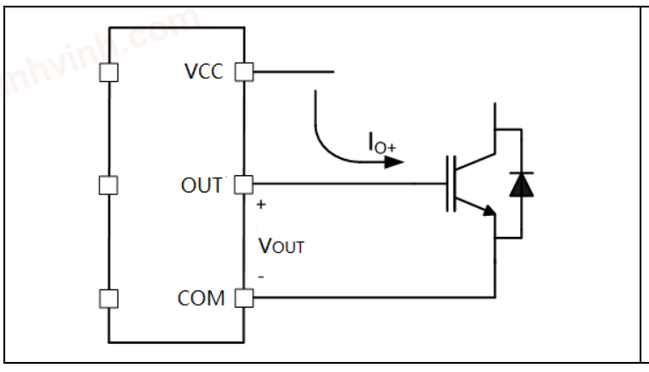


Figure 4 HVIC Sourcing current

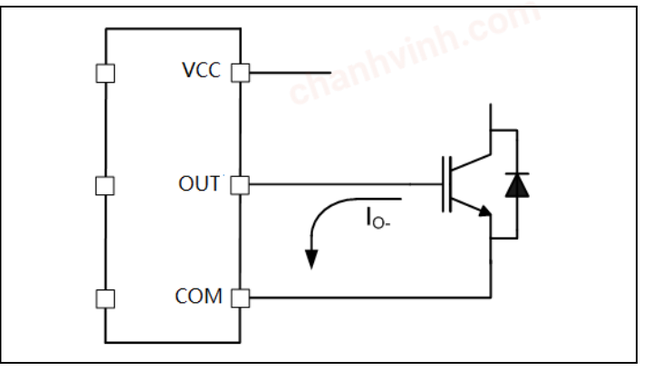


Figure 5 HVIC Sinking current

5.2 Switching relationships

The relationships between the input and output signals of the 6ED2231S12T are illustrated below in ***Figure 6***. We can see the definitions of several timing parameters (i.e. t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

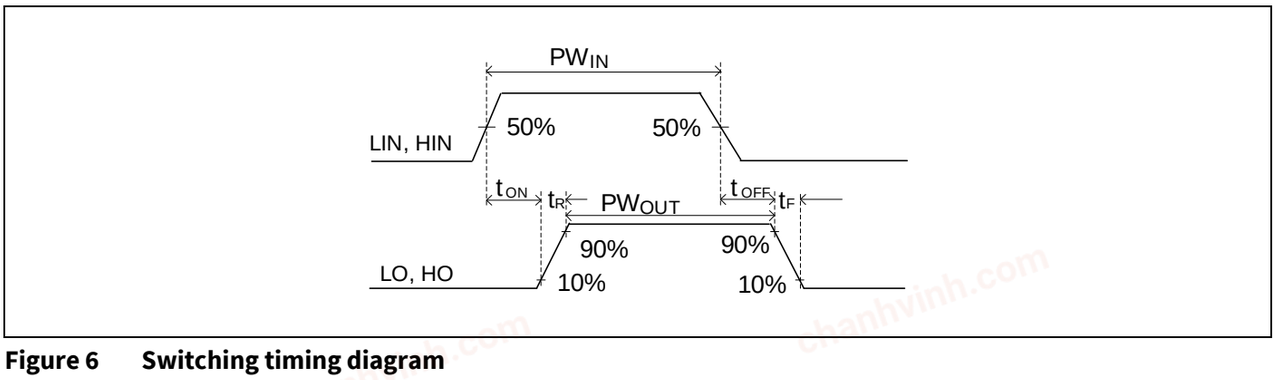


Figure 6 Switching timing diagram

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5.3 Timing diagram

Here below ***Figure 7*** and ***Figure 8*** illustrate the timing relationships of some of the functionality of the 6ED2231S12T; this functionality is described in further detail later in this document. During interval A of ***Figure 7***, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has. HVIC is keeping on output channel that is already on ignoring the 2nd input signal.

Interval B of ***Figure 7*** and ***Figure 8*** shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HO has returned to the low state; LO is also held low), and a fault condition is reported on the RFE pin, which goes 0V. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RFE pin charges up to VRFE+ threshold; the charging characteristics are dictated by the RC network attached to the RFE pin. After fault clear time HVIC is waiting for a new input signal on LIN/HIN before activate the output stage (LO/HO).

During interval C of ***Figure 7*** and ***Figure 9***, we can see that the RFE pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); these results in the outputs (HO and LO) being held in the low state until the RFE pin is pulled high. After an enable event HVIC will wait for a new input signal on LIN/HIN before activate the output stage (LO/HO).

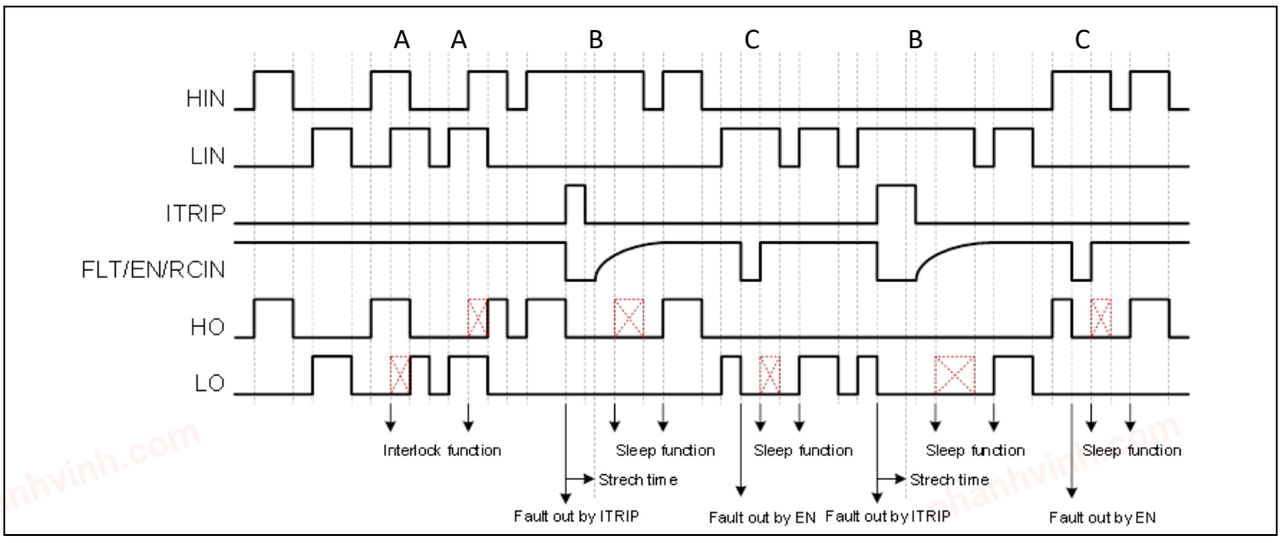


Figure 7 Input/output timing diagram

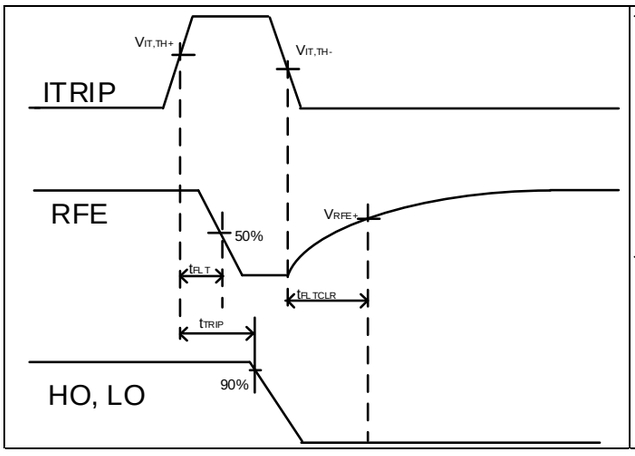


Figure 8 Detailed view of B interval

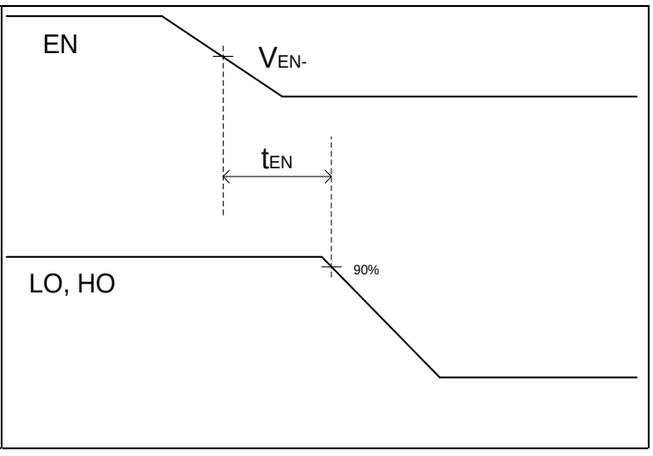


Figure 9 Detailed view of C interval

5.4 Deadtime and matched propagation delays

The 6ED2231S12T features integrated deadtime protection circuitry. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserter whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. ***Figure 10*** illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of 6ED2231S12T is matched with respect to the high- and low-side outputs. ***Figure 10*** defines the two deadtime parameters (i.e., DT_{LO-HO} and DT_{HO-LO}).

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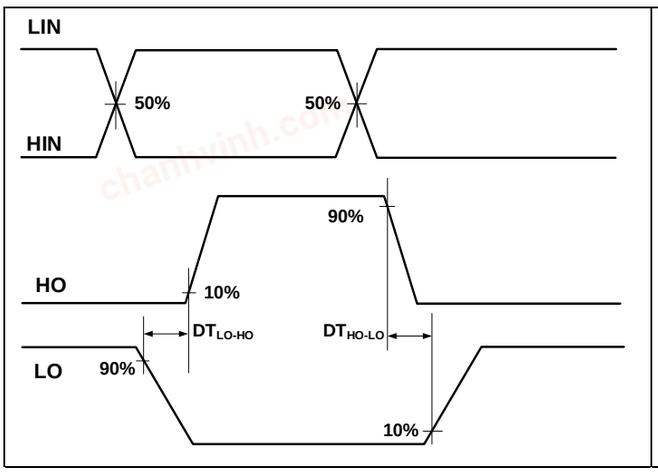


Figure 10 Dead Time Definitions

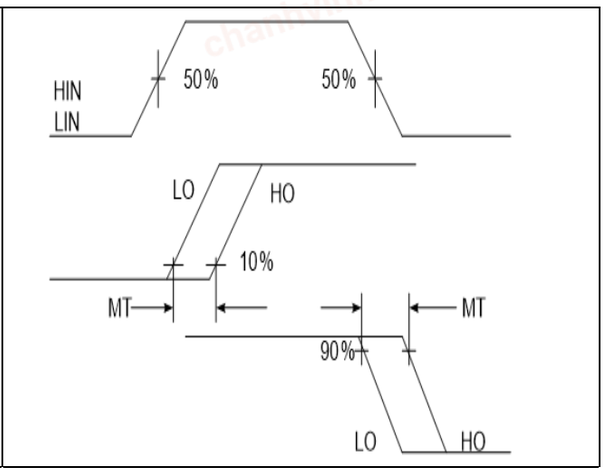


Figure 11 Delay Matching Waveform Definitions

The 6ED2231S12T is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the 6ED2231S12T is matched to the propagation turn-on delay (t_{OFF}).

5.5 Input logic compatibility

The input pins of are based on a TTL and CMOS compatible input-threshold logic that is independent of the Vcc supply voltage. With minimum high threshold (V_{IH}) of 2.3 V and maximum low threshold (V_{IL}) of 0.7 V, along with very little temperature variation as summarized in ***Figure 12***, the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 0.9 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 6ED2231S12T also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 6ED2231S12T features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram. The 6ED2231S12T has input pins that are capable of sustaining voltages higher than the bias voltage applied on the Vcc pin of the device.

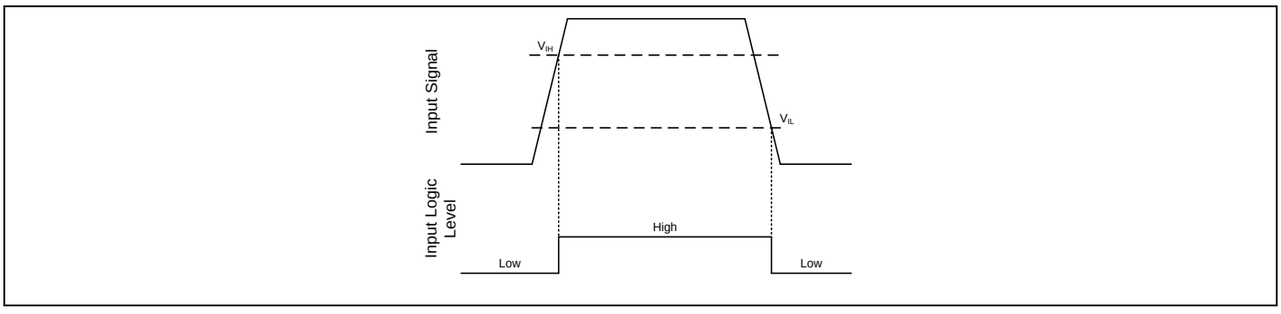


Figure 12 HIN & LIN input thresholds

5.6 Undervoltage lockout

6ED2231S12T provides undervoltage lockout protection on both the VCC (logic and low-side circuitry) power supply and the VBS (high-side circuitry) power supply. ***Figure 13*** is used to illustrate this concept; VCC (or VBS) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the VCC voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the VCC voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the VBS voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the VBS voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

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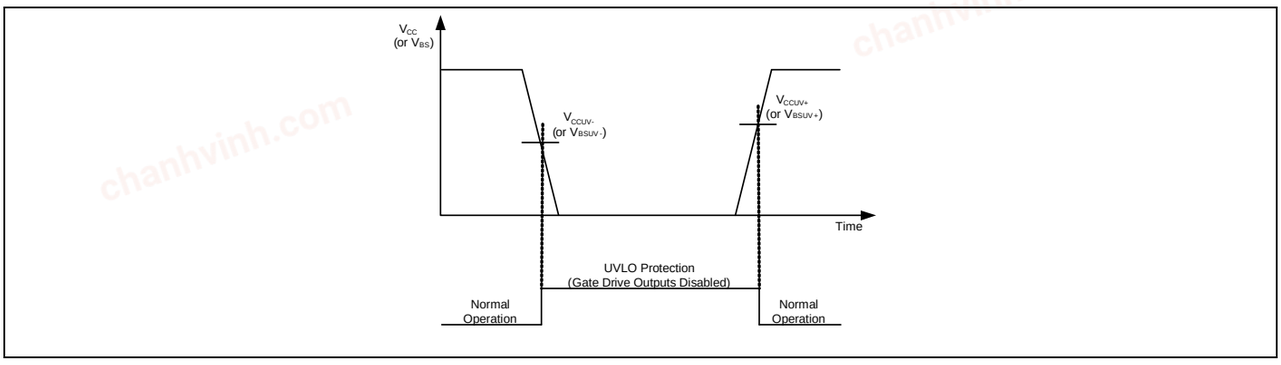


Figure 13 UVLO protection

5.7 Shoot-through protection

The 6ED2231S12T is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). ***Figure 14*** shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.

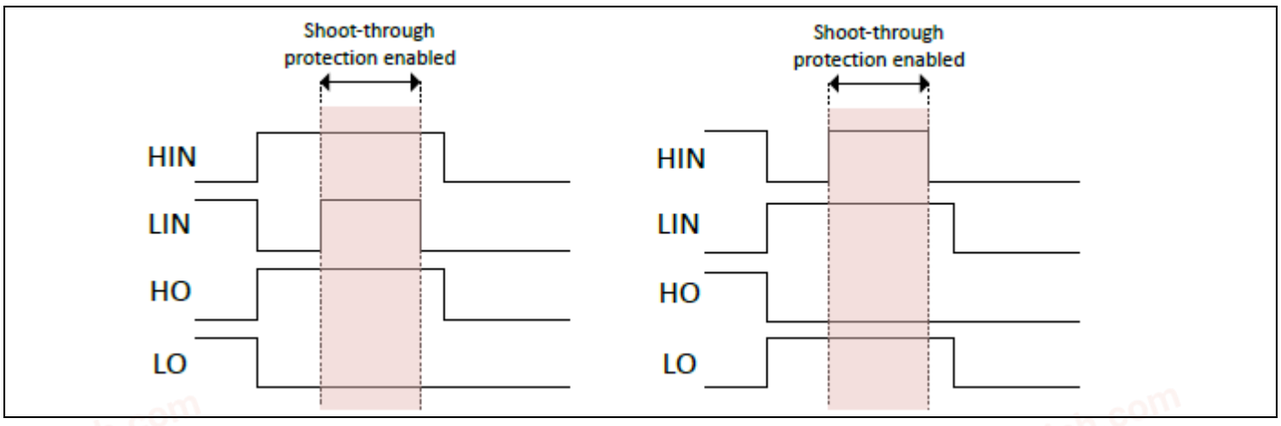


Figure 14 Illustration of shoot-through protection circuitry

5.8 Enable, Fault reporting and programmable fault clear timer

The 6ED2231S12T provides an enable functionality that allows it to shutdown or enable the HVIC and also provides an integrated fault reporting output along with an adjustable fault clear timer. There are two situations that would cause the IC to report a fault via the RFE pin. The first is an undervoltage condition of VCC and the second is if the over-current feature has recognized a fault. Once the fault condition occurs, the RFE pin is internally pulled to VSS and the fault clear timer is activated. The RFE output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the RFE pin will return to its external pull-up voltage.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RFE} and C_{RFE}. ***Figure 15*** shows that R_{RFE} is connected between the external supply (V_{DD})[1)] and the RFE pin, while C_{RFE} is placed between the RFE and VSS pins.

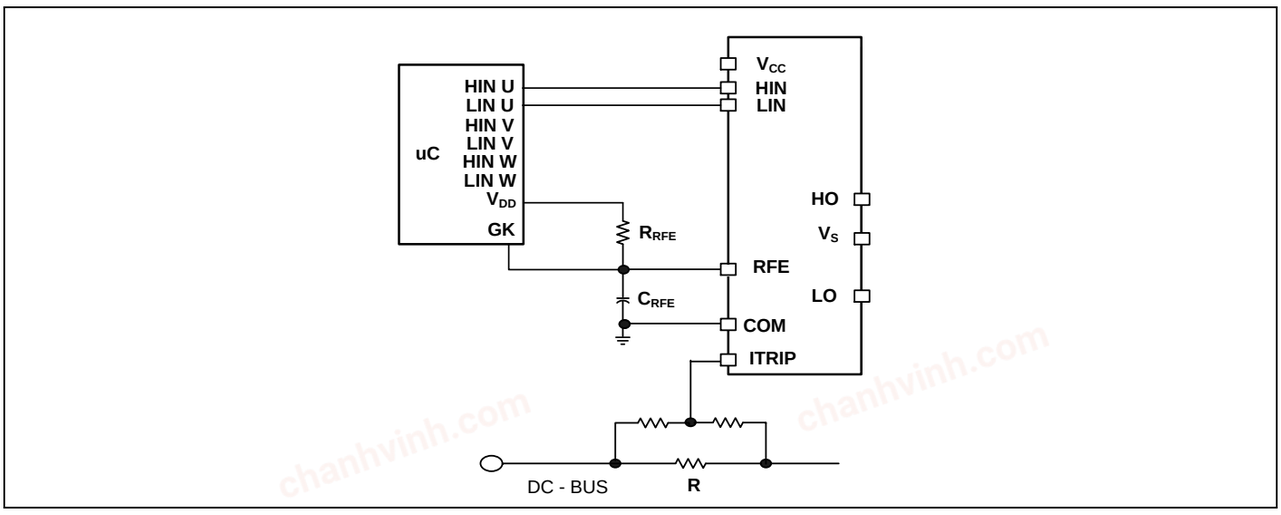


Figure 15 Programming the fault clear timer

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The design guidelines for this network are shown in Table 6

Table 6 Design guidelines

C_{RFE}	≤1 nF
	Ceramic
R_{RFE}	0.5 MΩ to 2 MΩ
	>> $R_{ON,REF}$

The length of the fault clear time period can be determined by using the formula below.

$v_C(t) = V_{f^*}(1-e^{-t/RC})$

$t_{FLTCLR} = - (R_{RF^*}C_{RF}) * \ln (1-V_{RF+}/V_{DD}) + 160us$

The voltage on the RF pin should not exceed the VDD of the uC power supply.

[1)]In case VDD is higher than 5V, the R_{RFE} resistor needs to be at least 200 KΩ in order to limit the IC power dissipation.

5.9 Over-current protection

The 6ED2231S12T is equipped with an over-current feature (ITRIP input pin). This functionality can sense over-current events in the DC- bus. Once the HVIC detects an over-current event, the outputs are shutdown, and RFE is pulled to VSS.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in ***Figure 16***, and the ITRIP threshold (V_{ITRIP+}). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold V_{ITRIP+} at that current level.

$V_{ITRIP+} = R_0 * I_{DC-}(R_1/(R_1+R_2))$

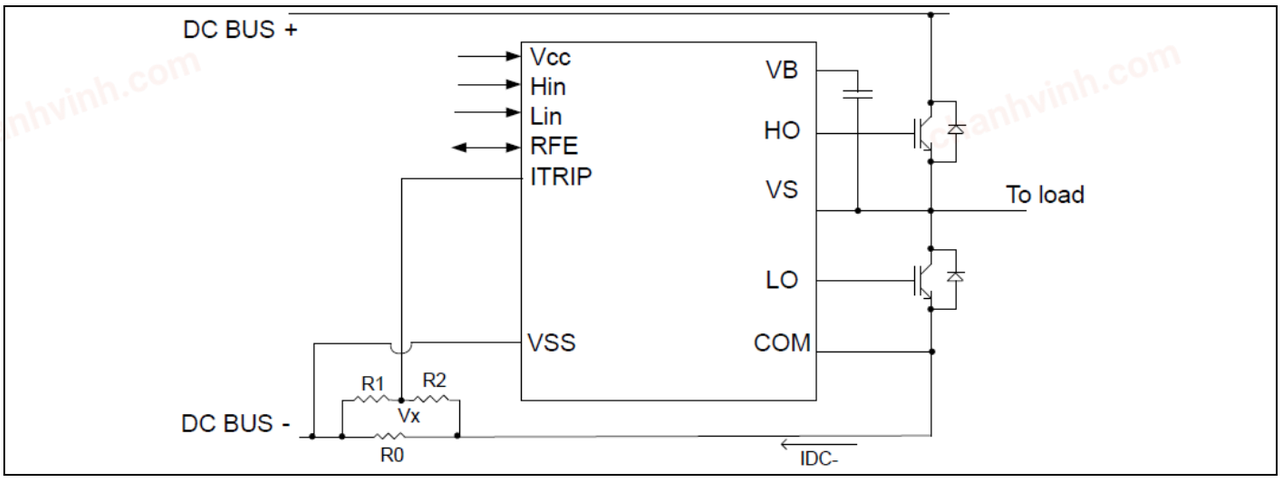


Figure 16 Programming the over-current protection

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

5.10 Truth table: Undervoltage lockout, ITRIP and enable

Table 7 provides the truth table for the 6ED2231S12T. The first line shows that the UVLO for VCC has been tripped; the RFE output has gone low and the gate drive outputs have been disabled. VCCUV is not latched in this case and when VCC is greater than VCCUV, the FAULT output returns the driver is functional.

The second case shows that the UVLO for VBS has been tripped and that the high-side gate drive outputs have been disabled. After VBS exceeds the VBSUV threshold, HO will stay low until the HVIC input receives a new rising transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled. This condition is stored in the external RC network waiting for fault clear time. The last case shows when the HVIC has received an enable command through the RFE input to shutdown; as a result, the gate drive outputs have been disabled.

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Table 7 6ED2231S12T UVLO, ITRIP, FLT/EN/RCIN

	VCC	VBS	ITRIP	RFE	LO	HO
UVLO V_{CC}	< V_{CCUV}	—	—	0	0	0
UVLO V_{BS}	15 V	< V_{BSUV}	0 V	HIGH	LIN	0
Normal operation	15 V	15 V	0 V	HIGH	LIN	HIN
ITRIP fault	15 V	15 V	> V_{ITRIP+}	0	0	0
Enable command	15 V	15 V	0 V	0	0	0

5.11 Advanced input filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN and LIN inputs. The working principle of the new filter is shown in ***Figures 17*** and ***18***.

Figure 17 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 18 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

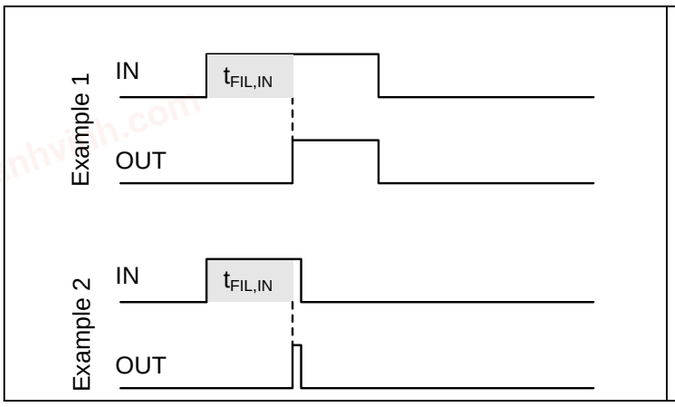


Figure 17 **Typical input filter**

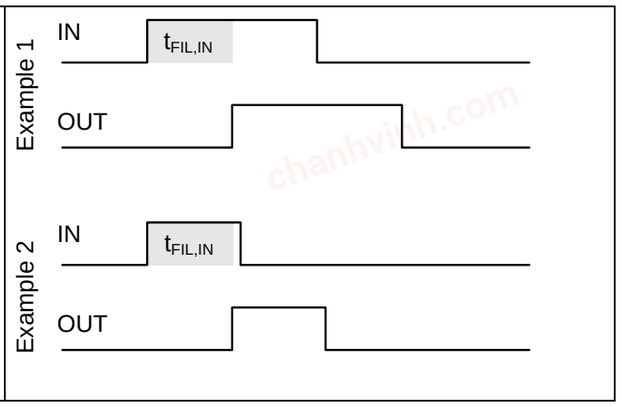


Figure 18 **Advanced input filter**

5.12 Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of ***Figure 19*** shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of ***Figure 19*** shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

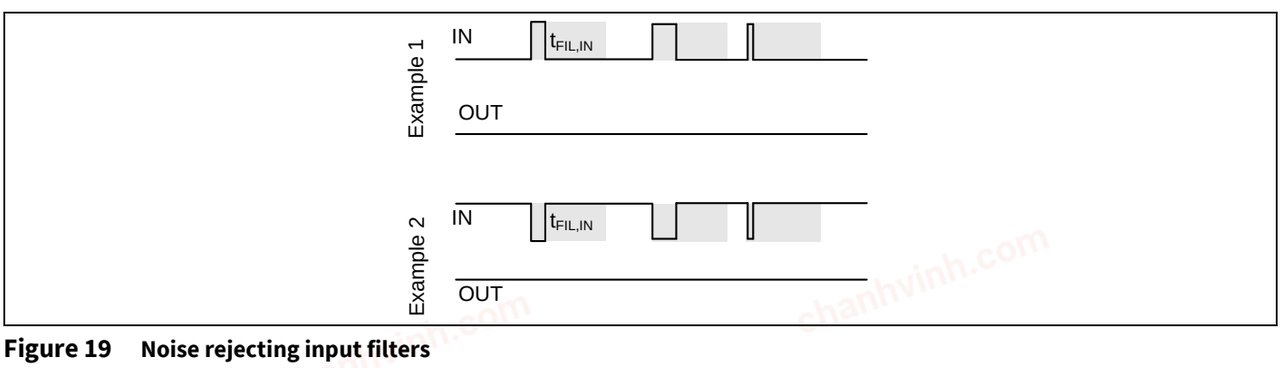


Figure 19 **Noise rejecting input filters**

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5.13 Bootstrap diode

An ultra-fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The integrated diode with its resistrance helps save cost and improve reliability by reducing external components as shown below ***Figure 20***.

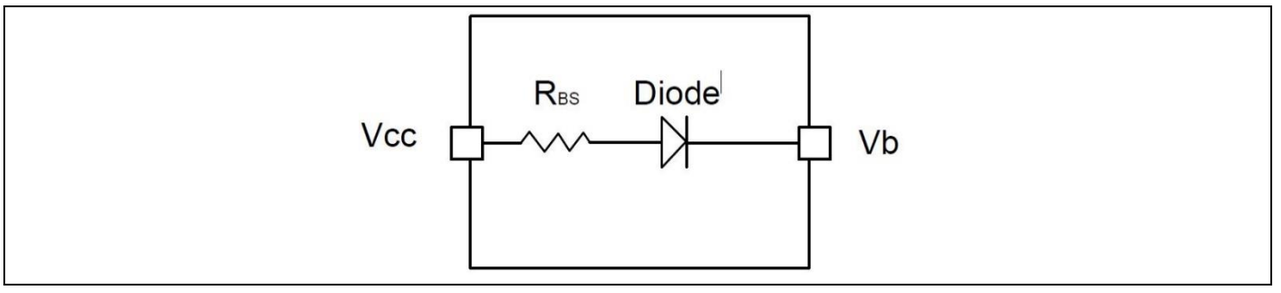


Figure 20 6ED2231S12T with integrated components

The low ohmic current limiting resistor provides essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 6ED2231S12T allows faster recharching of the bootstrap capacitor during periods of small duty cycles on the low side transistor. The bootstrap diode is usable for all kind power electronic converters. The bootstrap diode is a real pn-diode and is temperature robust. It can be used at high temperatures with a low duty cycle of the low side transistor.

The bootstrap diode of the 6ED2231S12T works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal motor drives control.

5.14 Calculating the bootstrap capacitance C_{BS}

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to ***Figure 21***. This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.

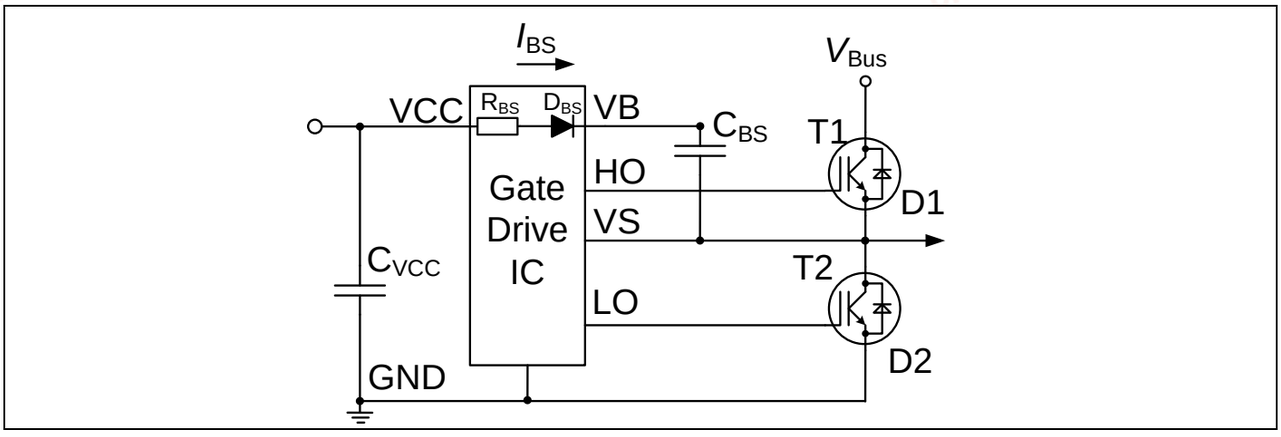


Figure 21 Half bridge bootstrap circuit in 6ED2231S12T

Here using the power IGBT for example, when the low side IGBT turns on, it will force the potential of pin V_S to GND. The existing difference between the voltage of the bootstrap capacitor V_{CBS} and VCC results in a charging current I_{BS} into the capacitor C_{BS}. The current I_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor. This pin is on high potential again after low side is turned off and high side is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VCC}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin V_B and VCC. The voltage of the bootstrap capacitor can now supply the high side gate drive sections. It is a general design rule for the location of bootstrap capacitors C_{BS}, that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual high side driver section. However, all parts of the 6ED2231S12T, which have the UVLO also contain a filter at each supply section in order to actively avoid such undesired UVLO triggers.

The current limiting resistor R_{BS} according to ***Figure 21*** reduces the peak of the pulse current during the low side IGBT turn-on. The pulse current will occur at each turn-on of the low side IGBT, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore, a smaller capacitor is suitable at higher switching

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frequencies. The bootstrap capacitor is mainly discharged by two effects: The high side quiescent current and the gate charge of the high side IGBT to be turned on.

The minimum size of the bootstrap capacitor is given by

$$C_{BS} = \frac{Q_{GTOT}}{\Delta V_{BS}}$$

ΔV_{BS} is the maximum allowable voltage drop at the bootstrap capacitor within a switching period, typically 1 V. It is recommended to keep the voltage drop below the undervoltage lockout (UVLO) of the high side and limit

$$\Delta V_{BS} \leq (VCC - V_F - V_{GSmin} - V_{DSon})$$

$V_{GSmin} > V_{BSUV-}$, V_{GSmin} is the minimum gate source voltage we want to maintain and V_{BSUV-} is the high-side supply undervoltage negative threshold.

VCC is the IC voltage supply, V_F is bootstrapdiode forward voltage and V_{DSon} is drain-source voltage of low side IGBT.

Please note, that the value Q_{GTOT} may vary to a maximum value based on different factors as explained below and the capacitor shows voltage dependent derating behavior of its capacitance.

The influencing factors contributing V_{BS} to decrease are:

- IGBT turn on required Gate charge (Q_G)
- IGBT gate-source leakage current (I_{LK_GS})
- Floating section quiescent current (I_{QBS})
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE})
- Charge required by the internal level shifters (Q_{LS}): typical 1nC
- Bootstrap capacitor leakage current (I_{LK_CAP})
- High side on time (T_{HON})

Considering the above,

$$Q_{GTOT} = Q_G + Q_{LS} + \left(I_{QBS} + I_{LK_{GS}} + I_{LK} + I_{LK_{DIODE}} + I_{LK_{CAP}}\right) * T_{HON}$$

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic capacitor and low ESR ceramic capacitor may result in an efficient solution).

The above C_{BS} equation is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of low side. The recommended bootstrap capacitance is therefore in the range up to 4.7 µF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances.

5.15 Negative voltage transient tolerance of V_S pin

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in ***Figure 22***, here we define the power switches and diodes of the inverter.
If the high-side switch (e.g., the IGBT Q1 in ***Figures 23*** and ***24***) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

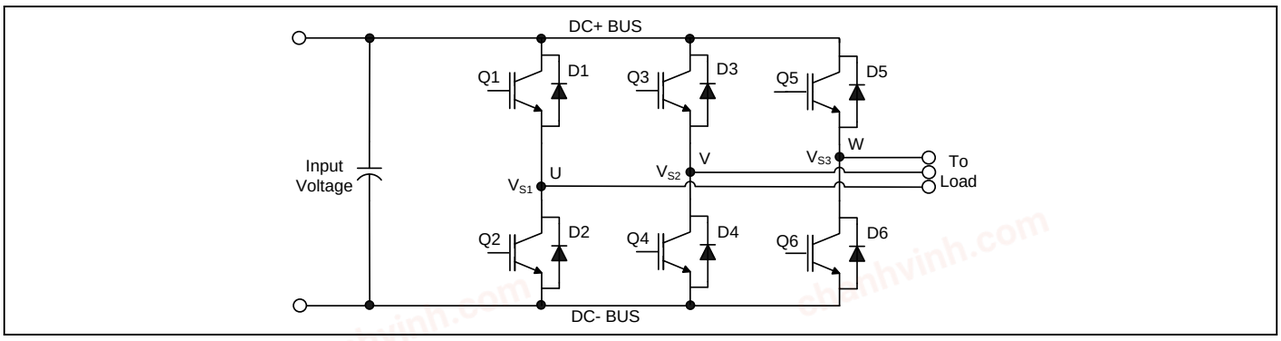


Figure 22 Three phase inverter

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Also, when the V phase current flows from the inductive load back to the inverter (see ***Figures 23-C*** and ***23-D***), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative V_S transient”

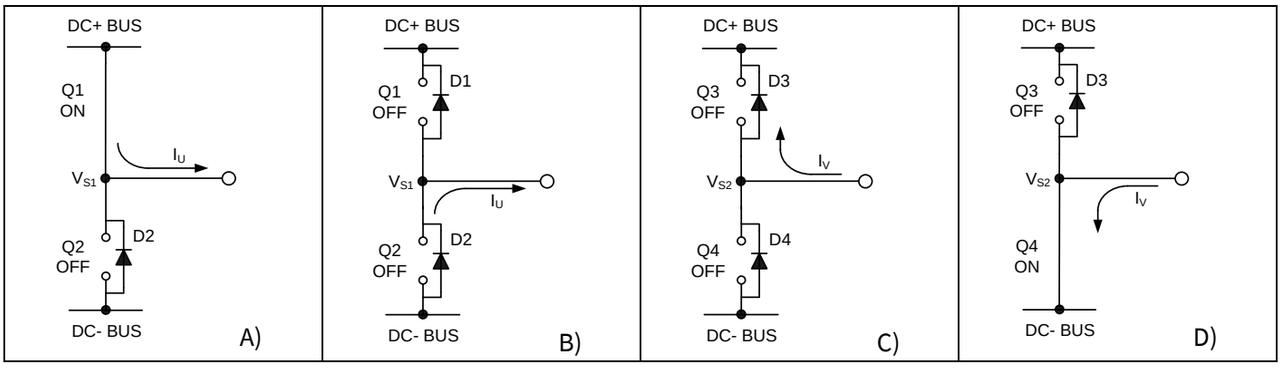


Figure 23 A) Q1 conducting B) D2 conducting C) D3 conducting D) Q4 conducting

The circuit shown in **Figure 24-A** depicts one leg of the three-phase inverter; ***Figures 24-B*** and ***24-C*** show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

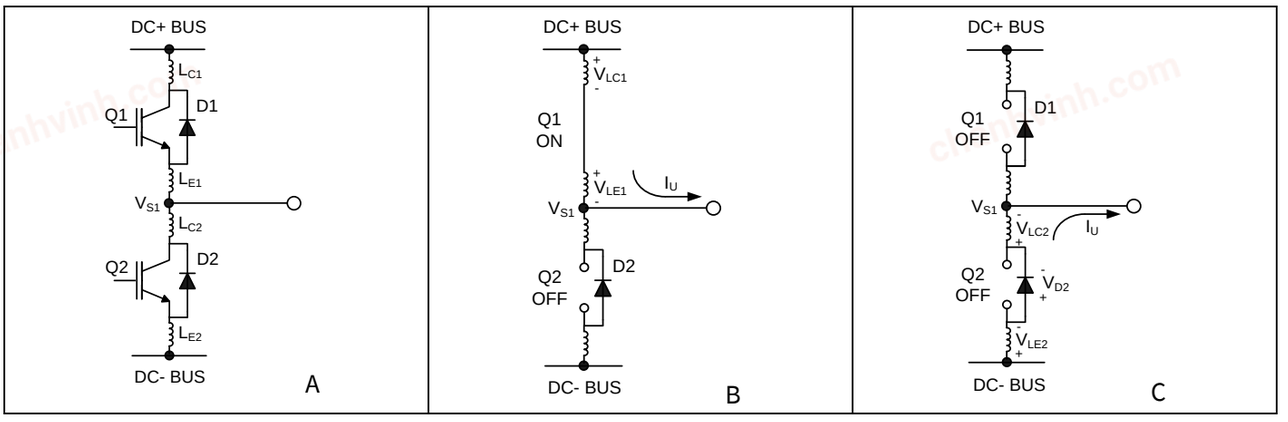


Figure 24 Figure A shows the Parasitic Elements. Figure B shows the generation of V_S positive. Figure C shows the generation of V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative Vs transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon’s HVICs have been designed for the robustness required in many of today’s demanding applications. An indication of the 6ED2231S12T’s robustness can be seen in ***Figure 25***, where the 6ED2231S12T Safe Operating Area is shown at VBS = 15 V based on repetitive negative Vs spikes. A negative Vs transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

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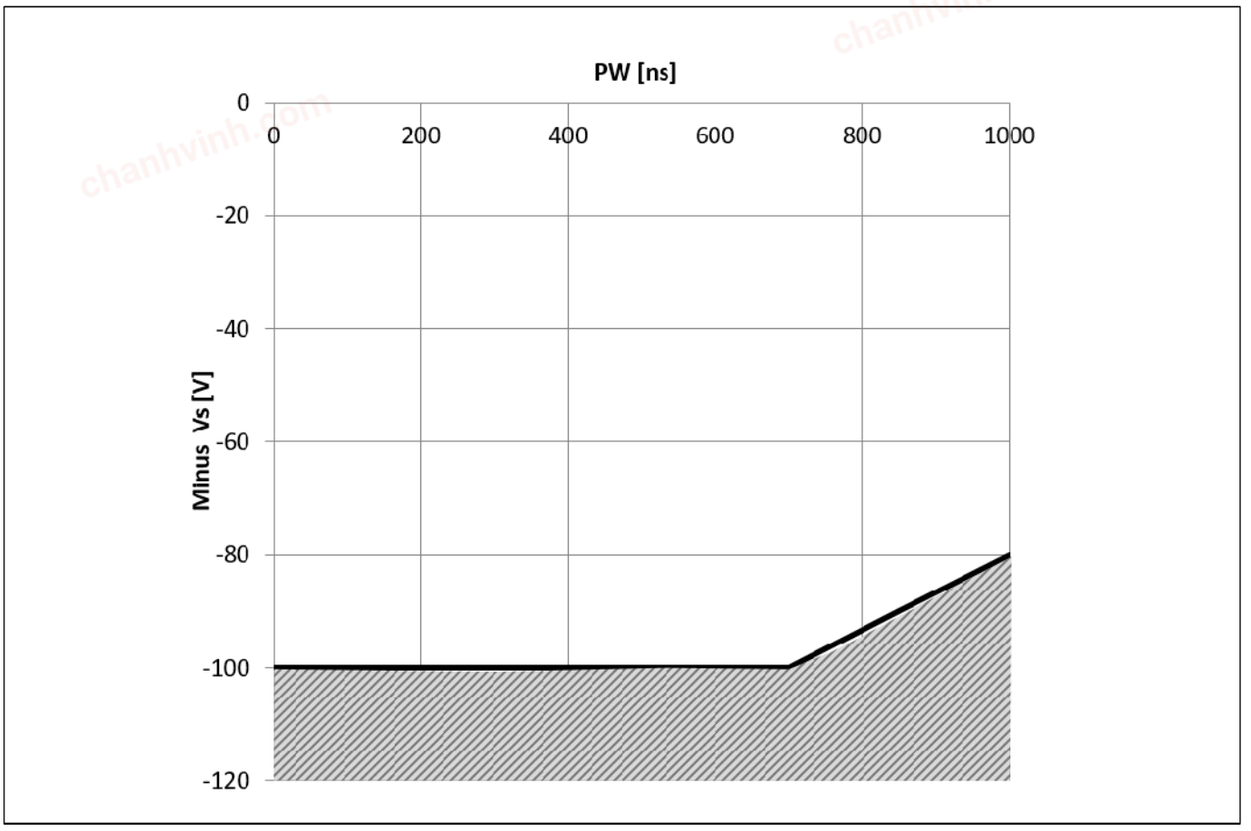


Figure 25 Negative Vs transient SOA for 6ED2231S12T @ VBS=15V

Even though the 6ED2231S12T has been shown to be able to handle these large negative Vs transient conditions, it is highly recommended that the circuit designer always limit the negative Vs transients as much as possible by careful PCB layout and component use.

5.16 PCB layout tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see ***Figure 26***). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT OR SIC MOSFET collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

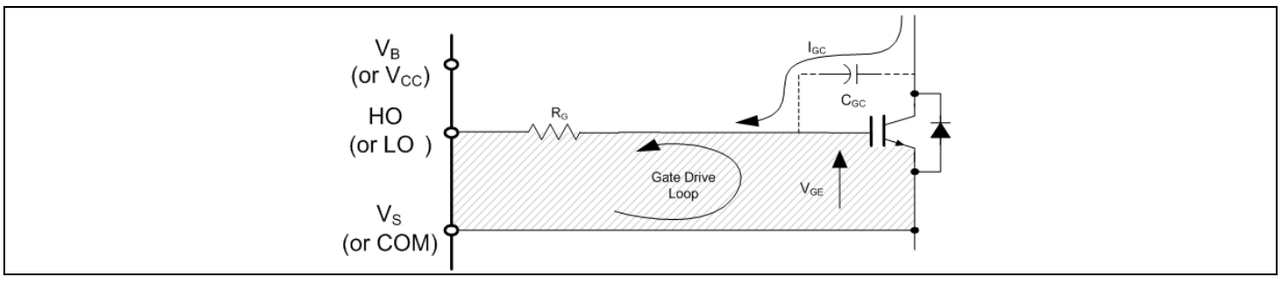


Figure 26 Avoid antenna loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the VCC and COM pins. A ceramic 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may

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be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see ***Figure 27***), and in some cases using a clamping diode between COM and V_S (see ***Figure 28***). See DT04-4 at ***www.infineon.com*** for more detailed explanations.

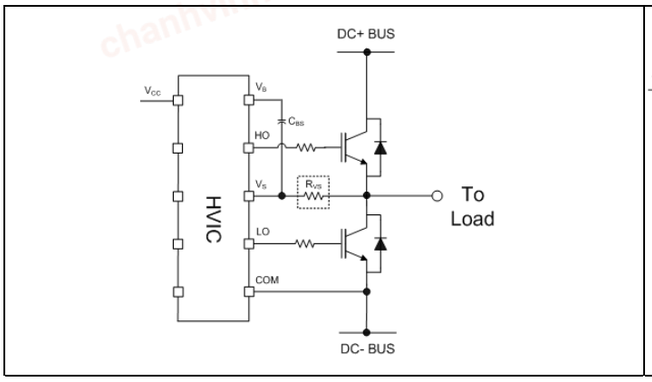


Figure 27 Resistor between the V_S pin and the switch node

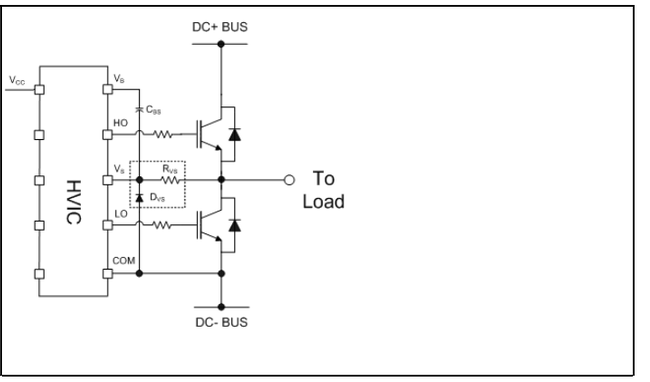


Figure 28 Clamping diode between COM and V_S

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6 Qualification information

Table 8 Qualification information[1]

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		DSO-24	MSL3[2], 260 °C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)	
	Charged Device Model	Class C4 (per JEDEC standard JS-022-2014)	
IC latch-up test		Class II Level A (per JESD78)	
RoHS compliant		Yes	

[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

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7 Related products

Table 9

Product	Description
Gate Driver ICs	
6ED2230S12T	1200 V, 0.65 A three phase gate driver with integrated low-ohmic bootstrap diodes and over current protection in DSO-24 package. By utilizing Infineon thin-film silicon-on-insulator (SOI) technology, 6ED2230S12T provides best-in-class robustness to protect against negative transient voltage spikes. $V_{BSUVLO+/-}$ = 10.4 V/9.4 V(Typ.); $V_{CCUVLO+/-}$ = 11.4 V/10.4 V(Typ.)
IR2214SS	1200 V Half-bridge gate driver with integrated dead-time, desaturation detection (DESAT), soft over-current shutdown, synchronized shutdown, two-stage turn-on for di/dt control, separate pull-up/pull-down output drive pins, matched propagation delays, and independent UVLO with hysteresis.
IR2213S	1200 V High and Low side gate driver with cycle by cycle shutdown logic, independent UVLO with hysteresis, matched propagation delays, and separate logic and power grounds.
IR2238Q	1200 V Three-phase motor controller with integrated programmable dead-time, desaturation detection (DESAT), brake chopper driver with protection, soft over-current shutdown, synchronized shutdown, hard shutdown, two-stage turn-on for dI/dt control, separate pull-up/pull-down output drive pins, matched propagation delays, and independent UVLO with hysteresis.
Power Switches	
IKW15N120BH6 IKW40N120CS6	High Speed 1200 V, 15 A/40 A/75 A hard-switching TRENCHSTOPTM IGBT6 co-packed with a very soft and fast recovery anti-parallel diode in a TO247 package/TO247PLUS 3pin package
IKW08T120 IKW15N120T2 IKW25N120T2 IKW40N120T2	The 1200 V, 8 A/15 A/25 A/40 A hard-switching TRENCHSTOPTM IGBT3 co-packed with free-wheeling diode in a TO247 package, provides significant improvement of static as well as dynamic performance of the device, due to combination of trench-cell and fieldstop concept.
IKQ40N120CT2	Infineon introduces the new package TO-247PLUS for 1200 V IGBT with increasing amounts of silicon in smaller, space saving packages with 40 A/50 A/75 A.
FP15R12W1T4 FP15R12W2T4 FP35R12W2T4	EasyPIMTM 1B/2B 1200 V, 15 A/35 A PIM IGBT module with fast Trench/Fieldstop IGBT Emitter Controlled 4 diode and NTC.
FP15R12W1T4_B11	EasyPIMTM 1B 1200 V, 15 A PIM IGBT module with fast Trench/Fieldstop IGBT4, Emitte Controlled 4 diode, NTC and PressFIT Contact Technology.
FS25R12W1T4 FS35R12W1T4	EasyPACKTM 1B 1200 V, 25 A/35 A sixpack IGBT module with Trench/Fieldstop IGBT4, Emitter Controlled 4 diode and NTC.
FS55MR12W1M1H_B11	EasyPACK™ 1B 1200 V / 55 mΩ sixpack module with CoolSiC™ MOSFET with enhanced generation 1, NTC and PressFIT Contact Technology.
IMW120R350M1H IMW120R220M1H IMW120R140M1H IMW120R090M1H IMW120R060M1H IMW120R040M1H IMW120R030M1H	The CoolSiC™ 1200 V, 350 mΩ ~ 20 mΩ SiC MOSFET in TO247-3 package build on a state-of-the-art trench semiconductor process optimized to combine performance with reliability. In comparison to traditional silicon (Si) based switches like IGBTs and MOSFETs, the SiC MOSFET offers a series of advantages. These include, the lowest gate charge and device capacitance levels seen in 1200 V switches, no reverse recovery losses of the internal commutation proof body diode, temperature independent low switching losses, and threshold-free on-state characteristic.
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field-oriented control (FOC) of permanent magnet synchronous motors (PMSM).

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8 Packaging information

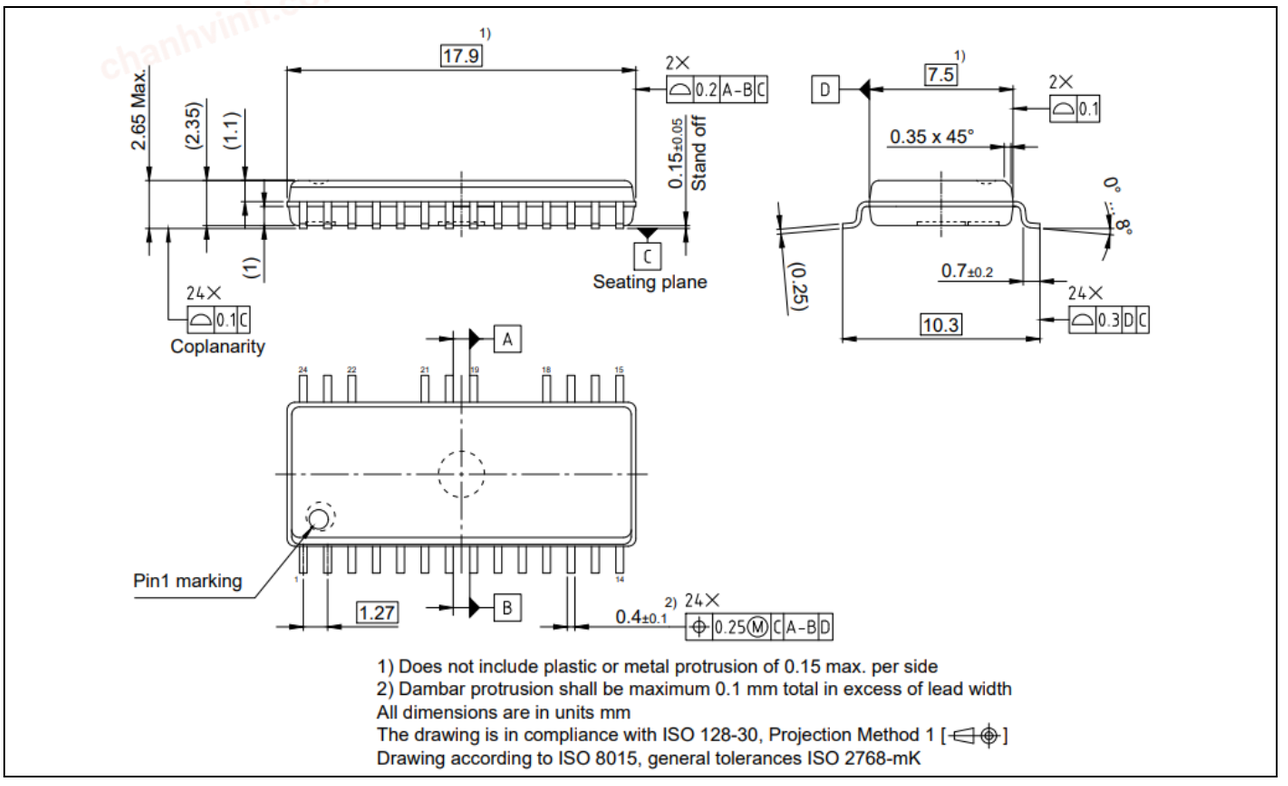


Figure 29 Package outline

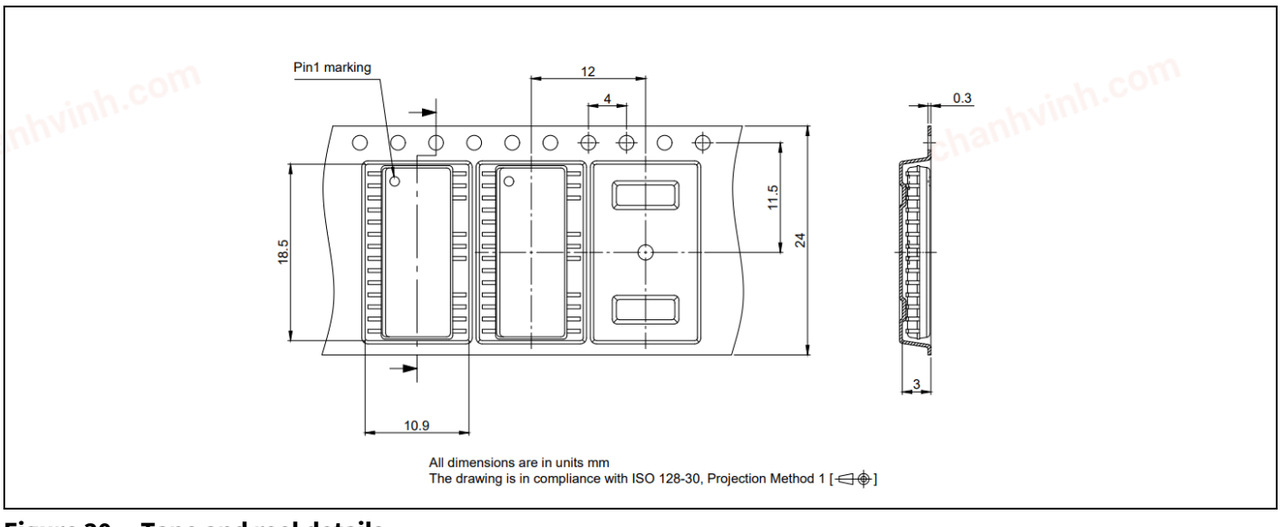


Figure 30 Tape and reel details

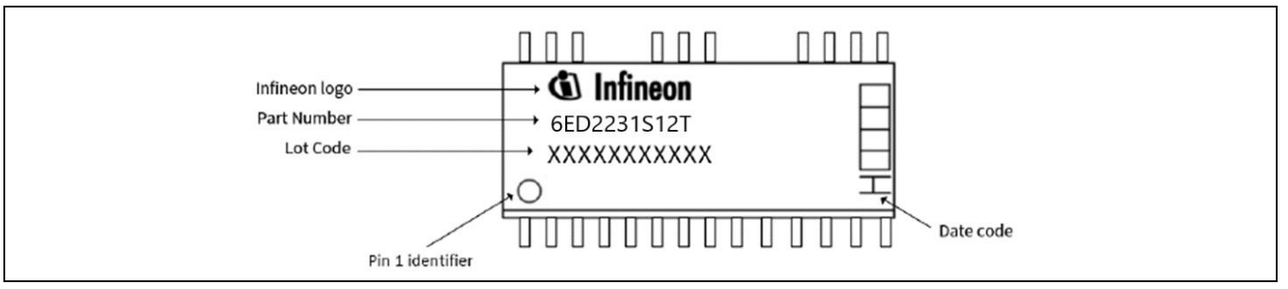


Figure 31 Marking information PG-DSO-24 (DSO-28 with 4 pins removed) [Marking Diagram to be updated]

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9 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBT OR SIC MOSFETs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

9.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

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10 Revision history

Document version	Date of release	Description of changes
0.91	January 20, 2020	Target Datasheet
0.92	February 26, 2021	Update Recommended operating conditions to 1200V
0.93	March 01, 2021	Remove power MOSFET related items
0.94	February 4, 2022	Update notes on chapter 6
1.0	Aug. 09, 2022	Final Datasheet
1.1	Aug. 26, 2022	Added the information of SiC MOSFET
1.2	Sep. 19, 2022	Changed package drawing

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