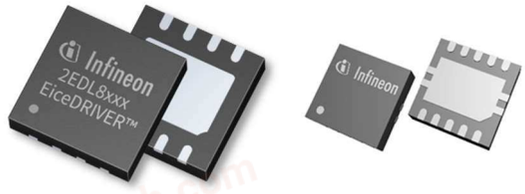
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EiceDRIVER™ 2EDL8x2x

120 V Boot, 3 A / 4 A, Junction-Isolated High Side and Low Side Gate Driver ICs

Features

- Level-shift high-side low-side dual channel driver
- (2EDL802x) Independently controlled high-side and low-side gate drivers
- (2EDL812x) Differential input for superb robustness with inherent shoot-through protection
- 3 A (2EDL8x23) or 4 A (2EDL8x24) source current capability for both high side and low side drivers
- Strong 5 A high side / 6 A low side sink current capability
- 120 V on-chip bootstrap diode
- Support operating frequency up to 1 MHz
- VDD/VHB under voltage lockout (UVLO)
- -10 V to 20 V Input pin capability for increased robustness
- (2EDL812x) -8 V to 15 V input pin common mode rejection
- -5 A output pin reverse current capability
- 8 V to 17 V supply voltage operating range
- Fast propagation delay
- <6 ns delay matching
- Offered in VDSON-8 (4 mm x 4 mm) and VSON-10 (3 mm x 3mm) package
- Lead free RoHS compliant package



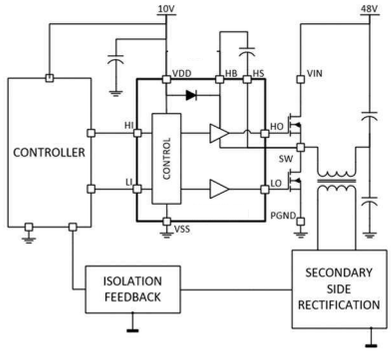
Feature Comparison

PART	INPUT	LOW/HIGH SIDE PEAK PULL UP CURRENT	LOW SIDE PEAK PULL DOWN CURRENT	HIGH SIDE PEAK PULL DOWN CURRENT
2EDL8023	Independent	3A	6A	5A
2EDL8024	Independent	4A		
2EDL8123	Differential	3A		
2EDL8124	Differential	4A		

Potential Applications

- DC-to-DC converter
- Isolated bus converter
- Synchronous rectification for SMPS
- Class-D Audio Amplifiers

Typical Application Diagram



Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

2EDL8x2x is a high-side low-side driver designed for advanced switching converters such as in telecom and datacom applications. 2EDL802x takes in independent inputs with built-in hysteresis for enhanced noise immunity, whereas 2EDL812x takes in differential input with built-in hysteresis for enhanced noise immunity. 2EDL812x's inherent shoot-through protection ensures the robustness of the system. 6 ns maximum delay matching ensures volt-second balance and avoids magnetic core saturation.

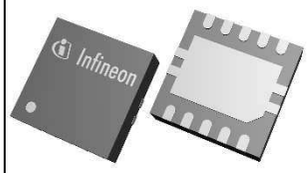
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1 Package Information

PG-VDSON-8-4	RoHS HAL	
PG-VSON-10-4	RoHS HAL	

1.1 Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
2EDL8023G	PG-VDSON-8-4	Tape and Reel	6000	2EDL8023GXUMA1
2EDL8023G3C	PG-VSON-10-4	Tape and Reel	3000	2EDL8023G3CXUMA1
2EDL8024G	PG-VDSON-8-4	Tape and Reel	6000	2EDL8024GXUMA1
2EDL8024G3C	PG-VSON-10-4	Tape and Reel	3000	2EDL8024G3CXUMA1
2EDL8123G	PG-VDSON-8-4	Tape and Reel	6000	2EDL8123GXUMA1
2EDL8123G3C	PG-VSON-10-4	Tape and Reel	3000	2EDL8123G3CXUMA1
2EDL8124G	PG-VDSON-8-4	Tape and Reel	6000	2EDL8124GXUMA1
2EDL8124G3C	PG-VSON-10-4	Tape and Reel	3000	2EDL8124G3CXUMA1

1.2 Pin Configuration and Descriptions

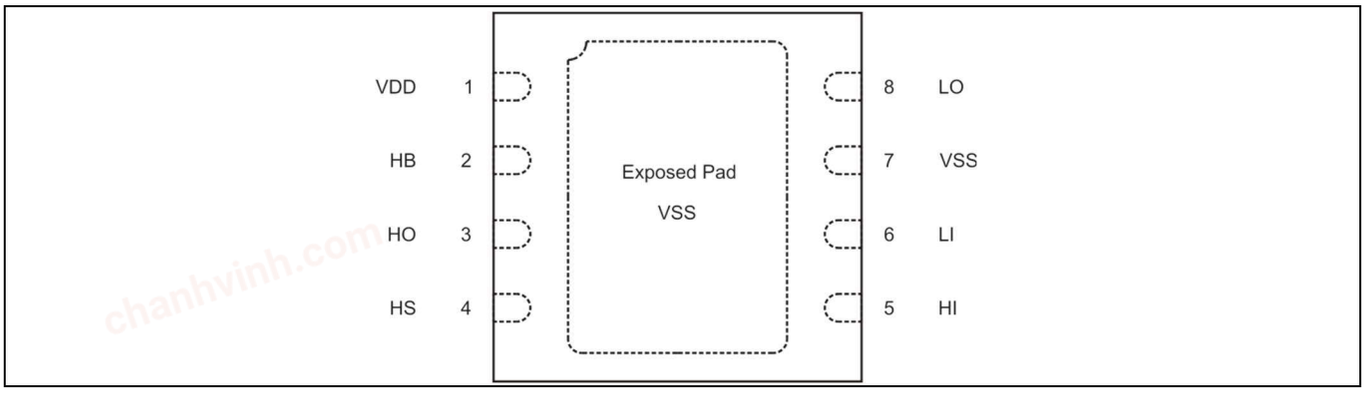


Figure 1 Pin Configuration of PG-VDSON-8-4, Top Transparent View

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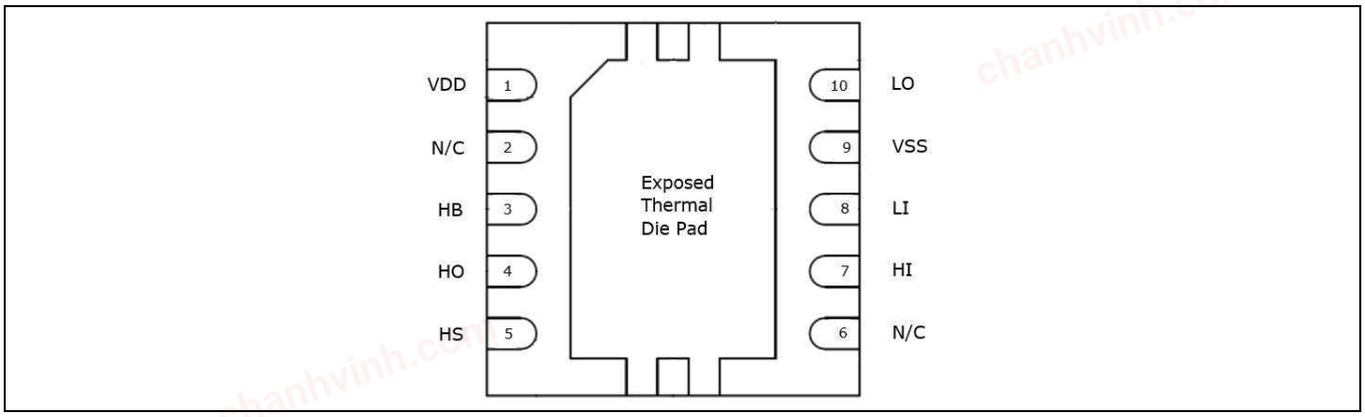


Figure 2 Pin Configuration of PG-VSON-10-4, Top Transparent View

Pin Name	VDSON-8 Pin #	VSON-10 Pin #	Pin Description
VDD	1	1	Gate drive supply
N/C	---	2,6	Not Connected
HB	2	3	High-side gate driver bootstrap rail
HO	3	4	High-side gate driver output
HS	4	5	High-side FET source connection
HI	5	7	High-side driver control input
LI	6	8	Low-side driver control input
VSS	7	9	Ground return, internally connected to exposed pad
LO	8	10	low-side gate driver output

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2 Block Diagram

A simplified functional block diagram is given in the figure below

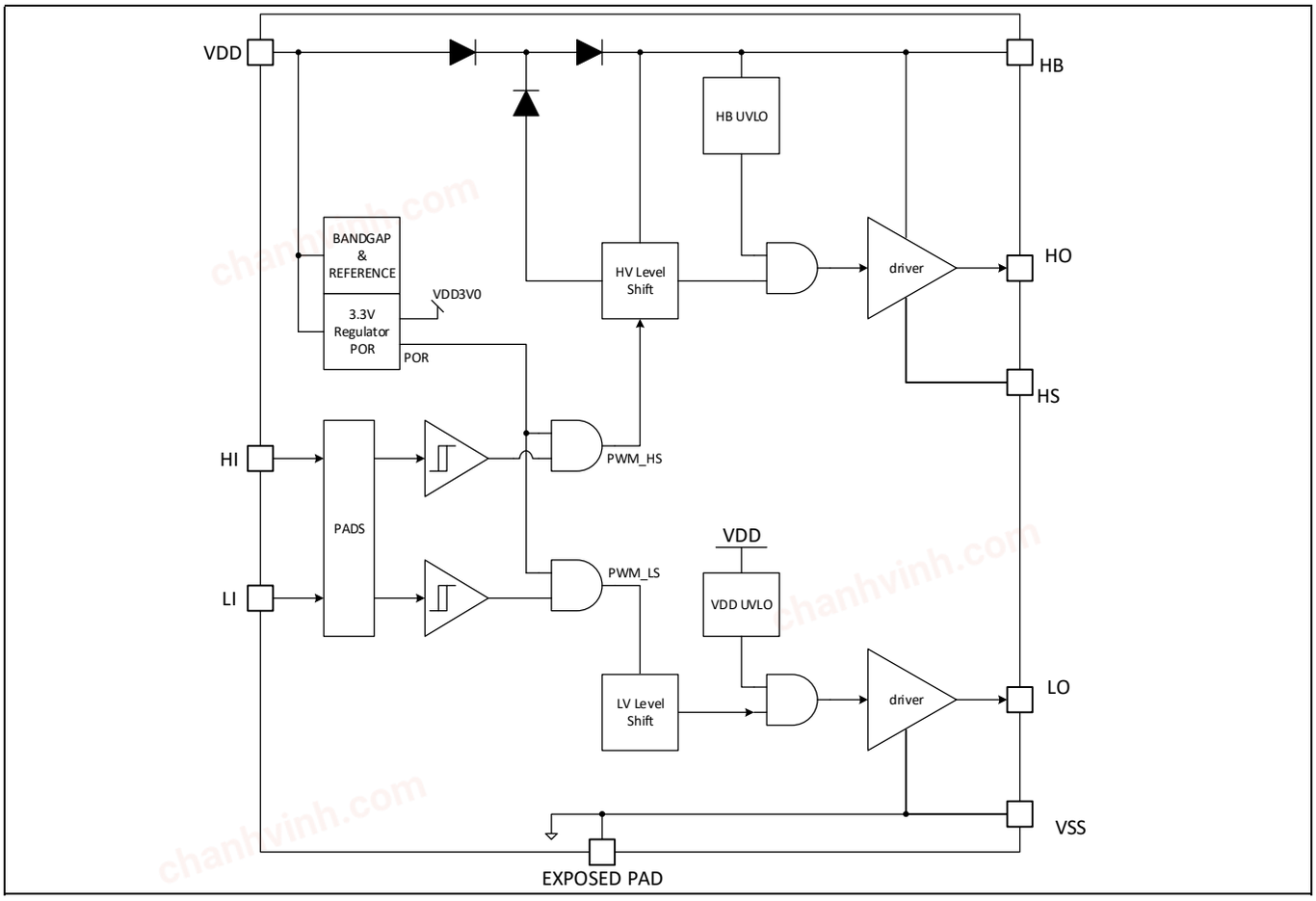


Figure 3 Block Diagram

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3 Functional Description

The device is a level-shifted 2-channel driver designed to support topologies with high-side and low-side configurations. The high side is level shifted by the combination of an on-chip 120 V rated bootstrap diode and an external bootstrap capacitor. The device provides 3 A (2EDL8x23) or 4 A (2EDL8x24) peak source current capability for both high-side and low-side and a strong 5 A high-side and 6 A low-side sink current capability. This allows driving large power MOSFETs with minimum or optimized switching losses during the transition through the MOSFET's Miller Plateau.

2EDL802x's input pins support TTL logic levels independently of supply voltage. They are capable to withstand voltages from -10 V to 20 V, allowing the device to interface with a broad range of analog and digital controllers. The input stage features built-in hysteresis for enhanced noise immunity. The low-side and high-side gate drivers are independently controlled and matched to typical 2 ns between the turn on and turn off of each other.

2EDL812x's input pins support TTL logic levels independently of supply voltage. They are capable to withstand voltages from -10 V to 20 V and ground potential shifts from -8 V to 15 V, allowing the device to interface with a broad range of analog and digital controllers. The input stage features built-in hysteresis for enhanced noise immunity. The low-side and high-side gate drivers are differentially controlled and matched to typical 2 ns between the turn on and turn off of each other. The differential inputs provide inherent shoot-through protection and ensure high-side and low-side outputs are never on at the same time.

The switching node (HS pin) is able to handle negative voltages down to –(24 - V_{DD}) V which allows the high-side channel to be protected from inherent negative voltages caused by parasitic inductance and stray capacitance.

Under-voltage lockout circuits are provided for both high- and low-side drivers. UVLO protects the system by forcing the output low when the supply voltage is lower than the specified threshold.

The following sections describe key functionalities.

3.1 Supply Voltage

The absolute maximum supply voltage is 20 V. The minimum operating supply voltage is set by the under voltage lockout function to a typical default value of 7.0 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

3.2 Input Stage

2EDL802x device responds to the two inputs signals (HI and LI) independently according to the following truth table.

Table 1 2EDL802x Truth Table

LI	HI	LO	HO
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

The high-side and low-side outputs respond to high-side and low-side inputs independently.

2EDL812x device responds to the combination of two inputs signals (HI and LI) according to the following truth table.

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Table 2 2EDL812x Truth Table

LI	HI	LO	HO
L	L	L	L
H	L	H	L
L	H	L	H
H	H	L	L

True differential input comes with inherent shoot through protection by preventing both low and high side to be on at the same time. It also provides noise immunity against ground bounce. The input stage is designed to operate reliably against –8 V / +15 V ground voltage drift. Input logic hysteresis also helps combat disturbances to the input signal.

The differential voltage between the two input pins is rated at 8 V maximum because of the back-to-back ESD diodes that connect the two input pins together. Above this voltage, the ESD diodes start clamping which causes a current flow from the high voltage potential input pin to the low voltage potential input pin.

3.3 Driver Outputs

The low output impedances allow fast transition of the load transistor. Specifically, the ultra-low impedance pull down resistances, typically 0.5 Ω for the high side and 0.35 Ω for the low side, keep the gate of the load transistor down during fast transient events – avoiding dv/dt induced re-turn-on.

3.4 Under Voltage Lockout (UVLO)

The under voltage lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO rising threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch on the device, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 7.0 V with 0.5 V hysteresis for supply voltage (V_{DD}) and 5.75 V with 0.25 V hysteresis for high side boot voltage (V_{HB}).

UVLO threshold trigger is synchronous. The clock gating ensures minimum pulse width set by the controller is obeyed at all times. This increases robustness of the integrated boot diode due to the controllability of the reverse recovery behavior.

A 5 us delay time and a PWM synchronization scheme are implemented in the high-side UVLO to ensure that the load transistor is not operated with marginal gate drive voltage which can lead to high power dissipation. The synchronization is done in such a way that the HO output is blocked when UVLO is released while the HI is high. HO is only propagated when the UVLO is released while the HI is low.

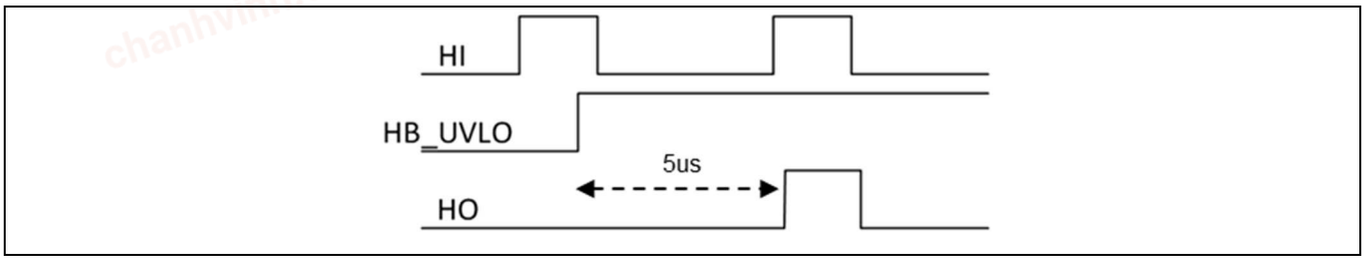


Figure 4 High-side UVLO implementation

3.5 Minimum Pulse Width

The device responds to input level according to the truth table in section 3.2 as long as the logic signal complies with the minimum pulse width requirement. Signal pulse longer than the minimum allowable input pulse width

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yields valid output. Any output in response to shorter pulses or glitches should be disregarded and filtered out by the user. Under all allowable operation above input minimum pulse width of 40 ns, the output behaves one to one to the input with minimal pulse width distortion.

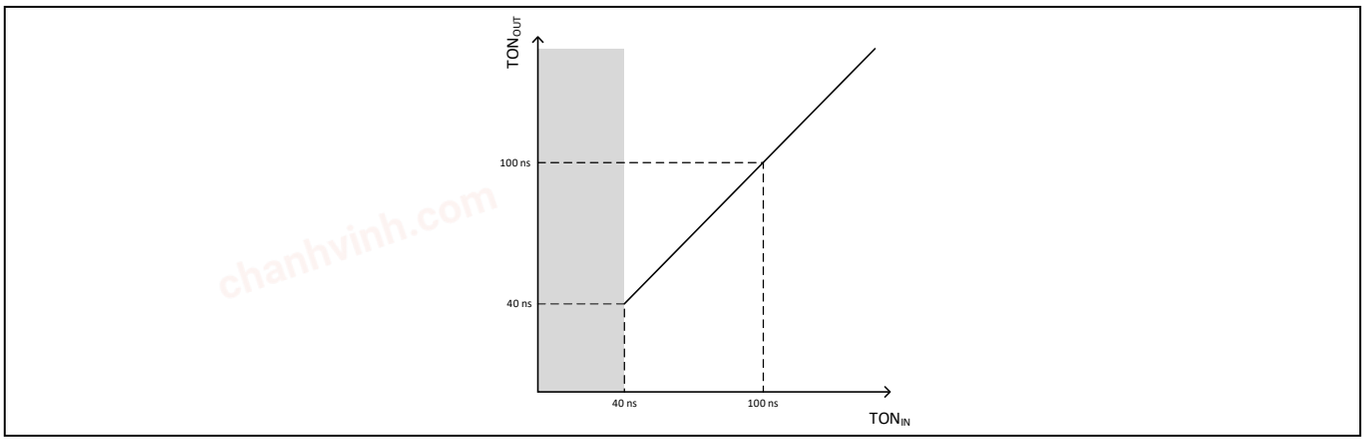


Figure 5 Minimum Pulse Width Input-output On-time Transfer Function

This diagram is illustrative only with typical value. Actual value and pulse width distortion is subject to process variation. Output pulse width could in some case be shortened or extended to prevent retoggling. See transient detector section below.

3.6 Transient Detector

The transient detector block is designed to prevent re-toggling of the HO output in case of potential instability of the level shifter caused by phase node movement. For example, a fast-rising phase node voltage could pull the power ground (PGND) down. This could result in potential between HI and PGND higher than the rising threshold of the high-side signal. Such a glitch or noise can be picked up by the driver and propagate through which can lead to a shoot-through event, transformer volt-second imbalance, and potential device destruction.

The following describes the basic operation of the block.

- The transient detector monitors the phase node and tracks its movement, and the rate of change over time for both rising and falling edge.
- Whenever the rate of change is larger than a certain dv/dt threshold[1], the transient detector is active and blocks the HO output from changing state.
- A High-side Input (HI) toggle triggers a decision to change the state, but HO waits until the transient detector's active state is removed, then the decision is propagated through.

Additional propagation delay caused by the transient detector is limited to one-half of the oscillation period, as the signal always propagates through whenever the transient detector sees a peak or valley where dv/dt approaches zero. See link to *Understanding the transient detector* [1] for more information.

[1] Reference slew rate threshold versus temperature under Section 6 Typical Characteristics

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4 Characteristics

4.1 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Symbol	Description	Min	Max	Unit
V_{DD}	Driver Supply Voltage[1]	-0.3	20	V
V_{HS}	Phase Voltage (DC)	-1	V_{HB} + 0.3	V
	Phase Voltage (Repetitive pulse < 100 ns)[2]	-(24 - V_{DD})	V_{HB} + 0.3	V
V_{HB}	High Side Bootstrap Voltage[2]	-0.3	120	V
V_{HI}, V_{LI}	LI and HI Input Voltage	-10	20	V
V_I	Differential Input Voltage[3]	---	8	V
V_{LO}	Output voltage on LO	-0.3	V_{DD} + 0.3	V
V_{HO}	Output voltage on HO	V_{HS} – 0.3	V_{HB} + 0.3	V
I_{OR}	LO and HO Peak Reverse Current[4]	---	5	A
T_J	Operating Junction Temperature	-40	150	°C
T_S	Storage Temperature	-55	150	°C

4.2 ESD Ratings

Symbol	Description	Value	Unit
ESD_{HBM}	Human Body Model sensitivity as per ANSI/ESDA/JEDEC JS-001	2000	V
ESD_{CDM}	Charged Device Model sensitivity as per ANSI/ESDA/JEDEC JS-002	1000	V

4.3 Recommended Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All parameters specified in the subsequent tables refer to these operating conditions.

Symbol	Description	Min	Typ	Max	Unit
V_{HS}	Phase Voltage (DC)	-1	---	80	V
	Phase Voltage (Repetitive pulse < 100 ns)	-(24 - V_{DD})	---	80	V
V_{DD}	Driver Supply Voltage	8	10	17	V
V_{HB}	High Side Bootstrap Voltage	-0.3	---	90	V
T_J	Junction Temperature	-40	---	125	°C
dv/dt	HS Slew Rate	---	---	50	V/ns
V_I	Differential Input Voltage	0	3.3	5	V
V_{ICMR}	Input Signal Common Mode Rejection (2EDL812x)	-8 + V_I/2	---	15 – V_I/2	V

[1] All voltage ratings in this section referenced to ground

[2] Not subject to production test. Verified by design/characterization

[3] Absolute voltage difference between HI and LI ($|V_{HI}-V_{LI}|$)

[4] For < 500 ns pulses

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4.4 Static Electrical Characteristics

V_{DD} = V_{HB} = 12 V, V_{HS} =V_{SS}=0V. T_C = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS}.

Symbol	Description	Min	Typ	Max	Units	Conditions
V_{DDR}	V_{DD} UVLO Rising Threshold	6.6	7.0	7.4	V	
V_{DDH}	V_{DD} UVLO Threshold Hysteresis	---	0.5	---	V	
V_{HBR}	V_{HB} UVLO Rising Threshold[1]	5.5	5.75	6.0	V	
V_{HBH}	V_{HB} UVLO Threshold Hysteresis	---	0.275	---	V	
I_{HB}	Boot voltage Quiescent Current	---	0.55	0.7	mA	V_{LI}=V_{HI}=0V
I_{HBO}	Boot voltage Operating Current	---	2.8	3.1	mA	f=500kHz, C_{LOAD}=0nF, 2EDL8x23
		---	2.9	3.2		f=500kHz, C_{LOAD}=0nF, 2EDL8x24
I_{DD}	V_{DD} Quiescent Current	---	0.55	0.7	mA	V_{LI}=V_{HI}=0V
I_{DDO}	V_{DD} Operating Current	---	2.8	3.1	mA	f=500kHz, C_{LOAD}=0nF, 2EDL8x23
		---	2.9	3.2		f=500kHz, C_{LOAD}=0nF, 2EDL8x24
R_{IN}	Input Pulldown Resistance	54	68	82	kΩ	
V_{IR}	Rising Input Voltage Threshold	1.6	2.25	2.9	V	
V_{IF}	Falling Input Voltage Threshold	1.0	1.65	2.3	V	
V_{IH}	Input Logic Voltage Hysteresis	---	0.6	---	V	
R_{PUH}	High Side Pull Up Resistance	---	1.45	---	Ω	2EDL8x23
		---	1.0	---		2EDL8x24
R_{PDH}	High Side Pull Down Resistance	---	0.5	---	Ω	
R_{PUL}	Low Side Pull Up Resistance	---	1.45	---	Ω	2EDL8x23
		---	1.0	---		2EDL8x24
R_{PDL}	Low Side Pull Down Resistance	---	0.35	---	Ω	

[1] HB (high side bootstrap) related ratings referenced to V_{HS}

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4.5 Dynamic Electrical Characteristics

V_{DD} = V_{HB} = 12 V, V_{HS} =V_{SS}=0V. T_C = 25°C unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions
I_{PUH}	High Side Peak Pull Up Current[1]	---	3	---	A	V_{HO} = 0 V , 2EDL8x23
		---	4	---		V_{HO} = 0 V , 2EDL8x24
I_{PDH}	High Side Peak Pull Down Current[1]	---	5	---	A	V_{HO} = 12 V
I_{PUL}	Low Side Peak Pull Up Current[1]	---	3	---	A	V_{LO} = 0 V , 2EDL8x23
		---	4	---		V_{LO} = 0 V , 2EDL8x24
I_{PDL}	Low Side Peak Pull Down Current[1]	---	6	---	A	V_{LO} = 12 V
T_{DR}	Rising Propagation Delay[2,3]	---	45	54	ns	C_{LOAD} = 0
T_{DF}	Falling Propagation Delay[4,3]	---	45	54	ns	C_{LOAD} = 0
T_{DM}	Delay Matching[5]	---	2	6	ns	
T_{PW}	Minimum Input Pulse Width[6]	---	---	40	ns	
T_{DRR}	Bootstrap Diode Turn off Time[7]	---	10	---	ns	I_F = 20 mA, I_{PRR} = 0.5 A

4.6 Thermal Mechanical Characteristics

Symbol	Description		Min	Typ	Max	Units	Conditions
R_{thJC}	Junction to Case Thermal Resistance	VDSON-8	---	3	---	°C/W	Bottom
			---	46	---	°C/W	Top
		VSON-10	---	5.8	---	°C/W	Bottom
			---	69	---	°C/W	Top
R_{thJA}	Device on PCB	VDSON-8	---	42	---	°C/W	6 cm^2 cooling area[8]
		VSON-10	---	60	---	°C/W	

[1] Not subject to production test.

[2] Rising propagation delay from LI to LO and from HI to HO

[3] A transient detector blocks the toggling of the high side output when it detects moving phase node (due to transition and/or oscillation). It prevents unwanted retoggling but may increase propagation delay. See transient detector activation in Figure 7.

[4] Falling propagation delay from LI to LO and from HI to HO

[5] Consolidated delay matching (1) ON: between LO rising and HO falling and (2) OFF: between LO falling and HO rising

[6] Minimum input pulse width that produces valid output signal

[7] External schottky boot diode in parallel recommended for high dv/dt application

[8] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB vertical in still air

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5 Descriptive Illustration

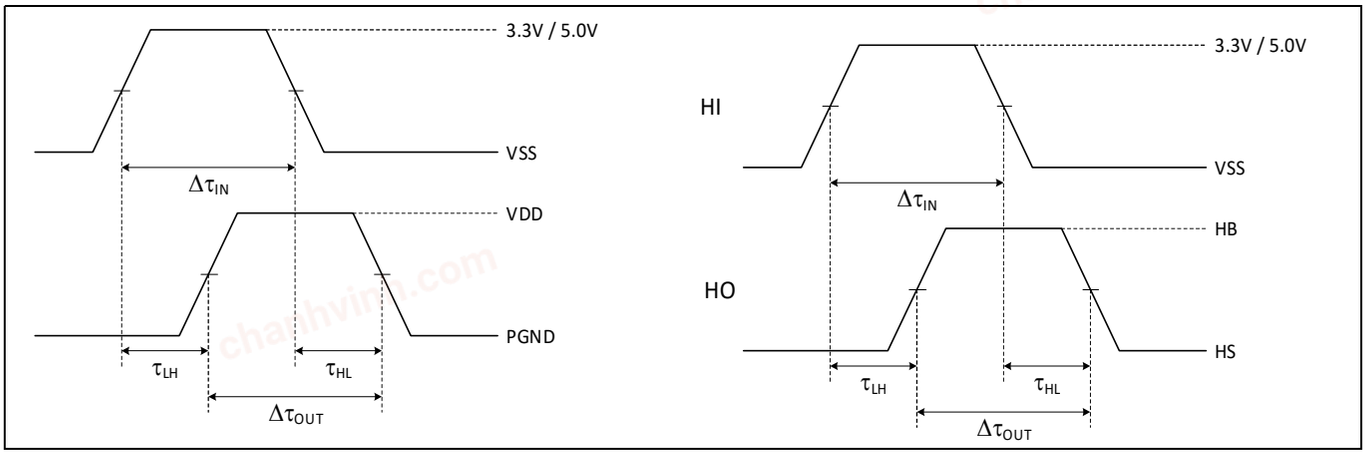


Figure 6 Propagation delay

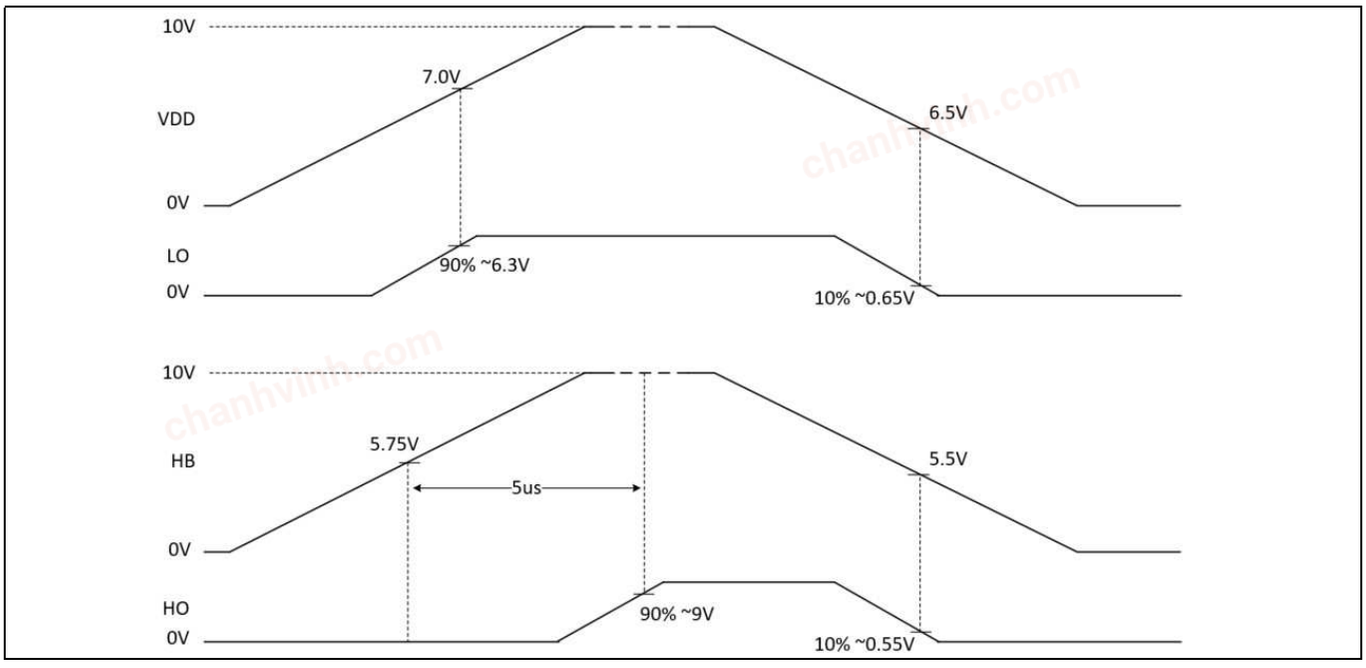


Figure 7 UVLO behavior

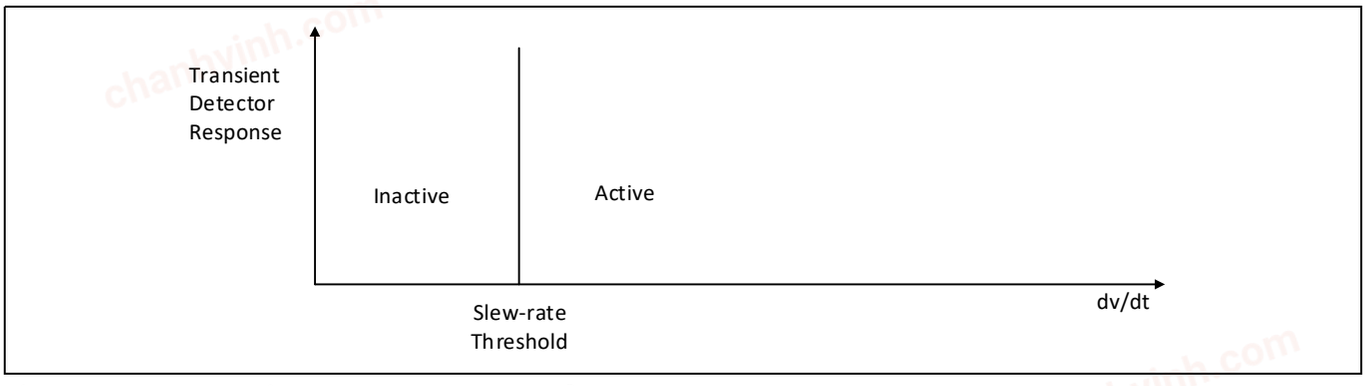
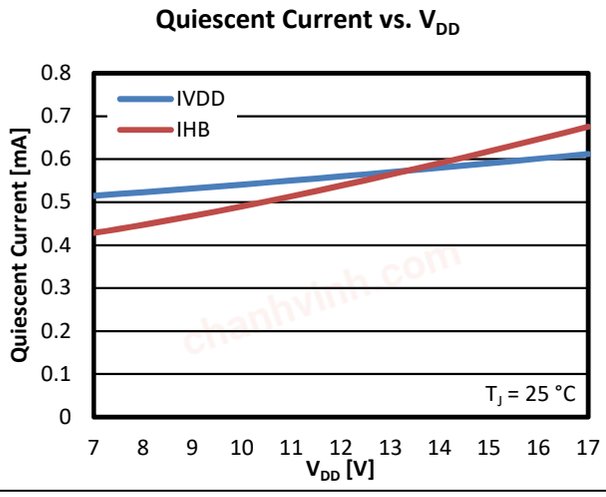


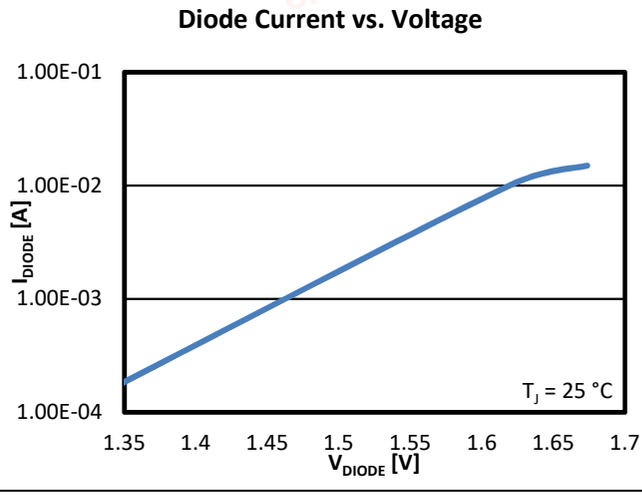
Figure 8 Transient Detector Response[3]

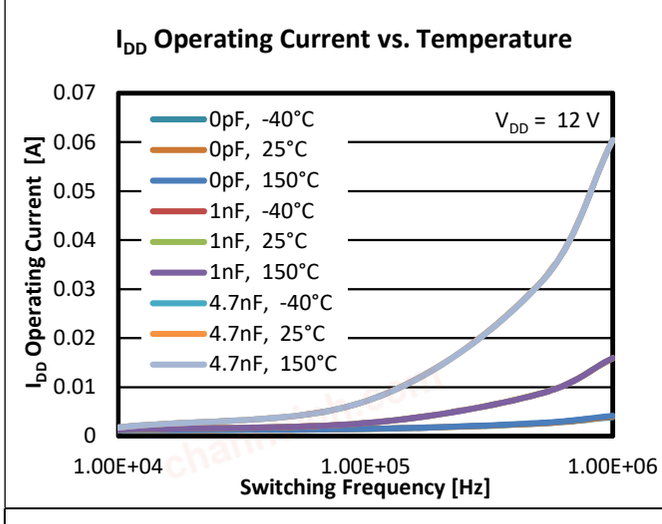
[3] Reference slew rate threshold versus temperature under Section 6 Typical Characteristics

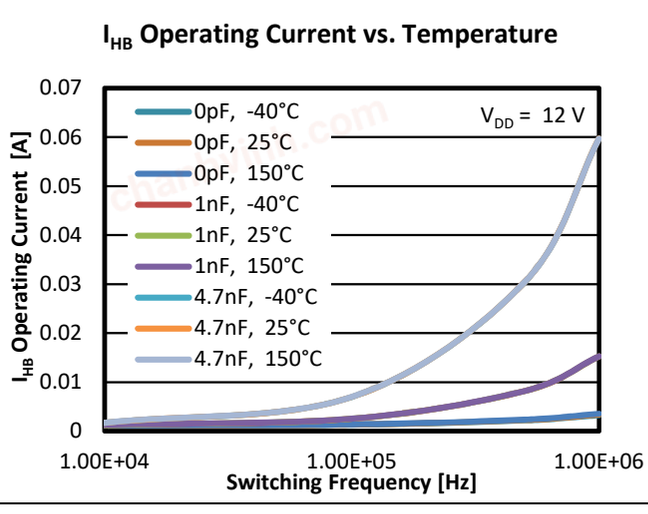
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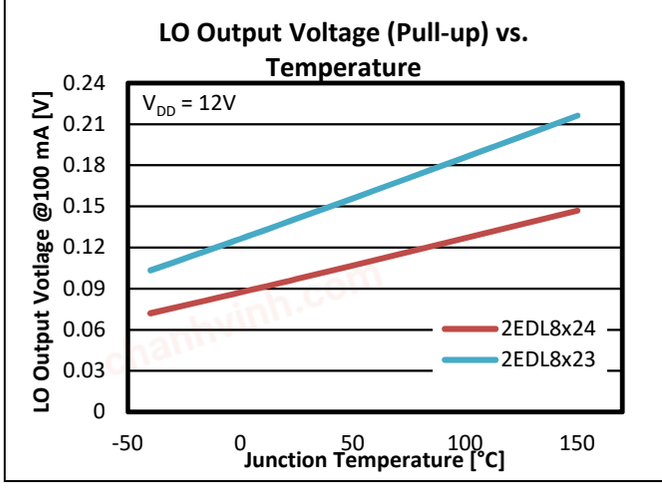
6 Typical Characteristics

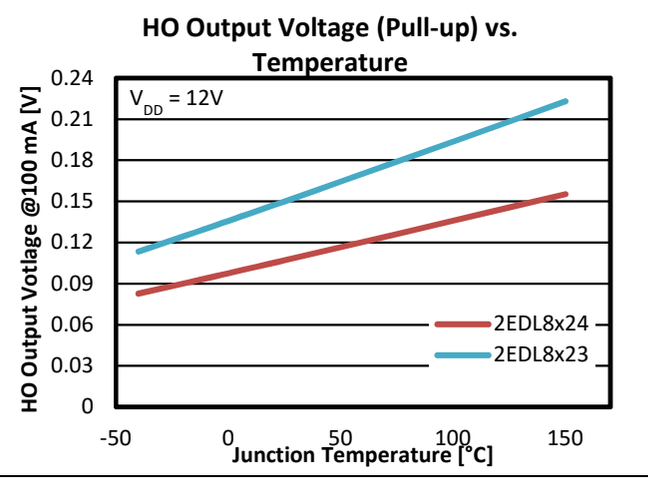






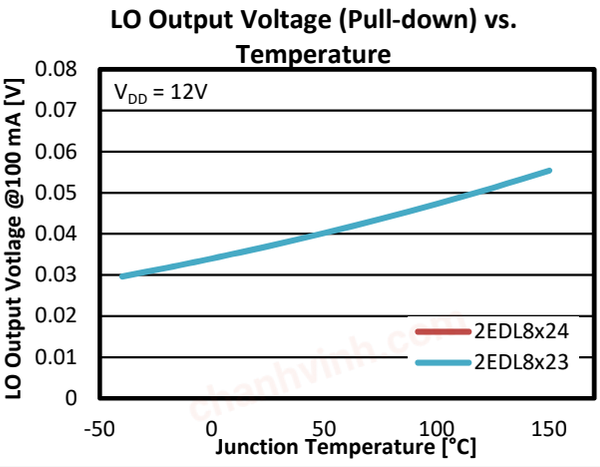


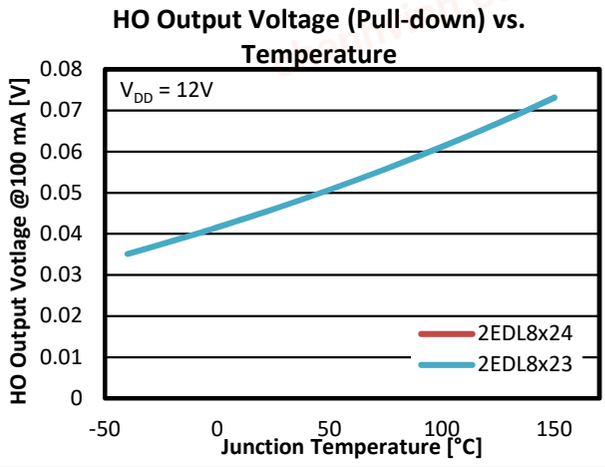


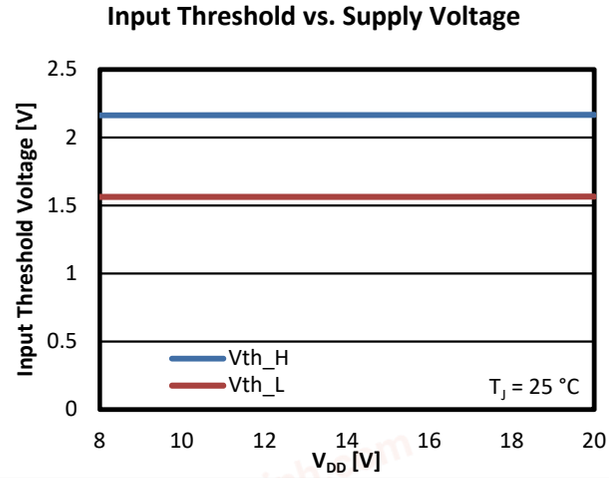


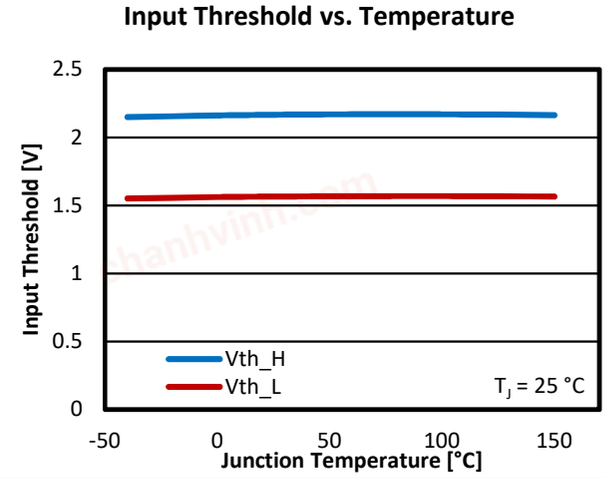
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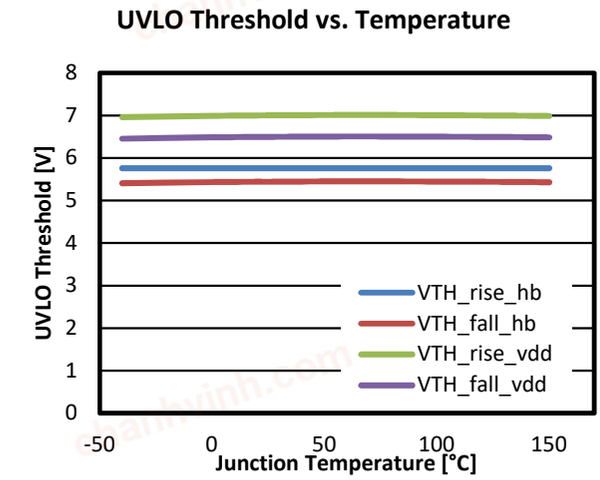
Typical Characteristics

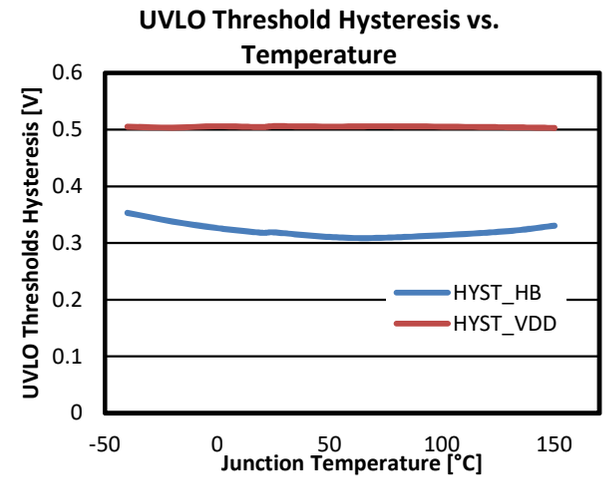






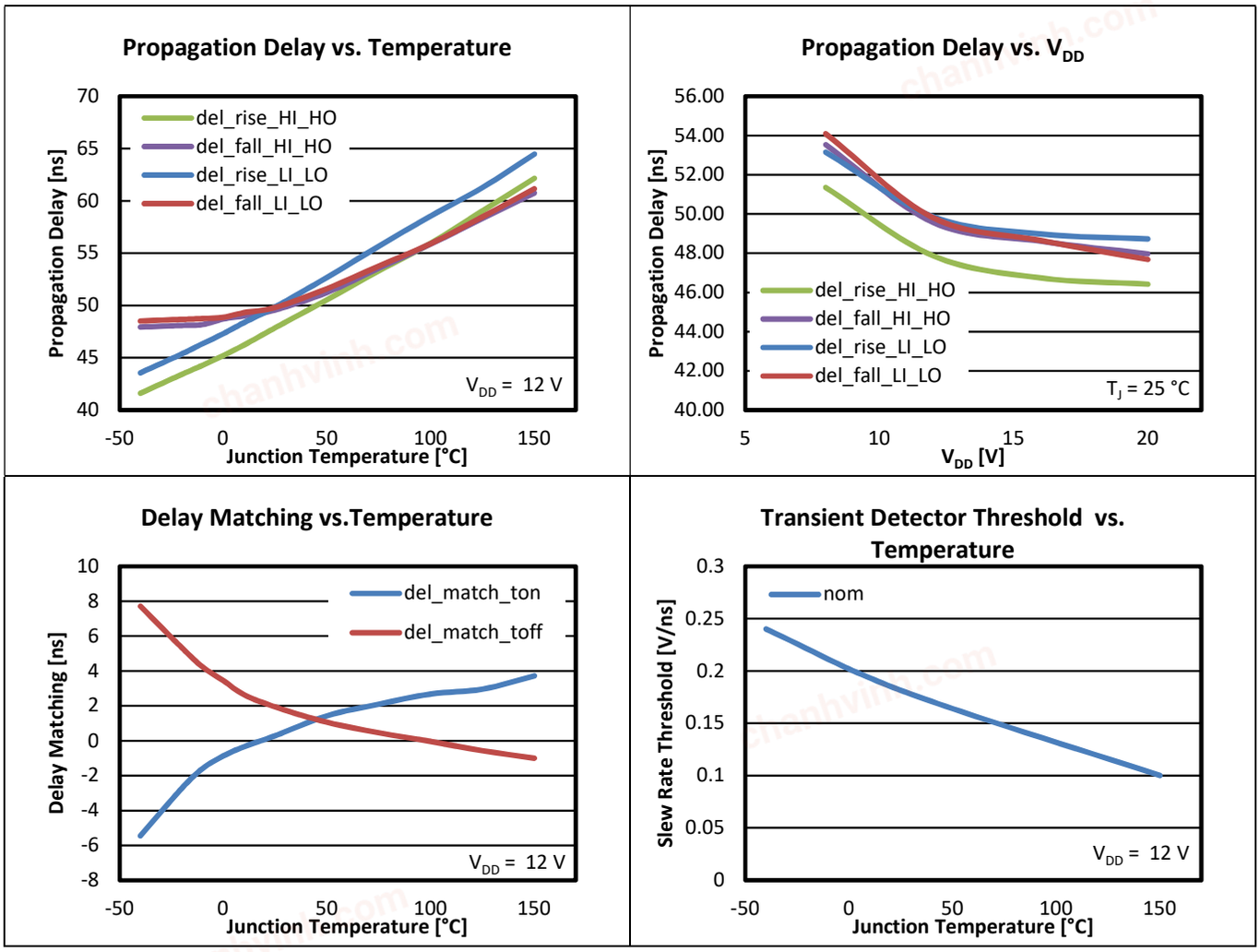






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Typical Characteristics



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7 Application and Guidelines

7.1 Typical Application Diagram

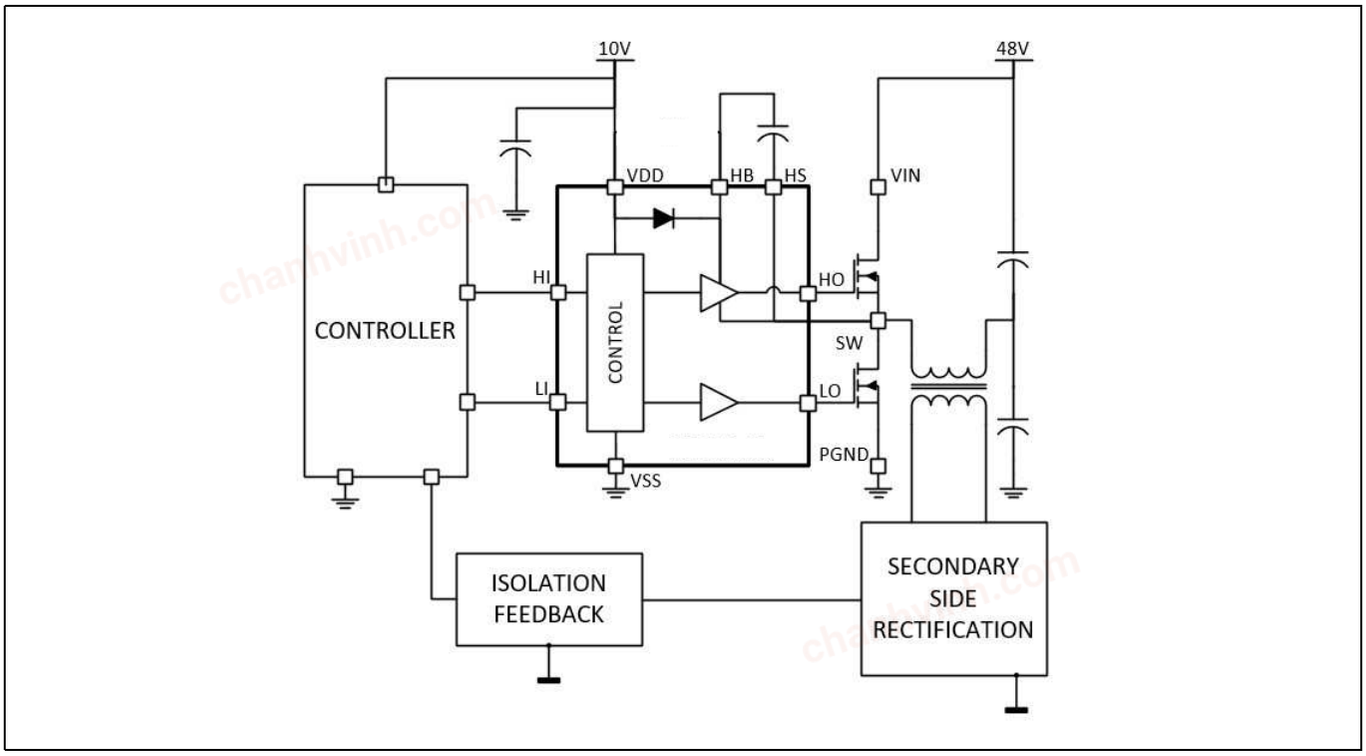


Figure 9 Typical Application 1 – Primary Side Half-bridge

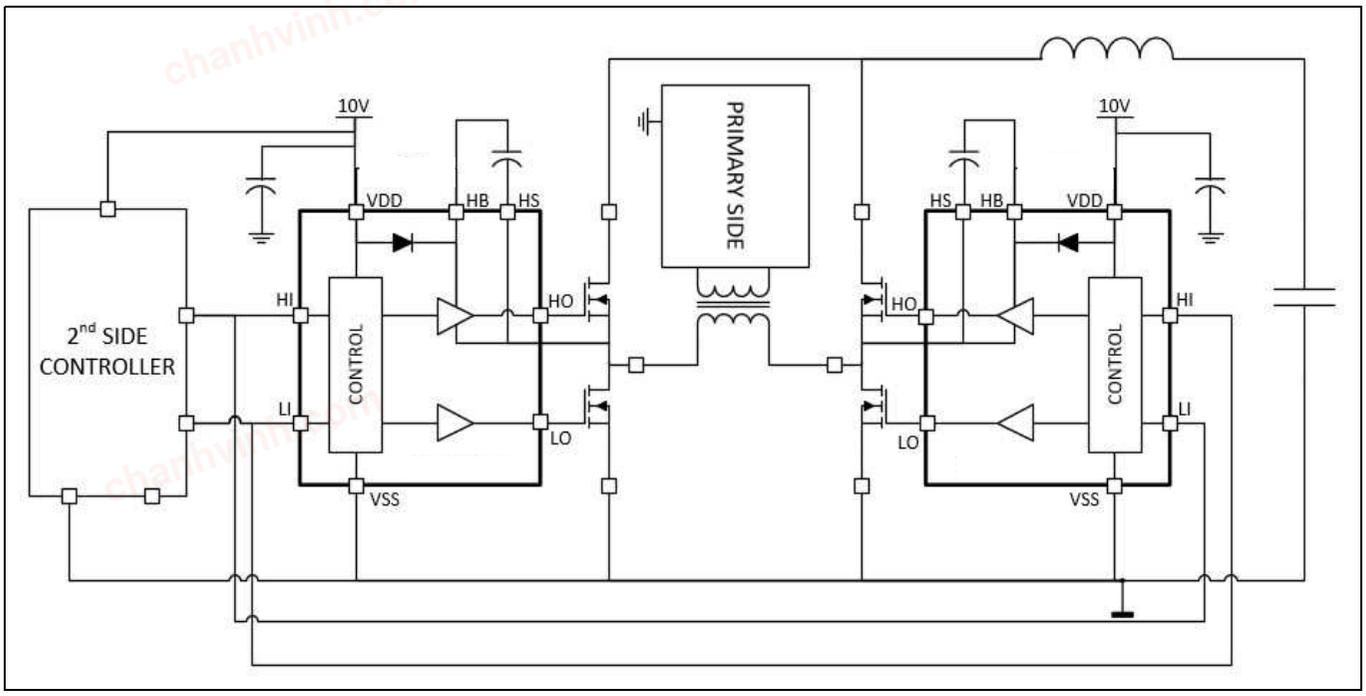


Figure 10 Typical Application 2 – Full-bridge Secondary Side Rectification

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7.2 Design Guidelines

In a half-bridge configurations, a high-side bias which is referenced to the switch node is needed in order to drive the gate of the high-side mosfet. One of the most common solutions due to its simplicity and low cost is the usage of a bootstrap circuit consisting of a resistor, a diode (internal to the driver) and a capacitor as seen in **Figure 11**. However, this method imposes limitation on the power converter's duty cycle due to the requirement of recharging the bootstrap capacitor. This limitation can be mitigated through the proper selection of the bootstrap components.

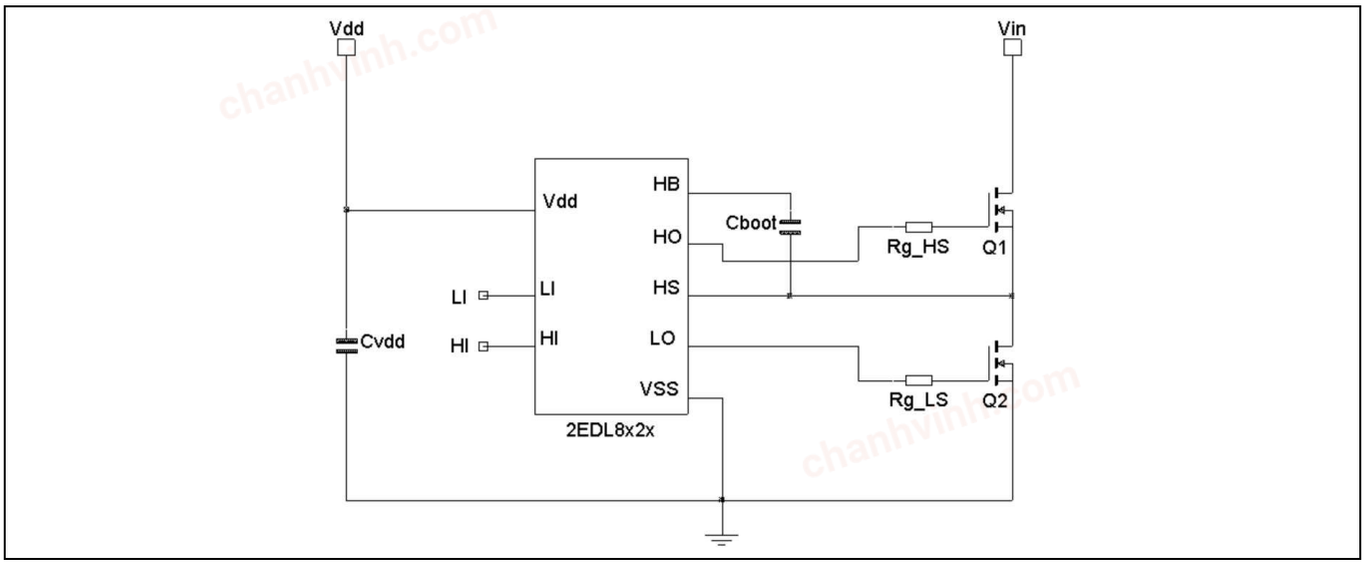


Figure 11 Gate drive circuitry using 2EDL8x2x to drive mosfet in a half-bridge configuration

The bootstrap circuit operation is defined by two main periods:

Charging period: When the low-side mosfet (Q2) is ON and the high-side mosfet (Q1) is OFF, the switch node / HS pin is pulled to ground creating a charging path for the bootstrap capacitor (C_{boot}) through the Vdd bypass capacitor (C_{Vdd}), and the internal bootstrap diode. For high dV/dt application, it is recommended to use an extrenal bootstrap diode.

Discharging period: When the low-side mosfet (Q2) is turned OFF and the high-side mosfet (Q1) starts conducting, the switch node / HS pin is pulled to the high voltage V_{in} thus the internal bootstrap diode gets reverse biased. The bootstrap capacitor (C_{boot}) will then discharge some of its stored charges to the gate of the high-side mosfet as well as to other contributing factors such as the mosfet's gate-source leakage current, floating section quiescent current, floating section leakage current and the internal bootstrap diode reverse bias leakage current.

Typical waveform for the voltage across C_{boot} as a function of time is shown in **Figure 12** where the various contributions have been distinguished. The voltage across C_{boot} increases during the charging period and then it drops with a high negative dV/dt as it charges the gate of the high-side mosfet (Q1). After which, the C_{boot} voltage continues to drop but with a much lower slope because only the high-side bias current and some leakage current is discharing the C_{boot} during this phase.

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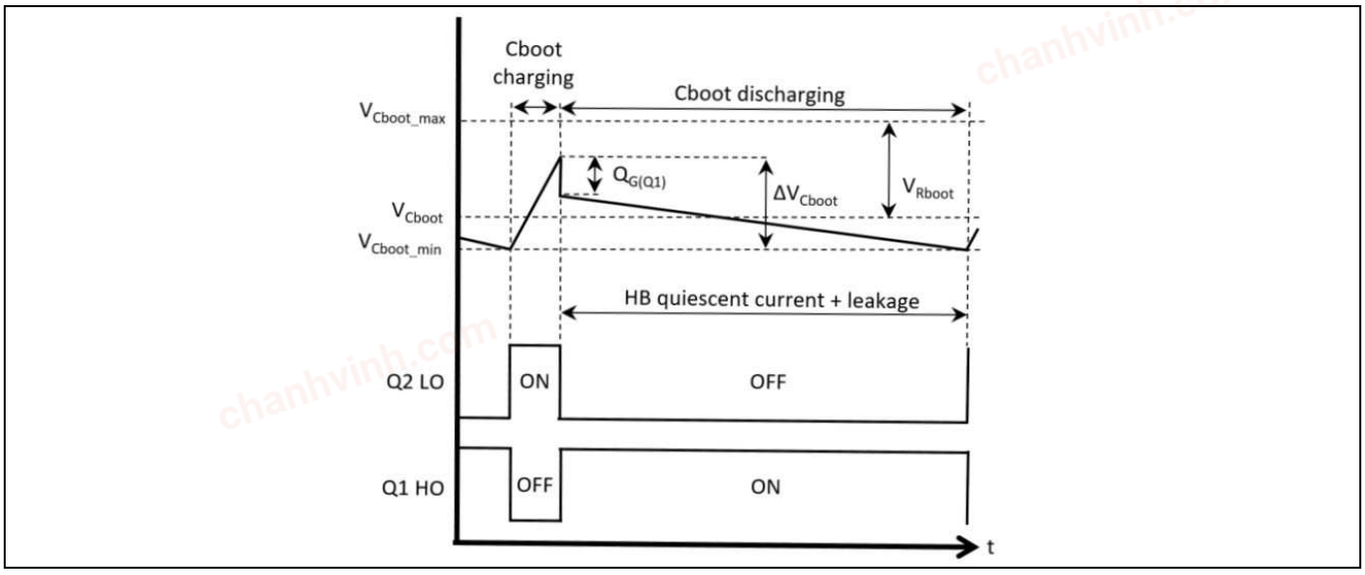


Figure 12 Typical C_{boot} waveform

7.2.1 Bootstrap Capacitor Selection

The bootstrap capacitor provides the necessary charge to drive the high-side mosfet and thus it needs to be sized in such a way that the maximum voltage drop across this capacitor will not fall below the high-side UVLO threshold during transient and normal operations. First, determine the maximum allowable voltage drop (ΔV_{Cboot_max}) when the high-side mosfet (Q1) is on which is given by the following formula:

$$\Delta V_{Cboot_max} = V_{dd} - V_F - V_{HBR} - V_{HBH} \quad (1)$$

Where:

V_{dd} = Gate driver supply voltage

V_F = Bootstrap diode forward voltage drop with typical value of 1.25 V at

I_F=100 uA and 2.15 V at I_F=100 mA , T_J=25°C

V_{HBR} = HB UVLO rising threshold

V_{HBH} = HB UVLO threshold hysteresis

Next, determine the total charge (Q_T) that must be delivered by the bootstrap capacitor at maximum duty cycle. As mentioned, there are several factors that contribute to the discharge of the bootstrap capacitor such as the Q1's total gate charge, Q1's gate-source leakage current, HB quiescent current, HB leakage current, bootstrap diode reverse bias leakage current and bootstrap capacitor leakage current (if using an electrolytic capacitor). For sake of simplicity, only Q1's total gate charge and HB quiescent and leakage current are considered as the other sources of leakage are negligible in comparison.

$$Q_T = Q_G + \frac{I_{HB}}{F_{sw}} + I_{HB} \times \frac{D_{max}}{F_{sw}} \quad (2)$$

Where:

Q_G = high-side mosfet (Q1) total gate charge

I_{HB} = HB maximum quiescent current

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I_{HBS} = HB to VSS leakage current with a typical value of 1.25 mA at 90 V HB voltage and T_J=25°C

D_{max} = maximum duty cycle

F_{sw} = switching frequency

The minimum bootstrap capacitor value can then be calculated using the formula:

$$C_{boot_min} \geq \frac{Q_T}{\Delta V_{Cboot_max}} \quad (3)$$

7.2.2 VDD Bypass Capacitor Selection

The Vdd bypass capacitor provides the charge for the bootstrap capacitor during the charging period. As a rule of thumb, the Vdd bypass capacitor should be sized to be atleast 10~20 times larger than the bootstrap capacitor. This equates to a voltage ripple of 5~10% in the Vdd capacitor.

$$C_{Vdd} \geq 10\sim20 \times C_{boot} \quad (4)$$

7.2.3 Bootstrap Resistor Selection

The bootstrap resistor limits the current in the bootstrap diode during start-up when the bootstrap capacitor is initially completely discharged. The peak current through this resistor is given by:

$$I_{Pk_Rboot} = \frac{V_{DD} - V_F}{R_{boot}} \quad (5)$$

The bootstrap resistor together with the bootstrap capacitor introduces a time constant and should be sized appropriately to achieve the desired start-up time. For this calculation, it is assumed that the bootstrap capacitor is fully charged after 4 time constant. With this, R_{boot} can be calculated using the following formula:

$$R_{boot} \leq \frac{t_{min}}{4 \times C_{boot}} \quad (6)$$

Where:

t_{min} = minimum on time of the low-side mosfet (Q2)

7.2.4 External Bootstrap Diode Selection

For high dV/dT applications, an external bootstrap diode is recommended to be in parallel with the internal bootstrap diode. A fast recovery or schottky diode with low forward voltage drop is recommended in order to minimize the losses and leakage current. It should be chosen such that it can handle the peak transient current from Equation (5) during start-up conditions and the blocking voltage rating should be higher than the maximum input voltage (V_{in}) with enough derating.

7.2.5 Gate Resistor Selection

The turn-on and turn-off external gate resistors control the turn-on and turn-off current of the gate driver providing an external way to control the switching speed of the mosfet for purposes such as voltage overshoot control, ringing reduction, EMI mitigation, spurious turn-on protection, shoot –through protection etc. The following formulas shows the effect of the external gate resistor to the output current capability of the gate driver.

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$$I_{HSRC} = \frac{V_{DD} - V_F}{R_{PUH} + R_{G_HS} + R_{G_int}} \quad (7)$$

$$I_{HSNK} = \frac{V_{DD} - V_F}{R_{PDH} + R_{G_HS} + R_{G_int}} \quad (8)$$

$$I_{LSRC} = \frac{V_{DD}}{R_{PU} + R_{G_LS} + R_{G_int}} \quad (9)$$

$$I_{LSNK} = \frac{V_{DD}}{R_{PDL} + R_{G_LS} + R_{G_int}} \quad (10)$$

Where:

I_{HSRC} = High-side peak source current
I_{HSNK} = High-side peak sink current
I_{LSRC} = Low-side peak source current
I_{LSNK} = Low-side peak sink current
R_{PUH} = High-side pull-up resistance
R_{PDH} = High-side pull-down resistance
R_{PUL} = Low-side pull-up resistance
R_{PDL} = Low-side pull-down resistance
V_{DD} = Gate driver supply voltage
V_F = Bootstrap diode forward voltage drop
R_{G_HS} = High-side external gate resistance
R_{G_LS} = Low-side external gate resistance
R_{G_int} = Mosfet internal gate resistance

For a detailed discussion on how to optimize the gate resistors, a dedicated application note with link in the reference section, e.g. [2], can be viewed.

7.3 PCB Layout Guidelines

In order to maximize the performance of EiceDRIVER™ 2EDL8x2x, below are some recommendations on how to optimize the PCB layout

- Use a low-ESR decoupling capacitors on VDD-GND and HB-HS and placed it as close as possible to the VDD-GND and HB-HS pins of the driver
- An option for a series boot resistor is recommended to control the high side mosfet slew rate and therefore the low side mosfet overshoot. The boot loop path including the VDD capacitor, boot diode, boot series resistor and boot capacitor should be as small as possible
- It is recommended to have an external boot diode placement for high dv/dt application.
- Placement for gate resistor is also recommended to control the switching speed of the mosfet. Both the gate resistor and the mosfet should be placed as close as possible to the driver in order to minimize the gate loop inductance.
- Use copper plane underneath the exposed GND pad of the driver and connect it to buried copper plane(s) with multiple thermal vias for better heat dissipation into the PCB.
- Connection to the HS pin of the driver from the high side mosfet source and low side mosfet drain should be as short and wide as possible and avoid connecting it directly through the high switching current path.
- LO and HO traces should be as short and wide as possible
- Avoid letting the LI and HI signal trace to come close to high dV/dT traces which might induce significant noise.

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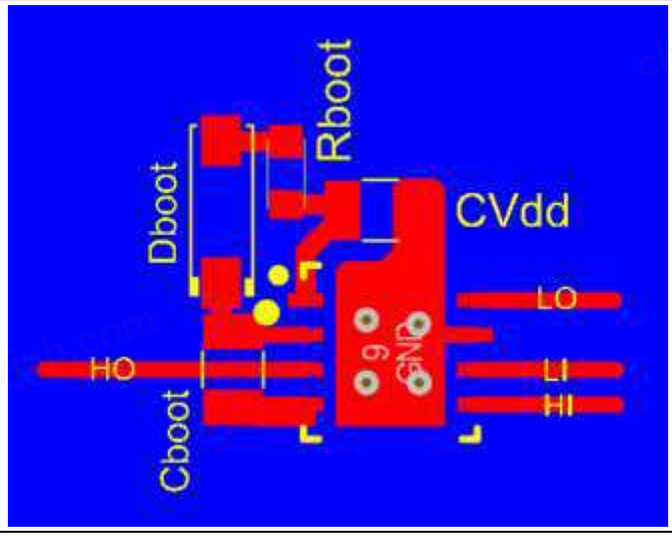
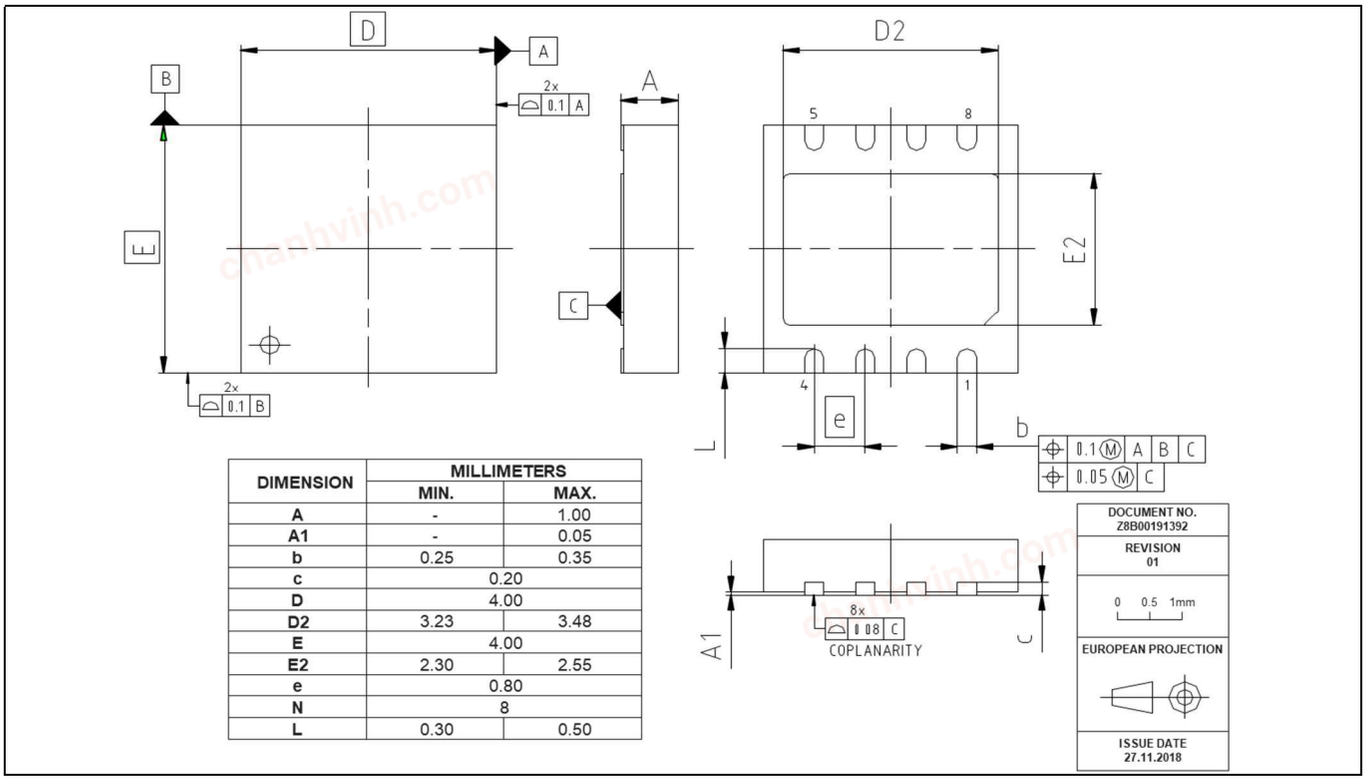


Figure 13 2EDL8x2x Layout Example

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8 Outline Dimensions

8.1 PG-VDSON-8-4 Package Outline



DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	-	1.00
A1	-	0.05
b	0.25	0.35
c	0.20	
D	4.00	
D2	3.23	3.48
E	4.00	
E2	2.30	2.55
e	0.80	
N	8	
L	0.30	0.50

Figure 14 PG-VDSON-8-4 Outline Dimensions

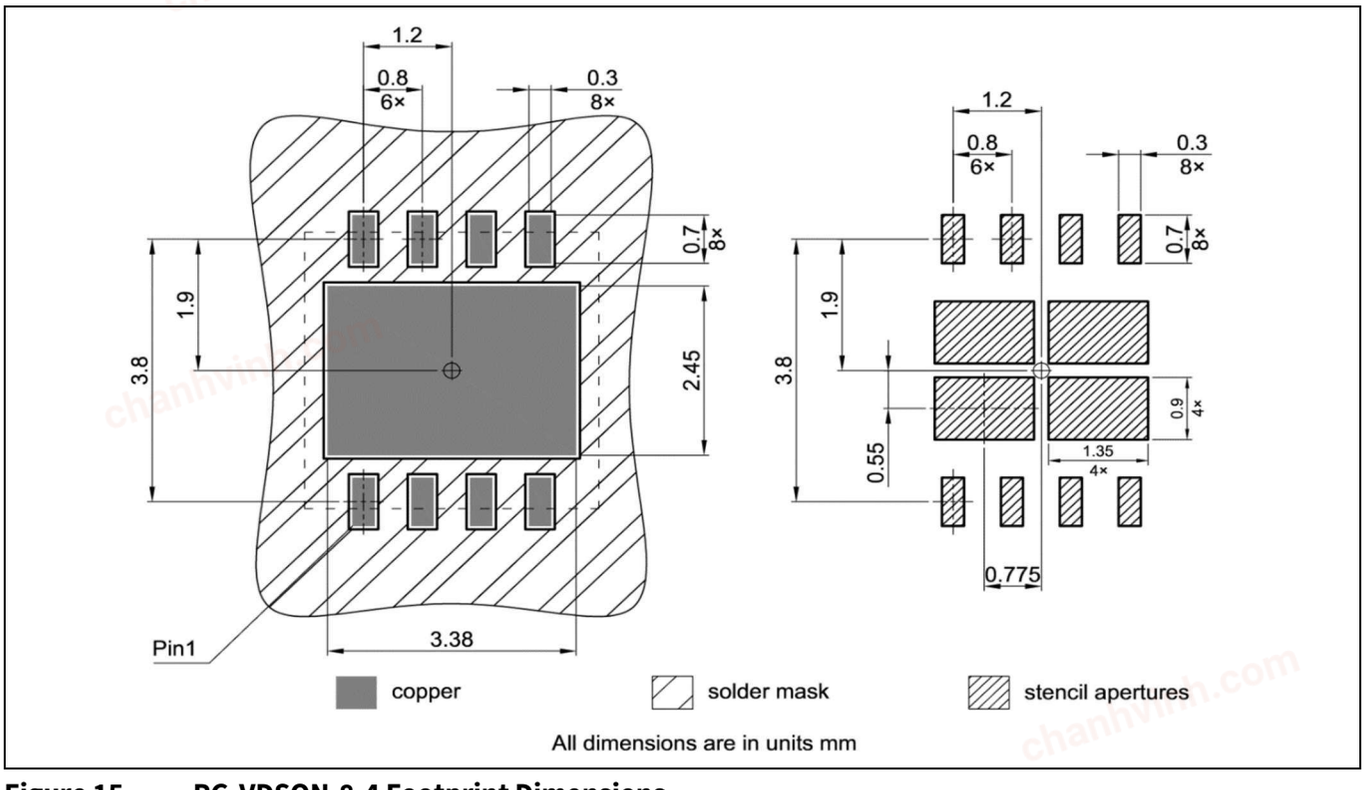


Figure 15 PG-VDSON-8-4 Footprint Dimensions

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8.2 PG-VSON-10-4 Package Outline

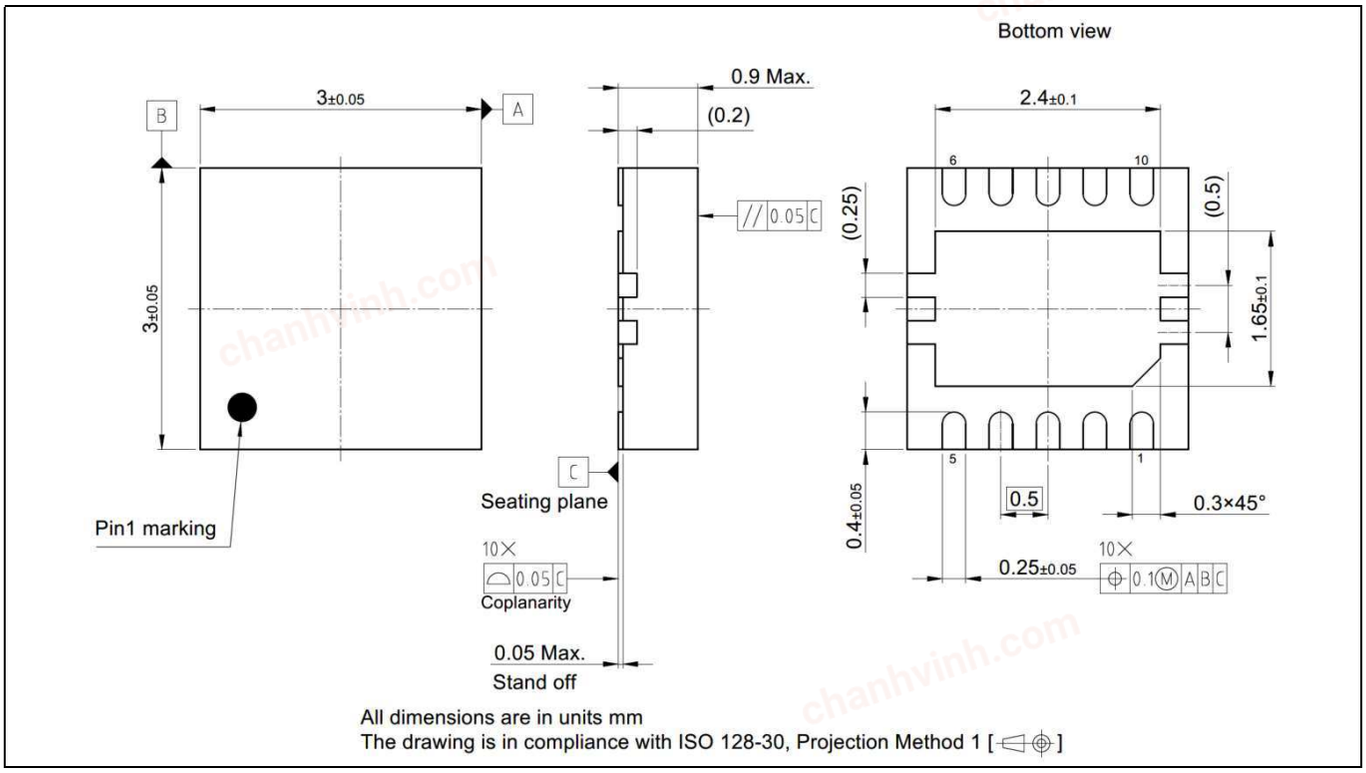


Figure 16 PG-VSON-10-4 Outline Dimensions

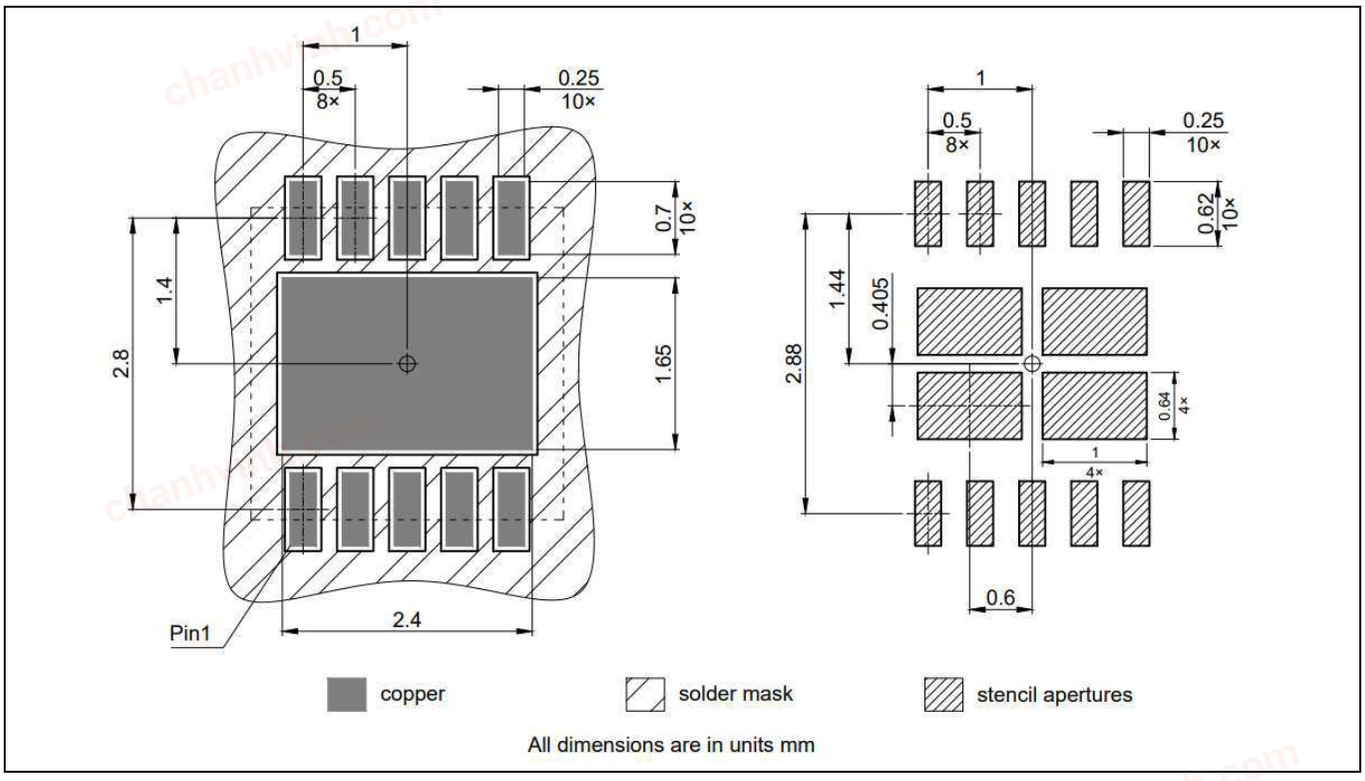


Figure 17 PG-VSON-10-4 Footprint Dimensions

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9 Reel and Tape

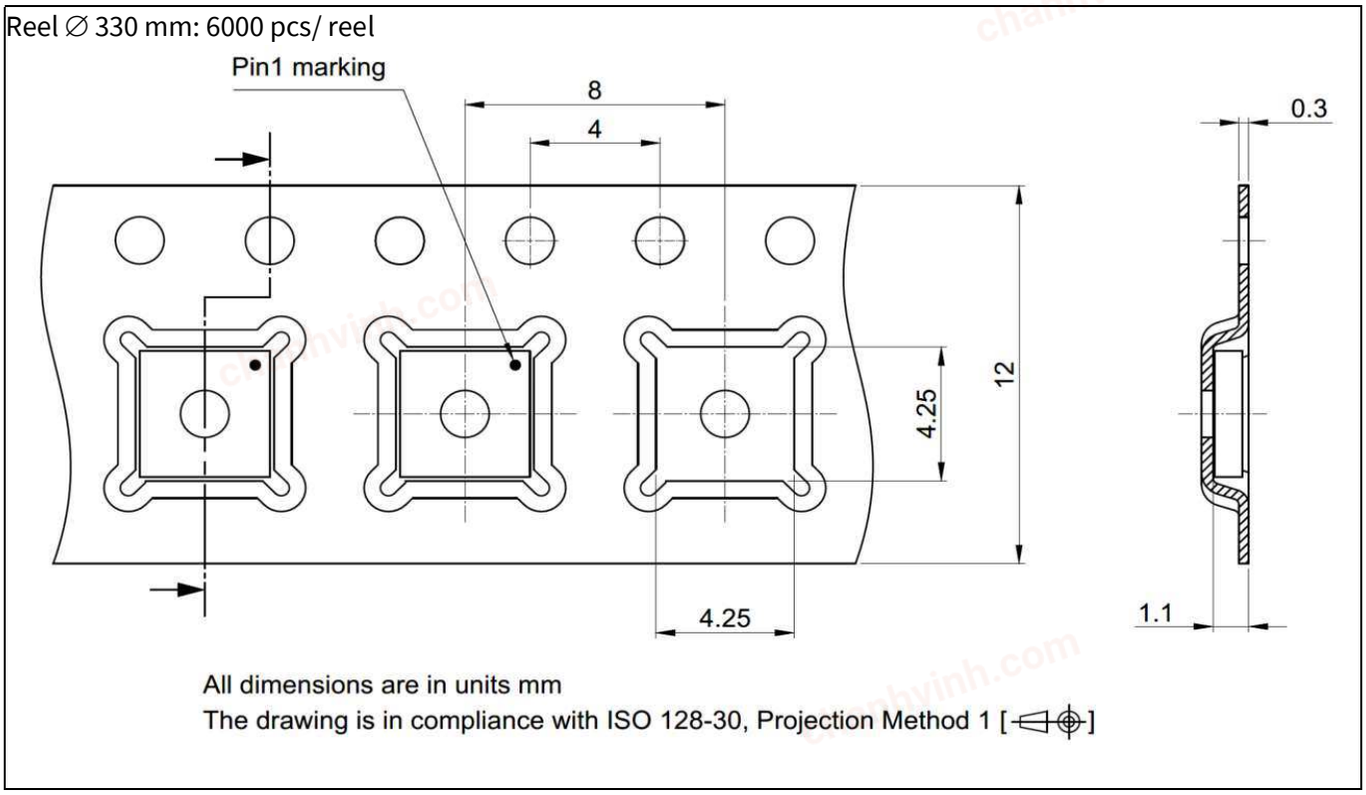


Figure 18 PG-VDSON-8-4 Reel and Tape

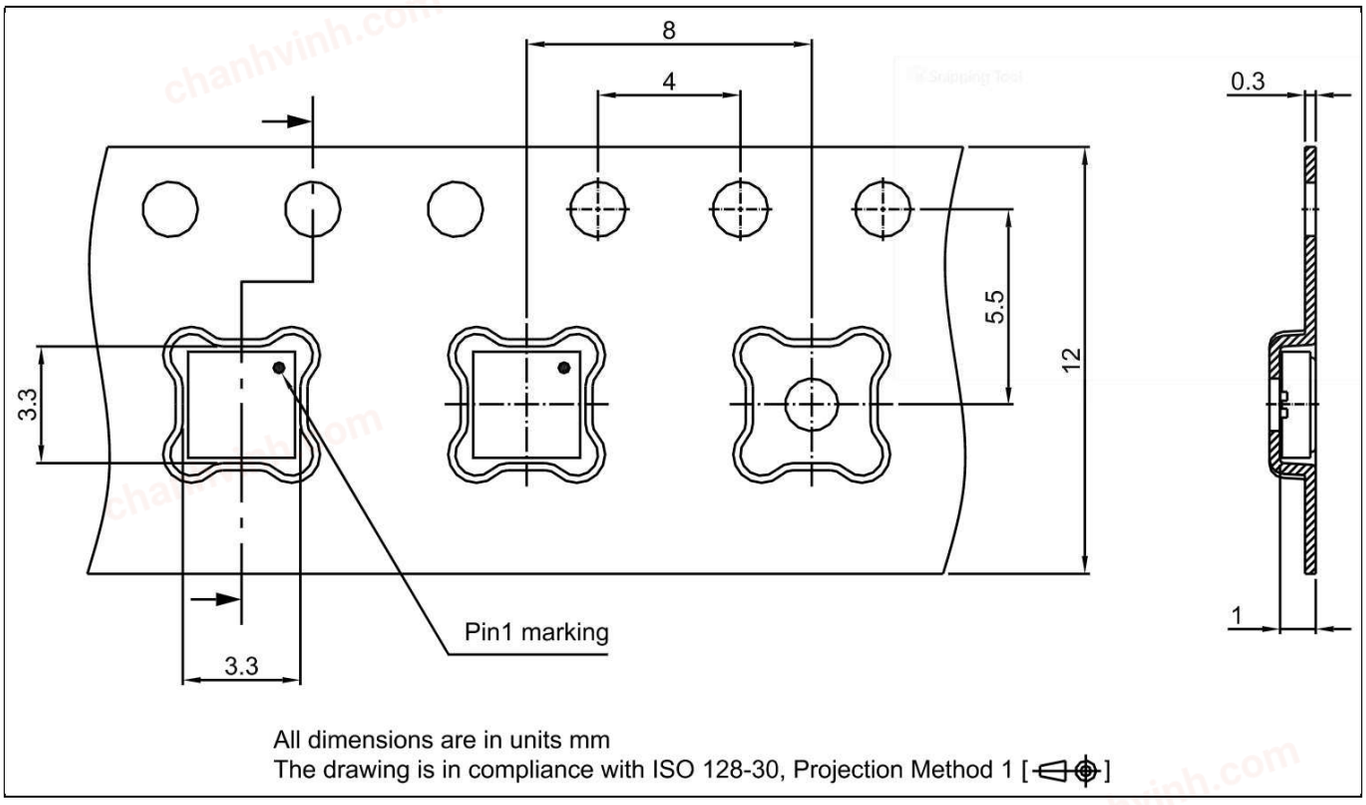


Figure 19 PG-VSON-10-4 Reel and Tape

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10 References

[1] Alan Huang, *Understanding the transient detector*, Infineon Technologies AG, Neubiberg 2020

[2] A2015-06 EiceDRIVER™ – gate resistor for power devices

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Revision History

2EDL8x2x

Revision: 2022-09-23, Rev. 2.8

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.2	2020-07-28	Separate table for ESD rating and remove footnote 1 under Abs Max Rating
2.3	2020-10-20	Update footprint, LO/HO Pull-up resistance, LO/HO Output voltage, maximum delay spec, HB operating current and remove external diode in diagrams.
2.4	2020-12-30	Update Tape and Reel specification
2.5	2021-10-11	Include VSON-10 3x3 package details
2.6	2022-04-25	Add repetitive pulse note, minimum DC rating for HS, differential input voltage, minimum input rising threshold, maximum input falling, description leakage current, removed 2EDL812x voltage description, rename "input control" and fix footnote numbering.
2.7	2022-05-12	Update marking pin in Tape and Reel and 3D drawing for PG-VSON-10-4
2.8	2022-09-23	Update UVLO illustration and description.

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