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1ED44176N01F

Single-channel low-side gate driver IC with over-current protection

Features

- Over-current detection with positive voltage input
- 0.5 V over-current threshold with accurate ±5% tolerance
- Single pin for fault output and enable
- Programmable fault clear time
- Under voltage lockout
- CMOS Schmitt-triggered inputs
- 3.3 V, 5 V and 15 V input logic compatible
- Output in phase with input
- Separate logic and power ground
- 2 kV ESD HBM
- RoHS compliant
- Evaluation board available: EVAL-1ED44176N01F

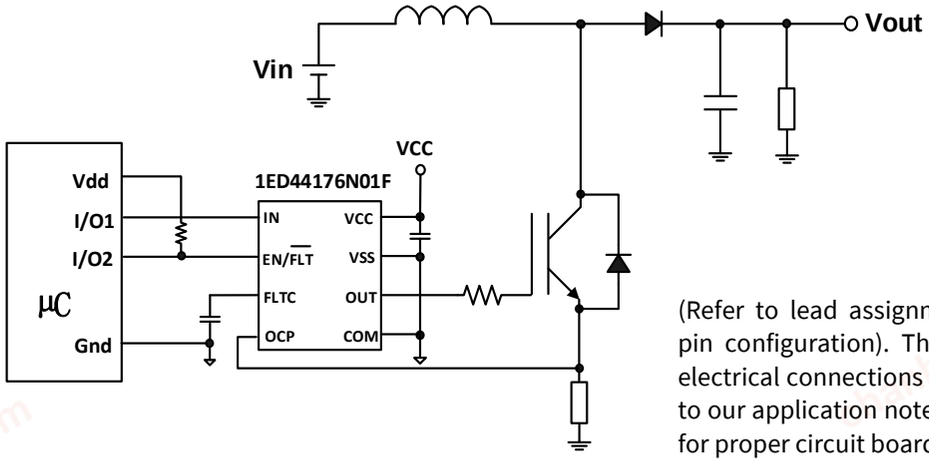
Potential applications

- Digitally controlled PFC
- Air conditioner
- Home appliances
- Industrial applications
- General purpose low-side gate driver for single-ended topologies



Description

The 1ED44176N01F is a low-voltage, power MOSFET and IGBT non-inverting gate driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output driver features a current buffer stage. The 1ED44176N01F has OCP pin for over current protection sense and a FAULT status output (Once it is active, EN/$\overline{\text{FLT}}$ pin is internally pulled down.). There is a dedicated pin (FLTC) to program fault clear time. The EN/$\overline{\text{FLT}}$ needs to be outside pulled up to provide normal operation, pulling EN/$\overline{\text{FLT}}$ low disable the driver. Internal circuitry on VCC pin provides an under voltage lockout protection that holds output low until Vcc supply voltage is within operating range.



(Refer to lead assignments for correct pin configuration). This diagram show electrical connections only. Please refer to our application notes and design tips for proper circuit board layout.

Figure 1 Typical application

Ordering information

Product type	Package	Standard pack		Orderable part number
		Form	Quantity	
1ED44176N01F	PG-DSO-8	Tape and Reel	2500	1ED44176N01FXUMA1

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47/22 and J-STD-020.

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1 Block diagram

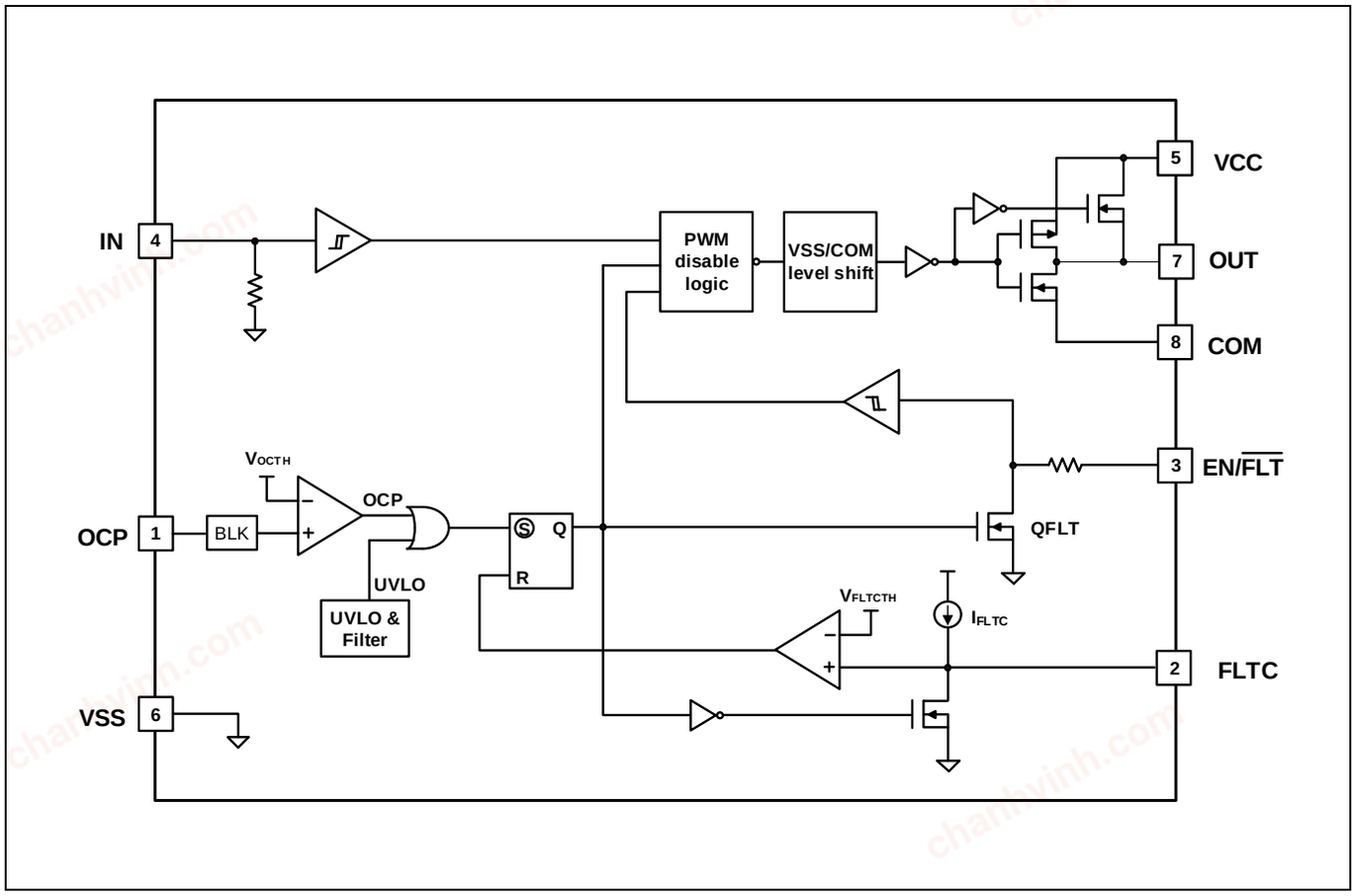

Figure 2 Block diagram

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2 Pin configuration and functionality

2.1 Pin configuration

Table 1 Pin configuration

Pin no.	Name	Function
1	OCP	Current sense input
2	FLTC	Fault clear time program input
3	EN/$\overline{\text{FLT}}$	Enable and fault reporting pin, two functions: 1. Logic input to enable I/O functionality. I/O logic functions when ENABLE is high and enable function is not latched. 2. Fault reporting function like over-current or undervoltage lockout, this pin has negative logic and an open-drain output.
4	IN	Logic input for gate driver output (OUT), in phase
5	VCC	Supply voltage
6	VSS	Logic ground
7	OUT	Gate drive output
8	COM	Gate drive return

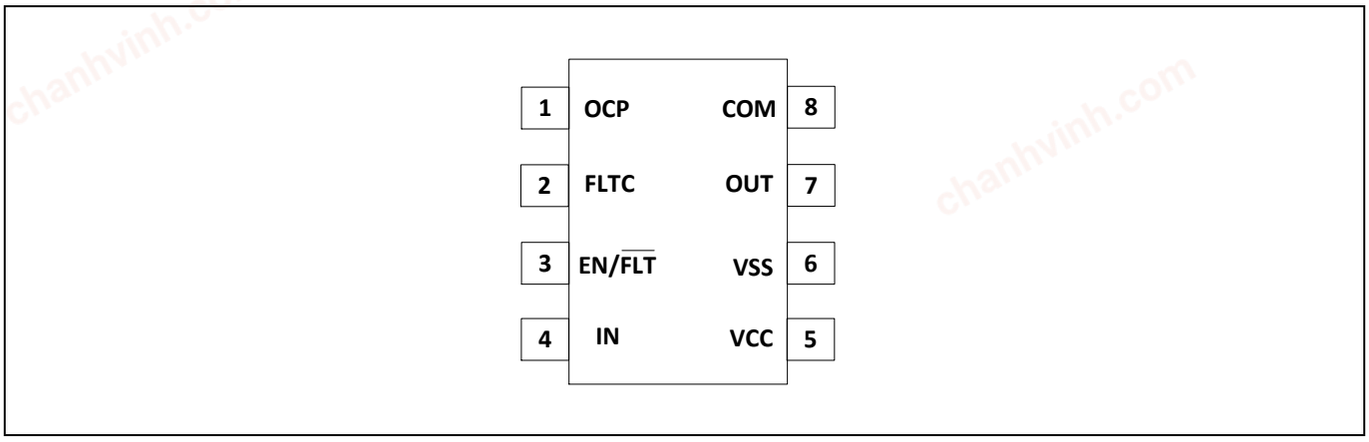

Figure 3 PG-DSO-8-70 (top view)

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2.2 Input/output logic truth table

Table 2 Input/output logic truth table

IN	UVLO [1]	OCP [2]	$EN/\overline{FLT}$ [3]	OUT	Note
L	L	L	H	L	OUT = L
H	L	L	H	H	OUT = H
X	H	X	L	L	OUT = L, $EN/\overline{FLT}$ = L, (UVLO protection will disable I/O logic until $EN/\overline{FLT}$ returns to high level.)
X	L	H	L	L	OUT = L, $EN/\overline{FLT}$ = L, (Over current protection will disable I/O logic until $EN/\overline{FLT}$ returns to high level.)
X	L	X	L	L	OUT = L (Externally pull down $EN/\overline{FLT}$ pin will disable I/O logic until $EN/\overline{FLT}$ returns to high level.)

1) UVLO “H” state is under-voltage protection.
2) OCP “H” state is over-current protection.
3) $EN/\overline{FLT}$ “H” state is $EN/\overline{FLT}$ pin externally pulling up and internally pull down MOSFET (Q_{FLT}) is off. (See block diagram.)

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3 Qualification information

Qualification level		Industrial [1)] Comments: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.
Moisture sensitivity level		MSL3 [2)] 260°C (per JEDEC standard J-STD-020)
ESD	Charged device model	1000 V (Class C3) (per ANSI/ESDA/JEDEC standard JS-002)
	Human body model	Class 2 (per ANSI/ESDA/JEDEC standard JS-001)
IC latch-up test		Class II, Level A (per JESD78)
RoHS compliant		Yes

1) Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
2) Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

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4 Electrical parameters

4.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. The device may not function or not be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. All voltage parameters are absolute voltages referenced to VSS. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 3 Absolute maximum ratings

Symbol	Definition		Min	Max	Units
V_{CC}	Fixed supply voltage		– 0.5	25	V
V_O	Output voltage (OUT)		COM - 0.5	V_{CC} + 0.5	
V_{OCP}	Voltage at current sense pin (OCP)		– 0.5	V_{CC} +0.5	
$V_{EN/\overline{FLT}}$	Voltage at enable and fault reporting pin ($EN/\overline{FLT}$)		– 0.5	V_{CC} + 0.5	
V_{FLTC}	Voltage at fault clear time program pin (FLTC)		– 0.5	V_{CC} + 0.5	
V_{IN}	Logic input voltage (IN)		– 0.5	V_{CC} + 0.5	
COM	Driver return voltage		– 5	V_{CC} + 0.5	
P_D	Package power dissipation @ $T_A \le 25°C$	PG-DSO-8	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient		—	200	°C/W
T_J	Junction temperature		– 40	150	°C
T_S	Storage temperature		– 55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	260	

4.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to VSS unless otherwise stated in the table.

Table 4 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	12.7	20	V
V_O	Output voltage	COM	V_{CC}	
V_{OCP}	Voltage at current sense pin (OCP)	0	V_{CC}	
$V_{EN/\overline{FLT}}$	Voltage at enable and fault reporting pin ($EN/\overline{FLT}$)	0	V_{CC}	
V_{FLTC}	Voltage at fault clear time program pin (FLTC)	0	V_{CC}	
V_{IN}	Logic input voltage (IN)	0	V_{CC}	
COM	Logic ground with respect to VSS	– 5	+5	
T_A	Ambient temperature	– 40	125	°C

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4.3 Static electrical characteristics

V_{CC} = 15 V, VSS=COM, T_A = 25°C unless otherwise specified. The V_{IN}, V_{EN}, V_{FLTCTH}, V_{OCTH}, I_{IN}, $I_{\overline{FLT}}$, and I_{FLTC} parameters are referenced to VSS and are applicable to input leads: IN,EN/$\overline{FLT}$, FLTC and OCP. The V_O and I_O parameters are referenced to COM and are applicable to the output lead: OUT.

Table 5 Static electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	Vcc supply undervoltage positive going threshold	11.2	11.9	12.7	V	
V_{CCUV-}	Vcc supply undervoltage negative going threshold	10.7	11.4	12.2		
V_{CCUVH}	Vcc supply undervoltage lockout hysteresis	—	0.5	—		
V_{INL}	Logic “0” input voltage (OUT = LO)	0.8	1	1.2		
V_{INH}	Logic “1” input voltage (OUT = HI)	1.7	2.1	2.5		
V_{ENL}	Logic “0” disable voltage	0.8	1	1.2		
V_{ENH}	Logic “1” enable voltage	1.7	2.1	2.5		
V_{FLTCTH}	Fault clear threshold Voltage	2.4	2.7	3		
V_{OH}	High level output voltage, V_{CC} -V_{OUT}	—	0.05	0.2		I_O = 2 mA
V_{OL}	Low level output voltage, V_{OUT}	—	0.02	0.1		I_O = 2 mA
V_{OCTH}	Current limit threshold voltage	475	500	525	mV	
I_{IN+}	Logic “1” input bias current IN pin	35	50	70	µA	V_{IN} = 5 V
I_{IN-}	Logic “0” input bias current IN pin	-5	—	—		V_{IN} = 0 V
I_{QCC}	Quiescent V_{CC} supply current	—	—	750		V_{IN} = 0 V or 5 V
I_{O+}	Output sourcing short circuit pulsed current	0.56	0.8	—	A	V_O = 0 V PW ≤ 10 µs
I_{O-}	Output sinking short circuit pulsed current	1.23	1.75	—		V_O = 15 V PW ≤ 10 µs
$I_{\overline{FLT}}$	EN/$\overline{FLT}$ pull down sinking current	20	—	—	mA	$V_{EN/\overline{FLT}}$ = 0.4 V
I_{FLTC}	Fault clear sourcing current	-40	-25	-15	µA	V_{FLTC} = 0 V

4.4 Dynamic electrical characteristics

V_{CC} = 15 V, T_A = 25°C, and C_L = 1000 pF unless otherwise specified.

Table 6 Dynamic electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	50	95	ns	Figure 6 V_{IN} pulse = 5 V
t_{off}	Turn-off propagation delay	—	50	95		
t_r	Turn-on rise time	—	50	80		
t_f	Turn-off fall time	—	25	35		
t_{EN}	Enable propagation delay	—	50	95		Figure 14 V_{EN} pulse = 5 V
t_{DISA}	Disable propagation delay	—	50	95		
t_{OCPDEL}	Over current protection propagation delay	—	380	470		Figure 10 Figure 11 R_{EN}=10kΩ to Vcc V_{OCP} pulse = 1 V
t_{OCPFLT}	OCP to low level EN/$\overline{FLT}$ signal delay	—	350	440		
t_{FLTC}	FAULT clear time	75	110	180	µs	Figure 10 Figure 11 C_{FLTC}=1nF to VSS
t_{BLK}	Over current protection blanking time	100	180	250	ns	Figure 11 R_{FLT}=0Ω, C_{FLT}= NC V_{OCP} pulse = 1V
tv_{CCUV}	VCC supply UVLO filter time	—	2	—	µs	Figure 8

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5 Application information and additional details

Information regarding the following topics is included as subsections within this section of the datasheet.

- IGBT/MOSFET gate driver
- Switching and timing relationships
- Input logic compatibility
- Undervoltage lockout protection
- Over current protection (OCP)
- Fault reporting and programmable fault clear timer
- Enable input

See the 1ED44176N01F application note AN2018-03 Low - Side Driver with Over Current Protection and Fault/Enable for interface circuit examples and recommended layout guidelines.

5.1 IGBT/MOSFET gate driver

The 1ED44176N01F is designed to drive MOSFET or IGBT power devices. Figure 4 and Figure 5 illustrate several parameters associated with the gate driver functionality of the driver. The output current of the driver, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{OUT}.

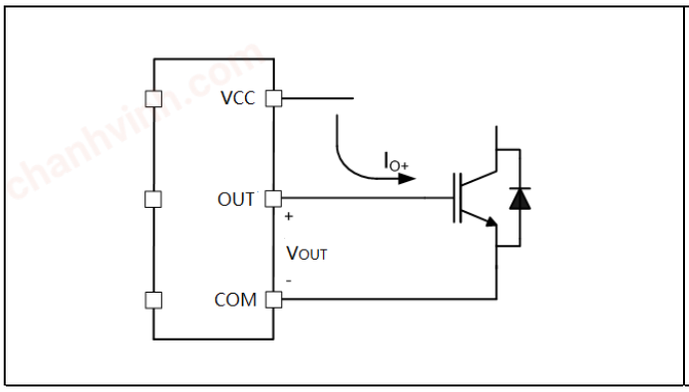

Figure 4 Gate output sourcing current

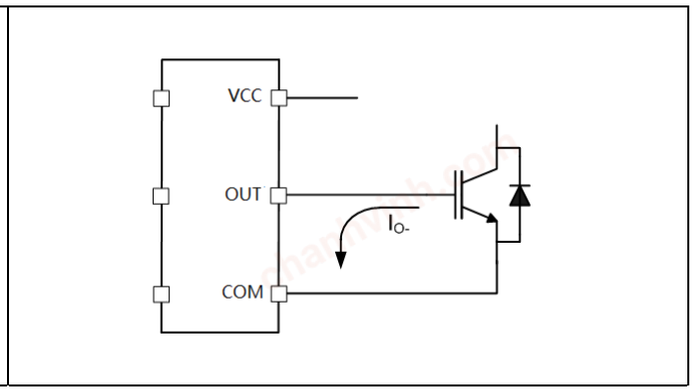

Figure 5 Gate output sinking current

5.2 Switching and timing relationships

The relationships between the input and output signals of the 1ED44176N01F are illustrated below in Figure 6. From the figure, we can see the definitions of several timing parameters (i.e. t_{on}, t_{off}, t_r, and t_f) associated with this device.

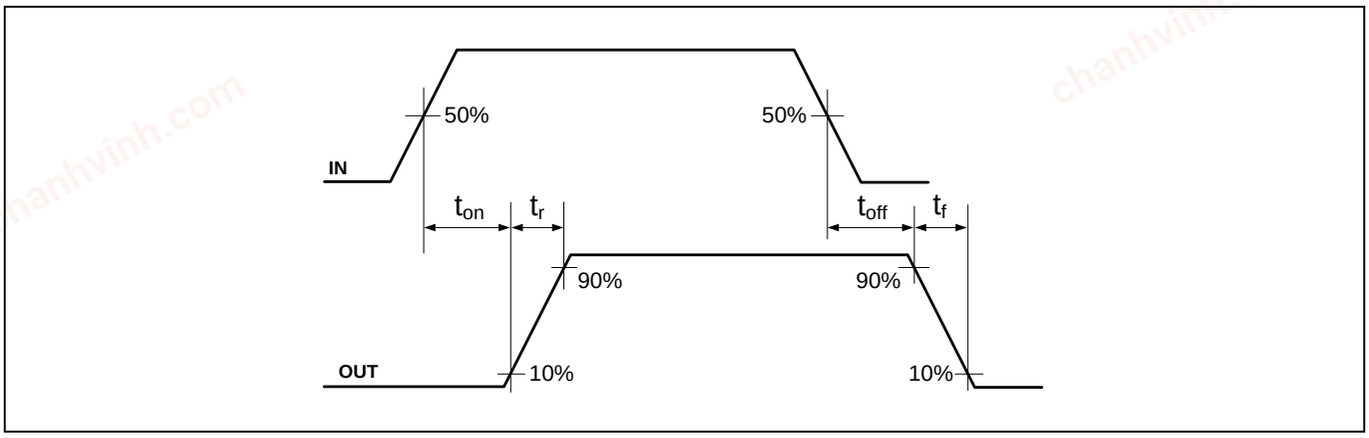

Figure 6 Switching time waveforms

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5.3 Input logic compatibility

The input of this IC is compatible with standard CMOS and TTL outputs. The 1ED44176N01F has been designed to be compatible with 3.3 V, 5 V and 15 V logic-level signals. The input high threshold (V_{INH}) is typ. 2.1 V and low threshold (V_{INL}) is typ. 1 V. Input hysteresis offers enhanced noise immunity. The 1ED44176N01F includes an important feature: wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using GND pull-down resistors on the input pin. Figure 7 illustrates an input signal to the 1ED44176N01F, its input threshold values, and the logic state of the IC as a result of the input signal.

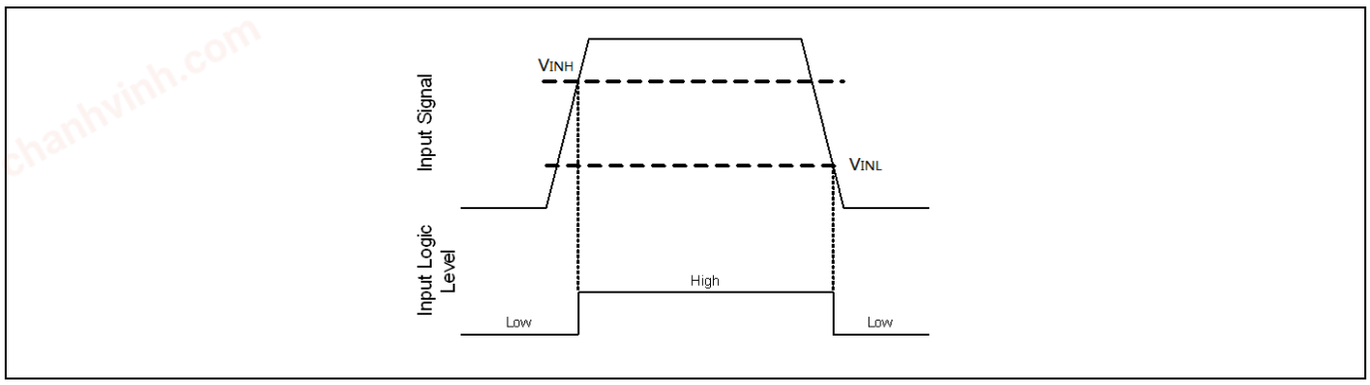

Figure 7 IN input thresholds

5.4 Undervoltage lockout (Vcc)

The 1ED44176N01F has an internal UVLO protection feature on the VCC pin supply circuit blocks.Upon power-up, if the VCC voltage fails to reach the V_{CCUV+} threshold, the driver cannot turn on. Additionally, if the VCC voltage decreases below the V_{CCUV-} threshold and the VCC bias voltage remains lower than the V_{CCUV-} threshold exceeding UVLO filter time (t_{VCCUV}) during operation, the undervoltage lockout circuitry will recognize a fault condition and shut-down the drive output. The $\mathrm{EN}/\overline{\mathrm{FLT}}$ will then transit to the low state to inform the controller of the fault condition, regardless of the status of the IN input pin. The t_{VCCUV} about 2µs helps to suppress noise from the UVLO circuit, so that negative-going voltage spikes at the supply pin will avoid parasitic UVLO events.

When VCC is higher than V_{CCUV+} and longer than t_{FLTC}, $\mathrm{EN}/\overline{\mathrm{FLT}}$ becomes high and the OUT will follow the input signal IN. (Figure 8 shows the UVLO time is shorter than t_{FLTC}.)

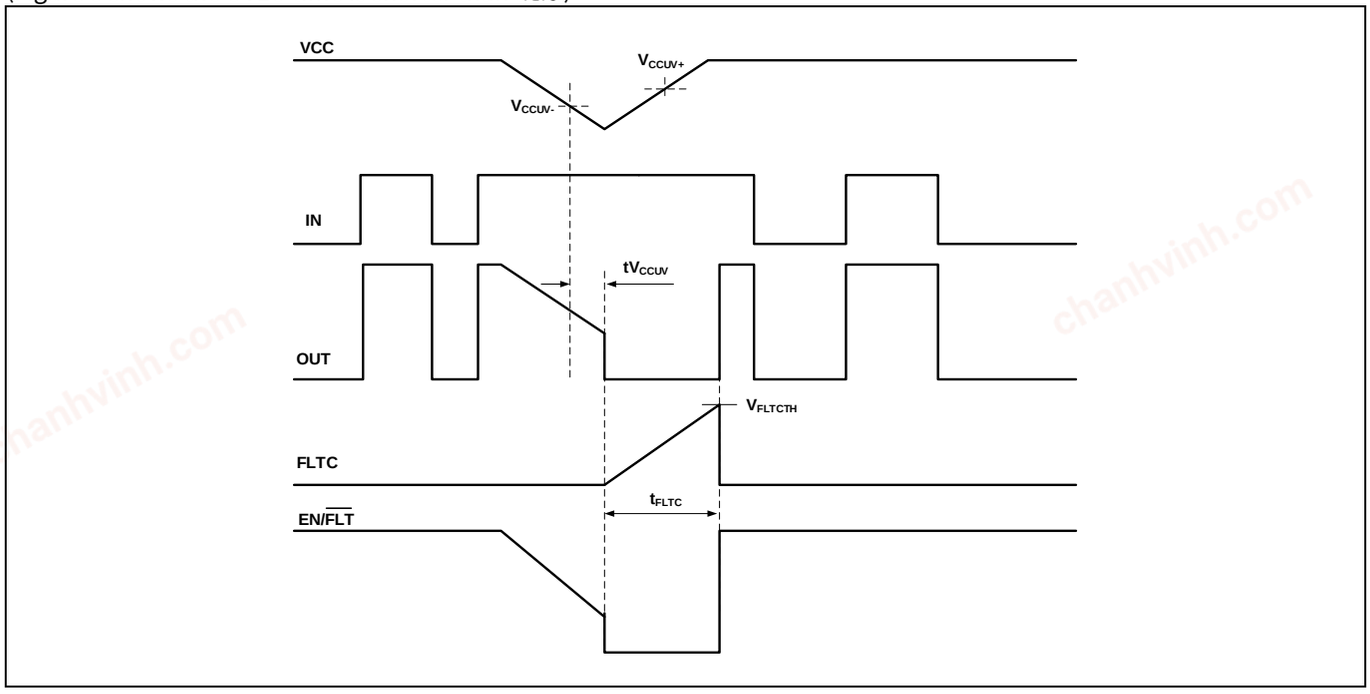

Figure 8 Vcc under voltage protection waveform definitions one

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Application information and additional details

Once EN/$\overline{\text{FLT}}$ enters UVLO mode, EN/$\overline{\text{FLT}}$ keeps low until t_{FLTC} is over and VCC supply voltage higher than V_{CCUV+}. (Figure 9 shows the UVLO time is longer than t_{FLTC}.)

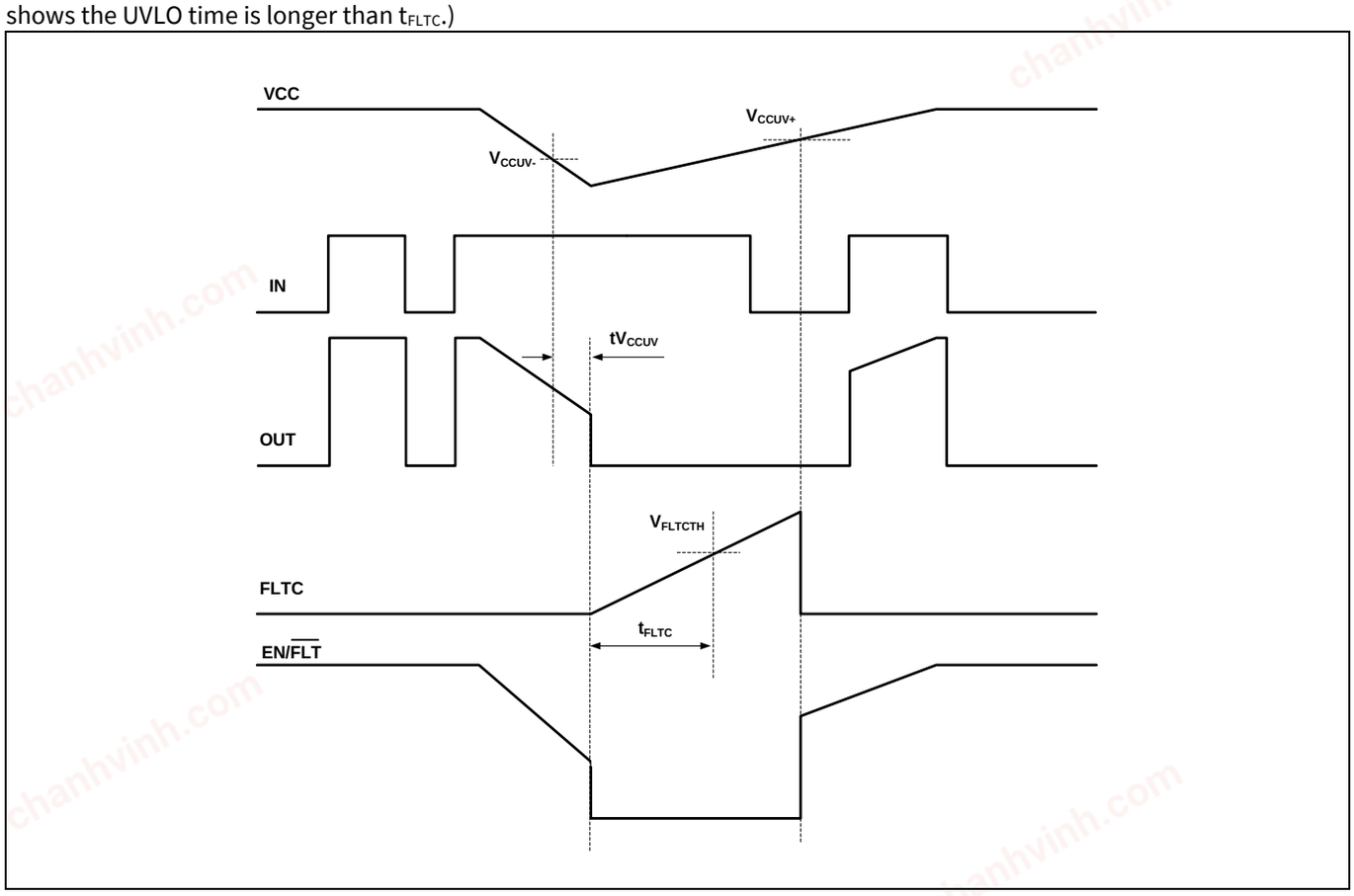

Figure 9 Vcc under voltage protection waveform definitions two

5.5 Over current protection (OCP)

The 1ED44176N01F has a function of over current protection with a threshold V_{OCTH} at the OCP pin. The voltage at this pin is the voltage across the current sense resistor. To avoid false tripping due to the fast high current switch on transient that occurs at the switch on of MOSFET or IGBT resulting from the circuit parasitic capacitors, there is blanking interval which disables over current detection for the period of t_{BLK}. (An additional RC filter is recommended, if the internal t_{BLK} is not sufficient to suppress the noise.) After t_{BLK} and the voltage of OCP pin is over V_{OCTH}, the 1ED44176N01F causes fault logic to initiate a fault shutdown sequence. This sequence starts with the generation of a fault signal. The internal MOSFET Q_{FLT} is turned on and EN/$\overline{\text{FLT}}$ pin is pulled down.
At the same time the 1ED44176N01F terminates the present cycle, and the gate output is immediately pulled down with internal propagation delay (t_{OCPDEL}), see the Figure 10 and Figure 11.

Figure 10 is the diagram of 1ED44176N01F in Boost application. And Figure 11 is the typical waveforms of the application.

If EN/$\overline{\text{FLT}}$ pin enters over current protection mode, EN/$\overline{\text{FLT}}$ pin keeps low until fault clear time is over and OCP terminal voltage lower than over current threshold voltage.

Figure 11 shows the OCP time is shorter than t_{FLTC}. Figure 12 shows the OCP time is longer than t_{FLTC}.

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Application information and additional details

Note: If OCP fault condition is removed and the time is longer than fault clear time (t_{FLTC}), the internal pull down MOSFET Q_{FLT} of $EN/\overline{FLT}$ is released and $EN/\overline{FLT}$ will be pull up again with Vdd, then the OUT will follow the input signal IN.

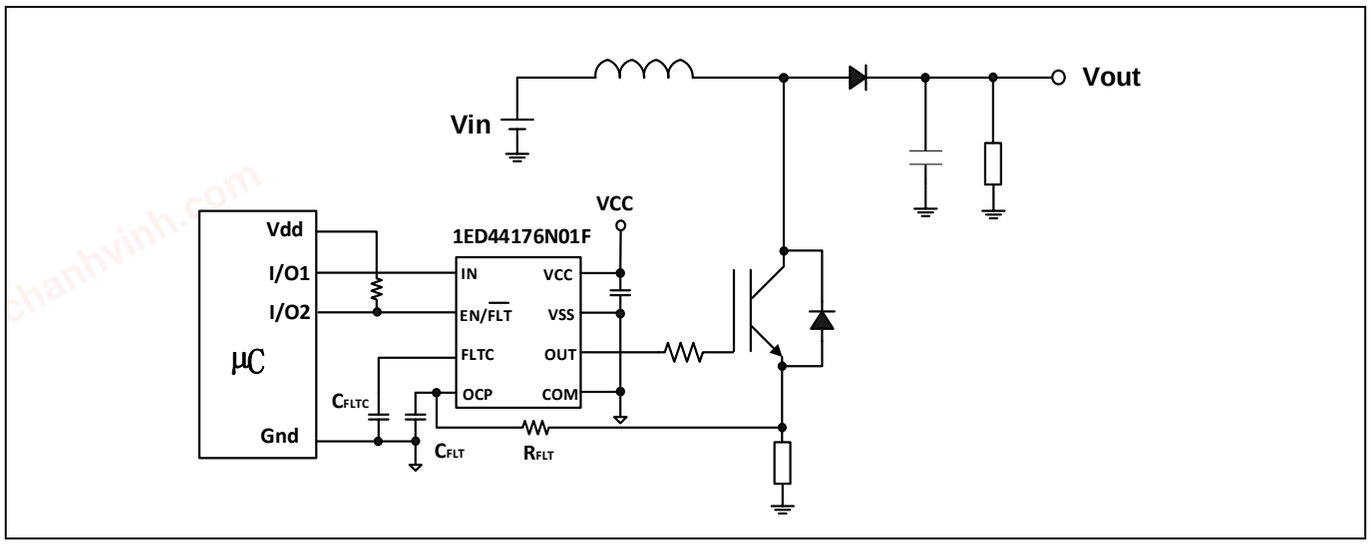

Figure 10 1ED44176N01F in Boost application

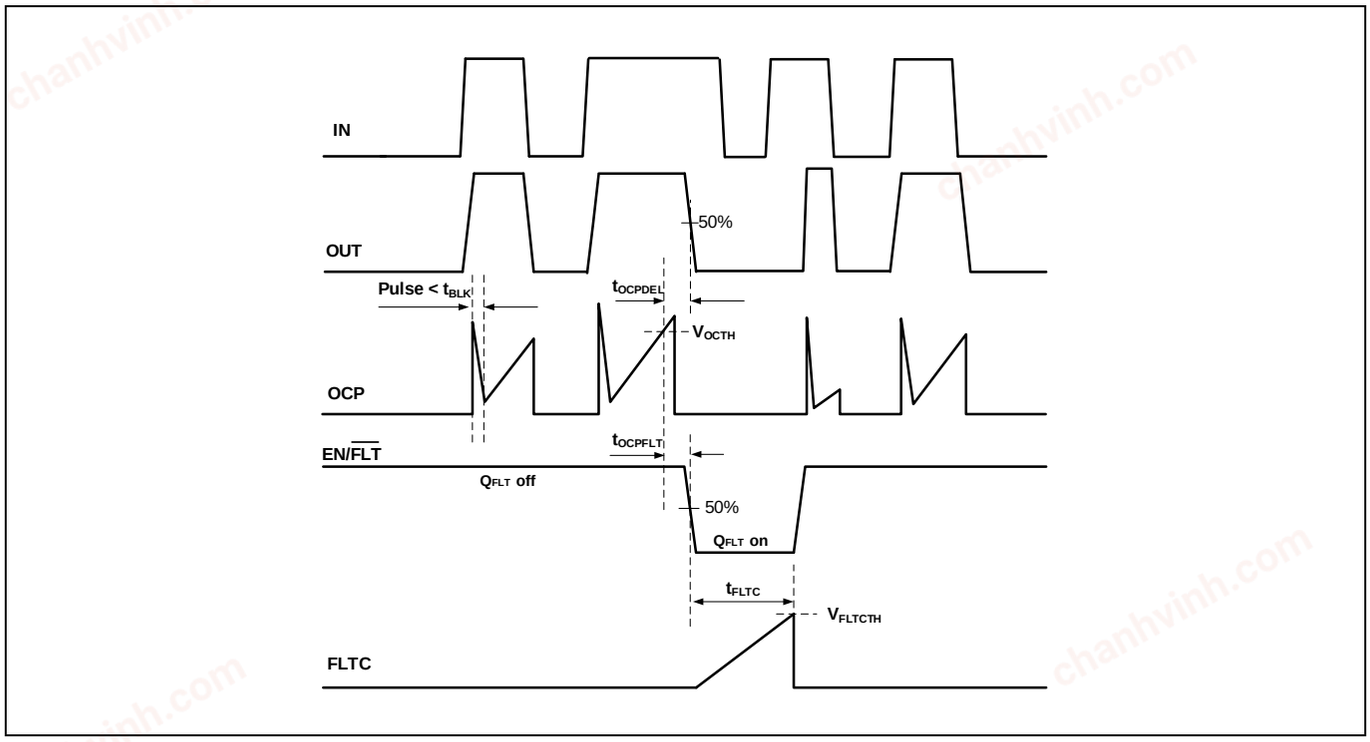

Figure 11 OCP fault detection and fault clear waveforms one

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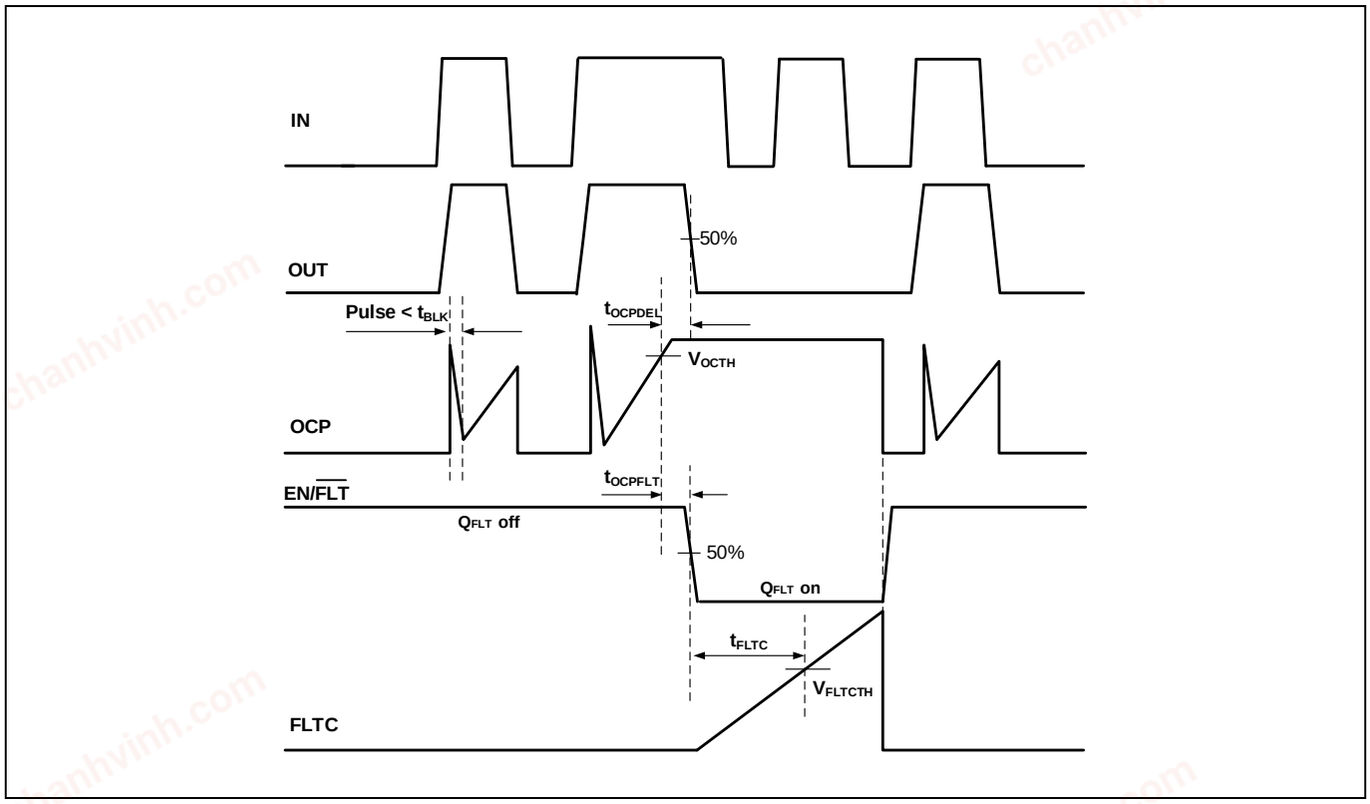

Figure 12 OCP fault detection and fault clear waveforms two

5.6 Fault reporting and programmable fault clear timer

The 1ED44176N01F provides a dedicated fault reporting output pin ($\mathrm{EN}/\overline{\mathrm{FLT}}$) and a programmable fault clear time pin (FLTC). There are two situations which would cause the driver to report a fault via the $\mathrm{EN}/\overline{\mathrm{FLT}}$ pin. The first is an under voltage condition of VCC and the second is if the OCP pin recognizes a fault. Once the fault condition occurs, the $\mathrm{EN}/\overline{\mathrm{FLT}}$ pin is internally pulled down to VSS. The $\mathrm{EN}/\overline{\mathrm{FLT}}$ output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the $\mathrm{EN}/\overline{\mathrm{FLT}}$ pin will return to its external pull-up voltage.

The length of the fault clear time period (t_{FLTC}) is programmed by external capacitor which connected between FLTC and VSS (C_{FLTC}). See Figure 10.

The length of the fault clear time period can be determined by using the equation below.

$$t_{FLTC} = C_{FLTC} * V_{FLTCTH} / I_{FLTC}$$

Note: If the OCP last time is longer than t_{FLTC}, the $\mathrm{EN}/\overline{\mathrm{FLT}}$ output keeps low until the OCP input voltage lower than OCP threshold voltage. See Figure 12.

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5.7 Enable input

1ED44176N01F provides an enable functionality that allows to shutdown or to enable the output. When EN/$\overline{\text{FLT}}$ is pulled up (the enable voltage is higher than V_{ENH}) the output is able to operate normally, pulling EN/$\overline{\text{FLT}}$ low (the enable voltage is lower than V_{ENL}) the output is disable. The enable function is not latched. The relationships between the input, output and enable signals of the 1ED44176N01F are illustrated below in Figure 13 - Figure 15. From these figures, we can see the definitions of several timing parameters and threshold voltages (i.e. t_{DISA}, t_{EN}, V_{ENH} and V_{ENL}) associated with this device.

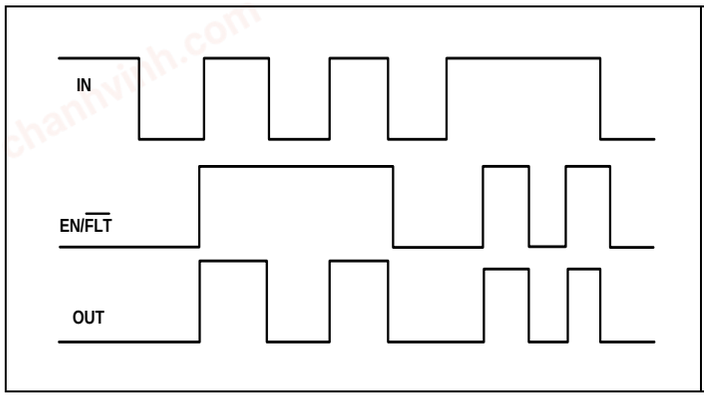

Figure 13 Input/output/enable pins timing diagram

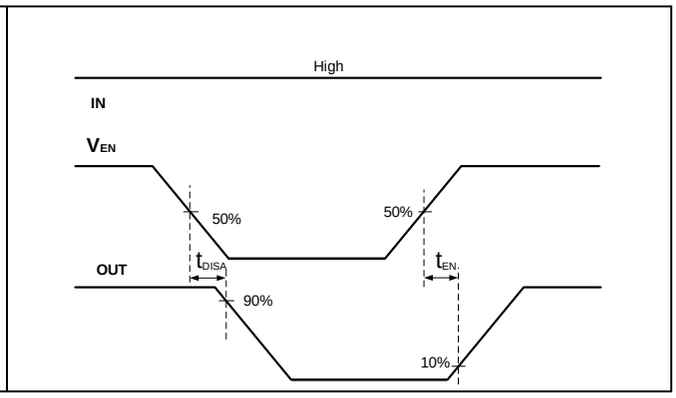

Figure 14 EN pin switching time waveform

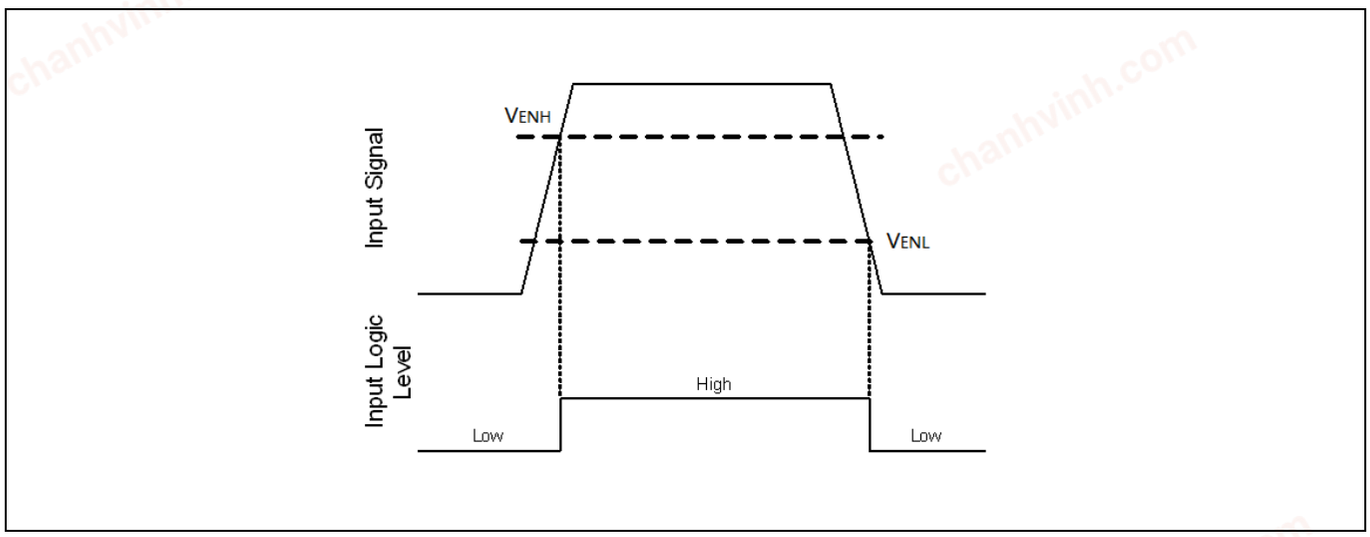

Figure 15 EN input thresholds

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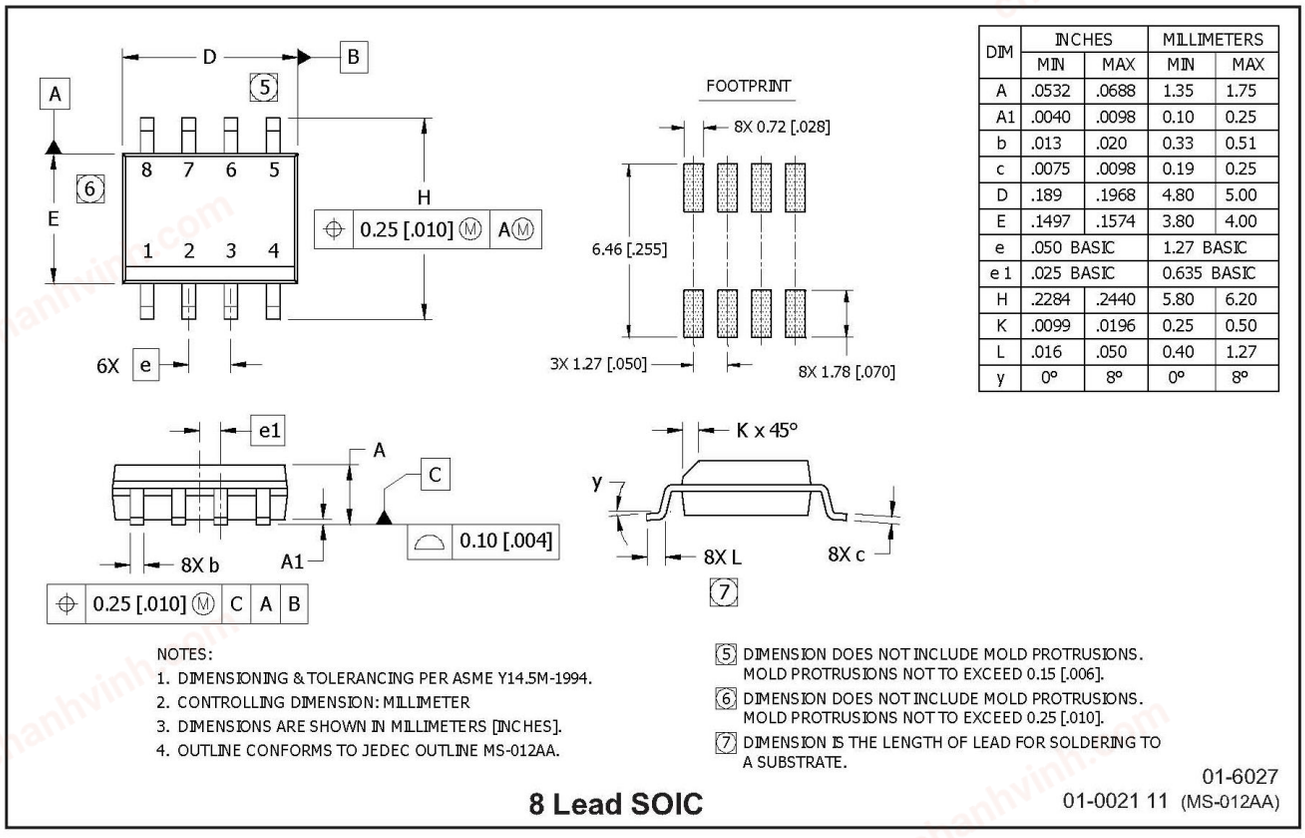
6 Package outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

Figure 16 Package outline

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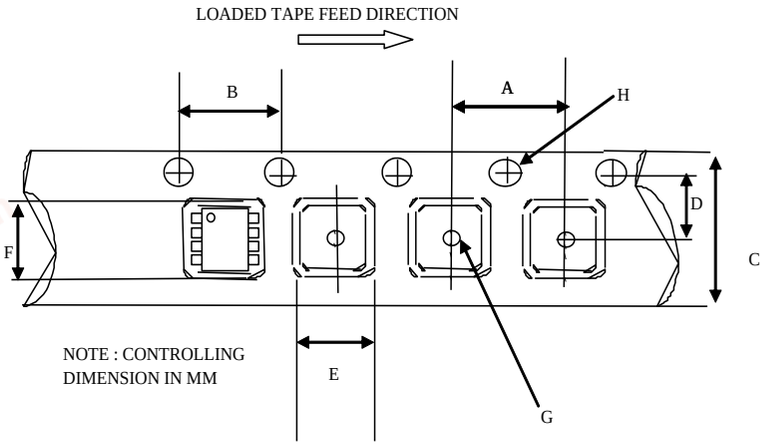
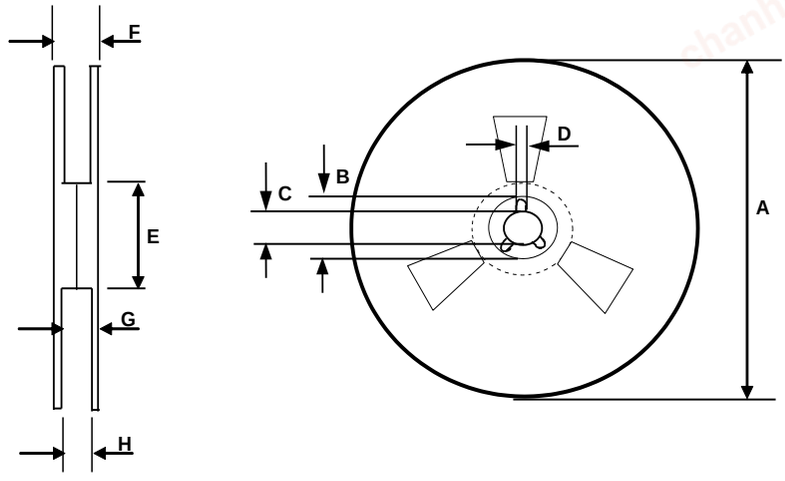
7 Tape and reel details: PG-DSO8



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 17 Tape and reel details

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8 Part marking information

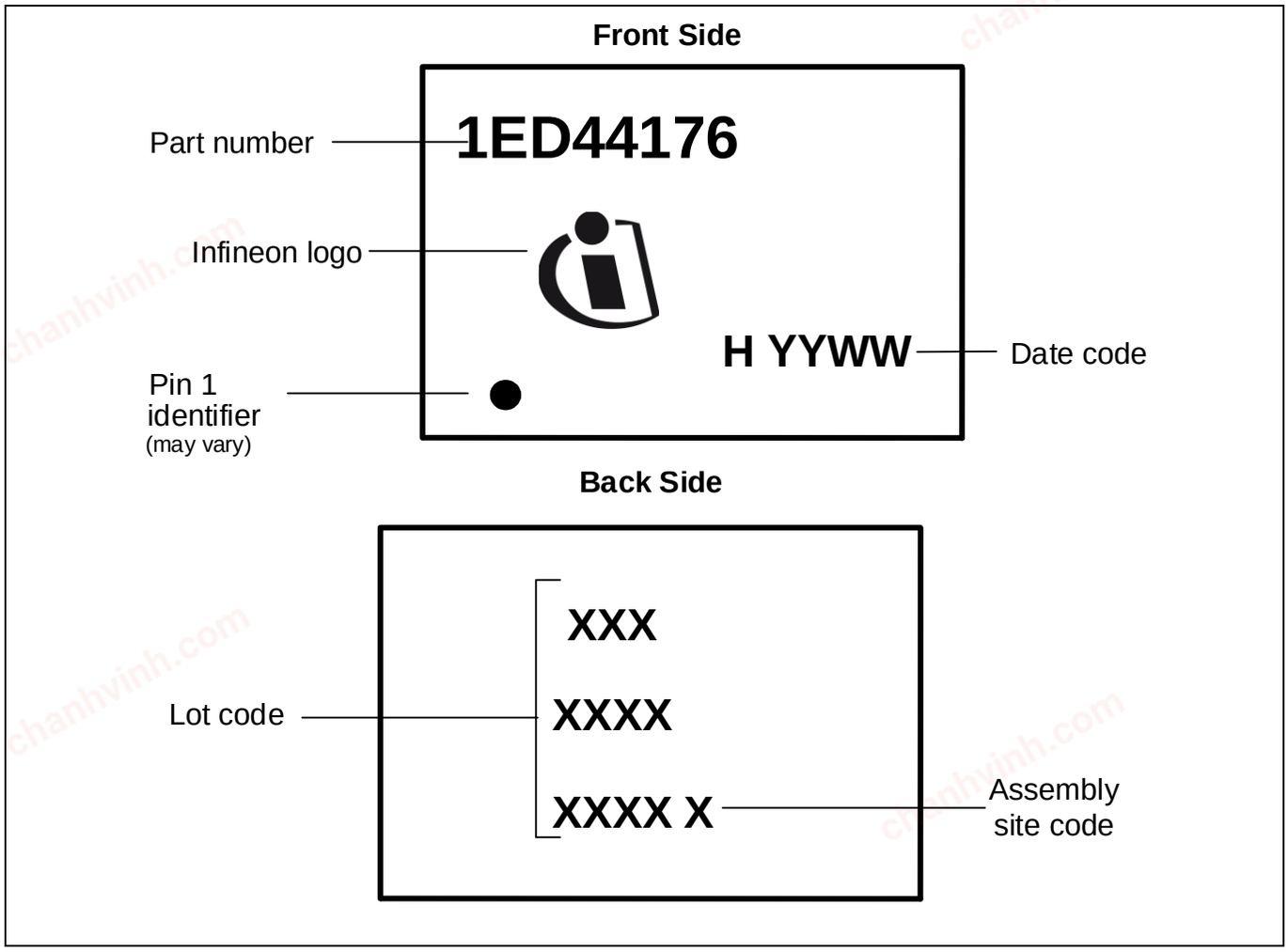

Figure 18 Part marking information

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9 Similar products

Channels	Typ. gate drive (Io+/Io-)	Part number	Max supply voltage	UVLO (on/off)	Typ. prop. delay (on/off)	Logic	Package options
	A		V	V	ns		
1	1.5 / 1.5	IRS44273L	25	10.2 / 9.2	50 / 50	Single non-inverting channel Dual OUT pins	SOT23-5L
	2.6 / 2.6	1ED44173	25	8/7.3	34 / 34	Single negative current sense OCP, fault out and ENABLE	SOT23-6-3
	2.6 / 2.6	1ED44175	25	11.9/11.4	50 / 50	Single negative current sense OCP, fault out and ENABLE	SOT23-6-3
2	2.3 / 3.3	IRS4426S	25		50 / 50	Dual inverting channels	SOIC-8L
		IRS44262S	20	10.2 / 9.2	50 / 50	Dual inverting channels	SOIC-8L
		IRS4427S	25		50 / 50	Dual non-inverting channels	SOIC-8L
		IRS4428S	25		50 / 50	Single inverting channel Single non-inverting channel	SOIC-8L

10 Related documents

1. AN2018-03 Low - Side Driver with Over Current Protection and Fault/Enable
2. AN2018-11 1ED44176N01F evaluation board

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Revision history

Document version	Date of release	Description of changes
2.0	2018-06-27	Create the document V 2.0
2.1	2019-06-13	Optimize parameter in table 6
2.2	2019-10-15	Optimize parameter in table 3
2.3	2020-07-16	Update the truth table, part marking and table of similar products

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