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FT4233HP / FT4232HP

(High Speed USB Bridge with Type-C/PD3.0 Controller)



The FT4233HP/FT4232HP is a Hi-Speed USB device with a Type-C/PD3.0 controller that fully supports the latest USB Type-C and Power Delivery (PD) standards enabling support for power negotiation with the ability to sink or source current to a USB host device. The USB bridge function delivers 4 independent channels compatible with the existing FT4232H – Quad Hi-speed USB to multipurpose UART/MPSSE solution.

The FT4233HP/FT4232HP has the following advanced features:

- Supports the PD specification Rev 3.0.
- Port 1 mode configuration for Sink or Dual-role.
- Port 2 works as Sink, supporting charge through to Port 1(FT4233HPQ and FT4233HPL only).
- Supports 5V3A, 9V3A, 12V3A, 15V3A and 20V3A PDOs as sink or source.
- Type-C/PD Physical Layer Protocol.
- PD policy engine using 32-bit RISC controller with 8kB data RAM and 48kB code ROM.
- PD mode configuration through external EEPROM.
- Options to use external MCU controlling PD policy through I2C interface.
- USB to quad serial ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- USB 2.0 High Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Two Multi-Protocol Synchronous Serial Engine (MPSSE) on channel A and channel B, to simplify synchronous serial protocol (USB to JTAG, I^2C, SPI or bit-bang) design.
- Independent Baud rate generators.
- RS232/RS422/RS485 UART Transfer Data Rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Optional traffic TX/RX indicators can be added with LEDs and an external 74HC595 shift register.
- Adjustable receive buffer timeout.
- Support for USB suspend and resume conditions via PWREN#, SUSPEND# and RI# pins.
- FTDI FT232R/FT-X style, asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Enable control for RS485 serial applications using TXDEN pin through external EEPROM.
- Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface.
- Low operating and USB suspend current.
- Configurable I/O drive strength (4, 8, 12 or 16mA) and slew rate.
- USB Bulk data transfer mode (512 byte packets in High Speed mode).
- Dedicated Windows/Linux DLLs available for USB to SPI, and USB to I^2C applications.
- +3.3V single supply operating voltage range.
- +3.3V I/O interfacing.
- Highly integrated design includes +1.2V LDO regulator for VCORE, integrated POR function and on chip clock multiplier PLL (12MHz – 480MHz).
- Extended -40°C to 85°C industrial operating temperature range.
- Available in Pb-free QFN-76/QFN-68/LQFP-80 package (RoHS compliant).

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1 Typical Applications

- USB Bridge with Type-C/PD3.0 (chargers and devices).
- Up to 60W power delivery via USB PD and/or Type-C port.
- Get power from USB device functions, e.g. portable USB host needs charging when USB is connected.
- Single chip USB to four channels UART (RS232, RS422 or RS485) or Bit-Bang interfaces.
- Single chip USB to 2 JTAG channels plus 2 UARTS.
- Single chip USB to 1 JTAG channel plus 3 UARTS.
- Single chip USB to 1 SPI channel plus 3 UARTS.
- Single chip USB to 2 SPI channels plus 2 UARTS.
- Single chip USB to 2 Bit-Bang channels plus 2 UARTS.
- Single chip USB to 1 SPI channel, plus 1 JTAG channel plus 2 UARTS.
- Single chip USB to 2 I^2C channels plus 2 UARTS.
- Numerous combinations of 4 channels.
- Upgrading Legacy Peripheral Designs to USB.
- Field Upgradable USB Products.
- Cellular and cordless phone USB data transfer cables and interfaces.
- Interfacing MCU / PLD / FPGA based designs to USB.
- PDA to USB data transfer.
- USB Smart Card Readers.
- USB Instrumentation.
- USB Industrial Control.
- USB FLASH Card Reader / Writers.
- Set Top Box PC – USB interface.
- USB Digital Camera Interface.
- USB Bar Code Readers.

1.1 Driver Support

The FT4233HP/FT4232HP requires USB drivers (listed below), available free from https://www.ftdichip.com, which are used to make the FT4233HP/FT4232HP appear as a virtual COM port (VCP). This allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT4233HP/FT4232HP through a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Mac OS-X
- Linux 2.4 and greater

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Mac OS-X
- Linux 2.4 and greater
- Android(J2xx)
-

For driver installation, please refer to the installation guides on our website:
https://ftdichip.com/document/installation-guides/

The following additional installation guides application notes and technical notes are also available:

- AN_113 - Interfacing FT2232H Hi-Speed Devices To I2C Bus
- AN_114 - Interfacing FT2232H Hi-Speed Devices To SPI Bus
- AN_177 - User Guide For libMPSSE – I2C
- AN_110 - Programmers Guide for High Speed FTCJTAG DLL
- AN_178 - User Guide For libMPSSE - SPI
- AN_135 - MPSSE Basics

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- AN_108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes
- AN_411 - FTx232H MPSSE I2C Master Example in C#
- TN_104 - Guide to Debugging Customers Failed Driver Installation
- AN_448 - FT4233HP_FT2233HP_FT233HP_Configuration_Guide
- AN_551 - FT4232HP_FT2232HP_FT232HP_Configuration_Guide

1.2 Part Numbers

Part Number	Package	Packing
FT4232HPQ-TRAY	QFN 68	260 pieces per tray
FT4232HPQ-REEL	QFN 68	3,000 pieces per reel
FT4233HPQ-TRAY	QFN 76	260 pieces per tray
FT4233HPQ-REEL	QFN 76	3,000 pieces per reel
FT4233HPL-TRAY	LQFP 80	Not yet available
FT4233HPL-REEL	LQFP 80	Not yet available

Please refer to Section 6 for all the package mechanical parameters.

1.3 USB Compliant

The FT4233HP/FT4232HP is fully compliant with the USB 2.0 specification and the USB PD 3.0 specification.

It has been given the USB-IF Test-ID 4484*.

* For PD port1

The timing of the rise/fall time of the USB signals is not only dependent on the USB signal drivers, but also on system and is affected by factors such as PCB layout, external components and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. Timing can be changed by adding appropriate passive components to the USB signals.



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2 FT4233HP Block Diagram

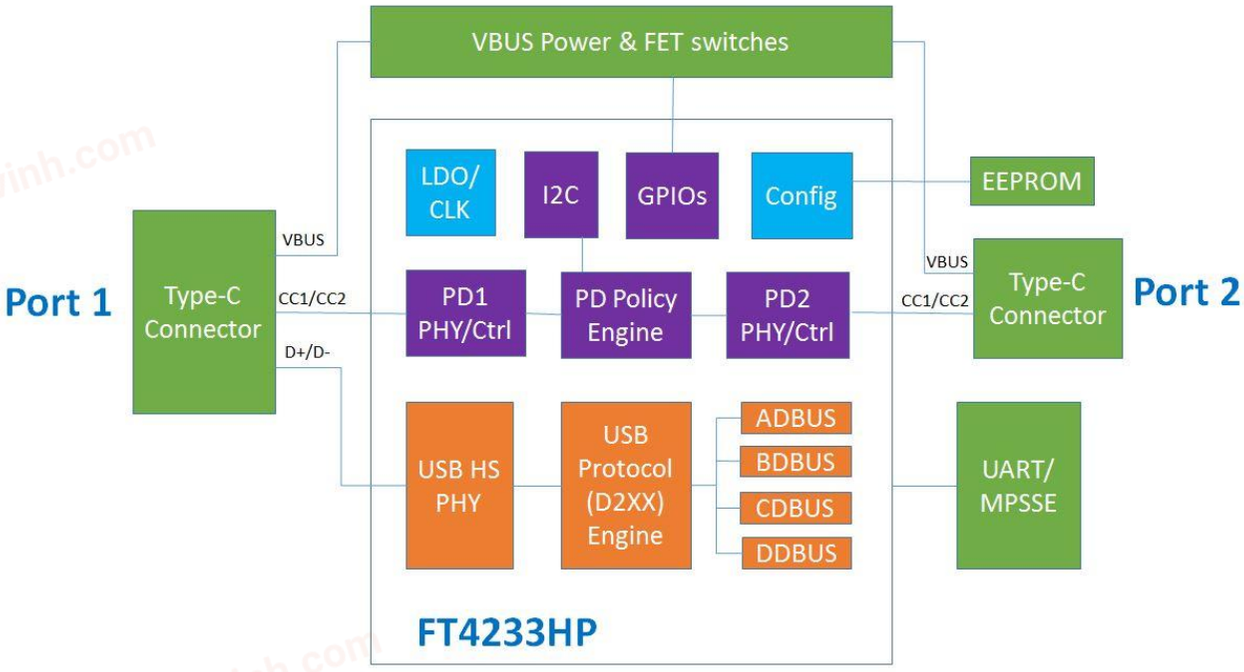


Figure 1 - FT4233HP Block Diagram

For a description of each function please refer to Section 4.

Note: FT4232HP does not include Port 2.

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3 Device Pin Out and Signal Description

3.1 QFN–76 Package Pin Out

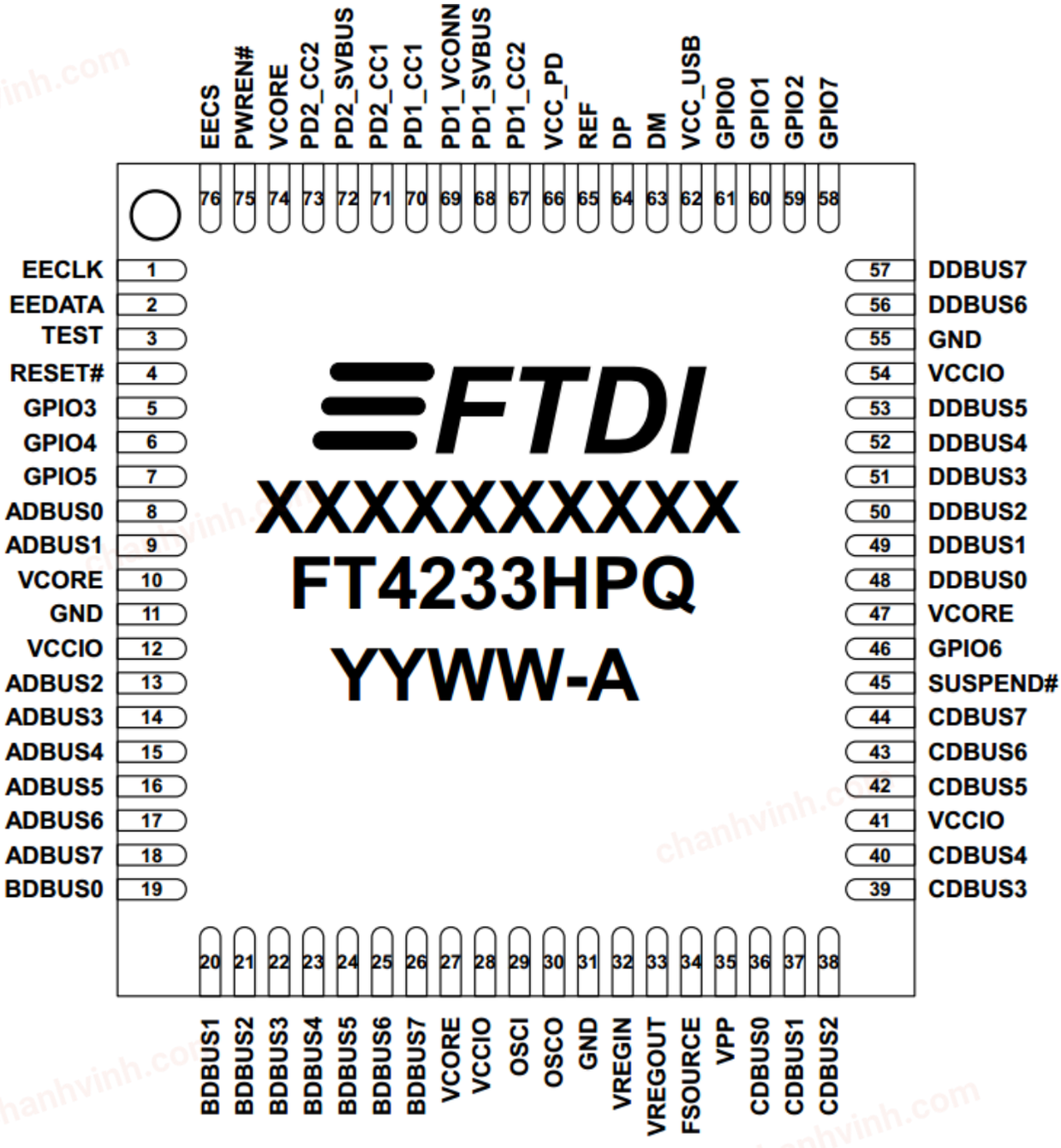


Figure 2 - QFN–76 Package Pin Out

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3.2 QFN–68 Package Pin Out

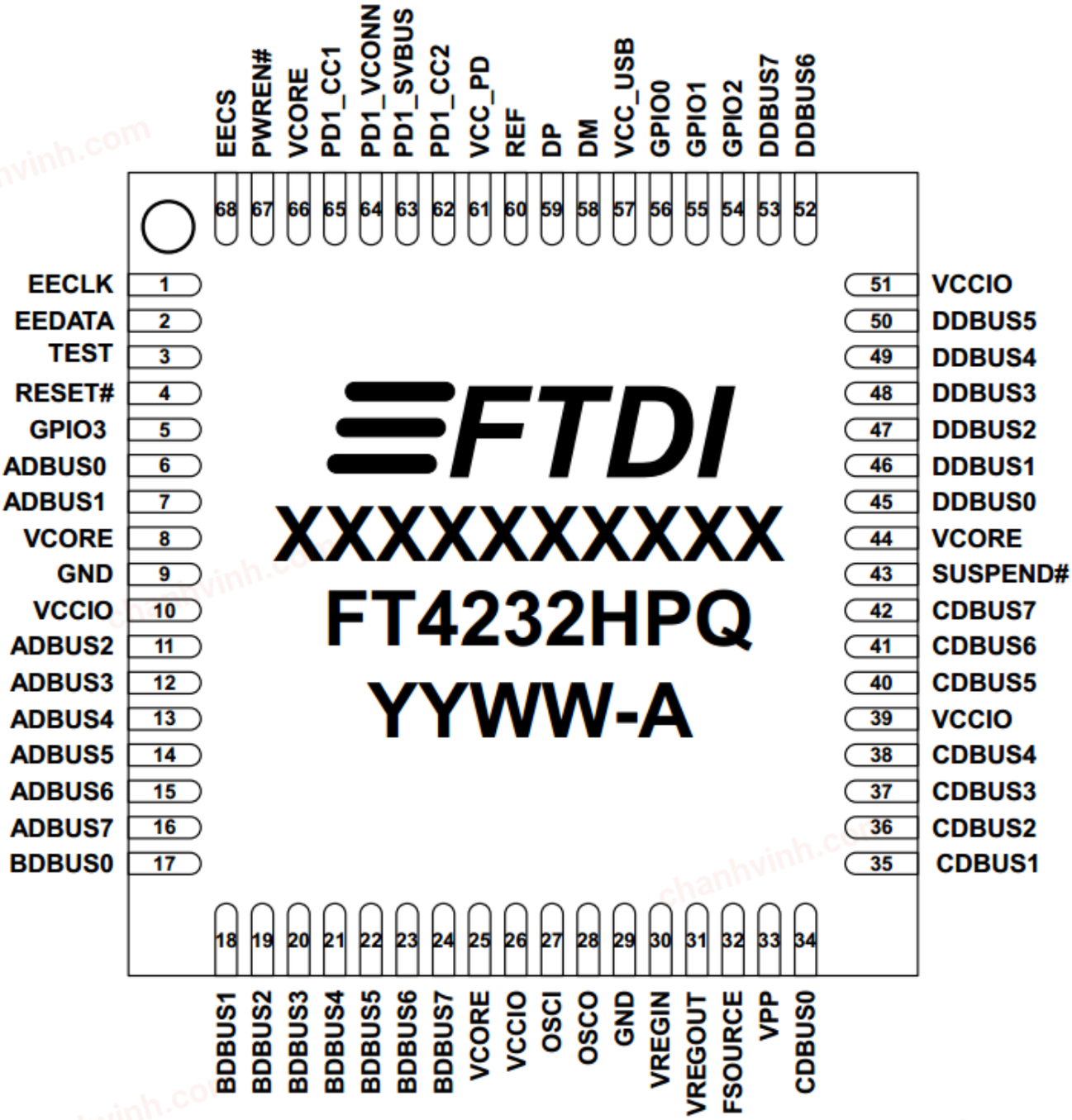


Figure 3 - QFN–68 Package Pin Out

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3.3 LQFP–80 Package Pin Out

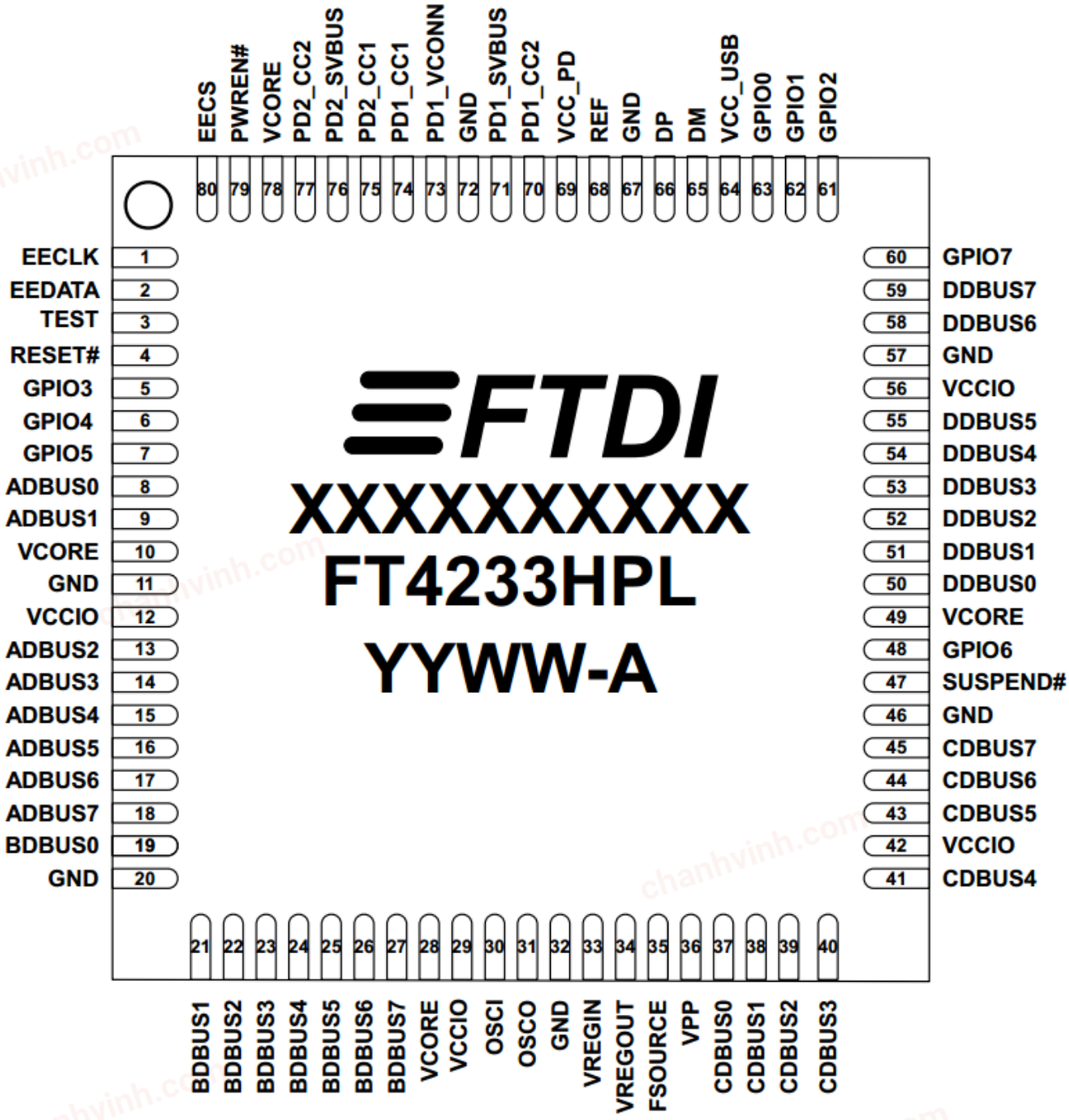


Figure 4 - LQFP–80 Package Pin Out

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3.4 Pin Description

This section describes the operation of the FT4233HP/FT4232HP pins. The function of many pins is determined by the configuration of the FT4233HP/FT4232HP. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions is described in **Table 1**.

Note: The convention used throughout this document for active low signals is the signal name followed by #

FT4233HP/FT4232HP							
Pins				Pin functions (depend on configuration)			
QFN -68	QFN-76	LQFP -80	Pin Name	ASYNC Serial UART (RS232/422/485)	ASYNC Bit-bang	SYNC Bit-bang	MPSSE
Channel A							
6	8	8	ADBUS0	TXD	D0	D0	TCK/SK
7	9	9	ADBUS1	RXD	D1	D1	TDI/DO
11	13	13	ADBUS2	RTS#	D2	D2	TDO/DI
12	14	14	ADBUS3	CTS#	D3	D3	TMS/CS
13	15	15	ADBUS4	DTR#	D4	D4	GPIOL0
14	16	16	ADBUS5	DSR#	D5	D5	GPIOL1
15	17	17	ADBUS6	DCD#	D6	D6	GPIOL2
16	18	18	ADBUS7	RI#/ TXDEN*	D7	D7	GPIOL3
Channel B							
17	19	19	BDBUS0	TXD	D0	D0	TCK/SK
18	20	21	BDBUS1	RXD	D1	D1	TDI/DO
19	21	22	BDBUS2	RTS#	D2	D2	TDO/DI
20	22	23	BDBUS3	CTS#	D3	D3	TMS/CS
21	23	24	BDBUS4	DTR#	D4	D4	GPIOL0
22	24	25	BDBUS5	DSR#	D5	D5	GPIOL1
23	25	26	BDBUS6	DCD#	D6	D6	GPIOL2
24	26	27	BDBUS7	RI#/ TXDEN*	D7	D7	GPIOL3
Channel C							
34	36	37	CDBUS0	TXD	D0	D0	UART (RS232/422/485) or Bit-Bang interface
35	37	38	CDBUS1	RXD	D1	D1	UART (RS232/422/485) or Bit-Bang interface
36	38	39	CDBUS2	RTS#	D2	D2	UART (RS232/422/485) or Bit-Bang interface
37	39	40	CDBUS3	CTS#	D3	D3	UART (RS232/422/485) or Bit-Bang interface
38	40	41	CDBUS4	DTR#	D4	D4	UART (RS232/422/485) or Bit-Bang interface
40	42	43	CDBUS5	DSR#	D5	D5	UART (RS232/422/485) or Bit-Bang interface
41	43	44	CDBUS6	DCD#	D6	D6	UART (RS232/422/485) or Bit-Bang interface
42	44	45	CDBUS7	RI#/ TXDEN*	D7	D7	UART (RS232/422/485) or Bit-Bang interface
Channel D							
45	48	50	DDBUS0	TXD	D0	D0	UART (RS232/422/485) or Bit-Bang interface
46	49	51	DDBUS1	RXD	D1	D1	UART (RS232/422/485) or Bit-Bang interface
47	50	52	DDBUS2	RTS#	D2	D2	UART (RS232/422/485)

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							or Bit-Bang interface
48	51	53	DDBUS3	CTS#	D3	D3	UART (RS232/422/485) or Bit-Bang interface
49	52	54	DDBUS4	DTR#	D4	D4	UART (RS232/422/485) or Bit-Bang interface
50	53	55	DDBUS5	DSR#	D5	D5	UART (RS232/422/485) or Bit-Bang interface
51	56	58	DDBUS6	DCD#	D6	D6	UART (RS232/422/485) or Bit-Bang interface
52	57	59	DDBUS7	RI#/ TXDEN*	D7	D7	UART (RS232/422/485) or Bit-Bang interface

Table 1 - FT4233HP/FT4232HP Pin Description

***** RI#/ or TXDEN is selectable in the EEPROM. Default is RI#.

Note: Initial Pin States - The device will always start up as four UART ports. Therefore pins which are output in UART mode will be driving out. If an application uses MPSSE or bit-bang, ensure that any external signals do not drive into these pins and cause contention until the application has configured the mode and direction of these lines.

3.5 Common Pins

The operation of the following FT4233HP/FT4232HP pins are the same regardless of the configured mode:-

FT4233HP/FT4232HP					
QFN-68	**QFN-76**	**LQFP-80**	**Name**	**Type**	**Description**
8,25, 44,66	10,27, 47, 74	10, 28, 49 78	VCORE	POWER Input	+1.2V input. Core supply voltage input. Connect to VREGOUT when using internal regulator.
10, 26, 39, 51	12,28, 41, 54	12, 29, 42, 56	VCCIO	POWER Input	+3.3V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.
57	62	64	VCC_USB	POWER Input	+3.3V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter.
61	66	69	VCC_PD	POWER Input	+3.3V Input. Internal PD PHY power supply input.
30	32	33	VREGIN	POWER Input	+3.3V Input. Integrated 1.2V voltage regulator input.
31	33	34	VREGOUT	POWER Output	+1.2V Output. Integrated voltage regulator output. Connect to VCORE with 3.3uF filter capacitor. This output should not be used to power other circuits apart from VCORE.
32	34	35	FSOURCE	POWER Input	FSOURCE input pin for EFUSE. Leave floating for normal operation
33	35	36	VPP	POWER Input	VPP input pin for EFUSE. Leave floating for normal operation
9, 29	11, 31, 55	11,20,32,46,57, 67, 72	GND	POWER Input	Ground.

Table 2 - FT4233HP/FT4232HP Power and Ground Pins

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FT4233HP/FT4232HP					
QFN-68	**QFN-76**	**LQFP-80**	**Name**	**Type**	**Description**
27	29	30	OSCI	INPUT	Oscillator input.
28	30	31	OSCO	OUTPUT	Oscillator output.
60	65	68	REF	INPUT	Current reference – connect via a 12K Ohm resistor @ 1% to GND.
58	63	65	DM	I/O	USB Data Signal Minus.
59	64	66	DP	I/O	USB Data Signal Plus.
3	3	3	TEST	INPUT	IC test pin – for normal operation should be connected to GND.
4	4	4	RESET#	INPUT	Reset input (active low).
67	75	79	PWREN#	OUTPUT	Active low power-enable output. PWREN# = 0: Normal operation. PWREN# = 1: USB SUSPEND mode or device has not been configured. This can be used by external circuitry to power down logic when device is in USB suspend or has not been configured.
43	45	47	SUSPEND#	OUTPUT	Active low when USB is in suspend mode.

Table 3 - Common Function Pins

FT4233HP/FT4232HP					
QFN-68	**QFN-76**	**LQFP-80**	**Name**	**Type**	**Description**
68	76	80	EECS*	I/O	EEPROM – Chip Select. Tri-State during device reset.
1	1	1	EECLK*	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
2	2	2	EEDATA*	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset.

Table 4 - EEPROM Interface Pins

* If no EEPROM, pull each of these pins via separate 10K resistor to VCCIO.

FT4233HP/FT4232HP					
QFN-68	**QFN-76**	**LQFP-80**	**Name**	**Type**	**Description**
63	68	71	PD1_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD1. VBUS is required to be divided by 10 before input to this pin.
64	69	73	PD1_VCONN	Power Input	Power input for PD1 VCONN power source. Connect to 3.3V.
65	70	74	PD1_CC1	AI/O	Analog IO pin. PD1 CC1 pin
62	67	70	PD1_CC2	AI/O	Analog IO pin. PD1 CC2 pin
-	72	72	PD2_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD2. VBUS is required to be divided by 10 before input to this pin.
-	71	75	PD2_CC1	AI/O	Analog IO pin. PD2 CC1 pin
-	73	77	PD2_CC2	AI/O	Analog IO pin. PD2 CC2 pin

Table 5 - Type-C/PD Port Pins

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FT4233HP / FT4232HP					
QFN-68	**QFN-76**	**LQFP-80**	**Name**	**Type**	**Description**
56	61	63	GPIO0	I/O	GPIO0 or I2C_SDA pin. Default function is GPIO0 input with weak pull-down.
55	60	62	GPIO1	I/O	GPIO1 or I2C_SCL pin. Default function is GPIO1 input with weak pull-down.
54	59	61	GPIO2	I/O	GPIO2 or I2C_INT# pin. Default function is GPIO2 input with weak pull-down.
5	5	5	GPIO3	I/O	GPIO3 pin. Default function is GPIO3 input with weak pull-down.
-	6	6	GPIO4	I/O	GPIO4 pin. Default function is GPIO4 input with weak pull-down.
-	7	7	GPIO5	I/O	GPIO5 pin. Default function is GPIO5 input with weak pull-down.
-	46	48	GPIO6	I/O	GPIO6 pin. Default function is GPIO6 input with weak pull-down.
-	58	60	GPIO7	I/O	GPIO7 pin. Default function is GPIO7 input with weak pull-down.

Table 6 - GPIO Pins

3.6 Configured Pins

The following sections describe the function of the configurable pins referred to in **Table 1**. This is determined by how the FT4233HP/FT4232HP is configured.

3.6.1 Pins used as an Asynchronous Serial Interface

Any of the 4 channels of the FT4233HP/FT4232HP can be configured as an asynchronous serial UART interface (RS232/422/485). When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 7**.

FT4233HP/FT4232HP														
Channel A Pin No.			Channel B Pin No.			Channel C Pin No.			Channel D Pin No.			**Name**	**Type**	**ASYNC Serial UART (RS232/422/485) Configuration Description**
QFN-68	**QFN-76**	**LQFP-80**	**QFN-68**	**QFN-76**	**LQFP-80**	**QFN-68**	**QFN-76**	**LQFP-80**	**QFN-68**	**QFN-76**	**LQFP-80**			
6	8	8	17	19	19	34	36	37	45	48	50	TXD	OUTPUT	TXD = transmitter output
7	9	9	18	20	21	35	37	38	46	49	51	RXD	INPUT	RXD = receiver input
11	13	13	19	21	22	36	38	39	47	50	52	RTS#	OUTPUT	RTS# = Ready To send handshake output
12	14	14	20	22	23	37	39	40	48	51	53	CTS#	INPUT	CTS# = Clear To Send handshake input
13	15	15	21	23	24	38	40	41	49	52	54	DTR#	OUTPUT	DTR# = Data Transmit Ready modem signaling line
14	16	16	22	24	25	40	42	43	50	53	55	DSR#	INPUT	DSR# = Data Set Ready modem signaling line
15	17	17	23	25	26	41	43	44	51	56	58	DCD#	INPUT	DCD# = Data Carrier Detect modem signaling line
16	18	18	24	26	27	42	44	45	52	57	59	RI#/TXDEN	INPUT/OUTPUT	RI# = Ring Indicator Control Input. When the Remote Wake-Up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (see note 1, 2 and 3) TXDEN = TRANSMIT ENABLE (TTL level). For use with RS485 level converters.

Table 7 - Channel A, B, C & D Asynchronous Serial Interface Configured Pin Descriptions

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Notes

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.
2. If remote wake-up is enabled, a peripheral is allowed to draw up to 2.5mA in suspend. If remote wake-up is disabled, the peripheral must draw no more than 500uA in suspend.
3. If a Pull-down is enabled, the FT4233HP/FT4232HP will not wake up from suspend.

3.6.2 Pins used in a Synchronous or Asynchronous Bit-Bang Interface

The FT4233HP/FT4232HP channel A, B, C or channel D can be configured as a bit-bang interface. There are two types of bit-bang modes: **synchronous** and **asynchronous**.

When configured in any bit-bang mode (synchronous or asynchronous), the pins used and the descriptions of the signals are shown in **Table 8**.

FT4233HP/FT4232HP					
QFN-68	**QFN-76**	**LQFP-80**	**Name**	**Type**	**Synchronous s or Asynchronous Bit-Bang Configuration Description**
6,7,11-16	8,9,13-18	8,9,13-18	ADBUS[7:0]	I/O	Channel A, D7 to D0 bidirectional bit-bang data
17-24	19-26	19,21-27	BDBUS[7:0]	I/O	Channel B, D7 to D0 bidirectional bit-bang data
34-38,40-42	36-44	37-41,43-45	CDBUS[7:0]	I/O	Channel C, D7 to D0 bidirectional bit-bang data
45-50, 52,53	48-53,56,57	50-55,58,59	DDBUS[7:0]	I/O	Channel D, D7 to D0 bidirectional bit-bang data

Table 8 - Channel A, B, C & D Synchronous/Asynchronous Bit-Bang Configured Pin Descriptions

For a functional description of this mode, please refer to Section **4.5**.

3.6.3 FT4233HP/FT4232HP pins used in an MPSSE

FT4233HP/FT4232HP channel A and channel B, each have a Multi-Protocol Synchronous Serial Engine (MPSSE). Each MPSSE can be independently configured to a number of industry standard serial interface protocols such as JTAG, I^2C or SPI, or it can be used to implement a proprietary bus protocol. For example, it is possible to use one of the FT4233HP/FT4232HP's channels (e.g. channel A) to connect to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The other MPSSE channel (e.g. channel B) would be available for another serial interface function while channel C and channel D can be configured as UART or bit-bang mode. Alternatively each MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 9**.

FT4233HP/FT4232HP								
Channel A Pin No.			**Channel B Pin No.**			**Name**	**Type**	**MPSSE Configuration Description**
QFN-68	**QFN-76**	**LQFP-80**	**QFN-68**	**QFN-76**	**LQFP-80**			
6	8	8	17	19	19	TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI – SK, Serial Clock
7	9	9	18	20	21	TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI – DO, serial data output
11	13	13	19	21	22	TDO/DI	INPUT	Serial Data Input. For example: JTAG – TDO, Test Data output SPI – DI, Serial Data Input

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12	14	14	20	22	23	TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI – CS, Serial Chip Select
13	15	15	21	23	24	GPIOL0	I/O	General Purpose input/output
14	16	16	22	24	25	GPIOL1	I/O	General Purpose input/output
15	17	17	23	25	26	GPIOL2	I/O	General Purpose input/output
16	18	18	24	26	27	GPIOL3	I/O	General Purpose input/output

Table 9 - Channel A & Channel B MPSSE Configured Pin Descriptions

For a functional description of this mode, please refer to section **4.4**.

When either Channel A or Channel B or both channels are used in MPSSE mode, Channel C and Channel D can be configured as asynchronous serial UART interface (RS232/422/485) or Bit-Bang mode or a combination of both.

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4 Function Description

The FT4233HP/FT4232HP is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC with USB Type-C/PD ports. It has the capability of being configured in a variety of industry standard serial interfaces. The FT4233HP/FT4232HP has four independent configurable interfaces. Two of these interfaces can be configured as UART, bit-bang mode or JTAG, SPI, I^2C mode, using the MPSSE, with independent baud rate generators. The remaining two interfaces can be configured as UART or bit-bang.

The FT4233HP has two Type-C/PD ports, with PD1 port supporting both power sink and source roles, and PD2 port (FT4233HPQ and FT4233HPL only) works as a power sink port. Both PD ports support 5V3A, 9V3A, 12V3A, 15V3A and 20V3A PDO profiles, and these profiles are configurable through the external EEPROM at power-up or reset. PD1 port share the same Type-C connector with USB data, and PD2 port is power port only without USB data.

4.1 Key Features

USB Type-C/PD Controller. FT4233HP/FT4232HP supports USB Type-C specification version 1.3. The FT4233H/ FT4232HP integrated with USB PD 3.0 controller. USB PD port 1 is USB PD 3.0 with the USB 2.0 function. The first USB PD power is initial power sink when local power source is presented, it can become power source via PD negotiation. FT4233HP has a second USB PD sink only port to connect to PD power source. FT4233HP/FT4232HP USB PD 3.0 function is backward compatible to USB PD 2.0 standard.

USB High Speed to Quad Interface. The FT4233HP/FT4232HP is a USB 2.0 High Speed (480Mbits/s) to four independent flexible/configurable serial interfaces. This function is backward compatible to FT4232H.

Functional Integration. The FT4233HP/FT4232HP integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 High Speed interface. The FT4233HP/FT4232HP include an integrated +1.2V Low Drop-Out (LDO) regulator and 12MHz to 480MHz PLL. It also includes 2kbytes Tx and Rx data buffers per channel. The FT4233HP/FT4232HP effectively integrates the entire USB protocol on a chip.

MPSSE. Multi-Purpose Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

Data Transfer Rate. The FT4233HP/FT4232HP support a data transfer rate up to 12 Mbit/s when configured as a UART (RS232/RS422/RS485) interface. Please note the FT4233HP/FT4232HP do not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud. Only limited high speed baud rates are possible down to 6Mbaud, below this rate the divider and sub-integer dividers start to have effect offering a wider range of baud rates.

Latency Timer. This is used as a timeout to flush short packets of data back to the PC. The default is 16ms, but it can be altered between 1ms and 255ms. At 2ms latency you get a packet transfer on every high speed micro frame. Lower values may reduce latency but may also increase USB bandwidth usage and reduce efficiency.

4.2 Functional Block Descriptions

Type-C/PD PHY and Controller. The FT4233HP (FT4233HPQ and FT4233HPL only) has two Type-C/PD ports. Each port has Type-C/PD required Physical Layer (PHY) and controllers. PD1 port has built-in VCONN switches supporting up to 660mW VCONN power.

PD Policy Engine. The PD policy engine is a 32bit RISC processor with 8kB data RAM and 48kB ROM. It manages both PD port 1 and port 2. Default PD configurations are stored in the ROM code. PD1 port can act as power sink or source role, supporting both normal power role swap. PD2 port (FT4233HPQ and FT4233HPL only) acts as power sink, which can be connected to a PD charger. By using an external EEPROM, it is possible to change the PD configuration based on specific use cases, such as Port 1 sink, Port 1 sink/source or PD charge through from Port 2 to Port 1. PDO voltage/current profiles can also be customised using EEPROM.

I2C Slave Interface. The application can also choose to control the PD policy by external MCU through I2C interface. In this case the built-in PD policy engine is halted. The external MCU has full control to the two PD controller registers (FT4233HPQ and FT4233HPL only) through I2C access. An interrupt signal is also provided, so that an interrupt to an external MCU could be asserted when a PD event occurs.

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GPIO block. The GPIO block provides up to 8 GPIO pins which can be used as power switch controls based on the PD policy and profiles.

Quad Multi-Purpose UART/MPSSE Controllers. The FT4233HP/FT4232HP have four independent UART/MPSSE Controllers. These blocks control the UART data or control the Bit-Bang mode if selected by the SETUP command. The blocks used on channel A and channel B also contain a MPSSE (Multi-Protocol Synchronous Serial Engine) in each of them which can be used independently of each other and the remaining UART channels. Using this, the device can be configured under software command to have 1 MPSSE + 3 UARTS (each UART can be set to Bit Bang mode to gain extra I/O if required) or 2 MPSSE + 2 UARTS.

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Dual Port FIFO TX Buffer (2Kbytes per channel). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Dual Port FIFO RX Buffer (2Kbytes per channel). Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT4233HP/FT4232HP. RESET# should be tied to VCCIO (+3.3v) if not being used.

Independent Baud Rate Generators - The Baud Rate Generators provide an x16 or an x10 clock input to the UART's from a 120MHz reference clock and consist of a 14 bit pre-scaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 million baud. The FT4233HP/FT4232HP do not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

Refer to application note AN_120 for more details.

LDO Regulator. The +1.2V LDO regulator generates the +1.2 volts for the core and the USB transceiver cell. Its input (VREGIN) must be connected to a +3.3V external power source. It is also recommended to add an external filtering capacitor to the VREGIN. There is no direct connection from the +1.2V output (VREGOUT) and the internal functions of the FT4233HP/FT4232HP. The PCB must be routed to connect VREGOUT to VCORE. This output should not be used to power other circuits apart from VCORE.

USB HS PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / High Speed SERDES (serialise – de-serialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal should be connected to the OSCI and OSCO pins. A 12K Ohm resistor should be connected between REF and GND on the PCB.

EEPROM Interface. EEPROM is optional. When used without an external EEPROM the FT4233HP/FT4232HP default to a quad USB to an asynchronous serial port device with default profiles on 2 Type-C/PD ports. Adding an external 93LC66 EEPROM allows customization of USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT4233HP/FT4232HP for OEM applications, as well as PD port configurations and power profiles. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM must have a 16 bit wide configuration such as a Microchip 93LC66B or equivalent capable of a 1Mbit/s clock rate at VCC = 3.0V to 3.6V. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site – www.ftdichip.com. This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT4233HP/FT4232HP will default to serial ports. The device uses its built-in default VID (0403), PID (6041), Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor. As for the power delivery configuration, please refer to AN_448 for FT4233HP and AN_551 for FT4232HP.

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4.3 FT232 UART Interface Mode Description

The FT4233HP/FT4232HP can be configured in similar UART modes as the FT232R/FT-X devices (an asynchronous serial interface). The following examples illustrate how to configure the FT4233HP with an RS232, RS422 or RS485 interfaces. The FT4233HP can be configured as a mixture of these interfaces.

4.3.1 RS232 Configuration

Figure 5 illustrates how the FT4233HP channel A can be configured with an RS232 interface. This can be repeated for channels B, C and D to provide a quad RS232, but has been omitted for clarity.

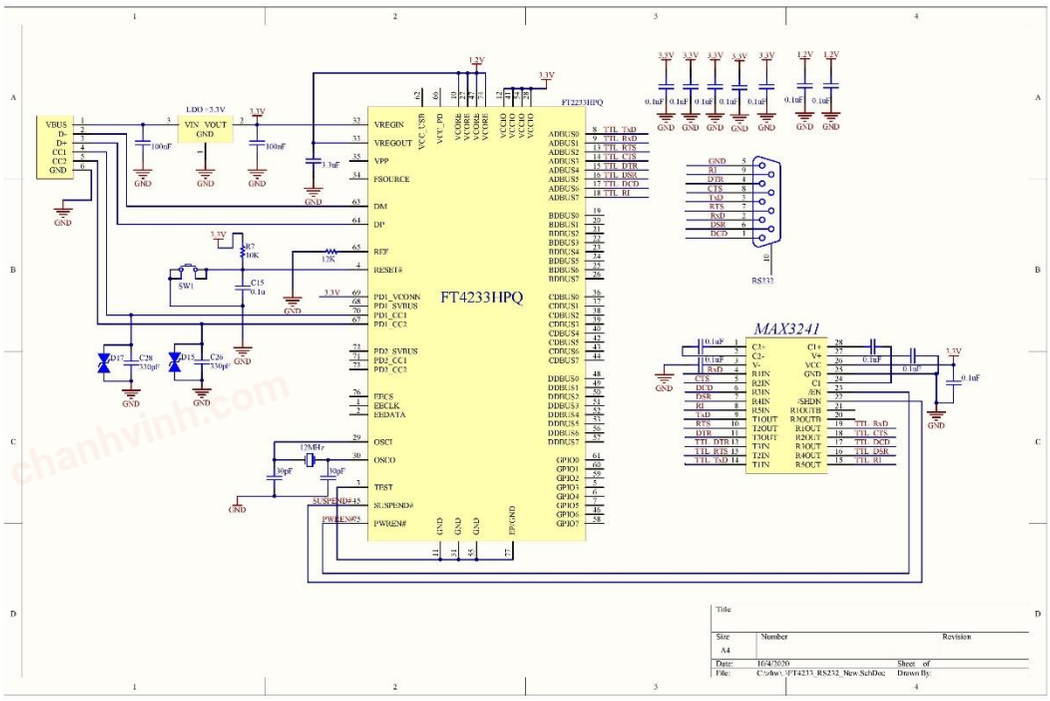


Figure 5 - Single RS232 Configurations

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4.3.2 RS422 Configuration

Figure 6Figure 6 – Dual RS422 Configuration

illustrates how the FT4233HP can be configured as a dual RS422 interface. The FT4233HP can have all 4 channels connected as RS422, but only channel A and channel C are shown for clarity.

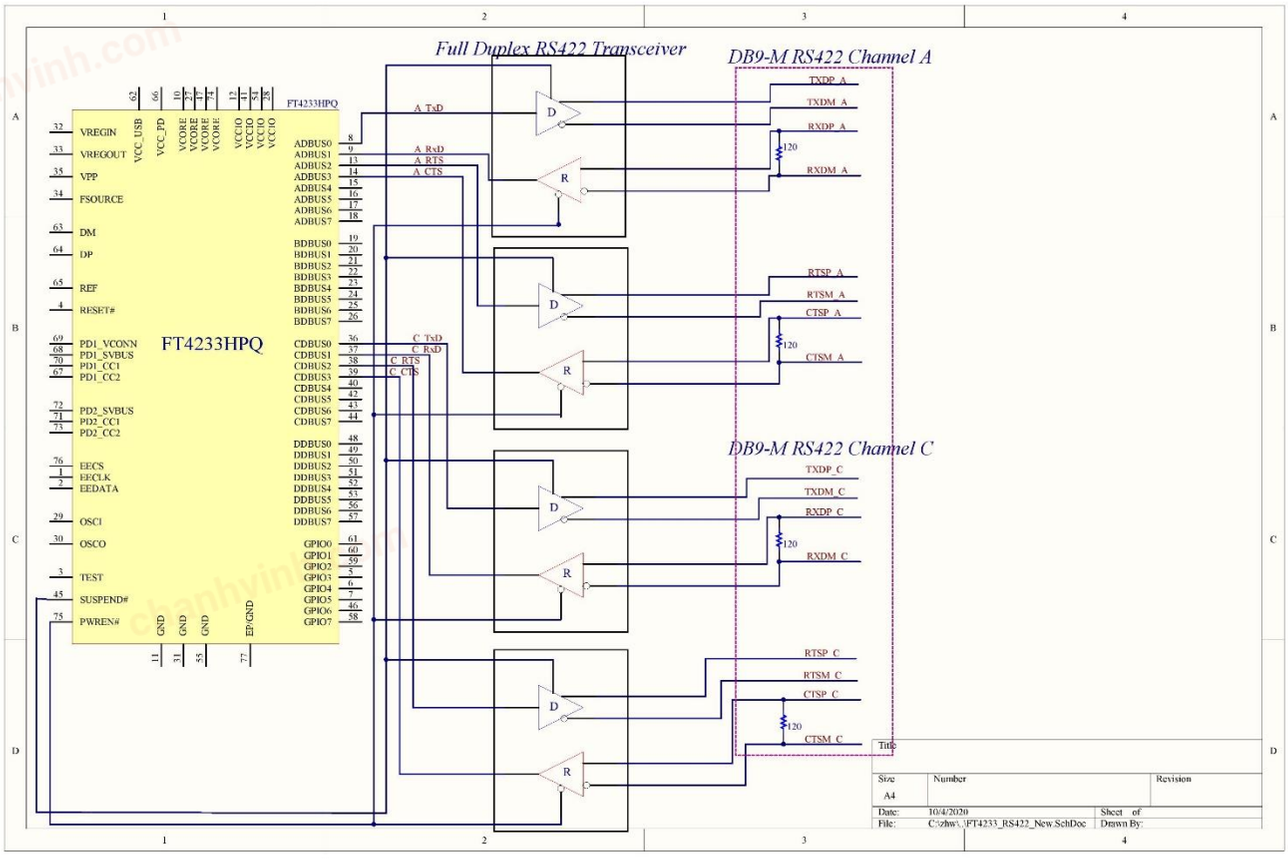


Figure 6 – Dual RS422 Configuration

In this case both channel A and channel C are configured as UART operating at TTL levels and a level converter device (full duplex RS485 transceiver) is used to convert the TTL level signals from the FT4233HP to RS422 levels. The PWREN# signal is used to power down the level shifters such that they operate in a low quiescent current when the USB interface is in suspend mode.

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4.3.3 RS485 Configuration

Figure 7 illustrates how the FT4233HP can be configured as a dual RS485 interface. The FT4233HP can have all 4 channels connected as RS485, but only channel A and channel C are shown for clarity.

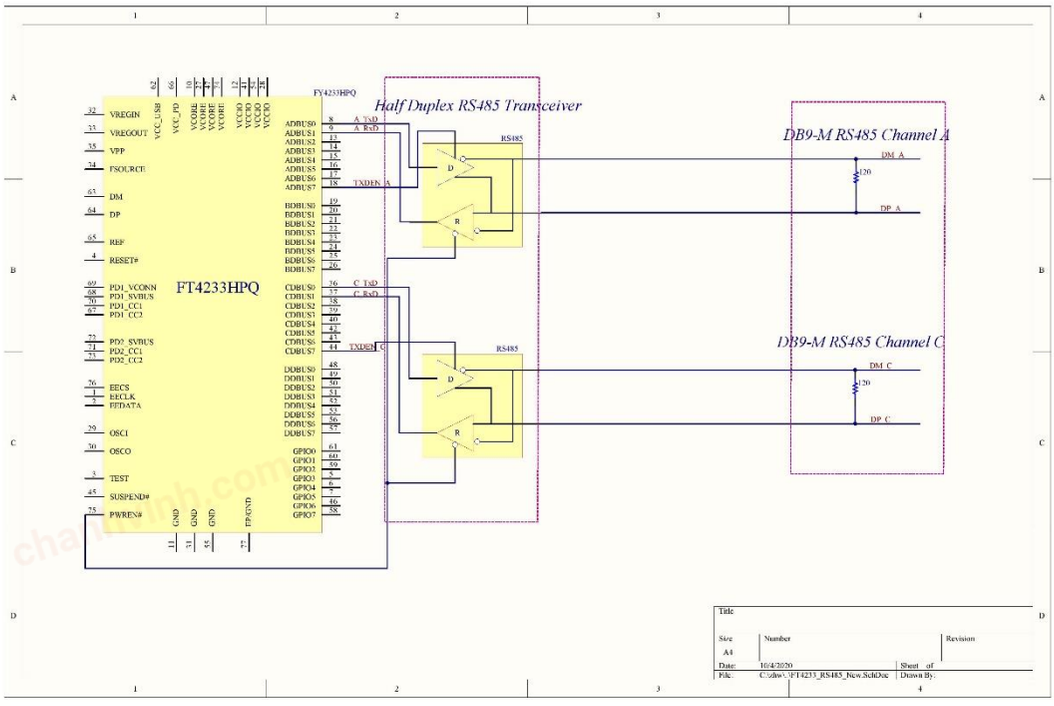


Figure 7 – Dual RS485 Configuration

In this case both channel A and channel C are configured as RS485 operating at TTL levels and a level converter device (half duplex RS485 transceiver) is used to convert the TTL level signals from the FT4233HP to RS485 levels. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pins on the FT4233HP are provided for exactly that purpose, and so the transmitter enables are wired to the TXDEN pins. The TXDEN function is enabled via the external EEPROM. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode.

RS485 is a multi-drop network – i.e. many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable. Links are provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

In this example the data transmitted by the FT4233HP is also received by the device that is transmitting. This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT4233HP it is possible to do this entirely in hardware – simply modify the schematic so that RXD of the FT4233HP is the logical OR of the level converter device receiver output with TXDEN using an HC32 or similar logic gate.

4.4 MPSSE Interface Mode Description

MPSSE Mode is designed to allow the FT4233HP/FT4232HP to interface efficiently with synchronous serial protocols such as JTAG, I2C and SPI Bus. It can also be used to program SRAM based FPGA's over USB. The MPSSE interface is designed to be flexible so that it can be configured to allow any synchronous serial protocol (industry standard or proprietary) to be implemented using the FT4233HP/FT4232HP. MPSSE is only available on channel A and channel B.

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MPSSE is fully configurable, and is programmed by sending commands down the data stream. These can be sent individually or more efficiently in packets. MPSSE is capable of a maximum sustained data rate of 30 Mbits/s.

When a channel is configured in MPSSE mode, the IO timing and signals used are shown in **Figure 8** and **Table 10**. These show timings for CLKOUT=30MHz. CLKOUT can be divided internally to be provide a slower clock.

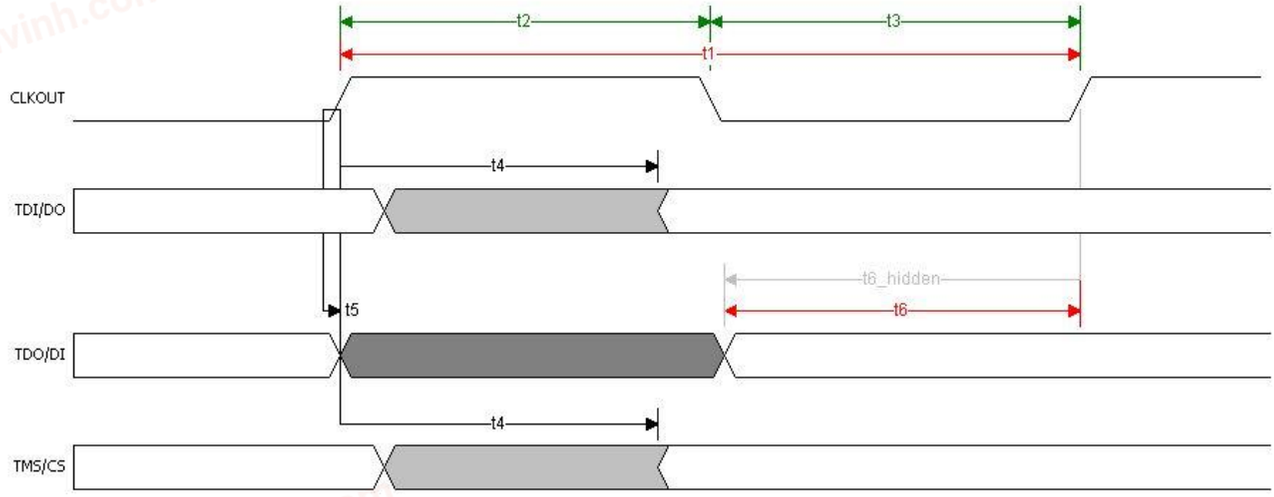


Figure 8 – MPSSE Signal Waveforms

NAME	MIN	NOM	MAX	Units	COMMENT
t1		33.33		ns	CLKOUT period
t2	15	16.67		ns	CLKOUT high period
t3	15	16.67		ns	CLKOUT low period
t4	1		7.15	ns	CLKOUT to TDI/DO delay
t5	0			ns	TDO/DI hold time
t6	11			ns	TDO/DI setup time

Table 10 - MPSSE Signal Timings

MPSSE mode is enabled using Set Bit Bang Mode driver command. A hex value of 2 will enable it, and a hex value of 0 will reset the device. See application note AN2232-02 - Bit Mode Functions for the FT2232 for more details and examples.

The MPSSE command set is fully described in application note AN_108 - Command Processor for MPSSE and MCU Host Bus Emulation Modes.

The application notes in the Document References section are available for configuring the MPSSE.

4.4.1 MPSSE Adaptive Clocking

Adaptive clocking is a new MPSSE feature added to the FT4233HP/FT4232HP MPSSE engine.

The mode is effectively handshaking the CLK signal with a return clock RTCK. This is a technique used by ARM processors.

The FT4233HP/FT4232HP will assert the CLK line and wait for the RTCK to be returned from the target device to GPIOL3 line before changing the TDO (data out line).

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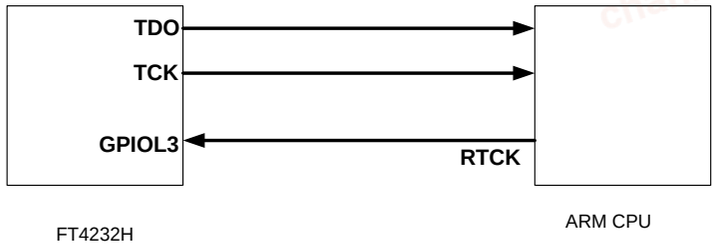


Figure 9 – Adaptive Clocking Interconnect

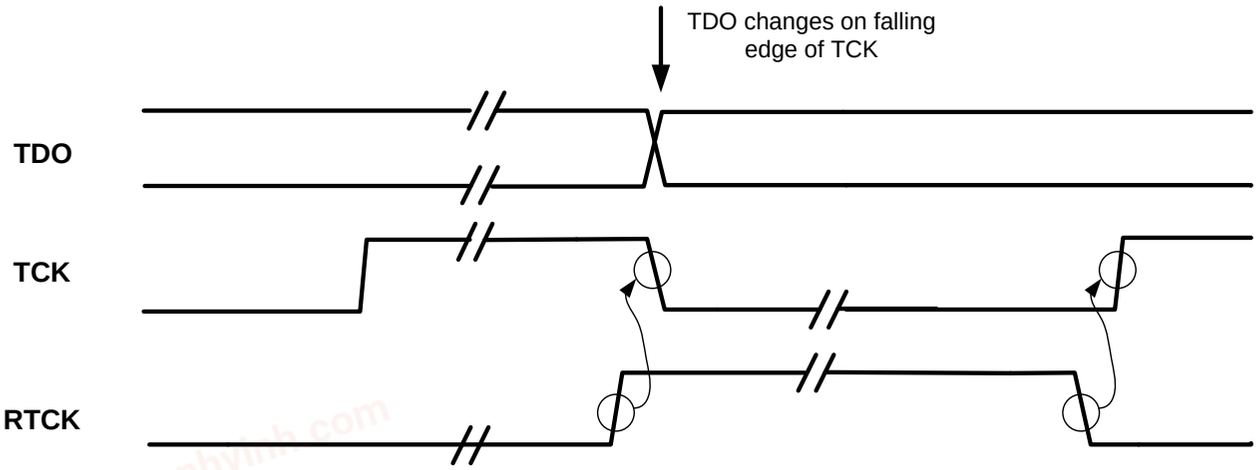


Figure 10 – Adaptive Clocking Waveform

Adaptive clocking is not enabled by default.

See: AN_108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes.

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4.5 Synchronous & Asynchronous Bit-Bang Interface Mode Desc.

The FT4233HP/FT4232HP channel A, B, C or channel D can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous.

4.5.1 Asynchronous Bit-Bang Mode

Asynchronous Bit-Bang mode is the same as BM-style Bit-Bang mode. On any channel configured in asynchronous bit-bang mode, data written to the device in the normal manner will be self-clocked onto the parallel I/O data pins (those which have been configured as outputs). Each I/O pin can be independently set as an input or an output. The rate that the data is clocked out at is controlled by the baud rate generator.

For the data to change there has to be new data written, and the baud rate clock has to tick. If no new data is written to the channel, the pins will hold the last value written.

4.5.2 Synchronous Bit-Bang Mode

The synchronous Bit-Bang mode will only update the output parallel I/O port pins whenever data is sent from the USB interface to the parallel interface. When this is done, data is read from the USB Rx FIFO buffer and written out on the pins. Data can only be received from the parallel pins (to the USB Tx FIFO interface) when the parallel interface has been written to.

With Synchronous Bit-Bang mode, data will only be sent out by the FT4233HP/FT4232HP if there is space in the FT4233HP/FT4232HP USB TXFIFO for data to be read from the parallel interface pins. This Synchronous Bit-Bang mode will read the data bus parallel I/O pins first, before it transmits data from the USB RxFIFO. It is therefore 1 byte behind the output, and so to read the inputs for the byte that you have just sent, another byte must be sent.

For example:-

(1) Pins start at 0xFF
Send 0x55, 0xAA
Pins go to 0x55 and then to 0xAA
Data read = 0xFF, 0x55

(2) Pins start at 0xFF
Send 0x55, 0xAA, 0xAA
(Repeat the last byte sent)
Pins go to 0x55 and then to 0xAA

Data read = 0xFF, 0x55, 0xAA

Synchronous Bit-Bang Mode differs from Asynchronous Bit-Bang mode in that the device parallel output is only read when the parallel output is written to by the USB interface. This makes it easier for the controlling program to measure the response to a USB output stimulus as the data returned to the USB interface is synchronous to the output data.

Asynchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 1 will enable Asynchronous Bit-Bang mode.

Synchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 4 will enable Synchronous Bit-Bang mode.

See application note AN2232-02 - Bit Mode Functions for the FT2232 for more details and examples of using the bit-bang modes.

An example of the synchronous bi-bang mode timing is shown in **Figure 11** and **Table 11.**

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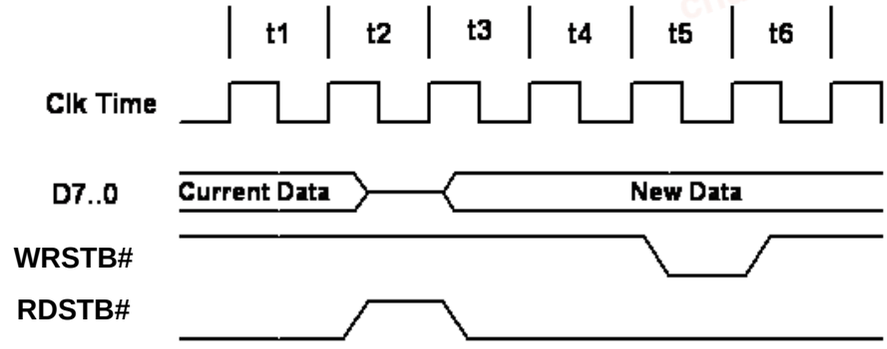


Figure 11 – Synchronous Bit-Bang Mode Timing Interface Example

It should be noted that the FT4233HP/FT4232HP do not output the WRSTB# or RDSTB# signals when configured in bit-bang mode.

Figure 11 shows these signals for **illustration** purposes only.

NAME	Description
t1	Current pin state is read
t2	RDSTB# is set inactive and data on the paralle I/O pins is read and sent to the USB host.
t3	RDSTB# is set active again, and any pins that are output will change to their new data
t4	1 clock cycle to allow for data setup
t5	WRSTB# goes active. This indicates that the host PC has written new data to the I/O parallel data
t6	WRSTB# goes inactive

Table 11 - Synchronous Bit-Bang Mode Timing Interface Example

4.6 USB Type-C/PD Controller

4.6.1 PD controller description

The FT4233HP/FT4232HP have a Type-C/PD controller that fully supports the latest USB Type-C and Power Delivery (PD) 3.0 standards enabling support for power negotiation with the ability to sink or source current to a USB host device. There are two PD ports in the device (FT4233HPQ and FT4233HPL only), one port is with the legacy USB 2.0 port to form USB PD port as a power sink or source, and the other port is standalone PD port as a sink which is used to connect to PD power source. Power Delivery function is designed to meet PD2.0/3.0 specification. If the device is configured to be operated in legacy USB2.0 mode it will be backward compatible to FT4232H in terms of USB2.0 and its peripheral IOs functions.

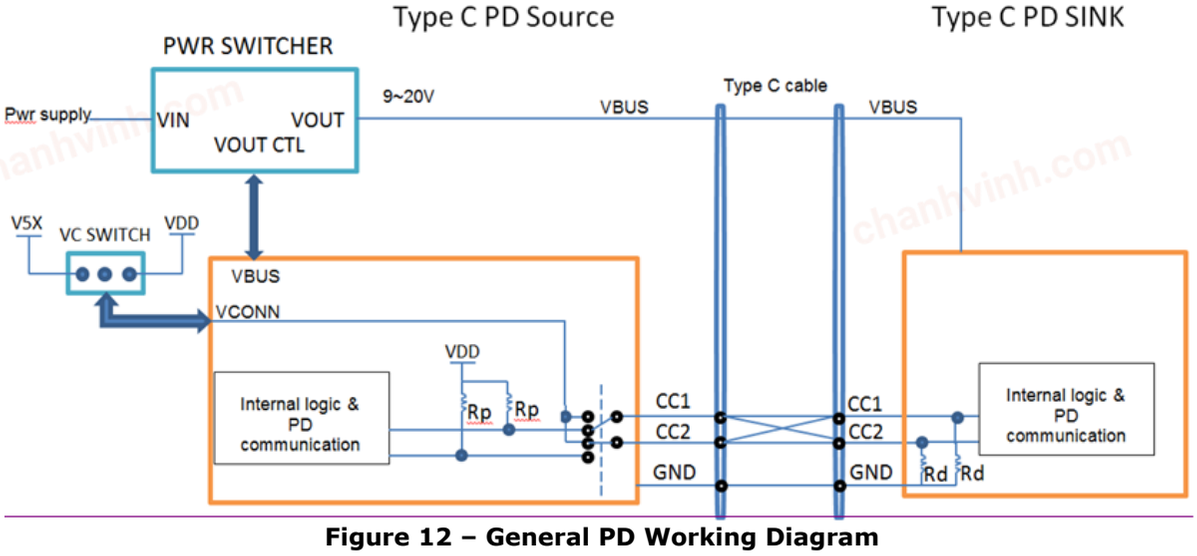


Figure 12 – General PD Working Diagram

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4.6.2 Features

- PD 3.0 Compliant.
- Physical layer and Policy Engine.
- Initial Sink, with Dual Role Power (Power Role Swap).
- Multiple Configurable Power Profiles.
- Supports up to 20V5A power profile.
- Charge through Support.
- Cable Attach and Orientation Detection.
- Supports 1.5A and 3A cables in Type-C legacy mode (NON-PD Mode).
- Profile Selection indication through GPIOs when operating In Sink Mode.
- Supports External MCU to take over the control.
- 8 bit register interface for a low speed processor, or optional I2C port
- Integrated Chapter 6 protocol reduces required MPU response time to 10mS.
- K code recognition/coding, preamble, CRC, etc offloaded from processor.
- VCONN 200mA protected driver switches
- Single 12MHz clock + 32KHz low power clock.
- Slew rate limited driving of CC cable lines drive to 1.1V and 300nS linear transition time.

4.6.3 AC timing on GPIO pins

Best case transition time with 5pF load		Worst case transition time with 15pF load	
Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)
1.2	1.1	6.0	6.5

Table 12 – AC Timing on GPIO

4.6.4 GPIO Timing for PD Operation

GPIOs are used as a power profile indicator as well as power supply controllers.

When operating as a Sink, GPIO pins are used for LOAD_EN and ISET.

Depending on the kind of profile negotiated, the appropriate ISET GPIO will go high followed by LOAD_EN pin.

The timing between this ISET going high to LOAD_EN can be as high as 12.5uS.

When operating as a Source, GPIO pins are used as power supply controller. During Source operation, initial voltage will be 5V and then depending on the profile setting, the PD controller can negotiate a higher voltage. The switching from 5V to higher Voltage or vice versa is by switching GPIOs. 5V could be controlled by one Pin whereas each higher Voltage is controlled by a different pin.

For example, **Table 19** – Operating Voltage and Current shows a sample GPIO states for 3 different voltage cases.

	5v	9V	20V
PS_EN	HIGH	HIGH	HIGH
GPIO_9v	LOW	HIGH	LOW
GPIO_20v	LOW	LOW	HIGH

Table 13 – Example GPIO States for Power Control

In this case 5V to 9V or 5v to 20V is just an additional GPIO pin going high. In this case the timing does not matter.

However in the scenario when the profile changes from 9V to 20V, there is one GPIO going Low where as another one going high. In this case the delay between one pin going low to another pin going high can be as high as 12.5uS.

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4.6.5 Voltage parameters

Based on USB Type-C specification, during initialization when Source connects to Sink, both are in the unattached state. Source firstly detects the Sink's pull down on CC then enters attached state, Source turns on VBUS and VCONN. So USB Type-C specification requests voltage parameters shown below:

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00V	0.15V	0.20V
Sink(vRd)	0.25V	1.50V	1.60V
No connect (vOPEN)	1.65V		

Table 14 – CC Voltage on Source Side – Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00V	0.35V	0.40V
Sink(vRd)	0.45V	1.50V	1.60V
No connect (vOPEN)	1.65V		

Table 15 – CC Voltage on Source Side – 1.5 A @ 5V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00V	0.75V	0.80V
Sink(vRd)	0.85V	2.45V	2.60V
No connect (vOPEN)	2.75V		

Table 16 – CC Voltage on Source Side – 3A @ 5V

To better achieve USB Type-C specification requests, we suggest to use a Schottky Diode to isolate DCDC power from Vcc_PD and PD1_Vconn of FT4233HP/FT4232HP in order to guarantee the expected voltage parameters. The capacitance between Vcc_PD/PD1_Vconn and ground should not be more than 1uF to avoid the slow rise up of CC line due to the leakage through Vcc_PD and PD1_Vconn to the capacitor. The equivalent circuit is shown below:

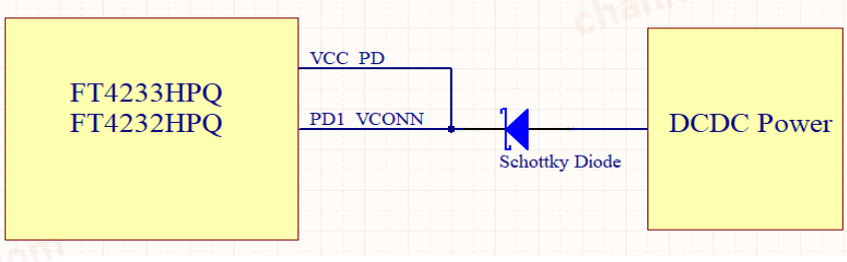


Figure 13 – Schottky Diode Equivalent Circuit

Recommended schottky diode parameters:

$V_{(R)}$	I_F	V_F (Forward Voltage)
-30V(max)	≤ 5A	≤ 0.3V

Table 17 – Schottky Diode Recommended Characteristics

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5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT4233HP/FT4232HP devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these values may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C
MTTF FT4233HP/FT4232HP	TBD	Hours
VCORE Supply Voltage	-0.3 to +2.0	V
VCCIO IO Voltage	-0.3 to +4.0	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V
DC Input Voltage – High Impedance Bi-directional (powered from VCCIO)	-0.3 to +5.8	V
DC Input Voltage – All Other Inputs	-0.5 to + (VCCIO +0.5)	V
DC Output Current – Outputs	16	mA

Table 18 – Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCORE	VCC Core Operating Supply Voltage	1.08	1.20	1.32	V	
VCCIO*	VCCIO Operating Supply Voltage	2.97	3.30	3.63	V	
VREGIN	VREGIN Voltage regulator Input	3.00	3.30	3.60	V	
VREGOUT	Voltage regulator Output	1.08	1.2	1.32	V	
Ireg	Regulator Current		21.11	150	mA	VREGIN +3.3V and data transfer with 12Mbps
Icc1s	VREGIN Suspend Supply Current		1.64		mA	USB Suspend
I_vcd_usb	VCC_USB operating supply current		22.7		mA	Data transfer with 12Mbps
I_vccio	VCC_IO operating supply current		0.87		mA	Data transfer with 12Mbps
I_vcc_pd	VCC_PD suspend supply current		209		uA	PD suspend

Table 19 – Operating Voltage and Current

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Note: Failure to connect all VCCIO pins will result in failure of the device.
The I/O pins are +3.3v cells, which are +5V tolerant (except the USB PHY pins).

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.40	3.14		V	Ioh = +/-2mA I/O Drive strength* = 4mA
			3.20		V	I/O Drive strength* = 8mA
			3.22		V	I/O Drive strength* = 12mA
			3.22		V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0.18	0.40	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0.12		V	I/O Drive strength* = 8mA
			0.08		V	I/O Drive strength* = 12mA
			0.07		V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold		-	0.80	V	LVTTL
Vih	Input High Switching Threshold	2.0	-		V	LVTTL
Vt	Switching Threshold		1.50		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage	0.80	1.10	-	V	
Vt+	Schmitt trigger positive going threshold voltage		1.60	2.0	V	
Rpu	Input pull-up resistance**	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	15	45	85	µA	Vin = 0
Ioz	Tri-state output leakage current		+/-10		µA	Vin = 5.5V or 0

Table 20 – I/O Pin Characteristics (except USB PHY pins)

*The I/O drive strength and slow slew-rate are configurable in the EEPROM.
**The voltage pulled up to is VCCIO-0.9V in the worst case.

5.3 ESD Tolerance

ESD protection for FT4233HP/FT4232HP IO's

Parameter	Reference	Minimum	Typical	Maximum	Units
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001 Class 2		±2kV		kV
Machine Mode (MM)	JEDEC EIA/JESD22-A115-C, Class B		±200V		V
Charge Device Model (CDM)	ANSI/ESDA/JEDEC JS-002, JEDEC JESD22-C101-D Class-III		±500V		V
Latch-up	JEDEC STANDARD EIA/JESD78, Trigger Class-II		±200mA		mA

Table 21 – ESD Tolerance

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5.4 Thermal Characteristics

Parameter	Minimum	Typical	Maximum	Units
Θ_{JA} (FT4233HPL)		50		°C/W
Θ_{JC} (FT4233HPL)		11		°C/W
Θ_{JA} (FT4233HPQ)		29		°C/W
Θ_{JC} (FT4233HPQ)		1.0		°C/W
Θ_{JA} (FT4232HPQ)		23.65*		°C/W
Θ_{JC} (FT4232HPQ)		9.35*		°C/W
T_J (FT4233HPL/FT4233HPQ/FT4232HPQ)	-40	25	125	°C

Table 22 – Thermal Characteristics

* Preliminary data

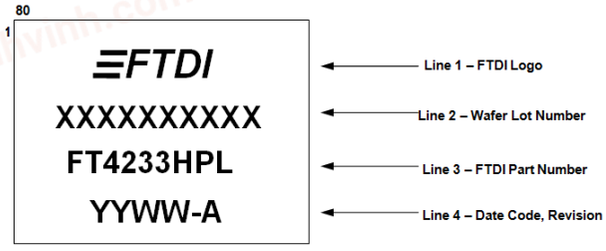
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6 Package Parameters

The FT4233HP/FT4232HP are available in three different packages. The FT4233HPL is the LQFP-80 package option, the FT4233HPQ is the QFN-76 package option and the FT4232HPQ is the QFN-68 package option. See TN_166 FTDI Example IC Footprints for PCB footprint guidelines.

6.1 FT4233HPL, LQFP-80 Package Dimensions

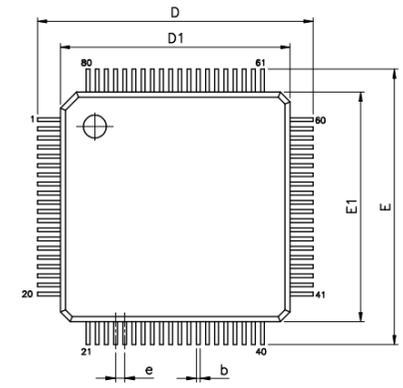


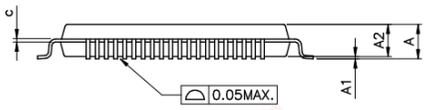
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

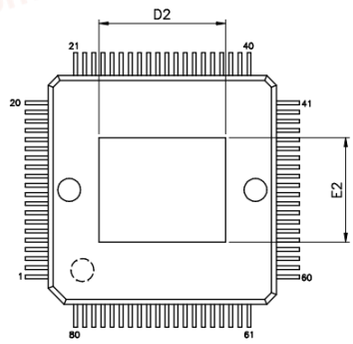
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

5 THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	D2		E2	
	MIN.	MAX.	MIN.	MAX.
218X18E	4.71	5.54	3.88	4.57







(THERMALLY ENHANCED VARIATIONS ONLY)

NOTES:
1. JEDEC OUTLINE:
   MS-026 BCE
   MS-026 BCE-HD(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

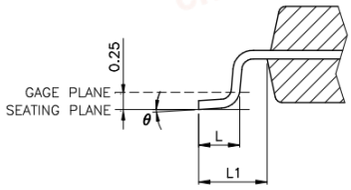
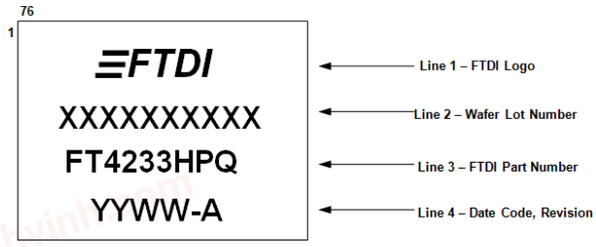
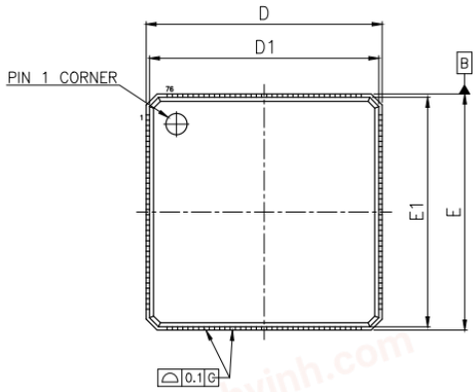


Figure 14 – 80 Pin LQFP Package Details

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6.2 FT4233HPQ, QFN-76 Package Dimensions





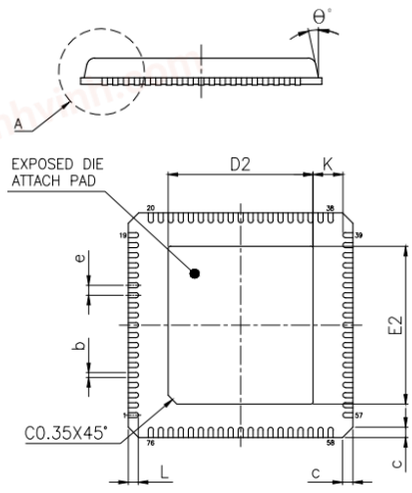
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.15	0.20	0.25
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.40 BSC.	
K	0.20	—	—
θ°	0.00	—	12.00

UNIT : mm

UNIT : mm	EXPOSED PAD						L		
	D2			E2					
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
2 245X26* MIL	5.56	5.81	6.06	6.06	6.31	6.56	0.30	0.40	0.50

2 "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.



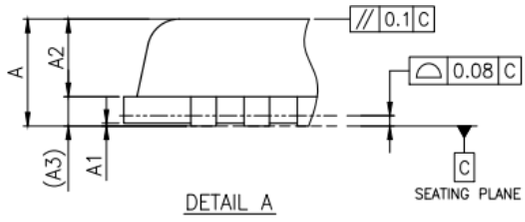
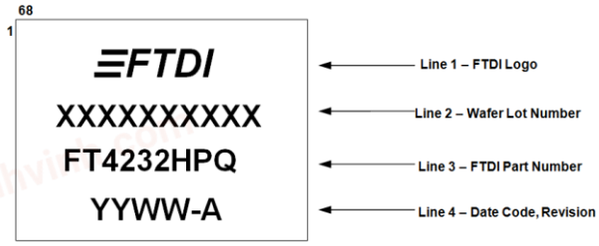


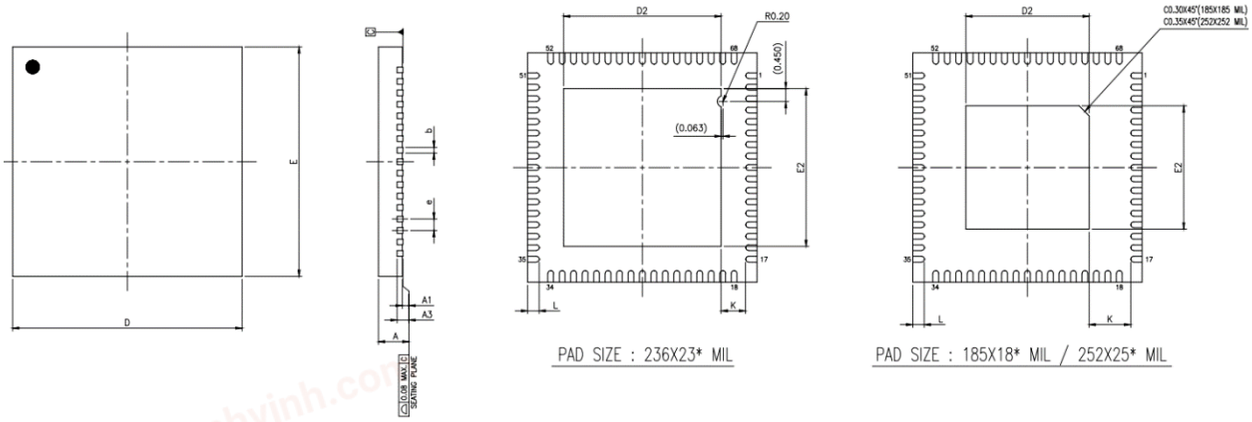
Figure 15 -76 Pin QFN Package Details

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6.3 FT4232HPQ, QFN-68 Package Dimensions





	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X868)			VQFN(Y868)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.15	0.20	0.25	0.15	0.20	0.25
D	8.00 BSC			8.00 BSC		
E	8.00 BSC			8.00 BSC		
e	0.40 BSC			0.40 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
6 185X18* MIL	4.25	4.30	4.35	4.25	4.30	4.35	V	X	N/A
6 236X23* MIL	5.45	5.50	5.55	5.45	5.50	5.55	V	X	N/A
6 252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	X	VLLE-1

6 "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 16 – 68 Pin QFN Package Details

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7 EEPROM Configuration

If an external EEPROM is fitted (93LC66) it can be programmed over USB using FT_PROG. The EEPROM must be 16 bits wide and capable of working at a VCC supply of +3.0 to +3.6 volts.

Adding an external EEPROM allows selecting the TXDEN for RS485 mode when asynchronous serial interface has been selected.

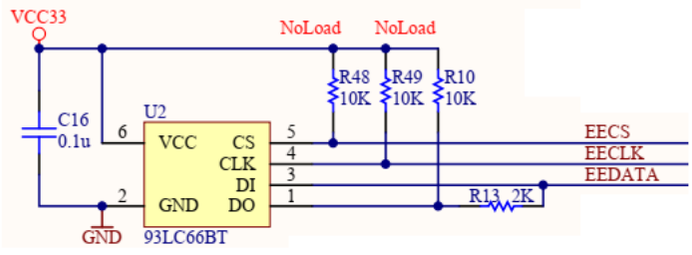


Figure 17 - EEPROM Interface

The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT4233HP/FT4232HP for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off, I/O pin drive strength and TXDEN selection.

If no EEPROM is connected (or the EEPROM is blank), the FT4233HP/FT4232HP uses its built-in default VID (0403), PID (6041/6043) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

7.1 Default EEPROM Configuration

The external EEPROM (if it's fitted) can be programmed over USB using FT_PROG. This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process. Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs.

See TN_100 USB Vendor ID/Product ID Guidelines for more information.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product ID (PID)	6041h 6043h	FTDI default PID (hex) for FT4233HP FTDI default PID (hex) for FT4232HP
bcd Device	0x2900 0x3100	for FT4233HP for FT4232HP
Serial Number Enabled?	Yes	
Serial Number	None	
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	FT4233HP FT4232HP	for FT4233HP for FT4232HP
Max Bus Power Current	500mA	
Power Source	Bus Powered	
Device Type	FT4233HP FT4232HP	for FT4233HP for FT4232HP
USB Version	0200h	Returns USB 2.0 device description to the host.
Remote Wake Up	Disabled	Taking RI# low will wake up the USB host controller from suspend in approximately 20 ms. If enabled.
RI RS485	Disabled	Enables TXDEN signal for RS485 buses.
High Current I/Os	Disabled	Enables the high drive level on the UART and ACBUS I/O pins.
IO Slew	Disabled	Slow slew rate if enabled

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Parameter	Value	Notes
Schmitt Trigger for Input pin	Normal trigger	Schmitt trigger for input pin if enabled
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.

Table 23 – Default Configuration with a blank/no EEPROM

7.2 PD Configuration and Default values

Refer to AN_448 FT4233HP_FT2233HP_FT233HP_Configuration_Guide for FT4233HP Power Delivery configuration and Default values.

Refer to AN_551_FT4232HP_FT2232HP_FT232HP_Configuration_Guide for FT4232HP Power Delivery configuration and Default values.

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Appendix A – References

Document References

AN_177 User Guide For libMPSSE-I2C
AN_178 User Guide For libMPSSE-SPI
AN 113 Interfacing FT2232H Hi-Speed Devices To I2C Bus
AN_114 Interfacing FT2232H Hi-Speed Devices To SPI Bus
AN_110 - Programmers Guide for High Speed FTCJTAG DLL
AN_135 MPSSE Basics
AN_108 Command Processor for MPSSE and MCU Host Bus Emulation Modes
TN_104 Guide to Debugging Customers Failed Driver Installation
TN_100 USB Vendor ID/Product ID Guidelines
AN_411 - FTx232H MPSSE I2C Master Example in C#
TN_166 FTDI Example IC Footprints
AN2232-02 - Bit Mode Functions for the FT2232
74HC595 datasheet
FT_PROG EEPROM Programming Utility
AN_448 FT4233HP_FT2233HP_FT233HP_Configuration_Guide
AN_551_FT4232HP_FT2232HP_FT232HP_Configuration_Guide
AN_449 FT4233HP_FT2233HP_FT4232HP_FT2232HP DCDC_Power Delivery
TN_180 FT4233HP_FT2233HP_FT233HP_Errata Technical Note
Evaluation Modules

Acronyms and Abbreviations

Terms	Description
DRP	Dual Role Power
EEPROM	Electrically Erasable Programmable Read-Only Memory
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
IC	Integrated Circuit
I2C	Inter Integrated Circuit
JTAG	Joint Test Action Group
LDO	Low Drop Out
LED	Light Emitting Diode
MCU	Microcontroller Unit
MPSSE	Multi-Protocol Synchronous Serial Engine
PD	Power Delivery
PLD	Programmable Logic Device
QFN	Quad Flat No-Lead
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
UTMI	Universal Transceiver Macrocell Interface
VCP	Virtual COM Ports

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Appendix C – Revision History

Document Title: FT4233HP Datasheet

Document Reference No.: FT_001473

Clearance No.: FTDI#555

Product Page: https://ftdichip.com/product-category/products/ic/?series_products=51

Document Feedback: Send Feedback

Revision	Changes	Date
Draft	Initial Release	03-06-2020
1.0	Update the Figure #12 caption Updated terms in section 4.6.2 and 4.6.4	02-07-2020
1.1	Updated the following: - Packing details for reel and tray in section 1.2 - vConn power in section 4.2 - vConn swap support has been removed in section 4.6.2 - circuit diagram and description in section 4.6.5 - Tables in section 5.2 - Table 15 in Section 5.3 with latest spec - Latency Timer description in Section 4.1 - Added new Chapter 7 for EEPROM configuration - Document References section	14-05-2020

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