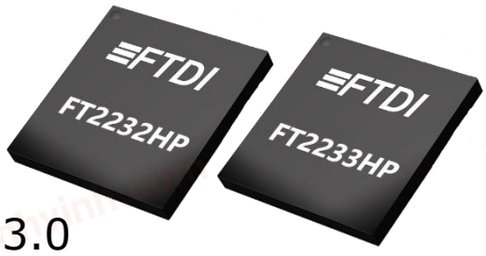
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FT2233HP/FT2232HP



(High Speed USB Bridge with Type-C/PD3.0 Controller)

The FT2233HP/FT2232HP is a Hi-Speed USB device with a Type-C/PD 3.0 controller that fully supports the latest USB Type-C and Power Delivery (PD) standards enabling support for power negotiation with the ability to sink or source current to a USB host device. The USB bridge function delivers 2 independent channels compatible with the FT2232H – Dual Hi-speed USB to multipurpose UART/MPSSE solution.

The FT2233HP/FT2232HP has the following advanced features:

- Support PD specification Rev 3.0.
- Port 1 mode configuration for Sink or Dual-role
- Port 2 works as Sink, supporting charge through to port1 (FT2233HPQ and FT2233HPL only)
- Support 5V3A, 9V3A, 12V3A, 15V3A and 20V3A PDOs as sink or source Type-C/PD Physical Layer Protocol
- PD policy engine using 32-bit RISC controller with 8kB data RAM and 48kB code ROM
- PD mode configuration through external EEPROM
- Options to use external MCU controlling PD policy through I2C interface
- USB to dual serial ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- USB 2.0 High Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Two Multi-Protocol Synchronous Serial Engine (MPSSE) on channel A and channel B, to simplify synchronous serial protocol (USB to JTAG, I^2C, SPI or bit-bang) design.
- Independent Baud rate generators.
- RS232/RS422/RS485 UART Transfer Data Rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Optional traffic TX/RX indicators can be added with LEDs.
- Adjustable receive buffer timeout.
- Support for USB suspend and resume conditions via PWREN#, SUSPEND# and RI# pins.
- FTDI FT232R/FT-X style, asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Auto-transmit enable control for RS485 serial applications using TXDEN pin through external EEPROM setting.
- Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface.
- Low operating and USB suspend current.
- Configurable I/O drive strength (4, 8, 12 or 16mA) and slew rate.
- USB Bulk data transfer mode (512 byte packets in High Speed mode).
- Dedicated Windows DLLs available for USB to SPI, and USB to I^2C applications.
- +3.3V single supply operating voltage range.
- +3.3V I/O interfacing.
- Highly integrated design includes +1.2V LDO regulator for VCORE, integrated POR function and on chip clock multiplier PLL (12MHz – 480MHz).
- Extended -40°C to 85°C industrial operating temperature range.
- Available in Pb-free QFN-76/QFN-68/LQDP-80 package (RoHS compliant)

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1 Typical Applications

- USB bridge with Type-C/PD (chargers and devices)
- High-power application via USB PD and/or Type-C port
- Get power from USB device functions, e.g. portable USB host needs charging when USB is connected.
- Single chip USB to two channels UART (RS232, RS422 or RS485) or Bit-Bang interfaces.
- Single chip USB to 2 JTAG channels
- Single chip USB to one JTAG channel and one UART.
- Single chip USB to one SPI channel and one UART.
- Single chip USB to two SPI channels.
- Single chip USB to two Bit-Bang channels.
- Single chip USB to one SPI channel and one JTAG channel.
- Single chip USB to two I^2C channels.
- Numerous combinations of two channels.
- Upgrading Legacy Peripheral Designs to USB
- Field Upgradable USB Products
- Cellular and cordless phone USB data transfer cables and interfaces.
- Interfacing MCU / PLD / FPGA based designs to USB
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB FLASH Card Reader / Writers
- Set Top Box PC – USB interface
- USB Digital Camera Interface
- USB Bar Code Readers

1.1 Driver Support

The FT2233HP/FT2232HP requires USB drivers (listed below), available for free at https://www.ftdichip.com, which are used to make the FT2233HP/FT2232HP appear as a virtual COM port (VCP). This allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT2233HP/FT2232HP through a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Mac OS-X
- Linux 2.4 and greater

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Linux 2.4 and greater
- Android(J2xx)
- Mac OS-X

For driver installation, please refer to the installation guides on our website:
http://www.ftdichip.com/Support/Documents/InstallGuides.htm

The following additional installation guides application notes and technical notes are also available:

- AN_113, "Interfacing FT2232H Hi-Speed Devices To I2C Bus".
- AN_117 – "User Guide For libMPSSE – I2C "
- AN_178 – "User Guide For libMPSSE - SPI"
- AN 113 – "Interfacing FT2232H Hi-Speed Devices To I2C Bus"
- AN114 – "Interfacing FT2232H Hi-Speed Devices To SPI Bus"
- AN135 – MPSSE Basics
- AN108 – Command Processor For MPSSE and MCU Host Bus Emulation Modes
- AN_448_FT4233HP_FT2233HP_User_Configuration_Guide Ver.1.0
- AN_449_FT4233HP_FT2233HP_DCDC_Application_Guide Ver.1.0
- AN_411 - FTx232H MPSSE I2C Master Example in C#
- TN_104, "Guide to Debugging Customers Failed Driver Installation"

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1.2 Part Numbers

Part Number	Package
FT2233HPQ-xxxx	76 Pin QFN
FT2233HPL-xxxx	80 Pin LQFP
FT2232HPQ-xxxx	68 Pin QFN

1.3 USB Compliant

The FT2233HP/FT2232HP is fully compliant with the USB 2.0 specification and the USB PD 3.0 specification.
It has been given the USB-IF Test-ID (XXXXX)*.

* For PD port1

The timing of the rise/fall time of the USB signals is not only depend on the USB signal drivers, it is also depend on system and is affected by factors such as PCB layout, external components and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. Timing can also be changed by adding appropriate passive components to the USB signals.

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2 FT2233HP Block Diagram

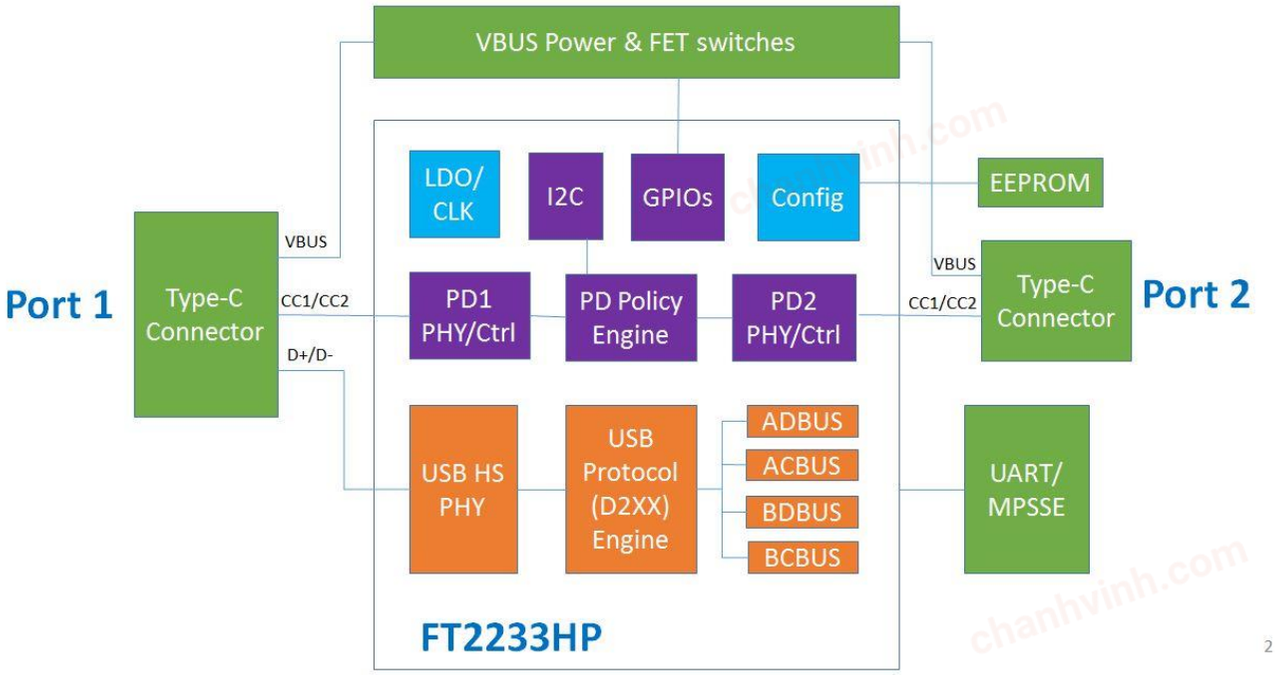


Figure 2.1 FT2233HP Block Diagram

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 QFN–76 Package Pin Out

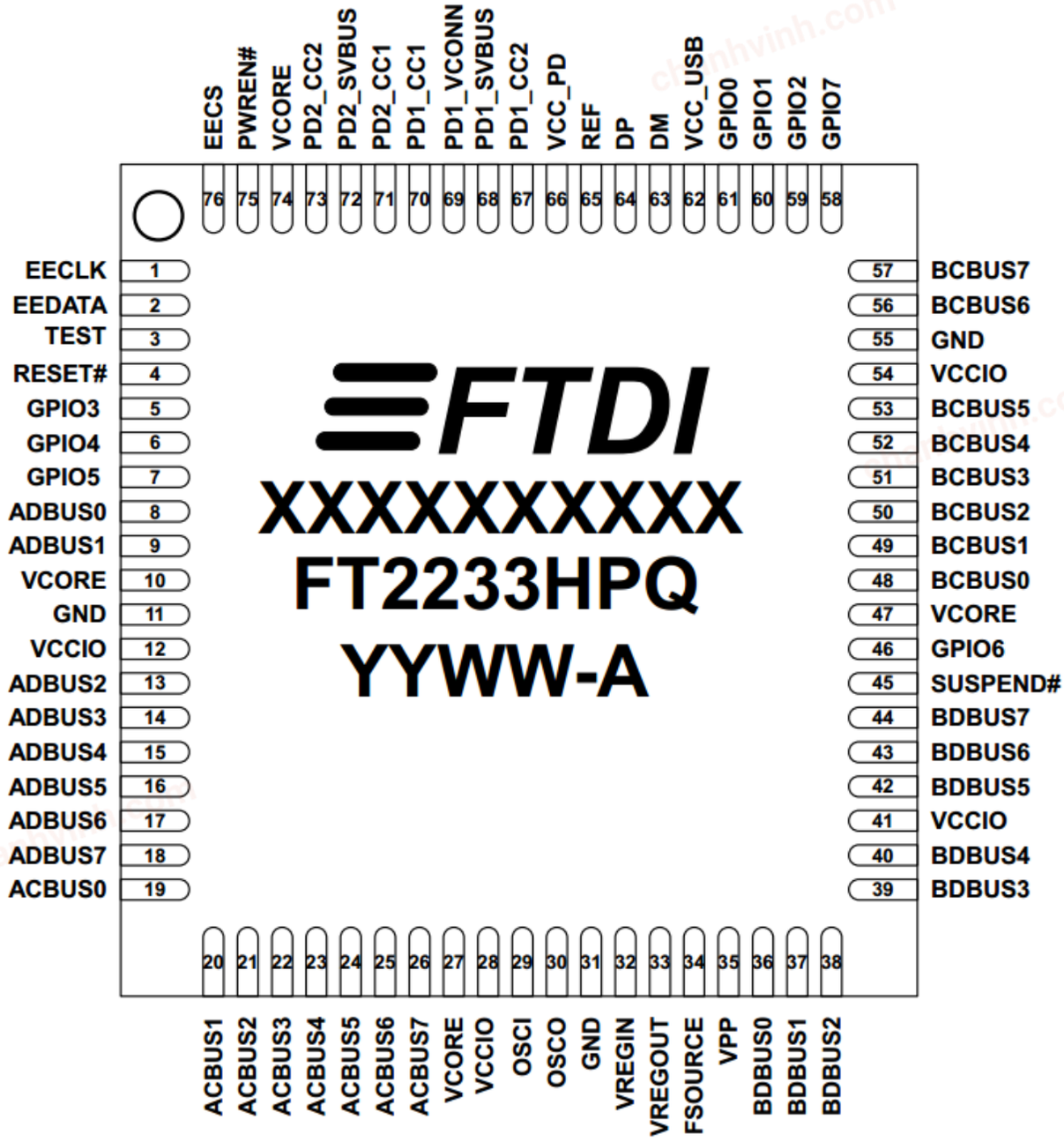


Figure 3.1 Pin Configuration QFN-76 (Top View)

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3.2 QFN–68 Package Pin Out

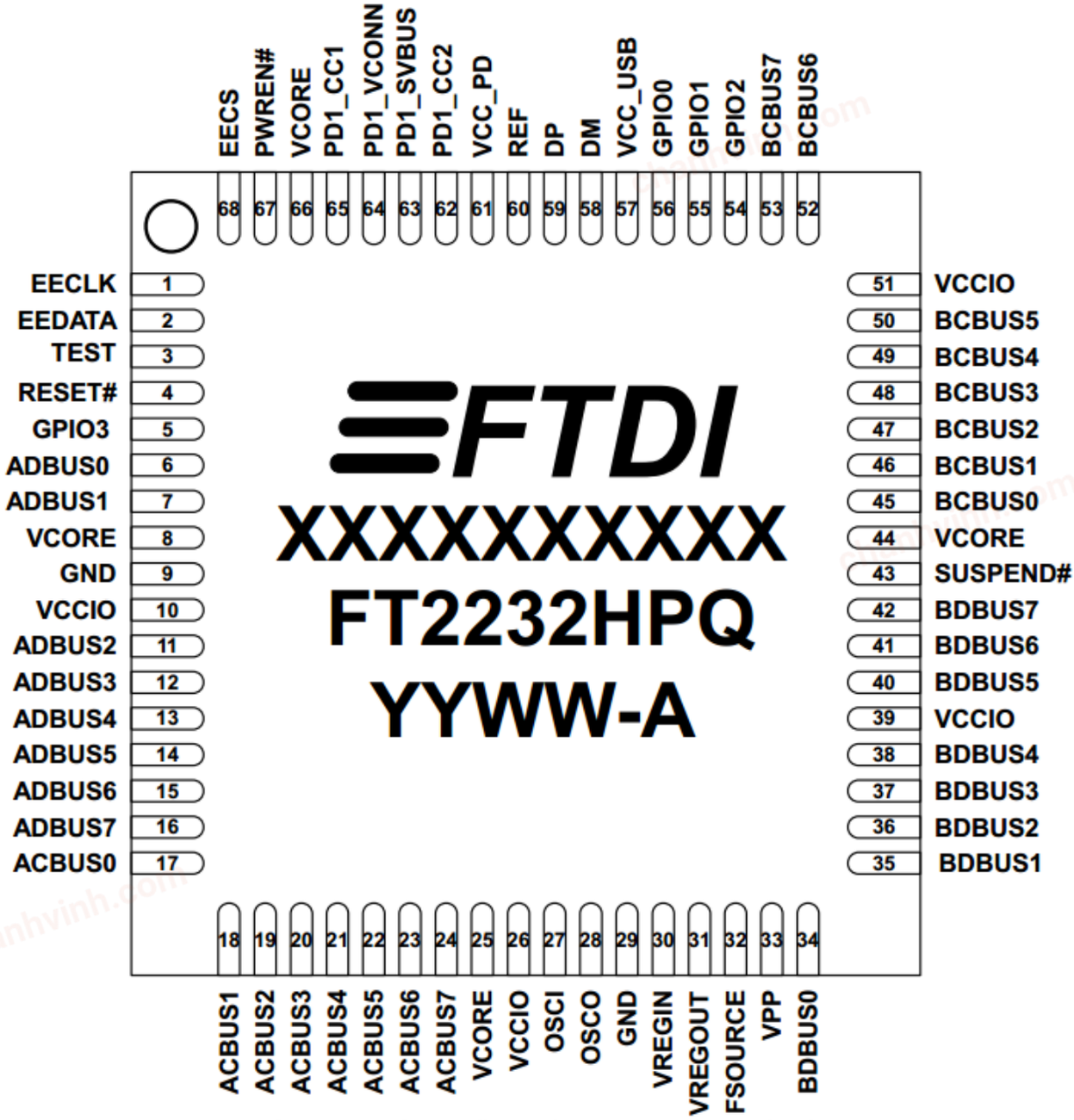


Figure 3.2 Pin Configuration QFN-68 (Top View)

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3.3 LQFP–80 Package Pin Out

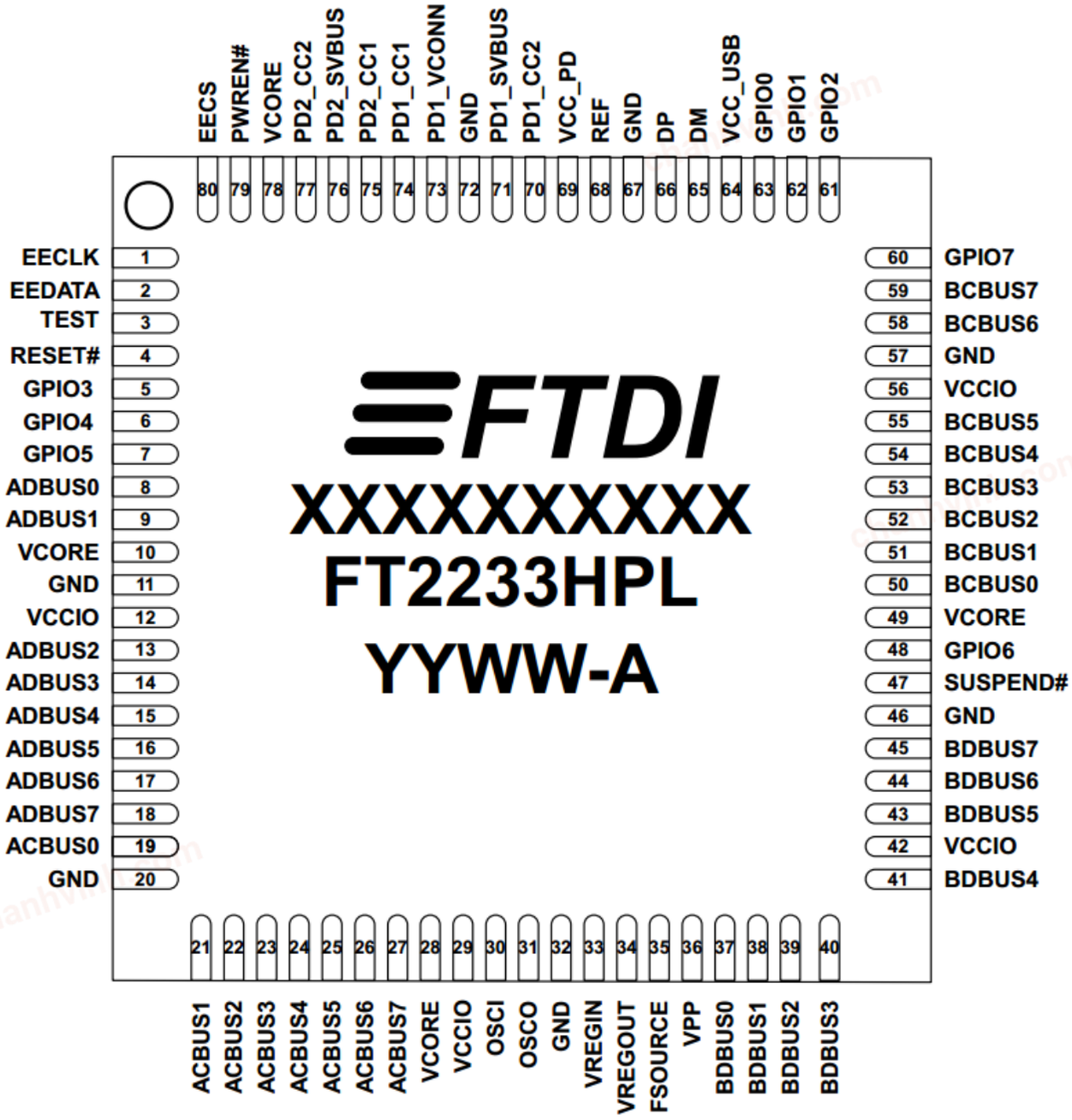


Figure 3.3 Pin Configuration LQFN-80 (Top View)

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3.4 Pin Description

This section describes the operation of the FT2233HP/FT2232HP pins. The function of many pins is determined by the configuration of the FT2233HP/FT2232HP. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions are described in Table 3.1.

Note: The convention used throughout this document for active low signals is the signal name followed by #.

FT2233HP/FT2232HP												
Pins#				Pin functions (depend on configuration)								
QFN68	QFN76	LQFP80	Pin Name	ASYNC Serial (RS232)	245 FIFO SYNC	245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	Host Bus Emulation
Channel A												
6	8	8	ADBUS0	TXD	D0	D0	D0	D0	TCK/SK		D0	AD0
7	9	9	ADBUS1	RXD	D1	D1	D1	D1	TDI/DO		D1	AD1
11	13	13	ADBUS2	RTS#	D2	D2	D2	D2	TDO/DI		D2	AD2
12	14	14	ADBUS3	CTS#	D3	D3	D3	D3	TMS/CS		D3	AD3
13	15	15	ADBUS4	DTR#	D4	D4	D4	D4	GPIOL0		D4	AD4
14	16	16	ADBUS5	DSR#	D5	D5	D5	D5	GPIOL1		D5	AD5
15	17	17	ADBUS6	DCD#	D6	D6	D6	D6	GPIOL2		D6	AD6
16	18	18	ADBUS7	RI#	D7	D7	D7	D7	GPIOL3		D7	AD7
17	19	19	ACBUS0	TXDEN	RXF#	RXF#	**	**	GPIOH0		CS#	A8
18	20	21	ACBUS1	**	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1		A0	A9
19	21	22	ACBUS2	**	RD#	RD#	RDSTB#	RDSTB#	GPIOH2		RD#	A10
20	22	23	ACBUS3	RXLED#	WR#	WR#	**	**	GPIOH3		WR#	A11
21	23	24	ACBUS4	TXLED#	SIWUA	SIWUA	SIWUA	SIWUA	GPIOH4	SIWUA	Note1	A12
22	24	25	ACBUS5	**	CLKOUT	**	**	**	GPIOH5		**	A13
23	25	26	ACBUS6	**	OE#	**	**	**	GPIOH6		**	A14
24	26	27	ACBUS7	**	**	**	**	**	GPIOH7		**	A15
Channel B												
34	36	37	BDBUS0	TXD		D0	D0	D0	TCK/SK	FSDI	D0	CS#
35	37	38	BDBUS1	RXD		D1	D1	D1	TDI/DO	FSCLK	D1	ALE
36	38	39	BDBUS2	RTS#		D2	D2	D2	TDO/DI	FSDO	D2	RD#

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37	39	40	BDBUS3	CTS#		D3	D3	D3	TMS/ CS	FSCTS	D3	WR#
38	40	41	BDBUS4	DTR#		D4	D4	D4	GPIO L0		D4	IORDY
40	42	43	BDBUS5	DSR#		D5	D5	D5	GPIO L1		D5	CLKO UT
41	43	44	BDBUS6	DCD#		D6	D6	D6	GPIO L2		D6	I/O0
42	44	45	BDBUS7	RI#		D7	D7	D7	GPIO L3		D7	I/O1
45	48	50	BCBUS0	TXDEN		RXF#	**	**	GPIO H0		CS#	**
46	49	51	BCBUS1	**		TXE#	WRST B#	WRSTB #	GPIO H1		A0	**
47	50	52	BCBUS2	**		RD#	RDST B#	RDSTB #	GPIO H2		RD#	**
48	51	53	BCBUS3	RXLED#		WR#	**	**	GPIO H3		WR#	**
49	52	54	BCBUS4	TXLED#		SIWU B	SIWU B	SIWUB	GPIO H4		Note1	**
50	53	55	BCBUS5	**		**	**	**	GPIO H5		**	**
52	56	58	BCBUS6	**		**	**	**	GPIO H6		**	**
53	57	59	BCBUS7	PWRSAV #	PWRS AV#	PWRS AV#	PWRS AV#	PWRSA V#	GPIO H7	PWRS AV#	PWRSA V#	PWRS AV#
67	75	79	PWREN#	PWREN#	PWRE N#	PWRE N#	PWRE N#	PWREN #	PWR EN#	PWRE N#	PWREN #	PWRE N#
43	45	47	SUSPEND #	SUSPEN D#	SUSP END#	SUSP END#	SUSP END#	SUSPE ND#	SUSP END #	SUSP END#	SUSPE ND#	SUSPE ND#

Table 3.1 FT2233HP/FT2232HP Pin Description

***** RI#/ or TXDEN is selectable in the EEPROM. Default is RI#.

Note: Initial Pin States - The device will always start up as four UART ports. Therefore pins which are output in UART mode will be driving out. If an application uses MPSSE or bit-bang, ensure that any external signals do not drive into these pins and cause contention until the application has configured the mode and direction of these lines.

Note: If wake up USB device in this mode, will put ACBUS0 from "High" to "LOW", ACBUS1 set "High", ACBUS3 from "High" to "LOW". Channel B is the same setting.

3.5 Common Pins

The operation of the following FT2233HP/FT2232HP pins are the same regardless of the configured mode:-

FT2233HP/FT2232HP					
QFN-68	QFN-76	LQFP-80	Name	Type	Description
8,25,44,66	10,27, 47, 74	10,28,49,78	VCORE	POWER Input	+1.2V input. Core supply voltage input. Connect to VREGOUT when using internal regulator.
10,26,39,51,	12,28, 41, 54	12,29,42,56	VCCIO	POWER Input	+3.3V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.
57	62	64	VCC_USB	POWER Input	+3.3V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter.
61	66	69	VCC_PD	POWER Input	+3.3V Input. Internal PD PHY power supply input.

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30	32	33	VREGIN	POWER Input	+3.3V Input. Integrated 1.2V voltage regulator input.
31	33	34	VREGOUT	POWER Output	+1.2V Output. Integrated voltage regulator output. Connect to VCORE with 3.3uF filter capacitor. This output should not be used to power other circuits apart from VCORE.
32	34	35	FSOURCE	POWER Input	FSOURCE input pin for EFUSE. Leave floating for normal operation
33	35	36	VPP	POWER Input	VPP input pin for EFUSE. Leave floating for normal operation
9,29	11, 31, 55	11,20,32,46,57,67	GND	POWER Input	Ground.

Table 3.2 Power and Ground Pins

FT2233HP/FT2232HP					
QFN-68	QFN-76	LQFP-80	Name	Type	Description
27	29	30	OSCI	INPUT	Oscillator input.
28	30	31	OSCO	OUTPUT	Oscillator output.
60	65	68	REF	INPUT	Current reference – connect via a 12K Ohm resistor @ 1% to GND.
58	63	65	DM	I/O	USB Data Signal Minus.
59	64	66	DP	I/O	USB Data Signal Plus.
3	3	3	TEST	INPUT	IC test pin – for normal operation should be connected to GND.
4	4	4	RESET#	INPUT	Reset input (active low).
67	75	79	PWREN#	OUTPUT	Active low power-enable output. PWREN# = 0: Normal operation. PWREN# = 1: USB SUSPEND mode or device has not been configured. This can be used by external circuitry to power down logic when device is in USB suspend or has not been configured.
43	45	47	SUSPEND#	OUTPUT	Active low when USB is in suspend mode.

Table 3.3 Common Function Pins

FT2233HP/FT2232HP					
QFN-68	QFN-76	LQFP-80	Name	Type	Description
68	76	80	EECS*	I/O	EEPROM – Chip Select. Tri-State during device reset.
1	1	1	EECLK*	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
2	2	2	EEDATA*	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset.

Table 3.4 EEPROM Interface Pins

*** Note:** Pull each of pins via separate 10K resistor to VCCIO if no EEPROM uses.

FT2233HP/FT2232HP					
QFN-68	QFN-76	LQFP-80	Name	Type	Description
63	68	71	PD1_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD1. VBUS is required to be divided by 10 before input to this pin.
64	69	73	PD1_VCONN	Power Input	Power input for PD1 VCONN power source. Connect to 3.3V.
65	70	74	PD1_CC1	AI/O	Analog IO pin. PD1 CC1 pin
62	67	70	PD1_CC2	AI/O	Analog IO pin. PD1 CC2 pin
-	72	76	PD2_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD2. VBUS is required to be divided by 10 before input to this pin.
-	71	75	PD2_CC1	AI/O	Analog IO pin. PD2 CC1 pin

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-	73	77	PD2_CC2	AI/O	Analog IO pin. PD2 CC2 pin

Table 3.5 Type-C/PD Port Pins

FT2233HP/FT2232HP					
QFN-68	QFN-76	LQFP-80	Name	Type	Description
56	61	63	GPIO0	I/O	GPIO0 or I2C_SDA pin. Default function is GPIO0 input with weak pull-down.
55	60	62	GPIO1	I/O	GPIO1 or I2C_SCL pin. Default function is GPIO1 input with weak pull-down.
54	59	61	GPIO2	I/O	GPIO2 or I2C_INT# pin. Default function is GPIO2 input with weak pull-down.
5	5	5	GPIO3	I/O	GPIO3 pin. Default function is GPIO3 input with weak pull-down.
-	6	6	GPIO4	I/O	GPIO4 pin. Default function is GPIO4 input with weak pull-down.
-	7	7	GPIO5	I/O	GPIO5 pin. Default function is GPIO5 input with weak pull-down.
-	46	48	GPIO6	I/O	GPIO6 pin. Default function is GPIO6 input with weak pull-down.
-	58	60	GPIO7	I/O	GPIO7 pin. Default function is GPIO7 input with weak pull-down.

Table 3.6 GPIO Pins

3.6 Configured Pins

The following sections describe the function of the configurable pins referred to in Table 3.1. This is determined by how the FT2233HP/FT2232HP is configured.

3.6.1 FT2233HP/FT2232HP pins used in an RS232 Interface

The FT2233HP/FT2232HP channel A or channel B can be configured as an RS232 interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.7.

FT2233HP/FT2232HP								
Channel A Pin No.			Channel B Pin No.			Name	Type	RS232 Configuration Description
QFN-68	QFN-76	LQFP-80	QFN-68	QFN-76	LQFP-80			
6	8	8	34	36	37	TXD	OUTPUT	TXD = transmitter output
7	9	9	35	37	38	RXD	INPUT	RXD = receiver input
11	13	13	36	38	39	RTS#	OUTPUT	RTS# = Ready To send handshake output
12	14	14	37	39	40	CTS#	INPUT	CTS# = Clear To Send handshake input
13	15	15	38	40	41	DTR#	OUTPUT	DTR# = Data Transmit Ready modem signaling line
14	16	16	40	42	43	DSR#	INPUT	DSR# = Data Set Ready modem signaling line
15	17	17	41	43	44	DCD#	INPUT	DCD# = Data Carrier Detect modem signaling line
16	18	18	42	44	45	RI#	INPUT	RI# = Ring Indicator Control Input. When the Remote Wake-Up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (see note 1, 2 and 3)
17	19	19	45	48	50	TXDEN	OUTPUT	TXDEN = (TTL level). For use with RS485 level converters.
20	22	23	48	51	53	RXLED#	OUTPUT	RXLED = Receive signaling output when data is transferred from FT2233HP/FT2232HP to USB Host. Pulses low when receiving data (RXD) via USB. This should be connected to an LED.
21	23	24	49	52	54	TXLED#	OUTPUT	TXLED = Transmit signaling output when data is transferred from USB Host to FT2233HP. Pulses low when transmitting data (TXD) via USB. This should be

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								connected to an LED.

Table 3.7 Channel A & B RS232 Configured Pin Descriptions

3.6.2 FT2233HP/FT2232HP pins used in an FT245 Style Synchronous FIFO Interface

The FT2233HP/FT2232HP only channel A can be configured as a FT245 style synchronous FIFO interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.8. To enter this mode the external EEPROM must be set to make port A 245 mode. A software command (Set Bit Mode option) is then sent by the application to the FTDI driver to tell the chip to enter single channel synchronous FIFO mode. In this mode the 'B' channel is not available as all resources have been switched onto channel A. In this mode, data is written or read on the rising edge of the CLKOUT.

FT2233HP/FT2232HP					
Channel A Pin No.			Name	Type	FT245 Configuration Description
QFN-68	QFN-76	LQFP-80			
6,7,11-16	8,9,13-18	8,9,13-18	ADBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless OE# is low.
17	19	19	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When in synchronous mode, data is transferred on every clock that RXF# and RD# are both low. Note that the OE# pin must be driven low at least 1 clock period before asserting RD# low.
18	20	21	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by driving WR# low. When in synchronous mode, data is transferred on every clock that TXE# and WR# are both low.
19	21	22	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. The next FIFO data byte (if available) is fetched from the receive FIFO buffer each CLKOUT cycle until RD# goes high.
20	22	23	WR#	INPUT	Enables the data byte on the D0...D7 pins to be written into the transmit FIFO buffer when WR# is low. The next FIFO data byte is written to the transmit FIFO buffer each CLKOUT cycle until WR# goes high.
22	24	25	CLKOUT	OUTPUT	60 MHz Clock driven from the chip. All signals should be synchronized to this clock.
23	25	26	OE#	INPUT	Output enable when low to drive data onto D0-7. This should be driven low at least 1 clock period before driving RD# low to allow for data buffer turn-around.
21	23	24	SIWU	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 3.8 Channel A FT245 Style Synchronous FIFO Configured Pin Descriptions

3.6.3 FT2233HP/FT2232HP pins used in an FT245 Style Asynchronous FIFO Interface

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The FT2233H/FT2232HP channel A or channel B can be configured as a FT245 asynchronous FIFO interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.9. To enter this mode the external EEPROM must be set to make port A or B or both 245 mode. In this mode, data is written or read on the falling edge of the RD# or WR# signals.

FT2233HP/FT2232HP								
Channel A Pin No.			Channel B Pin No.			Name	Type	FT245 Configuration Description
QFN-68	QFN-76	LQFP-80	QFN-68	QFN-76	LQFP-80			
6,7,11-16	8,9,13-18	8,9,13-18	34-38,40-42	36-40, 42-44	37-41,43-45	Channel A = ADBUS[7:0] Channel B = BDBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless RD# is low.
17	19	19	45	48	50	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When RD# goes high again RXF# will always go high and only become low again if there is another byte to read. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor.
18	20	21	46	49	51	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR# high, then low. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor.
19	21	21	47	50	52	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes high.
20	22	23	48	51	53	WR#	INPUT	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR# goes from high to low.
21	23	24	49	52	54	SIWU	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. It should be pulled up to high level before strobing low. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 3.9 Channel A & B FT245 Style Asynchronous FIFO Configured Pin Descriptions

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3.6.4 FT2233HP/FT2232HP pins used in a Synchronous or Asynchronous Bit-Bang Interface

The FT2233HP/FT2232HP channel A or channel B can be configured as a synchronous or asynchronous bit-bang interface. Bit-bang mode is a special FTDI FT2233HP/FT2232HP device mode that changes the 8 IO lines on either (or both) channels into an 8 bit bi-directional data bus. There are two types of bit-bang modes: synchronous and asynchronous.

When configured in any bit-bang mode, the pins used and the descriptions of the signals are shown in Table 3.10.

FT2233HP/FT2232HP								
Channel A Pin No.			Channel B Pin No.			Name	Type	Configuration Description
QFN-68	QFN-76	LQFP-80	QFN-68	QFN-76	LQFP-80			
6,7,11-16	8,9,13-18	8,9,13-18	34-38,40-42	36-40, 42-44	37-41,43-45	Channel A = ADBUS[7:0] Channel B = BDBUS[7:0]	I/O	D7 to D0 bidirectional Bit-Bang parallel I/O data pins
18	20	21	46	49	51	WRSTB#	OUTPUT	Write strobe, active low output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).
19	21	22	47	50	52	RDSTB#	OUTPUT	Read strobe, this output rising edge indicates when data has been read from the parallel I/O pins and sent to the Host PC (via the USB interface).
21	23	24	49	52	54	SIWU	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 3.10 Channel A & B Synchronous or Asynchronous Bit-Bang Configured Pin Description

3.6.5 FT2233HP/FT2232HP Pins used as a Fast Serial Interface

The FT2233HP/FT2232HP channel B can be configured for use with high-speed optical bi-directional isolated serial data transfer: Fast Serial Interface. (Not available on channel A). A proprietary FTDI protocol designed to allow galvanic isolated devices to communicate synchronously with the FT2233HP/FT2232HP using just 4 signal wires (over two dual opto-isolators), and two power lines. The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. Maximum USB full speed data rates can be achieved. Both 'A' and 'B' channels can communicate over the same 4 wire interface if desired.

When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.11.

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FT2233HP/FT2232HP					
Channel B Pin No.			Name	Type	Fast Serial Interface Configuration Description
QFN-68	QFN-76	LQFP-80			
34	36	37	FSDI	INPUT	Fast serial data input.
35	37	38	FSCLK	INPUT	Fast serial clock input. Clock input to FT2233HP/FT2232HP chip to clock data in or out.
36	38	39	FSDO	OUTPUT	Fast serial data output.
37	39	40	FSCTS	OUTPUT	Fast serial Clear To Send signal output. Driven low to indicate that the chip is ready to send data

Table 3.11 Channel B Fast Series Interface Configured Pin Descriptions

3.6.6 FT2233HP/FT2232HP Pins Configured as a CPU-style FIFO Interface

The FT2233HP/FT2232HP channel A or channel B can be configured in a CPU-style FIFO interface mode which allows a CPU to interface to USB via the FT2233HP. This mode is enabled in the external EEPROM.

When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.12.

FT2233HP/FT2232HP								
Channel A Pin No.			Channel B Pin No.			Name	Type	Fast Serial Interface Configuration Description
QFN-68	QFN-76	LQFP-80	QFN-68	QFN-76	LQFP-80			
6,7,11-16	8,9,13-18	8,9,13-18	34-38,40-42	36-40, 42-44	37-41,43-45	Channel A = ADBUS[7:0] Channel B = BDBUS[7:0]	I/O	D7 to D0 bidirectional data bus
17	19	19	45	48	50	CS#	INPUT	Active low chip select input
18	20	21	46	49	51	A0	INPUT	Address bit A0
19	21	22	47	50	52	RD#	INPUT	Active Low FIFO Read input
20	22	23	48	51	53	WR#	INPUT	Active Low FIFO Write input

Table 3.12 Channel A & B CPU-style FIFO Interface Configured Pin Descriptions

3.6.7 FT2233HP/FT2232HP pins used in an MPSSE

The FT2233HP/FT2232HP channel A and channel B, each have a Multi-Protocol Synchronous Serial Engine (MPSSE). Each MPSSE can be independently configured to a number of industry standard serial interface protocols such as JTAG, I^2C or SPI, or it can be used to implement a proprietary bus protocol. For example, it is possible to use one of the FT2233HP/FT2232HP's channels (e.g. channel A) to connect to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The other MPSSE channel (e.g. channel B) would be available for another serial interface function. Alternatively each MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.13.

FT2233HP/FT2232HP								
Channel A Pin No.			Channel B Pin No.			Name	Type	MPSSE Configuration Description
QFN-68	QFN-76	LQFP-80	QFN-68	QFN-76	LQFP-80			
6	8	8	34	36	37	TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI – SK, Serial Clock
7	9	9	35	37	38	TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI – DO, serial data output

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11	13	13	36	38	39	TDO/DI	INPUT	Serial Data Input. For example: JTAG – TDO, Test Data output SPI – DI, Serial Data Input
12	14	14	37	39	40	TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI – CS, Serial Chip Select
13	15	15	38	40	41	GPIOL0	I/O	General Purpose input/output
14	16	16	40	42	43	GPIOL1	I/O	General Purpose input/output
15	17	17	41	43	44	GPIOL2	I/O	General Purpose input/output
16	18	18	42	44	45	GPIOL3	I/O	General Purpose input/output

Table 3.13 Channel A & B MPSSE Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.6.

3.6.8 FT2233H/FT2232HP Pins Configured as a Host Bus Emulation Interface

The FT2233HP/FT2232HP can be used to combine channel A and channel B to be configured as a host bus emulation interface mode which emulates a standard 8048 or 8051 MCU host.

When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.14.

FT2233HP/FT2232HP					
Pin No.			Name	Type	Fast Serial Interface Configuration Description
QFN-68	QFN-76	LQFP-80			
6,7,11-16	8,9,13-18	8,9,13-18	ADBUS[7:0]	I/O	Multiplexed bidirectional Address/Data bus AD7 to AD0
17-24	19-26	19, 21-27	A[15:8]	OUTPUT	Extended Address A15 to A8
34	36	37	CS#	OUTPUT	Active low chip select device during Read or Write.
35	37	38	ALE	OUTPUT	Positive pulse to latch the address
36	38	39	RD#	OUTPUT	Active low read output.
37	39	40	WR#	OUTPUT	Active low write output. (Data is setup before WR# goes low, and is held after WR# goes high)
38	40	41	IORDY	INPUT	Extends the time taken to perform a Read or Write operation if driven low. Pull up to VCORE if not being used.
40	42	43	CLKOUT	OUTPUT	Master clock. Outputs the clock signal being used by the configured interface.
41	43	44	I/O0	I/O	MPSSE mode instructions to set / clear or read the high byte of data can be used with this pin. Please refer to Application Note AN_108 for operation of these instructions.
42	44	45	I/O1	I/O	MPSSE mode instructions to set / clear or read the high byte of data can be used with this pin. In addition this pin has instructions which will make the controller wait until it is high, or wait until it is low. This can be used to connect to an IRQ pin of a peripheral chip. The FT2233HP/FT2232HP will wait for the interrupt, and then read the device, and pass the answer back to the host PC. I/O1 must be held in input mode if this option is used. Please refer to Application Note AN_108 for operation of these instructions.

Table 3.14 Channel A & B Host Bus Emulation Interface Configured Pin Descriptions

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4 Function Description

The FT2233HP/FT2232HP are a USB 2.0 High Speed (480Mb/s) to UART/MPSSE IC with USB Type-C/PD ports. It has the capability of being configured in a variety of industry standard serial interfaces.

The FT2233HP/FT2232HP have two independent configurable interfaces. Both interfaces can be configured as UART, bit-bang mode or JTAG, SPI, I^2C mode, using the MPSSE, with independent baud rate generators..

The FT2233HP has two Type-C/PD ports (FT2233HPQ and FT2233HPL only), with PD1 port supporting both power sink and source roles, and PD2 port works as a power sink port. Both PD ports support 5V3A, 9V3A, 12V3A, 15V3A and 20V3A PDO profiles, and these profiles are configurable through the external EEPROM at power-up or reset. PD1 port share the same Type-C connector with USB data, and PD2 port is power port only without USB data.

4.1 Key Features

USB Type-C/PD Controller. The FT2233HP has 2 USB Type-C and PD port controllers (FT2233HPQ and FT2233HPL only), one port is with the legacy USB 2.0 port to form USB PD port, and the other port is standalone PD port it is used to connect to PD power source. Power Delivery function is designed to meet PD2.0/3.0 specification.

USB High Speed to Dual Interface. The FT2233HP/FT2232HP are a USB 2.0 High Speed (480Mbits/s) to dual independent flexible/configurable serial interfaces. This function is backward compatible to FT2232H.

Functional Integration. The FT2233HP/FT2232HP integrate a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 High Speed interface. The FT2233HP includes an integrated +1.2V Low Drop-Out (LDO) regulator and 12MHz to 480MHz PLL. It also includes 2kbytes Tx and Rx data buffers per channel. The FT2233HP effectively integrates the entire USB protocol on a chip.

MPSSE. Multi-Purpose Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

Data Transfer Rate. The FT2233HP/FT2232HP support a data transfer rate up to 12 Mbit/s when configured as an RS232/RS422/RS485 UART interface. Please note the FT2233HP/FT2232HP do not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

Latency Timer. This is really a feature of the driver and is used to as a timeout to flush short packets of data back to the PC. The default is 16ms, but it can be altered between 2ms and 255ms. At 2ms latency you get a packet transfer on every high speed micro frame. Lower values may reduce latency but may also increase USB bandwidth usage and reduce efficiency.

4.2 Functional Block Descriptions

Type-C/PD PHY and Controller. The FT2233HP has two Type-C/PD ports. Each port has Type-C/PD required Physical Layer (PHY) and controllers. PD1 port has built-in VCONN switches supporting up to 100mW VCONN power (FT2233HPQ and FT2233HPL only).

PD Policy Engine. The PD policy engine is a 32bit RISC processor with 8kB data RAM and 48kB ROM. It manages both PD port 1 and port 2(FT2233HPQ and FT2233HPL only). Default PD configurations are stored in the ROM code. PD1 port can act as power sink or source role, supporting both normal power role swap protocols. PD2 port acts as power sink, which can be connected to a PD charger. By using an external EEPROM, it is possible to change the PD configuration based on specific use cases, such as port 1 sink, port 1 sink/source or PD charge through from port 2 to port 1. PDO voltage/current profiles can also be customised using EEPROM.

I2C Slave Interface. The application can also choose to control the PD policy by external MCU through I2C interface. In this case the built-in PD policy engine is halted. The external MCU has full control to the two PD controller registers (FT2233HPQ and FT2233HPL only) through I2C access. An interrupt signal is also provided, so that an interrupt to an external MCU could be asserted when a PD event occurs.

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GPIO block. The GPIO block provides up to 8 GPIO pins which can be used as power switch controls based on the PD policy and profiles.

Dual Multi-Purpose UART/MPSSE Controllers. The FT2233HP/FT2232HP have two independent UART/MPSSE Controllers. These blocks control the UART data or control the Bit-Bang mode if selected by the FT_SetBitMode command. Both can be used independently of each other and the remaining UART channels. Using this, the device can be configured under software command to have 1 MPSSE + 1 UARTS (each UART can be set to Bit Bang mode to gain extra I/O if required).

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Dual Port FIFO TX Buffer (2Kbytes per channel). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Dual Port FIFO RX Buffer (2Kbytes per channel). Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT2233HP/FT2232HP. RESET# should be tied to VCCIO (+3.3v) if not being used.

Independent Baud Rate Generators - The Baud Rate Generators provide an x16 or an x10 clock input to the UART's from a 120MHz reference clock and consist of a 14 bit pre-scaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 million baud. The FT2233HP/FT2232HP do not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

See FTDI application note AN_120 for more details.

LDO Regulator. The +1.2V LDO regulator generates the +1.2 volts for the core and the USB transceiver cell. Its input (VREGIN) must be connected to a +3.3V external power source. It is also recommended to add an external filtering capacitor to the VREGIN. There is no direct connection from the +1.2V output (VREGOUT) and the internal functions of the FT2233HP/FT2232HP. The PCB must be routed to connect VREGOUT to VCORE, the pins that require the +1.2V including VREGIN. This output should not be used to power other circuits apart from VCORE.

USB HS PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / High Speed SERDES (serialise – de-serialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal should be connected to the OSCI and OSCO pins. A 12K Ohm resistor should be connected between REF and GND on the PCB.

EEPROM Interface. EEPROM is optional. When used without an external EEPROM the FT2233HP/FT2232HP default to a dual USB to an asynchronous serial port device with default profiles on 2 Type-C/PD ports (FT2233HPQ and FT2233HPL only). Adding an external 93LC66 EEPROM allows customization of USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT2233HP/FT2232HP for OEM applications, as well as PD port configurations and power profiles. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM must have a 16 bit wide configuration such as a Microchip 93LC66B or equivalent capable of a 1Mbit/s clock rate at VCC = 3.0V to 3.6V. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site - www.ftdichip.com. This allows a blank EEPROM device to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT2233HP/FT2232HP will default to serial ports. The device uses its built-in default VID (0403), PID (6040), Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

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4.3 FT232 UART Interface Mode Description

The FT2233HP/FT2232HP can be configured in similar UART modes as the FTDI FT232 devices (an asynchronous serial interface). The following examples illustrate how to configure the FT2233HP/FT2232HP with an RS232, RS422 or RS485 interfaces. The FT2233HP/FT2232HP can be configured as a mixture of these interfaces.

4.3.1 RS232 Configuration

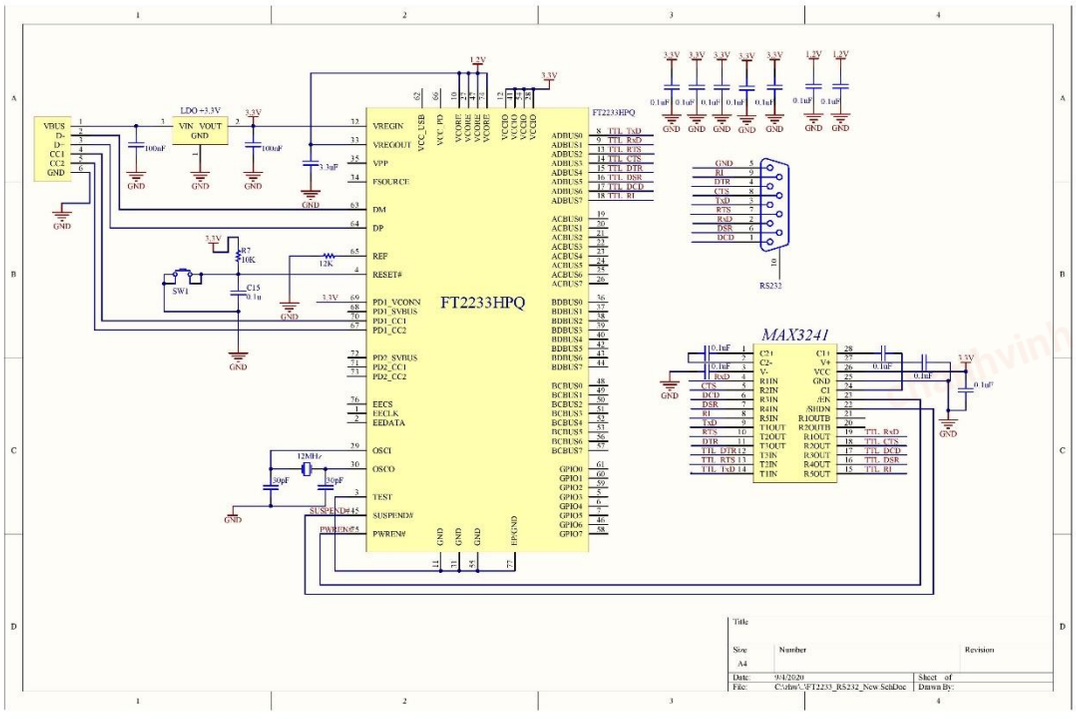


Figure 4.1 Single RS232 Configurations

Figure 4.2 illustrates how the FT2233HP/FT2232HP channel A can be configured with an RS232 UART interface. This can be repeated for channels B to provide a quad RS232, but has been omitted for clarity.

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4.3.2 RS422 Configuration

Figure 4.3 illustrates how the FT2233HP/FT2232HP can be configured as a dual RS422 interface. The FT2233HP/FT2232HP can have all 2 channels connected as RS422.

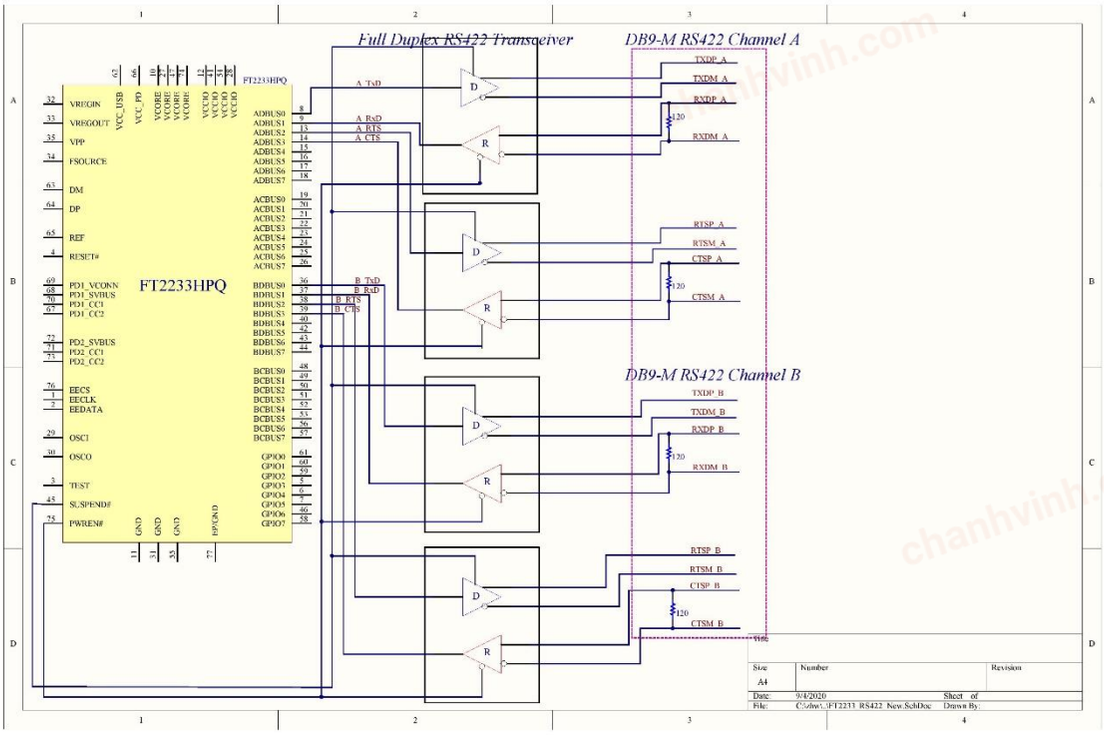


Figure 4.3 Dual RS422 Configurations

In this case both channel A and channel B are configured as UART operating at TTL levels and a level converter device (full duplex RS422 transceiver) is used to convert the TTL level signals from the FT2233HP/FT2232HP to RS422 levels. The PWREN# signal is used to power down the level shifters such that they operate in a low quiescent current when the USB interface is in suspend mode.

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4.3.3 RS485 Configuration

Figure 4.4 illustrates how the FT2233HP/FT2232HP can be configured as a dual RS485 interface. The FT2233HP/FT2232HP can have all 2 channels connected as RS485.

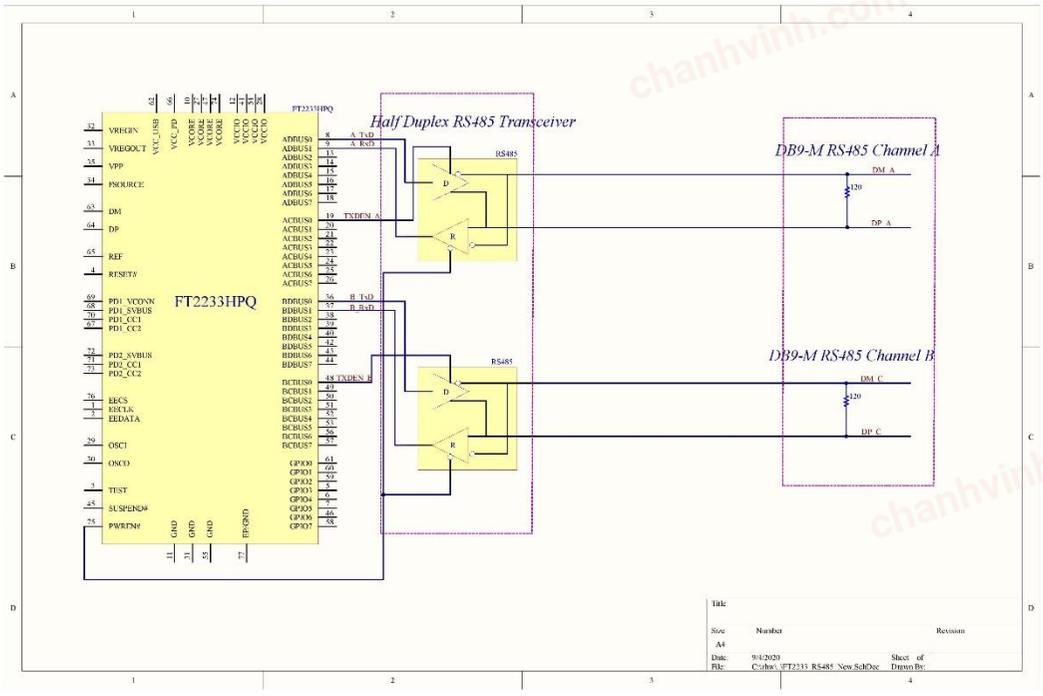


Figure 4.4 Dual RS485 Configurations

In this case both channel A and channel B are configured as RS485 operating at TTL levels and a level converter device (half duplex RS485 transceiver) is used to convert the TTL level signals from the FT232H to RS485 levels. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pins on the FT2233HP/FT2232HP are provided for exactly that purpose, and so the transmitter enables are wired to the TXDEN"s. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode.

RS485 is a multi-drop network – i.e. many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable. Links are provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

In this example the data transmitted by the FT2233HP/FT2232HP are also received by the device that is transmitting. This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT2233HP/FT2232HP it is possible to do this entirely in hardware – simply modify the schematic so that RXD of the FT2233HP/FT2232HP is the logical OR of the level converter device receiver output with TXDEN using an HC32 or similar logic gate.

4.4 FT245 Synchronous FIFO Interface Mode Description

When channel A is configured in an FT245 Synchronous FIFO interface mode the IO timing of the signals used are shown in **Error! Reference source not found.**, which shows details for read and write accesses. The timings are shown in Table 4.1.

Note: that only a read or a write cycle can be performed at any one time. Data is read or written on the rising edge of the CLKOUT clock.

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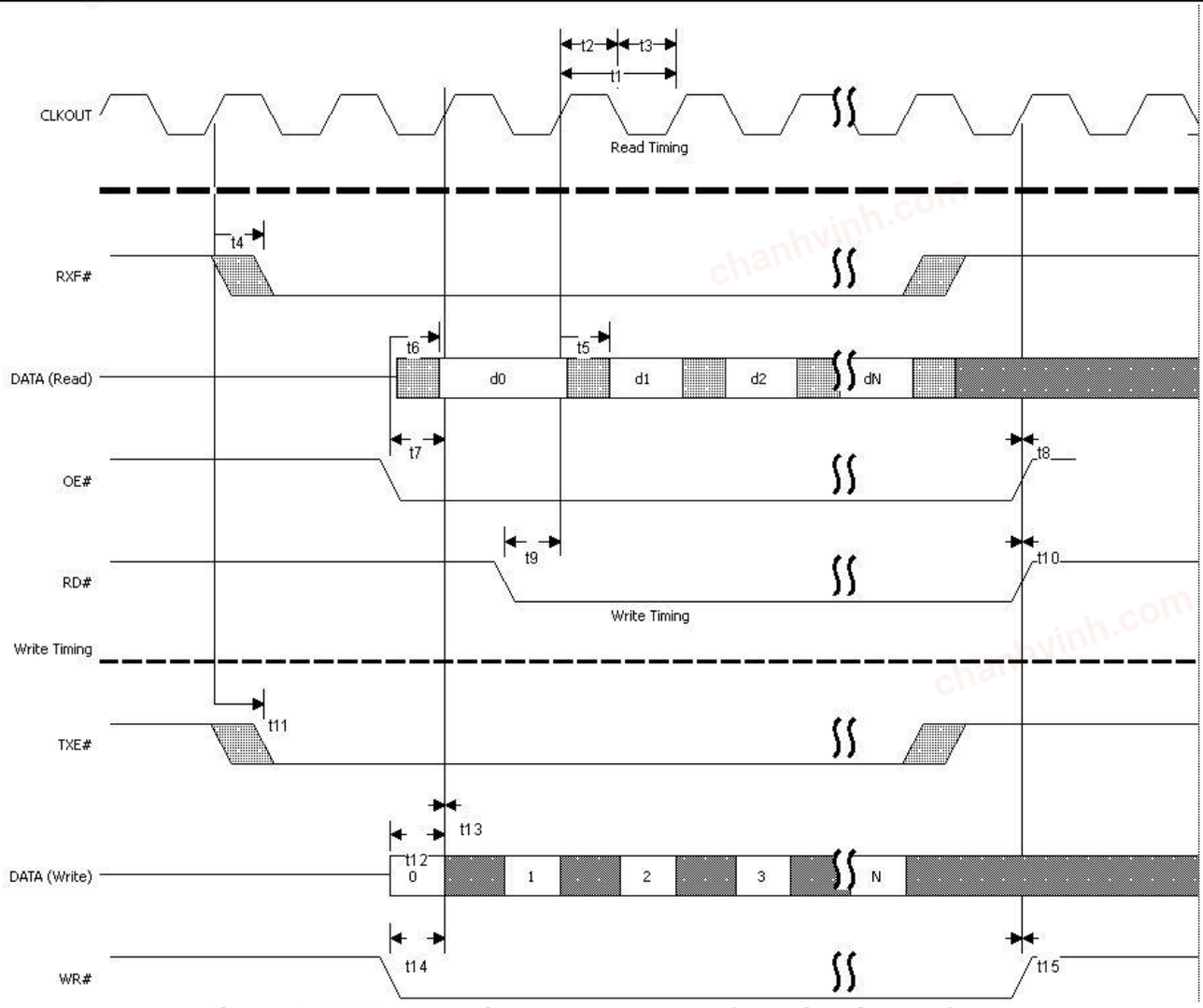


Figure 4.5 FT245 Synchronous FIFO Interface Signal Waveforms

Name	Minimum	Typical	Maximum	Units	Description
t1		16.67		ns	CLKOUT period
t2		8.33		ns	CLKOUT high period
t3		8.33		ns	CLKOUT low period
t4	1		7.15	ns	CLKOUT to RXF#
t5	1		11	ns	CLKOUT to read DATA valid
t6	1		10	ns	OE# to read DATA valid
t7	8		16.67	ns	OE# setup time
T8	0			ns	OE# hold time
T9	8		16.67	ns	RD# setup time to CLKOUT (RD# low after OE# low)
T10	0			ns	RD# hold time
t11	1		7.15	ns	CLKOUT TO TXE#
t12	9		16.67	ns	Write DATA setup time
t13	0			ns	Write DATA hold time
t14	9		16.67	ns	WR# setup time to CLKOUT (WR# low after TXE# low)
t15	0			ns	WR# hold time

Table 4.1 FT245 Synchronous FIFO Interface Signal Timings

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Note: These timing numbers are preliminary and subject to change.

This single channel mode uses a synchronous interface to get high data transfer speeds. The chip drives a 60 MHz CLKOUT clock for the external system to use.

Note that Asynchronous FIFO mode must be selected on both channels before selecting the Synchronous FIFO mode in software.

4.4.1 FT245 Synchronous FIFO Read Operation

A read operation is started when the chip drives RXF# low. The external system can then drive OE# low to turn around the data bus drivers before acknowledging the data with the RD# signal going low. The first data byte is on the bus after OE# is low. The external system can burst the data out of the chip by keeping RD# low or it can insert wait states in the RD# signal. If there is more data to be read it will change on the clock following RD# sampled low. Once all the data has been consumed, the chip will drive RXF# high. Any data that appears on the data bus, after RXF# is high, is invalid and should be ignored.

4.4.2 FT245 Synchronous FIFO Write Operation

A write operation can be started when TXE# is low. WR# is brought low when the data is valid. A burst operation can be done on every clock providing TXE# is still low. The external system must monitor TXE# and its own WR# for each byte of data to check that data has been accepted. Both TXE# and WR# must be low for data to be accepted.

4.5 FT245 Asynchronous FIFO Interface Mode Description

The FT2233HP/FT2232HP can be configured as a dual channel asynchronous FIFO interface. This mode is similar to the synchronous FIFO interface with the exception that the data is written to or read from the FIFO on the falling edge of the WR# or RD# signals.

This mode does not provide a CLKOUT signal and it does not expect an OE# input signal. The following diagrams illustrate the asynchronous FIFO mode timing.

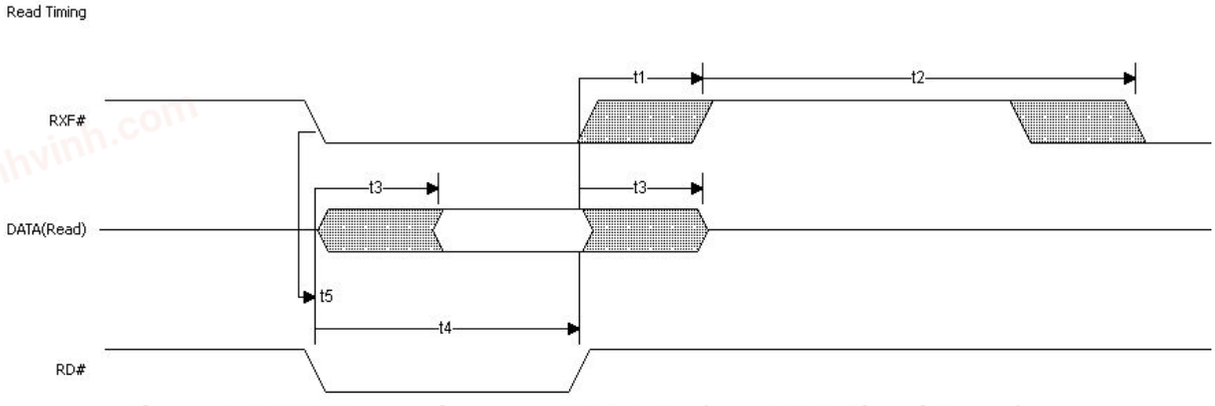


Figure 4.6 FT245 asynchronous FIFO Interface READ Signal Waveforms

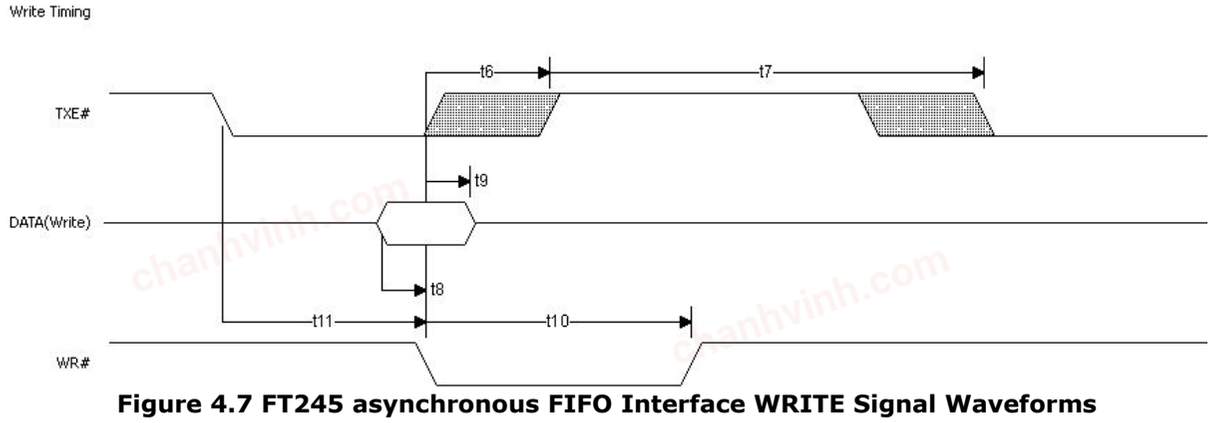


Figure 4.7 FT245 asynchronous FIFO Interface WRITE Signal Waveforms

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Name	Minimum	Typical	Maximum	Units	Description
t1	1		14	ns	RD# inactive to RX#
t2	49			ns	RXF# inactive after RD# cycle
t3	1		14	ns	RD# to DATA
t4	30			ns	RD# active pulse width
t5	0			ns	RD# active after RXF#
t6	1		14	ns	WR# active to TXE# inactive
t7	49			ns	TXE# inactive after WR# cycle
t8	5			ns	DATA to WR# active setup time
t9	5			ns	DATA hold time after WR# inactive
t10	30			ns	WR# active pulse width
t11	0			ns	WR# active after TXE#

Table 4.2 Asynchronous FIFO Timings (based on standard drive level outputs)

Note: These timing numbers are preliminary and subject to change.

4.6 MPSSE Interface Mode Description

MPSSE Mode is designed to allow the FT2233HP/FT2232HP to interface efficiently with synchronous serial protocols such as JTAG, I2C and SPI Bus. It can also be used to program SRAM based FPGA's over USB. The MPSSE interface is designed to be flexible so that it can be configured to allow any synchronous serial protocol (industry standard or proprietary) to be implemented using the FT2233HP/FT2232HP. MPSSE is only available on channel A and channel B.

MPSSE is fully configurable, and is programmed by sending commands down the data stream. These can be sent individually or more efficiently in packets. MPSSE is capable of a maximum sustained data rate of 30 Mbits/s.

When a channel is configured in MPSSE mode, the IO timing and signals used are shown in Figure 4.8 and Table 4.3 MPSSE Signal Timings

Note: These timing numbers are preliminary and subject to change.

. These show timings for CLKOUT=30MHz. CLKOUT can be divided internally to be provide a slower clock.

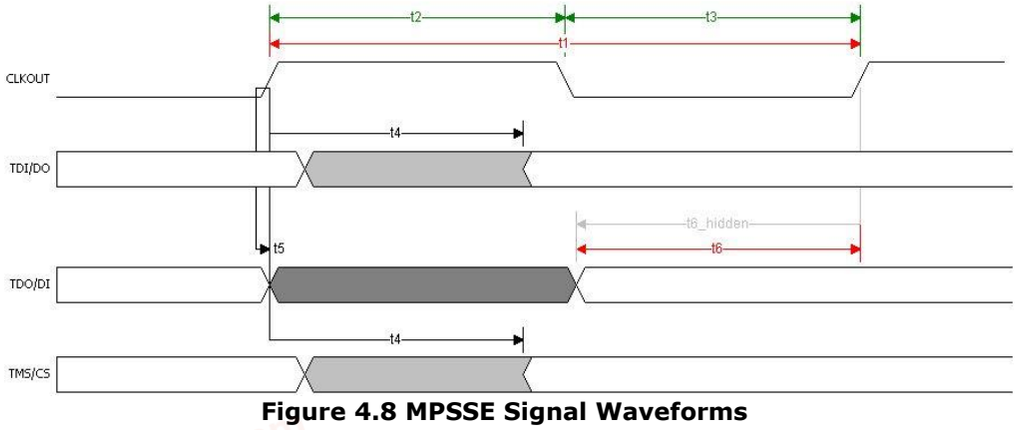


Figure 4.8 MPSSE Signal Waveforms

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NAME	MIN	NOM	MAX	Units	COMMENT
t1		33.33		ns	CLKOUT period
t2	15	16.67		ns	CLKOUT high period
t3	15	16.67		ns	CLKOUT low period
t4	1		7.15	ns	CLKOUT to TDI/DO delay
t5	0			ns	TDO/DI hold time
t6	11			ns	TDO/DI setup time

Table 4.3 MPSSE Signal Timings

Note: These timing numbers are preliminary and subject to change.

MPSSE mode is enabled using FT_SetBitMode driver command. A hex value of 2 will enable it, and a hex value of 0 will reset the device. See application note AN2232-02, "Bit Mode Functions for the FT2232" for more details and examples.

The MPSSE command set is fully described in application note AN_108 – "Command Processor for MPSSE and MCU Host Bus Emulation Modes".

The following additional application notes are available for configuring the MPSSE:

- AN_109 – "Programming Guide for High Speed LibMPSSEI2C DLL"
- AN_110 – "Programming Guide for High Speed LibMPSSEJTAG DLL"
- AN_111 – "Programming Guide for High Speed LibMPSSESPI DLL"

4.6.1 MPSSE Adaptive Clocking

Adaptive clocking is a new MPSSE feature added to the FT2233HP/FT2232HP MPSSE engine.

The mode is effectively handshaking the CLK signal with a return clock RTCK. This is a technique used by ARM processors.

The FT2233HP/FT2232HP will assert the CLK line and wait for the RTCK to be returned from the target device to GPIOL3 line before changing the TDO (data out line).

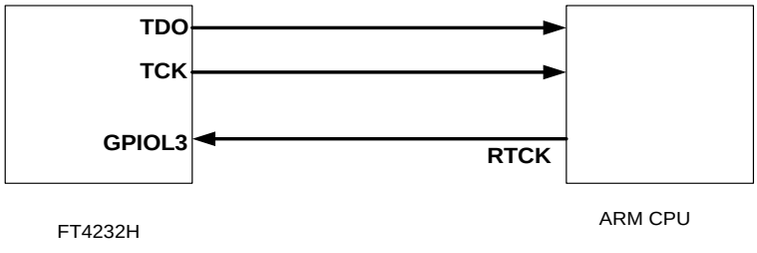
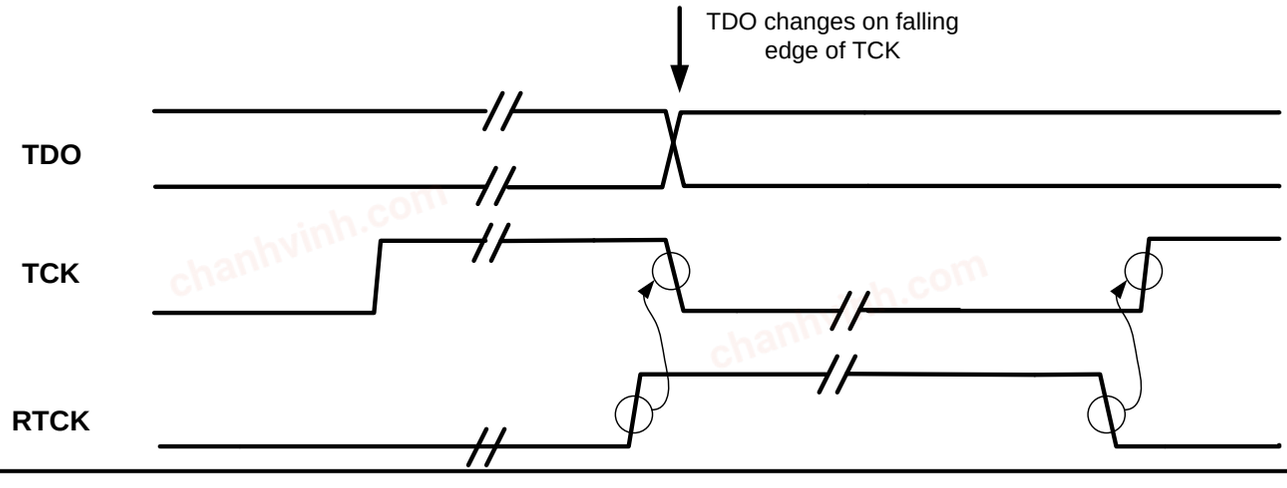


Figure 4.9 Adaptive Clocking Interconnect



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Figure 4.10 Adaptive Clocking Waveform

Adaptive clocking is not enabled by default.

See: AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes.

4.7 MCU Host Bus Emulation Mode

MCU host bus emulation mode uses both of the FT2233HP/FT2232HP's A and B channel interfaces to make the chip emulate a standard 8048/8051 MCU host bus. This allows peripheral devices for these MCU families to be directly connected to USB via the FT2233HP/FT2232HP.

The lower 8 bits (AD7 to AD0) is a multiplexed Address / Data bus. A15 to A8 provide upper (extended) addresses. There are 4 basic operations:-

1) Read (does not change A15 to A8)
2) Read Extended (changes A15 to A8)
3) Write (does not change A15 to A8)
4) Write Extended (changes A15 to A8)

MCU Host Bus Emulation mode is enabled using FT_SetBitMode driver command. A hex value of 8 will enable it, and a hex value of 0 will reset the device. The FT2233HP/FT2232HP operates in the same way as the FT2232D. See application note AN2232-02, "Bit Mode Functions for the FT2232D" for more details and examples.

The MCU Host Bus Emulation Mode command set is fully described in application note AN_108 – "Command Processor for MPSSE and MCU Host Bus Emulation Modes".

When MCU Host Bus Emulation mode is enabled the IO signal lines on both channels work together and the pins are configured. The following sections give some details of the read and write cycle waveforms and timings. The CLKOUT output clock can operate up to 60MHz.

In Host Bus Emulation mode the clock divisor has no effect. The clock divisor is used for serial data and is a different part of the MPSSE block. In host bus emulation the 60MHz clock is always output and doesn't change with any commands.

4.7.1 MCU HOST Bust Emulation Mode Signal Timing – Write Cycle

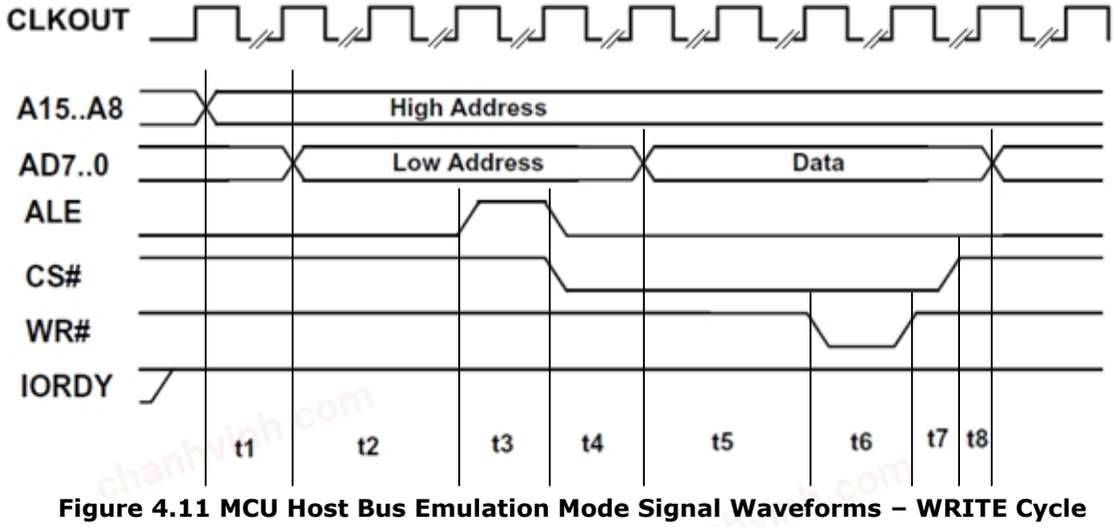


Figure 4.11 MCU Host Bus Emulation Mode Signal Waveforms – WRITE Cycle

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	Number of clock cycles For Write				
Div By 5	On		Off		
IORDY	Low	High	Low	High	
t1	6	6	2	2	A15-8 to AD7-0
t2	3	3	1	1	AD7-0 to ALE
t3	10	5	2	1	ALE width
t4	2	2	2	2	ALE to Address not Valid
t5	13	3	1	1	AD7-0 Data Valid to WRn
t6	10	5	6	1	WRn width
t7	1	1	1	1	WRn inactive to CSn inactive
t8	1	1	1	1	CSn inactive to AD7-0 not valid

Table 4.4 MCU Host Bus Emulation Mode Signal Timings – WRITE Cycle

When Div By 5 is on the device will return 2 bytes (the same value) when doing a read. When it is off the device will return 1 byte when doing a read. The clock period is 16.67 nS so most devices would need the Div By 5 to be set on. IORDY can be held low permanently to extend all cycles.

4.7.2 MCU Host Bus Emulation Mode Signal Timing – Read Cycle

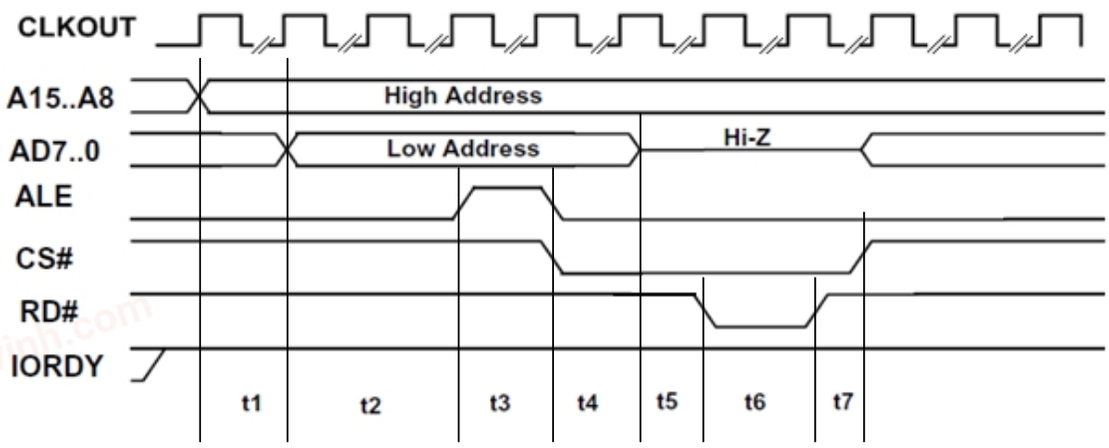


Figure 4.12 MCU Host Bus Emulation Mode Signal Waveforms – READ cycle

	Number of clock cycles For Read				
Div By 5	On		Off		
IORDY	Low	High	Low	High	
t1	6	6	2	2	A15-8 to AD7-0
t2	3	3	1	1	AD7-0 to ALE
t3	10	5	2	1	ALE width
t4	2	5	2	1	ALE to Address not Valid
t5	13	0	1	0	Address not Valid to RDn active
t6	10	10	6	2	RDn active
t7	1	1	1	1	RDn inactive to CSn inactive

Table 4.5 MCU Host Bus Emulation Mode Signal Timings– READ cycle

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When Div By 5 is on the device will return 2 bytes when doing a read. When it is off the device will return 1 byte when doing a read. The clock period is 16.67 nS so most devices would need the Div By 5 to be set on. IORDY can be held low permanently to extend all cycles.

An example of the MCU Host Emulation Interface enabling a USB interface to CAN Bus using a CANBus Controller is shown in the figure.

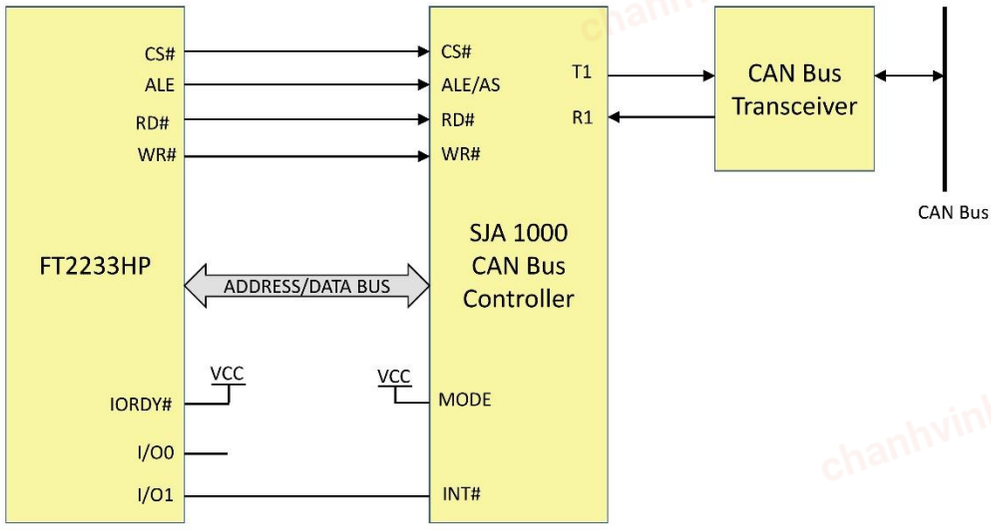


Figure 4.13 MCU Host Emulation Example using a CANBus Controller

4.8 Fast Opto-Isolated Serial Interface Mode Description

Fast Opto-Isolated Serial Interface Mode provides a method of communicating with an external device over USB using 4 wires that can have opto-isolators in their path, thus providing galvanic isolation between systems. If either channel A or channel B is enabled in Fast Opto-Isolated Serial mode then the pins on channel B are switched to the fast serial interface configuration. The I/O interface for fast serial mode is always on channel B, even if both channels are being used in this mode. An address bit is used to determine the source or destination channel of the data. It therefore makes sense to always use at least channel B or both for fast serial mode, but not A own its own.

Fast serial mode is enabled by setting the appropriate bits in the external EEPROM. The fast serial mode can be held in reset by setting a bit value of 10 using the Set Bit Bang Mode command. While this bit is set the device is held reset – data can be sent to the device, but it will not be sent out by the device until the device is enabled again. This is done by sending a bit value of 0 using the set bit mode command. See application note AN2232L-02, "Bit Mode Functions for the FT2232D for more details and examples.

When either Channel B or both Channel A and B are configured in Fast Opto-Isolated Serial Interface mode the IO timing of the signals used are shown in the figure given below. The timings are shown in Table 4.6.

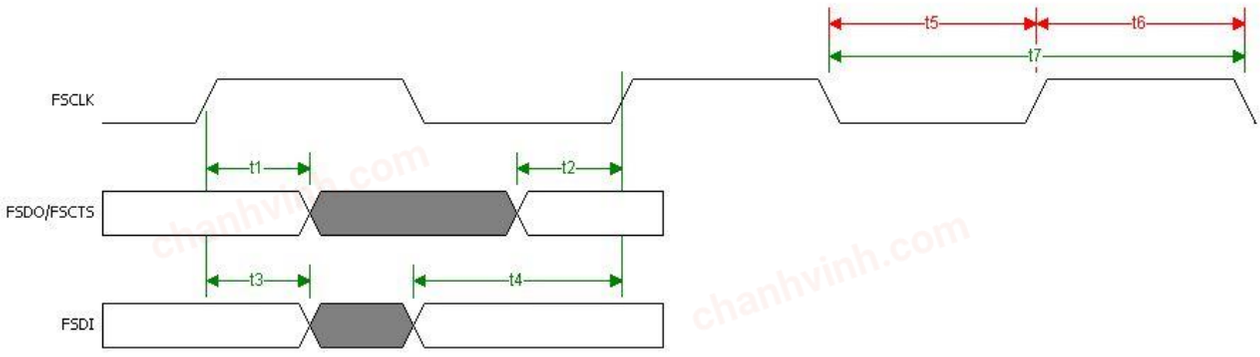


Figure 4.14 Fast Opto-Isolated Serial Interface Signal Waveforms

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Name	Minimum	Typical	Maximu	Units	Description
t1	1			ns	FSDO/FSCTS hold time
t2	5			ns	FSDO/FSCTS setup time
t3	5			ns	FSDI hold time
t4	10			ns	FSDI Setup Time
t5		8.33		ns	FSCLK low
t6		8.33		ns	FSCLK high
t7		16.67		ns	FSCLK Period

Table 4.6 Fast Opto-Isolated Serial Interface Signal Timings

Note: These timing numbers are preliminary and subject to change.

4.8.1 Outgoing Fast Serial Data

To send fast serial data out of the FT2233HP/FT2232HP, the external device must drive the FSCLK clock. If the FT2233HP/FT2232HP have data ready to send, it will drive FSDO output low to indicate the start bit. It will not do this if it is currently receiving data from the external device. This is illustrated in the figure given below -.

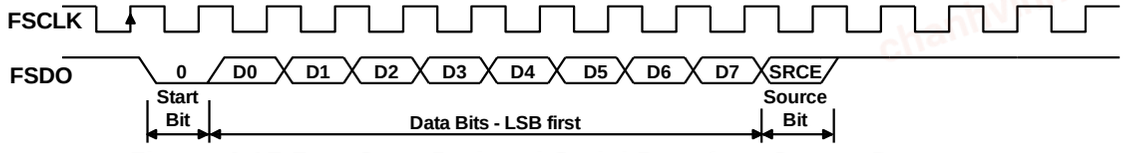


Figure 4.15 Fast Opto-Isolated Serial Interface Output Data

Notes:

1. The first bit output (Start bit) is always 0.
2. FSDO is always sent LSB first.
3. The last serial bit output is the source bit (SRCE). It indicates which channel the data has come from. A '0' means that it has come from Channel A, a '1' means that it has come from Channel B.
4. If the target device is unable to accept the data when it detects the START bit, it should stop the FSCLK until it can accept the data.

4.8.2 Incoming Fast Serial Data

An external device is allowed to send data into the FT2233HP/FT2232HP if FSCTS is high. On receipt of a zero START bit on FSDI, the FT2233HP/FT2232HP will drop FSCTS on the next positive clock edge. The data from bits 0 to 7 are then clocked in (LSB first). The last bit (DEST) determines where the data will be written to. The data can be sent to either channel A or to channel B. If DEST= '0', the data is sent to channel A, (assuming channel A is enabled for fast serial mode, otherwise the data is sent to channel B). If DEST= '1' the data is sent to channel B, (assuming channel B is enabled for fast serial mode, otherwise the data will go to channel A. (Either channel A, channel B or both channels must be enabled as fast serial mode or the function is disabled). This is illustrated in the figure given below -

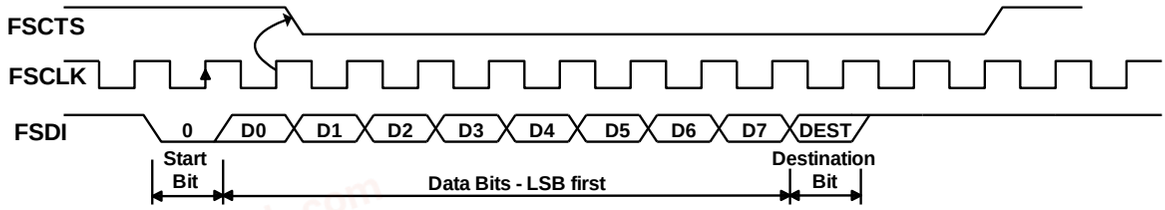


Figure 4.16 Fast Opto-Isolated Serial Interface Input Data

Notes:

1. The first bit input (Start bit) is always 0.
2. FSDI is always received LSB first.
3. The last received serial bit is the destination bit (DEST).It indicates which channel the data should go to. A '0' means that it should go to channel A, a '1' means that it should go to channel B.

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4. The target device should ensure that CTS is high before it sends data. CTS goes low after data bit 0 (D0) and stays low until the chip can accept more data.

4.8.3 Fast Opto-Isolated Serial Data Interface Example

The following example, (figure given below) shows two Agilent HCPL-2430 (see the semiconductor section at www.agilent.com high speed opto-couplers used to optically isolate an external device which interfaced to USB using the FT2233HP/FT2232HP. In this example VCC5V is the USB VBUS supply and VCCE is the supply to the external device.

Care must be taken with the voltage used to power the photo-LED's. It must be the same voltage as that the FT2233HP/FT2232HP I/Os are driving to, or the LED's may be permanently on. Limiting resistors should be fitted in the lines that drive the diodes. The outputs of the opto-couplers are open-collector and require a pull-up resistor.

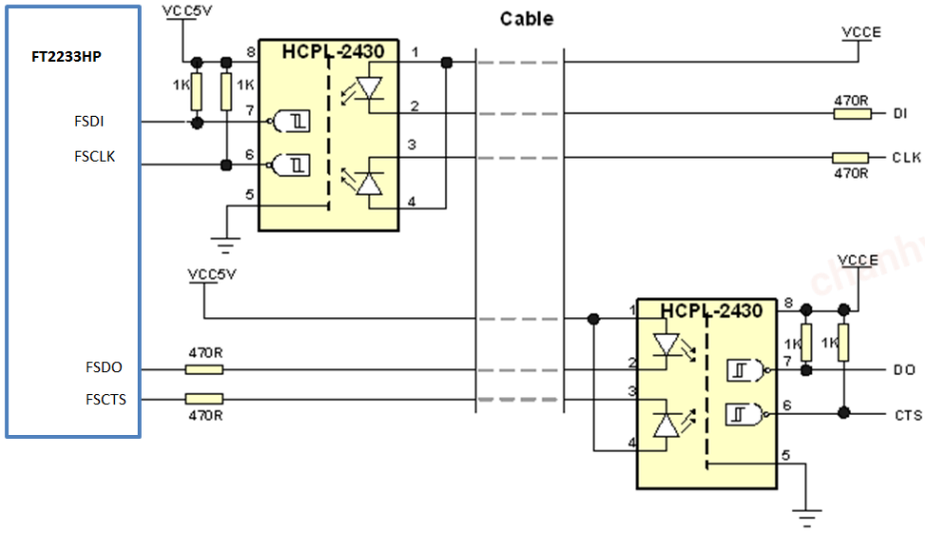


Figure 4.17 Fast Opto-Isolated Serial Interface Example

4.9 CPU-Style FIFO Interface Mode Description

CPU-style FIFO interface mode is designed to allow a CPU to interface to USB via the FT2233HP/FT2232HP. This mode is enabled in the external EEPROM. The interface is achieved using a chip select bit (CS#) and address bit (A0). When either Channel A or Channel B are in CPU-style Interface mode the IO signal lines are configured as given in Table 3.12.

This mode uses a combination of CS# and A0 to determine the operation to be carried out. The following truth-table, Table 4.7, gives the decode values for particular operations.

CS#	A0	RD#	WR#
1	X	X	X
0	0	Read Data Pipe	Write Data Pipe
0	1	Read Status	Send Immediate

Table 4.7 CPU-Style FIFO Interface Operation Select

The Status read is shown in Table 4.8 -

Data Bit	Data	Status
bit 0	1	Data available (=RXF)
bit 1	1	Space available (=TXE)
bit 2	1	Suspend
bit 3	1	Configured
bit 4	X	X
bit 5	X	X
bit 6	X	X
bit 7	X	X

Table 4.8 CPU-Style FIFO Interface Operation Read Status Description

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Note that bits 7 to 4 can be arbitrary values and that X= not used.

The timing of reading and writing in this mode is shown in the figure given below and Table 4.9.

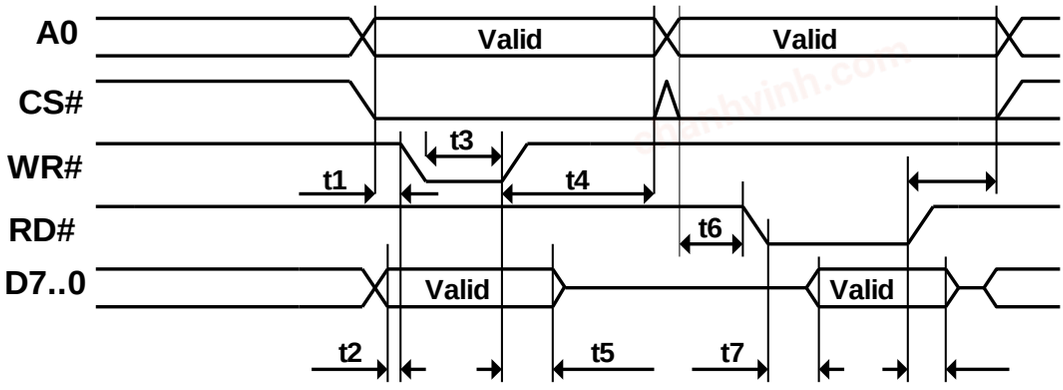


Figure 4.18 CPU-Style FIFO Interface Operation Signal Waveforms

Name	Minimum	Typical	Maximum	Units	Description
t1	15			ns	A0 / CS Setup to WR#
t2	15			ns	Data setup to WR#
t3	20			ns	WR# Pulse width
t4	5			ns	A0/CS Hold from WR#
t5	5			ns	Data hold from WR#
t6	15			ns	A0/CS Setup to RD#
t7	15		50	ns	Data delay from RD#
t8	5			ns	A0/CS hold from RD#
t9	0		30	ns	Data hold time from RD#

Table 4.9 CPU-Style FIFO Interface Operation Signal Timing

Note: These timing numbers are preliminary and subject to change.

An example of the CPU-style FIFO interface connection is shown in the figure given below -

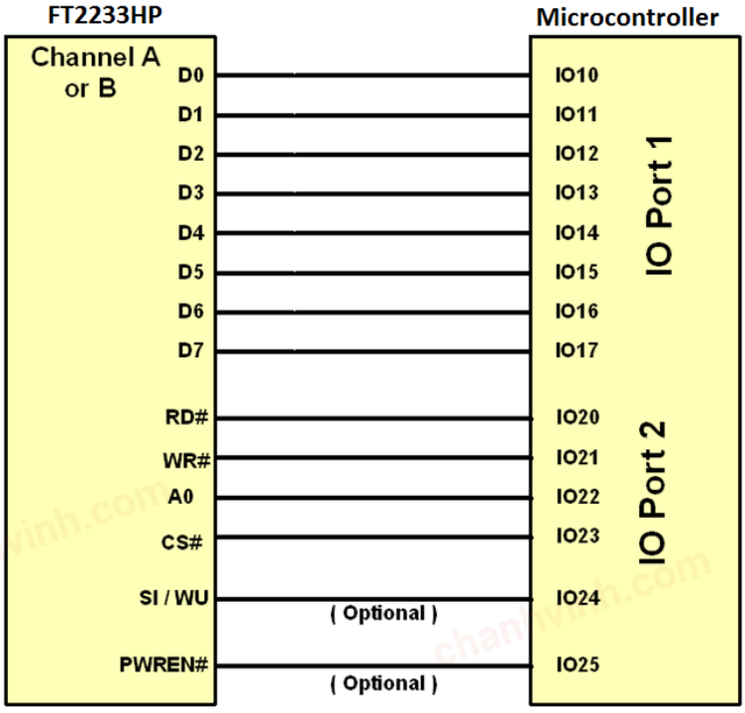


Figure 4.19 CPU-Style FIFO Interface Example

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4.10 Synchrnous\Asynchronous Bit-Bang Interface Mode Desc.

The FT2233HP/FT2232HP channel A or channel B can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous.

4.10.1 Asynchronous Bit-Bang Mode

Asynchronous Bit-Bang mode is the same as BM-style Bit-Bang mode, except that the internal RD# and WR# strobes (RDSTB# and WRSTB#) are now brought out of the device to allow external logic to be clocked by accesses to the bit-bang IO bus.

On either or both channels any data written to the device in the normal manner will be self-clocked onto the data pins (those which have been configured as outputs). Each pin can be independently set as an input or an output. The rate that the data is clocked out at is controlled by the baud rate generator.

For the data to change there has to be new data written, and the baud rate clock has to tick. If no new data is written to the channel, the pins will hold the last value written.

4.10.2 Synchronous Bit-Bang Mode

The synchronous Bit-Bang mode will only update the output parallel port pins whenever data is sent from the USB interface to the parallel interface. When this is done, the WRSTB# will activate to indicate that the data has been read from the USB Rx FIFO buffer and written out on the pins. Data can only be received from the parallel pins (to the USB Tx FIFO interface) when the parallel interface has been written to.

With Synchronous Bit-Bang mode data will only be sent out by the FT2233HP/FT2232HP if there is space in the FT2233HP/FT2232HP USB TXFIFO for data to be read from the parallel interface pins. This Synchronous Bit-Bang mode will read the data bus parallel I/O pins first, before it transmits data from the USB RxFIFO. It is therefore 1 byte behind the output, and so to read the inputs for the byte that you have just sent, another byte must be sent.

For example:

(1) Pins start at 0xFF
Send 0x55,0xAA
Pins go to 0x55 and then to 0xAA
Data read = 0xFF,0x55

(2) Pins start at 0xFF
Send 0x55,0xAA,0xAA
(repeat the last byte sent)
Pins go to 0x55 and then to 0xAA
Data read = 0xFF,0x55,0xAA

Synchronous Bit-Bang Mode differs from Asynchronous Bit-Bang mode in that the device parallel output is only read when the parallel output is written to by the USB interface. This makes it easier for the controlling program to measure the response to a USB output stimulus as the data returned to the USB interface is synchronous to the output data.

Asynchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 1 will enable Asynchronous Bit-Bang mode.

Synchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 4 will enable Synchronous Bit-Bang mode.

See application note AN2232-02, "Bit Mode Functions for the FT2232 for more details and examples of using the bit-bang modes.

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An example of the synchronous bi-bang mode timing is shown in the figure given below -

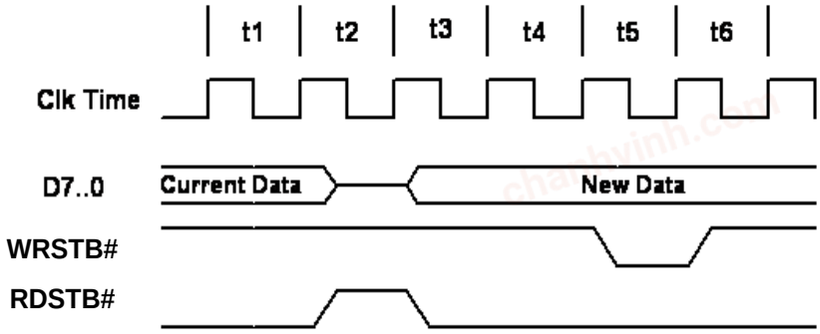


Figure 4.20 Synchronous Bit-Bang Mode Timing Interface Example

Name	Description
t1	Current pin state is read
t2	RDSTB# is set inactive and data on the paralle I/O pins is read and sent to the USB host.
t3	RDSTB# is set active again, and any pins that are output will change to their new data
t4	1 clock cycle to allow for data setup
t5	WRSTB# goes active. This indicates that the host PC has written new data to the I/O parallel data pins
t6	WRSTB# goes inactive

Table 4.10 Synchronous Bit-Bang Mode Timing Interface Example Timings

WRSTB# = this output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).

RDSTB# = this output rising edge indicates when data has been read from the I/O pins and sent to the Host PC (via the USB interface).

The WRSTB# goes active in t4. The WRSTB# goes active when data is read from the USB RXFIFO (i.e. sent from the PC). The RDSTB# goes inactive when data is sampled from the pins and written to the USB TXFIFO (i.e. sent to the PC). The FT_SetBitMode command to the FT2233HP/FT2232HP are used to setup the bit-mode. This command also contains a byte wide data mask to set the direction of each bit. The direction on each pin doesn't change unless a new FT_SetBitMode command is used to modify the direction.

The WRSTB# and RDSTB# strobes is only a guide to what may be happening depending on the direction of the bus. For example if all pins are configured as inputs, it is still necessary to write to these pins in order to get the FT2233HP/FT2232HP to read those pins even though the data written will never appear on the pins.

Signals and data-flow are illustrated in the figure given below -

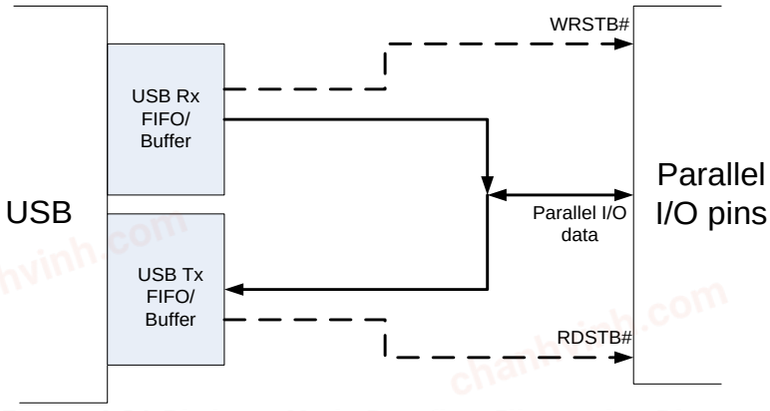


Figure 4.21 Bit-bang Mode Dataflow Illustration Diagram

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4.11 RS232 UART Mode LED Interface Description

When configured in UART mode the FT2233HP/FT2232HP has two IO pins on each channel dedicated to controlling LED status indicators, one for transmitted data the other for received data. When data is being transmitted / received the respective pins drive from tri-state to low in order to provide indication on the LED's of data transfer. A digital one-shot timer is used so that even a small percentage of data transfer is visible to the end user.

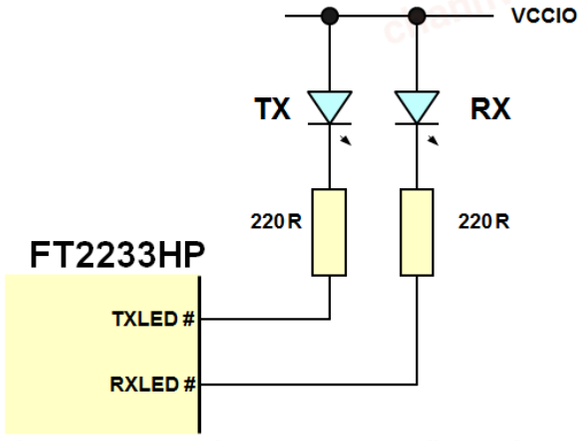


Figure 4.22 Dual LED UART Configuration

The above figure shows a configuration using two individual LED's – one for transmitted data the other for received data.

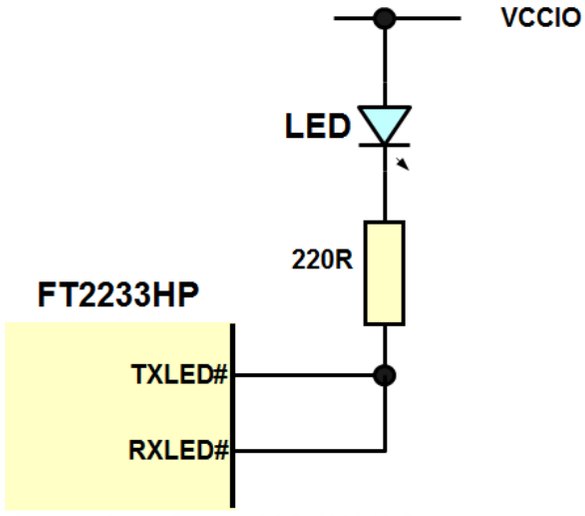


Figure 4.23 Single LED UART Configuration

The above figure illustrates how to transmit and receive LED indicators are wire-OR'ed together to give a single LED indicator which indicates any transmit or receive data activity.

Note that the LED's are connected to the same supply as VCCIO.

4.12 Send Immediate / Wake Up (SIWU#)

The SIWU# function is available in the FIFO modes and in bit-bang mode.

The Send Immediate portion is used to flush data from the chip back to the PC. This can be used to get short packets of data back to the PC without waiting for the latency timer to expire.

This mechanism should only be used when you have stopped sending data to the chip to avoid overrun.

The data transfer is flagged to the USB host by the falling edge of the signal.

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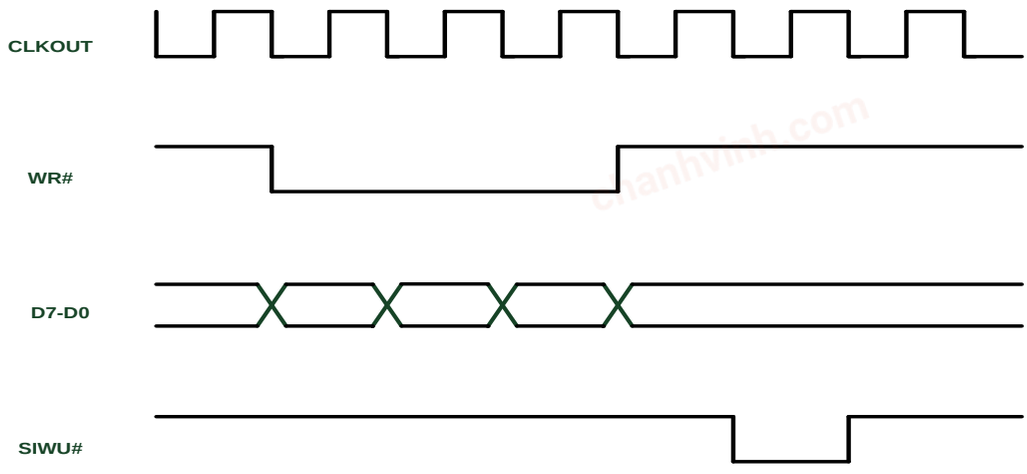


Figure 4.24 Using SIWU#

When the pin is being used for a Wake Up function to wake up a sleeping PC a 20ms negative pulse on this pin is required. When the pin is being used to flush the buffer (Send Immediate), a 250ns negative pulse on this pin is required.

Notes

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.
2. If remote wake-up is enabled, a peripheral is allowed to draw up to 2.5mA in suspend. If remote wake-up is disabled, the peripheral must draw no more than 500uA in suspend.
3. If a Pull-down is enabled, the FT2233HP/FT2232HP will not wake up from suspend.

4.13 FT2233HP/FT2232HP Mode Selection

The two channels of the FT2233H/FT2232HP reset to two asynchronous serial interfaces.

Following a reset the required mode of each channel is determined by the contents of the EEPROM (programmed using FT_PROG).

The EEPROM contents determine if the two channels have been configured as FT232 asynchronous serial interface, FT245 FIFO interface, CPU-style FIFO interface or Fast Serial Interface.

Following a reset, the EEPROM is read to determine which mode is configured. After device enumeration, an ***FT_SetBitMode*** command (refer to *D2XX_Programmers_Guide*) can be sent to the USB driver to switch the selected interface into the required mode – asynchronous bit-bang, synchronous bit-bang or MPSSE.

When in FT245 FIFO mode, the ***FT_SetBitMode*** command can be used to select either Synchronous FIFO (***FT_SetBitMode*** = 0x40) or Asynchronous FIFO mode. (Note that Asynchronous FIFO mode must be selected on both channels before selecting the Synchronous FIFO mode. This means that an EEPROM is needed to initially configure Asynchronous FIFO mode before software configures the Synchronous FIFO mode).

When Synchronous FIFO mode selected, channel A uses all the memory resources of channel B. As such channel B is then not available. In this case the state of the channel B pins is determined when the configuration is switched to Asynchronous FIFO mode. If channel B had not been used for any data transfer before configuration of Asynchronous FIFO mode, then the channel B pins will remain in their default mode (D7:0=tri-stated but pulled high trough 75K resistor, TXE# =low, RXF# =high. RD# and WR# are inputs and should be pulled high). An MPSSE command, ***set_data_bits*** can be used to configure the channel B pins as inputs before configuring channel A as Synchronous FIFO. This avoids the channel B pins driving against any interfaces (such as SPI) which may have been configured previous to any switching of channel A to Synchronous FIFO mode. Refer to AN108 Command Processor for MPSSE and

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MCU Host Bus Emulation Modes for the ***set_data_bits*** command and further information on the MPSSE used in MCU Host BUS Emulation mode.

The MPSSE can be configured directly using the D2XX commands. Refer to the D2XX Programmers Guide. FTDI have a range of application and software examples for MPSSE. Refer to the Application Notes for further explanation and examples at https://www.ftdichip.com/Support/FTDocuments.htm.

4.13.1 Do I need an EEPROM?

The following Table 4.11 summarises what modes are configurable using the EEPROM or the application software.

	ASYNC Serial UART	ASYNC 245 FIFO	SYNC 245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU-Style FIFO	Host Bus Emulation
EEPROM configured	YES	YES	YES				YES	YES	
Application Software configured			YES	YES	YES	YES			YES

Table 4.11 Configuration Using EEPROM and Application Software

4.14 USB Type-C/PD Controller

4.14.1 PD controller description

The FT2233HP has a Type-C/PD controller that fully supports the latest USB Type-C and Power Delivery (PD) 3.0 standards enabling support for power negotiation with the ability to sink or source current to a USB host device. There are two PD ports in the device (FT2233HPQ and FT2233HPL only), one port is with the legacy USB 2.0 port to form USB PD port as a power sink or source, and the other port is standalone PD port as a sink which is used to connect to PD power source. Power Delivery function is designed to meet PD2.0/3.0 specification. If the device is configured to be operated in legacy USB2.0 mode it will be backward compatible to FT2232H in terms of USB2.0 and its peripheral IOs functions.

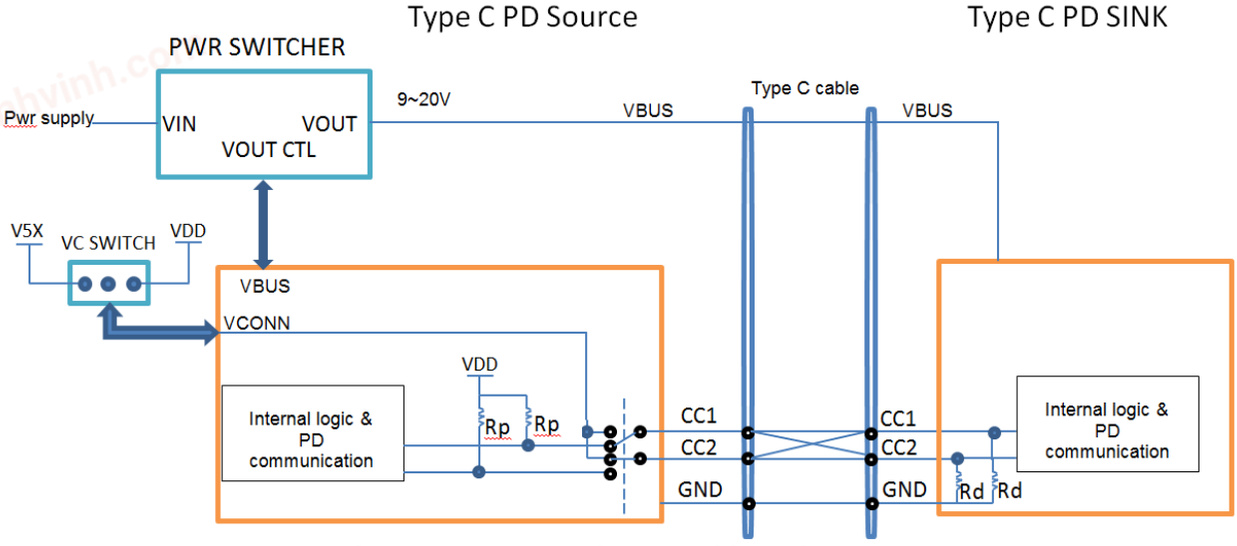


Figure 4.25 General PD Working Diagram

4.14.2 Features

- PD 3.0 Compliant.
- Physical layer and Policy Engine.
- Initial Sink, with Dual Role Power (Power Role Swap) and vConn Swap support.
- Multiple Configurable Power Profiles.
- Supports up to 20V5A power profile.
- Charge through Support.

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- Cable Attach and Orientation Detection.
- Supports 1.5A and 3A cables in Type-C legacy mode (NON-PD Mode).
- Profile Selection indication through GPIOs when operating In Sink Mode.
- Supports External MCU to take over the control.
- 8 bit register interface for a low speed processor, or optional I2C port
- Integrated Chapter 6 protocol reduces required MPU response time to 10mS.
- K code recognition/coding, preamble, CRC, etc offloaded from processor.
- VCONN 200mA protected driver switches
- Single 12MHz clock + 32KHz low power clock.
- Slew rate limited driving of CC cable lines drive to 1.1V and 300nS linear transition time.

4.14.3 AC timing on GPIO pins

Best case transition time with 5pF load		Worst case transition time with 15pF load	
Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)
1.2	1.1	6.0	6.5

Table 4.12 AC timing on GPIO

4.14.4 GPIO Timing for PD Operation

GPIOs are used as a power profile indicator as well as power supply controllers.

When operating as a Sink, GPIO pins are used for LOAD_EN and ISET.

Depends on the kind of profile negotiated, the appropriate ISET GPIO will go high followed by LOAD_EN pin.

The timing between this ISET going high to LOAD_EN can be as high as 12.5uS.

When operating as a Source, GPIO pins are used as power supply controller.

During Source operation, initial voltage will be 5V and then depends on the profile setting, the PD controller can negotiate a higher voltage. The switching from 5V to higher Voltage or vice versa is by switching GPIOs. 5V could be controlled by one Pin where as another higher Voltage is controlled by another pin.

For example, below table shows a sample GPIO states for 3 different voltage cases.

	5v	9V	20V
PS_EN	HIGH	HIGH	HIGH
GPIO_9v	LOW	HIGH	LOW
GPIO_20v	LOW	LOW	HIGH

Table 4.13 Example GPIO states for power control

In this case 5V to 9V or 5v to 20V is just an additional GPIO pin going high. In this case the timing does not matter.

However in the scenario when the profile changes from 9V to 20V, there is one GPIO going Low where as another one going high. In this case the delay between one pin going low to another pin going high can be as high as 12.5uS.

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4.14.5 Voltage parameters

Based on USB Type-C specification, during initialization when Source connects to Sink, both are in the unattached state. Source firstly detects the Sink's pull down on CC then enters attached state, Source turns on VBUS and VCONN. USB Type-C specification requests voltage parameters shown below:

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/ Adapter(vRa)	0.00V	0.15V	0.20V
Sink(vRd)	0.25V	1.50V	1.60V
No connect (vOPEN)	1.65V		

Table 4.14 CC Voltages on Source Side – Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/ Adapter(vRa)	0.00V	0.35V	0.40V
Sink(vRd)	0.45V	1.50V	1.60V
No connect (vOPEN)	1.65V		

Table 4.15 CC Voltages on Source Side – 1.5A @ 5V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/ Adapter(vRa)	0.00V	0.75V	0.80V
Sink(vRd)	0.85V	2.45V	2.60V
No connect (vOPEN)	2.75V		

Table 4.16 CC Voltages on Source Side – 3A @ 5V

For better achieving USB Type-C specification request, we suggest to use P channel MOSFET to isolate DCDC power and FT2233HP/FT2232HP power in order to guarantee the expected voltage parameters. The equivalent circuit shown below:

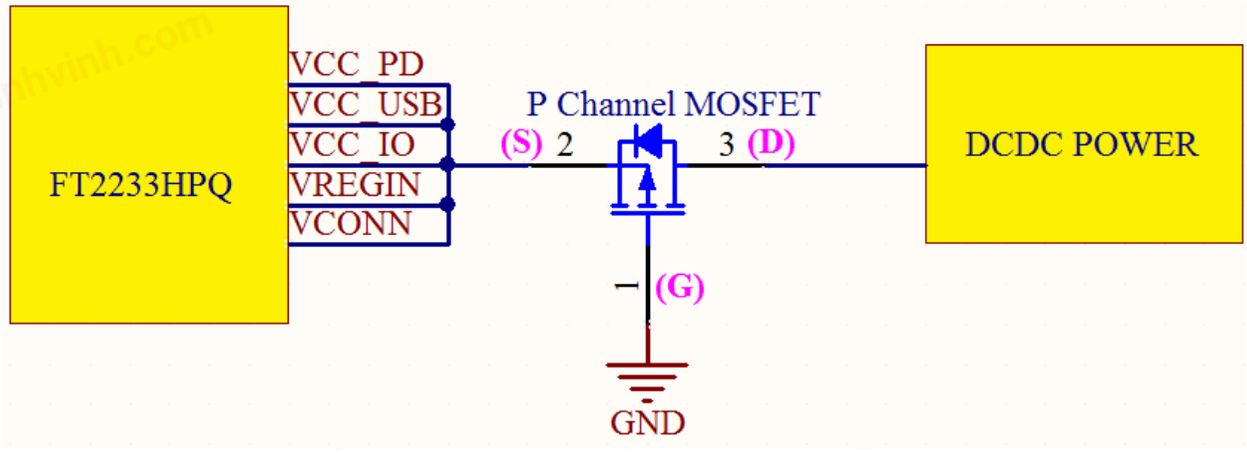


Figure 4.26 Channel MOFST Equivalent Circuit

Recommended MOSFET parameters:

$V_{(BR)DSS}$	I_D	Gate Threshold Voltage
-20V(typical)	< -150mA	< -0.6V

Table 4.17 P-channel MOSFET Character recommendation

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5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT2233HP devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these values may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C
MTTF FT2233HPQ	TBD	hours
VCORE Supply Voltage	-0.3 to +2.0	V
VCCIO IO Voltage	-0.3 to +4.0	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V
DC Input Voltage – High Impedance Bi-directional (powered from VCCIO)	-0.3 to +5.8	V
DC Input Voltage – All Other Inputs	-0.5 to + (VCCIO +0.5)	V
DC Output Current – Outputs	16	mA

Table 5.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCORE	VCC Core Operating Supply Voltage	1.08	1.20	1.32	V	
VCCIO*	VCCIO Operating Supply Voltage	2.97	3.30	3.63	V	Cells are 5V tolerant
VREGIN	VREGIN Voltage regulator Input	3.00	3.30	3.60	V	
VREGOUT	Voltage regulator Output	1.08	1.2	1.32	V	
Ireg	Regulator Current		22.37	150	mA	VREGIN +3.3V and data transfer with 12Mbps
Icc1s	VREGIN Suspend Supply Current		132.2		µA	USB Suspend
I_vcc_usb	VCC_USB operating supply current		22.36		mA	Data transfer with 12Mbps
I_vccio	VCC_IO operating supply current		1.72		mA	Data transfer with 12Mbps
I_vcc_pd	VCC_PD suspend supply current		23.5		uA	PD suspend

Table 5.2 Operating Voltage and Current

Note: Failure to connect all VCCIO pins will result in failure of the device.

The I/O pins are +3.3v cells, which are +5V tolerant (except the USB PHY pins).

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.40	3.14		V	Ioh = +/-2mA I/O Drive strength* = 4mA
			3.20		V	I/O Drive strength* = 8mA
			3.22		V	I/O Drive strength* = 12mA
			3.22		V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0.18	0.40	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0.12		V	I/O Drive strength* = 8mA
			0.08		V	I/O Drive strength* = 12mA
			0.07		V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold		-	0.80	V	LVTTL
Vih	Input High Switching Threshold	2.0	-		V	LVTTL
Vt	Switching Threshold		1.50		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage	0.80	1.10	-	V	
Vt+	Schmitt trigger positive going threshold voltage		1.60	2.0	V	
Rpu	Input pull-up resistance**	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	15	45	85	µA	Vin = 0
Ioz	Tri-state output leakage current		+/-10		µA	Vin = 5.5V or 0

Table 5.3 I/O Pin Characteristics (except USB PHY pins)

*The I/O drive strength and slow slew-rate are configurable in the EEPROM.

**The voltage pulled up to is VCCIO-0.9V in the worst case.

5.3 ESD Tolerance

ESD protection for FT2233HP IO's

Parameter	Reference	Minimum	Typical	Maximum	Units
Human Body Model (HBM)	JEDEC EIA/JESD22-A114-B, Class 2		±2kV		kV
Machine Mode (MM)	JEDEC EIA/JESD22-A115-A, Class B		±200V		V
Charge Device Model (CDM)	JEDEC EIA/ JESD22-C101-D, Class-III		±500V		V
Latch-up	JESD78, Trigger Class-II		±200mA		mA

Table 5.4 ESD Tolerance

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5.4 Thermal Characteristics

Parameter	Minimum	Typical	Maximum	Units
Θ_{JA} (FT2233HPL)		50		°C/W
Θ_{JC} (FT2233HPL)		11		°C/W
Θ_{JA} (FT2233HPQ)		29		°C/W
Θ_{JC} (FT2233HPQ)		1.0		°C/W
Θ_{JA} (FT2232HPQ)		23.65*		°C/W
Θ_{JC} (FT2232HPQ)		9.35*		°C/W
T_J (FT2233HP/FT2232HP)	-40	25	125	°C

Table 5.5 Thermal Characteristics

* Preliminary data

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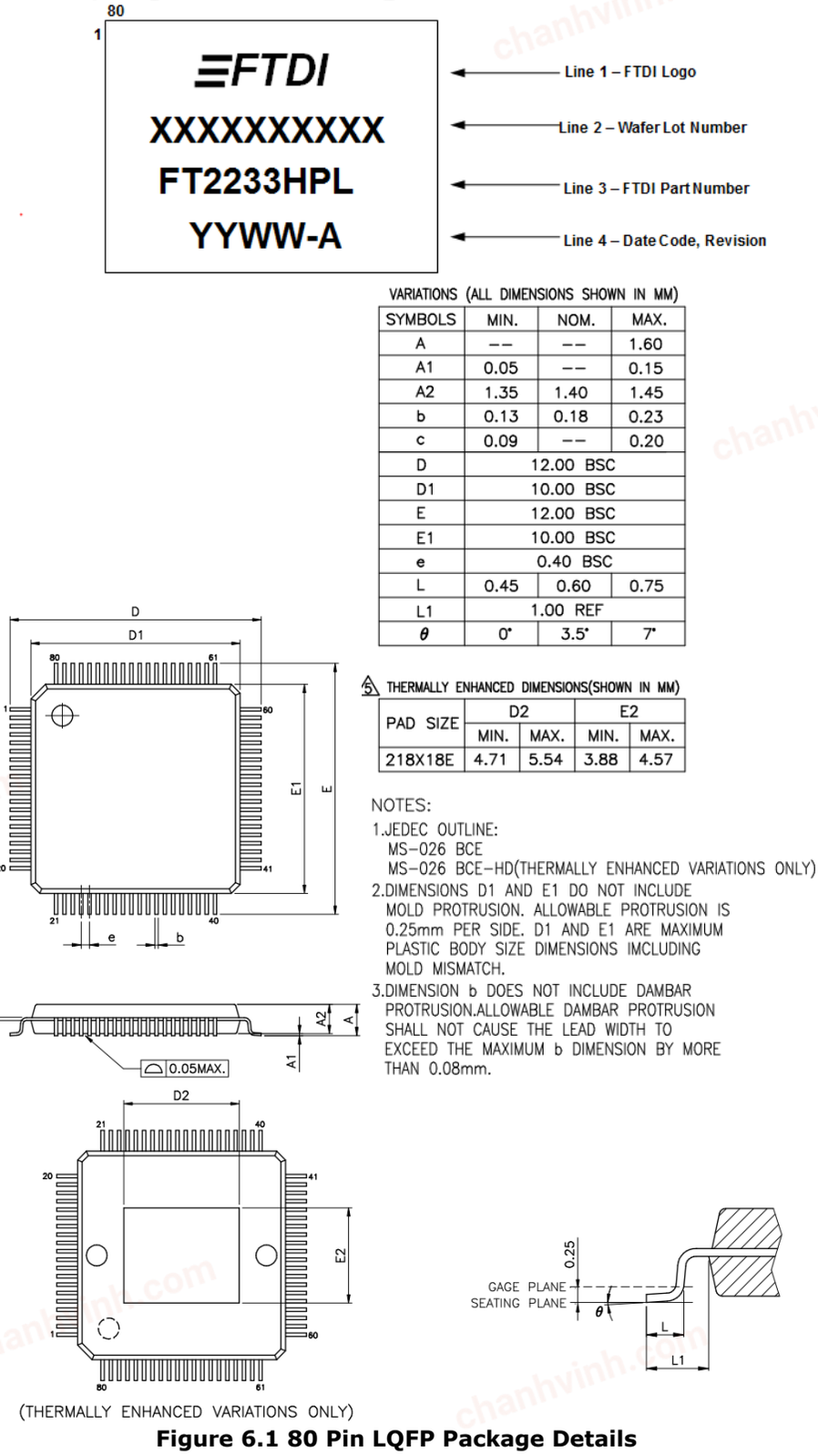
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6 Package Parameters

The FT2232HP is available in three different packages. The FT2233HPL is the LQFP-80 package option, the FT2233HPQ is the QFN-76 package option and the FT2232HPQ is the QFN-68 package option. See TN_166 FTDI Example IC Footprints for PCB footprint guidelines.

6.1 FT2233HPL, LQFP-80 Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

5 THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	D2		E2	
	MIN.	MAX.	MIN.	MAX.
218X18E	4.71	5.54	3.88	4.57

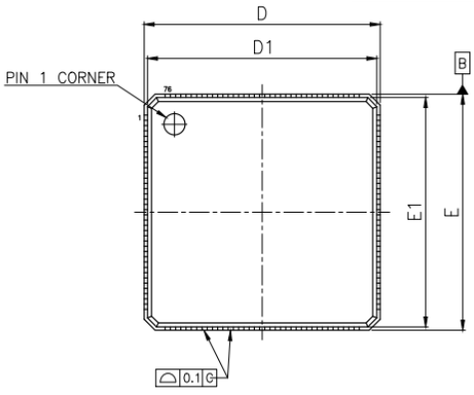
NOTES:
1.JEDEC OUTLINE:
MS-026 BCE
MS-026 BCE-HD(THERMALLY ENHANCED VARIATIONS ONLY)
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

Figure 6.1 80 Pin LQFP Package Details

6.2 FT2233HPQ, QFN-76 Package Dimensions

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SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.15	0.20	0.25
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.40 BSC.	
K	0.20	—	—
θ°	0.00	—	12.00

UNIT : mm

UNIT : mm	EXPOSED PAD						L		
	D2			E2					
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
2 245X26* MIL	5.56	5.81	6.06	6.06	6.31	6.56	0.30	0.40	0.50

2 "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

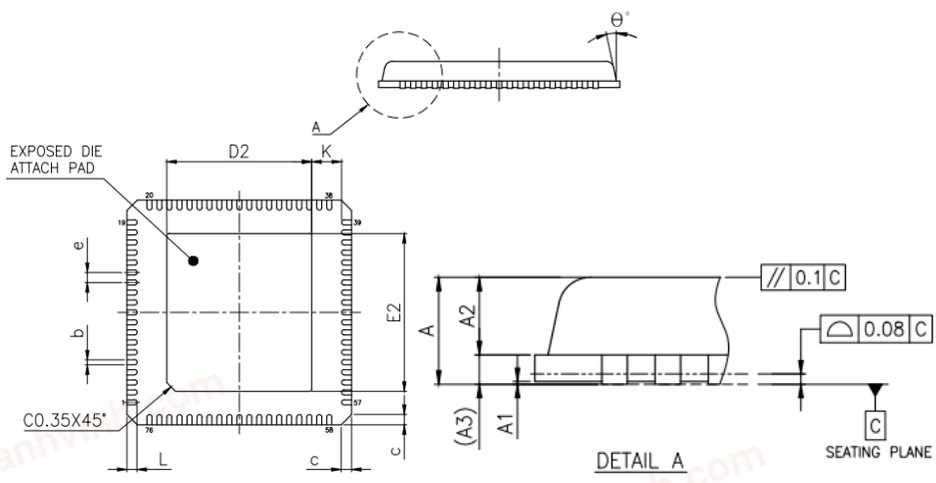
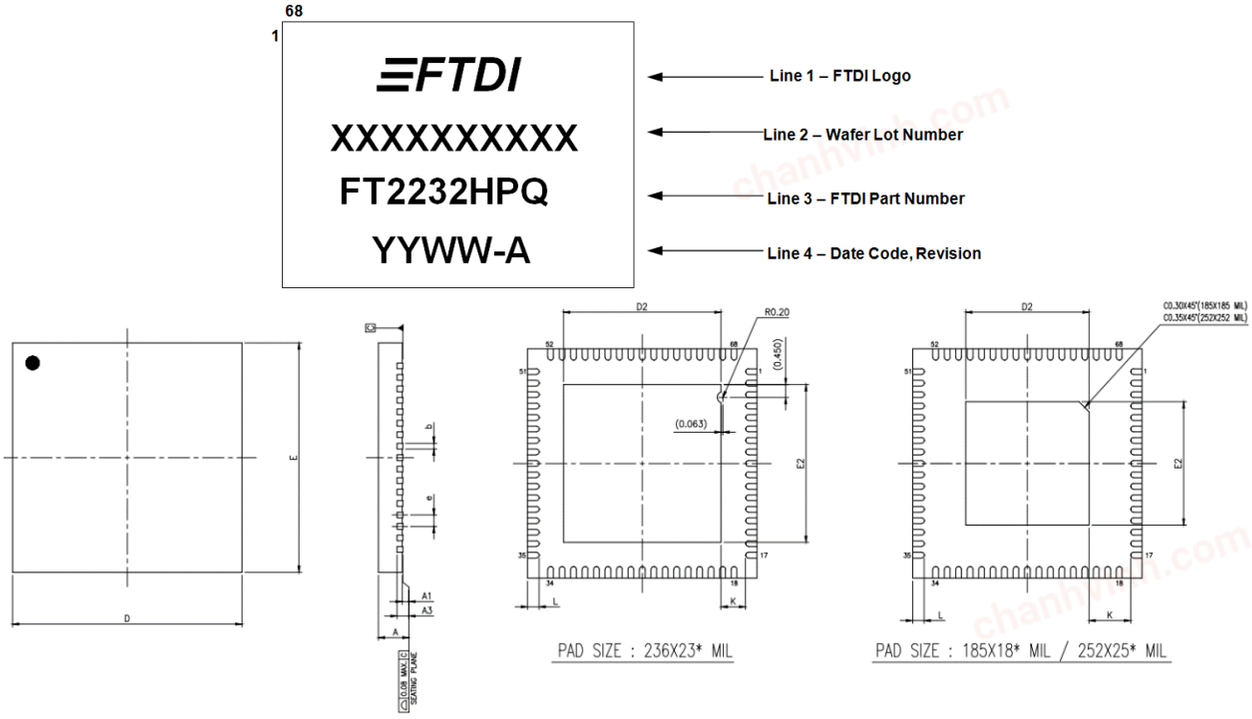


Figure 6.2 76 Pin QFN Package Details

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6.3 FT2232HPQ, QFN-68 Package Dimensions



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X868)			VQFN(Y868)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.15	0.20	0.25	0.15	0.20	0.25
D	8.00 BSC			8.00 BSC		
E	8.00 BSC			8.00 BSC		
e	0.40 BSC			0.40 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
6 185X18* MIL	4.25	4.30	4.35	4.25	4.30	4.35	V	X	N/A
6 236X23* MIL	5.45	5.50	5.55	5.45	5.50	5.55	V	X	N/A
6 252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	X	VLLE-1

6 "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 6.3 68 Pin QFN Package Details

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Appendix A – References

Document References

AN_113, "Interfacing FT2232H Hi-Speed Devices To I2C Bus

AN_177 – "User Guide For libMPSSE – I2C"

AN_178 – "User Guide For libMPSSE - SPI"

AN 113 – "Interfacing FT2232H Hi-Speed Devices To I2C Bus

AN114 – "Interfacing FT2232H Hi-Speed Devices To SPI Bus

AN135 – MPSSE Basics

AN108 – Command Processor For MPSSE and MCU Host Bus Emulation Modes

TN_104, "Guide to Debugging Customers Failed Driver Installation

TN_100 USB Vendor ID/Product ID Guidelines

TN_166 FTDI Example IC Footprints

AN2232-02, "Bit Mode Functions for the FT2232

74HC595 datasheet

FT_PROG EEPROM Programming Utility

Acronyms and Abbreviations

Terms	Description
DRP	Dual Role Power
EEPROM	Electrically Erasable Programmable Read-Only Memory
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
IC	Integrated Circuit
I2C	Inter Integrated Circuit
JTAG	Joint Test Action Group
LDO	Low Drop Out
LED	Light Emitting Diode
MCU	Microcontroller Unit
MPSSE	Multi-Protocol Synchronous Serial Engine
PD	Power Delivery
PLD	Programmable Logic Device
QFN	Quad Flat No-Lead
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
UTMI	Universal Transceiver Macrocell Interface
VCP	Virtual COM Ports

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Appendix C – Revision History

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