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SEIKO EPSON CORPORATION

Clock OSC SG3225EAN

Product name SG3225EAN 400.000000MHz KEGA
Product Number / Ordering code X1G0042510026xx
Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LV-PECL
Pb free / Complies with EU RoHS directive
Reference weight Typ. 25 mg

1.Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	+4	V	-
Storage temperature	T_stg	-40	-	+125	ºC	Storage as single product
Input voltage	Vin	-0.3	-	Vcc+0.3	V	ST or OE Terminal

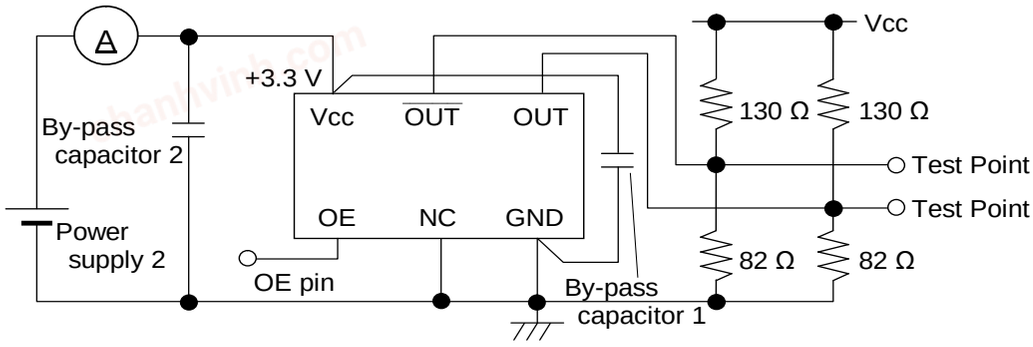
2.Specifications(characteristics)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f0		400.0000		MHz	
Supply voltage	Vcc	2.25	-	3.63	V	-
Operating temperature	T_use	-40	-	+85	ºC	-
Frequency tolerance	f_tol	-30	-	30	$x10^{-6}$	-
Current consumption	Icc	-	-	65	mA	OE = Vcc , L_ECL = 50 ohm
Stand-by current	I_std	-	-	-	mA	-
Disable current	I_dis	-	-	20.0	mA	OE=GND
Symmetry	SYM	45	-	55	%	At output crossing point
Output voltage(LV-PECL)	V_{OH}	Vcc-1.0	-	-	V	-
	V_{OL}	-	-	Vcc-1.62	V	-
Output load condition(ECL)	L_ECL	-	50	-	Ω	Terminated to Vcc - 2.0V
Input voltage	V_{IH}	70% Vcc	-	-		OE Terminal
	V_{IL}	-	-	30% Vcc		OE Terminal
Rise time	t_r	-	-	350	ps	At 20% to 80% output swing
Fall time	tf	-	-	350	ps	At 20% to 80% output swing
Start-up time	t_str	-	-	3	ms	-
Jitter	t_{DJ}	-	11.3	-	ps	Deterministic Jitter Vcc=2.5V
	T_{RJ}	-	1.3	-	ps	Random Jitter Vcc=2.5V
	t_{RMS}	-	5.3	-	ps	δ(RMS of total distribution) Vcc=2.5V
	t_{p-p}	-	29.5	-	ps	Peak to Peak Vcc=2.5V
	t_{acc}	-	7.8	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles Vcc=2.5V
Phase jitter	t_{PJ}	-	0.35	-	ps	Offset Frequency: 12kHz to 20MHz Vcc=2.5V
Phase noise	L(f)	-	-39	-	dBc/Hz	Offset 1Hz Vcc=2.5V
		-	-73	-	dBc/Hz	Offset 10Hz Vcc=2.5V
		-	-100	-	dBc/Hz	Offset 100Hz Vcc=2.5V
		-	-112	-	dBc/Hz	Offset 1kHz Vcc=2.5V
		-	-122	-	dBc/Hz	Offset 10kHz Vcc=2.5V
		-	-127	-	dBc/Hz	Offset 100kHz Vcc=2.5V
		-	-128	-	dBc/Hz	Offset 1MHz Vcc=2.5V
Frequency aging	f_age	-5	-	5	$x10^{-6}$/Year	@+25ºC first year

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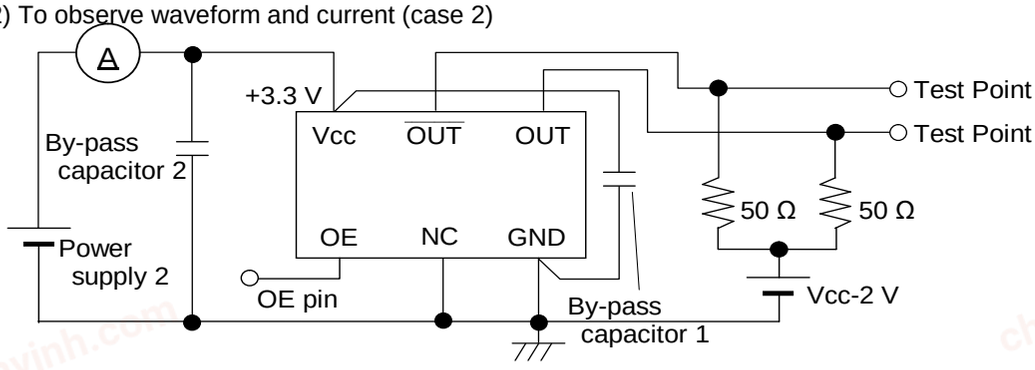
3.Test circuit

1) To observe waveform and current (case 1)



* The lines from OUT and $\overline{OUT}$ pin are same length.
* To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



* The lines from OUT and $\overline{OUT}$ pin are same length.
* To measure the disable current, OE pin is connected to GND

3) Measurement condition

A) Oscilloscope

•Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).

•Probe ground should be placed closely from test point and lead length should be as short as possible.

B) By-pass capacitor 1 (approx. 0.01 µF to 0.1 µF) places closely between Vcc and GND.

C) By-pass capacitor 2 (approx. 10 µF) places closely between power supply terminals on the board.

D) Use the current meter whose internal impedance value is small.

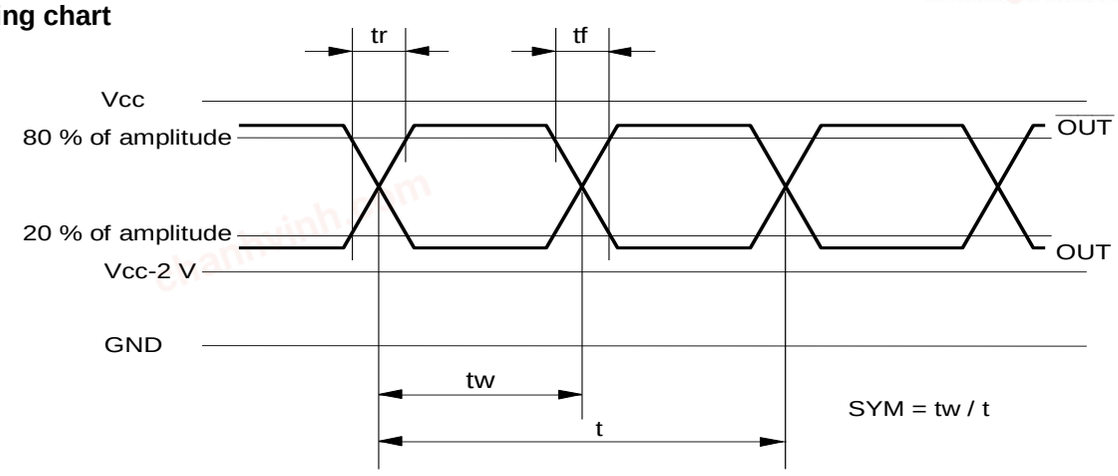
E) Power supply

• Start up time (0 Vg90 %Vcc) of power source should be more than 150 µs and slew rate should be less than 19.8 mV/µs.

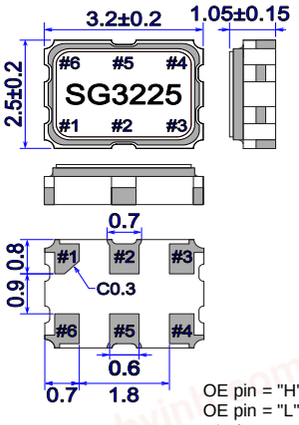
• Impedance of power supply should be as low as possible.

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4.Timing chart



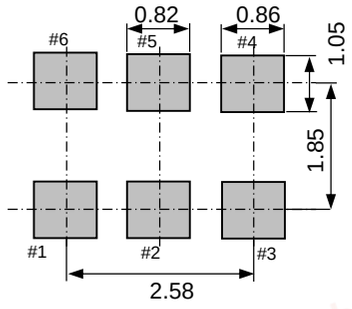
5.External dimensions (Unit: mm)



Pin	Connection
1	OE
2	N.C.
3	GND
4	OUT
5	$\overline{OUT}$
6	VCC

OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.
#2 pin connection = GND is acceptable.
The metal cap is connected to #3 pin.

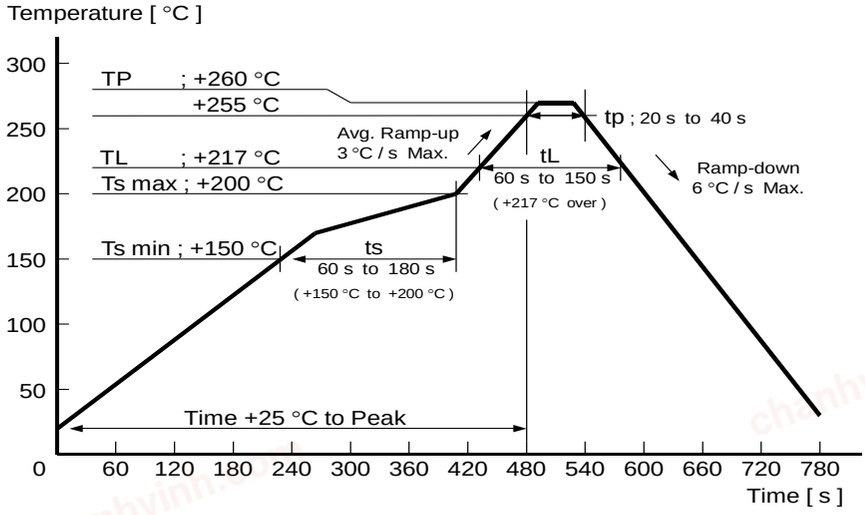
6.Footprint(Recommended) (Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

7.Reflow profile

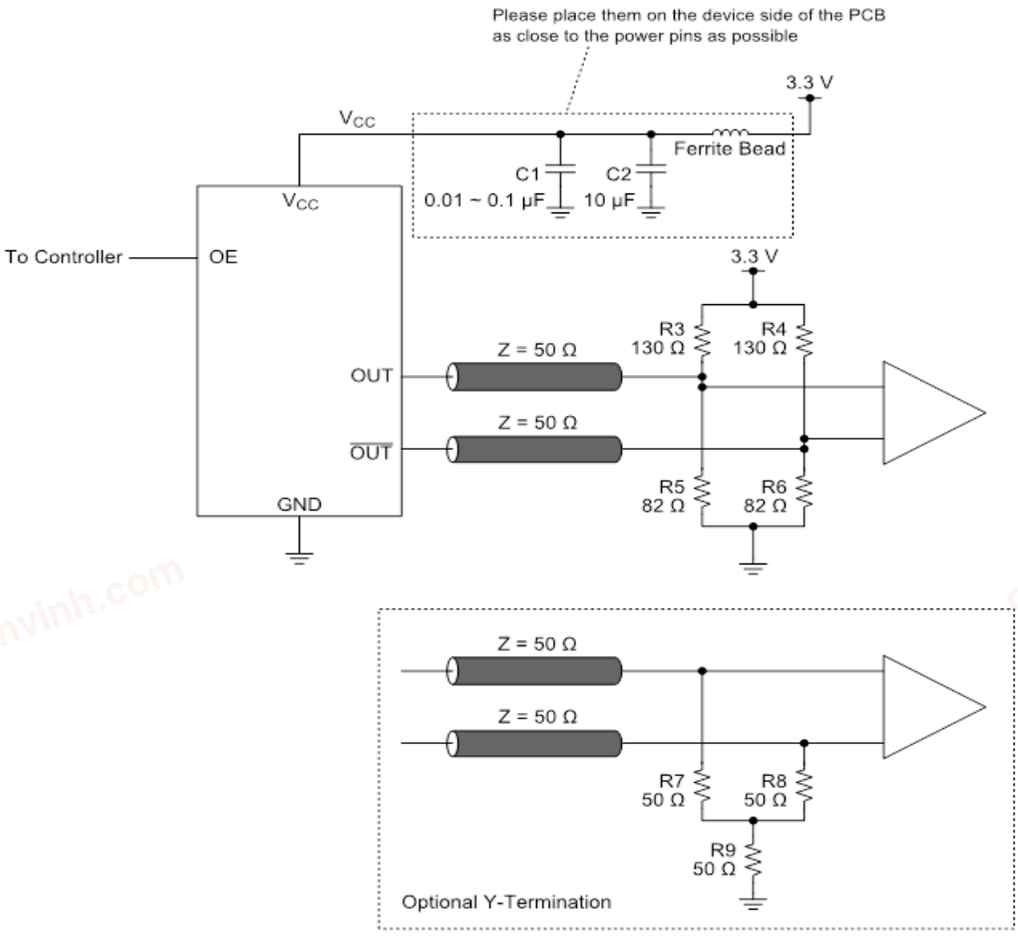
Reflow condition (Follow of JEDEC STD-020D.01)



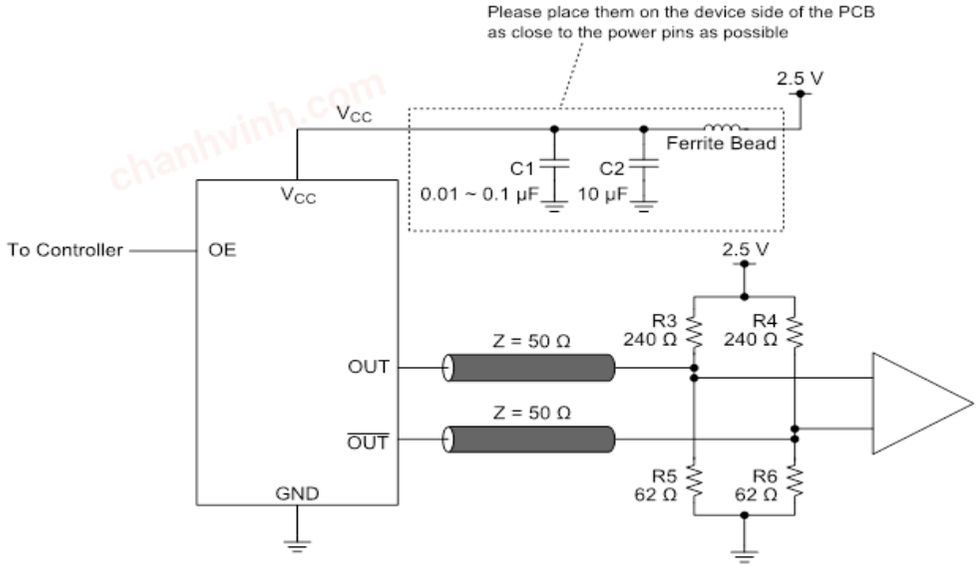
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8.Example of schematic layout

This figure shows an example of this product's application schematic.
As with any high speed analog circuitry, the power supply pins for this device are vulnerable to noise. In order to achieve optimum jitter performance, power isolation with filter device is required for power supply pins.
In order to achieve best performance of the power isolation filter, it is recommended that the filter composing devices is placed on the device side of the PCB as close to the power pins as possible. The component value of this filter is just an example, it may have to be adjusted.



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* By-pass capacitor (approx. 0.01 µF to 0.1 µF) places closely between Vcc and GND.
* By-pass capacitor (approx. 10 µF) places closely between power supply terminals on the board.
* Please design the two output lines by characteristic impedance 50 Ω and same length, and try to make the output lines as short as possible.
* Terminators place near the input device.

9.Packing information

[1]Product number last 2 digits code(xx) description The recommended code is "00"

X1G0042510026xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	14	1000pcs / Reel
12	250pcs / Reel	00	2000pcs / Reel

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[2] Taping specification

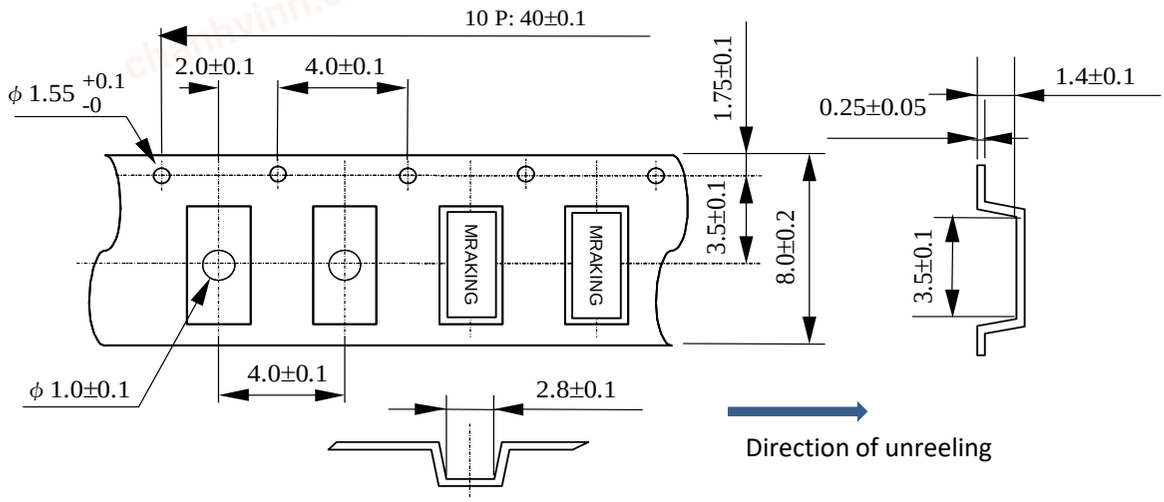
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

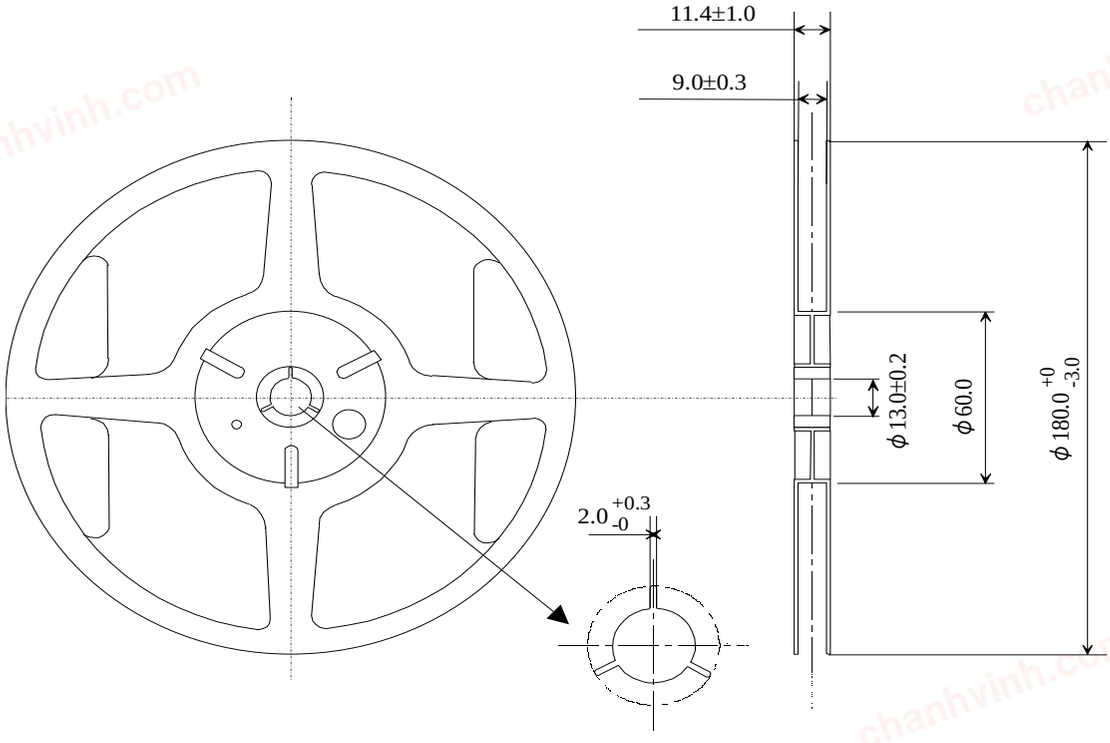
Unit: mm



(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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