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A product Line of
Diodes Incorporated

PI3USB102G

USB 2.0 High-Speed (480 Mbps) Switch with 5V Protection with Improved Ioff Voltage Range

Features

- USB 2.0 compliant (high speed, full speed, and low speed)
- R_{ON}: 4.0Ω typical @ V_{DD} = 3.0V
- Channel On Capacitance: 6.0pF
- Wide -3dB Bandwidth: 1,000MHz
- Low bit-to-bit skew
- Low Crosstalk: -29B @ 480 Mbps
- Off Isolation: -28dB @ 480 Mbps
- Near-Zero propagation delay: 250ps
- Support 1.8-V logic on control pins
- V_{DD} Operating Range: 3.0V to 5.5V
- ESD: 8kV HBM on Y+/Y- pins per JESD22 standard
- Y+/Y- pins have over-voltage protection and can tolerate a short to VBUS
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Packaging (Pb-free & Green):
  - —10-contact TQFN, 1.3mm x 1.6mm x 0.75mm (ZL10)

Description

The PI3USB102G is a single differential channel 2:1 multiplexer/demultiplexer USB 2.0 Switch. Industry leading advantages include a propagation delay of 250ps, resulting from its low channel resistance and I/O capacitance. PI3USB102G is bidirectional and offers very little attenuation of high-speed signals. It is designed for low bit-to-bit skew, high channel-to-channel noise isolation and is compatible with various standards, such as High Speed USB 2.0 (480 Mb/s).

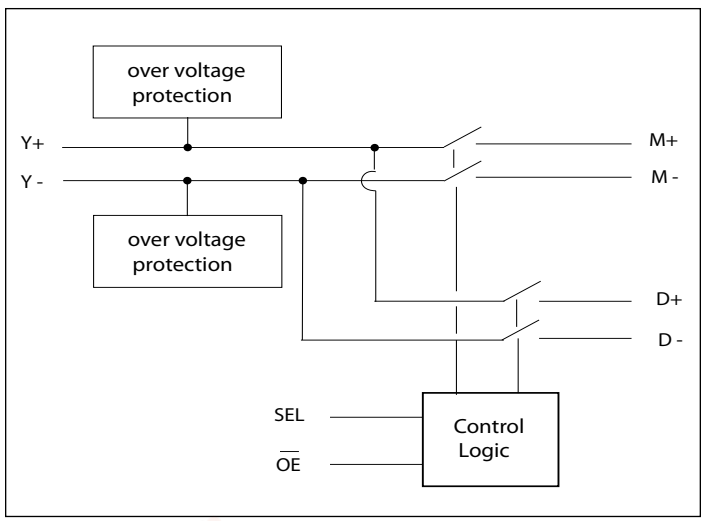
The PI3USB102G offers over voltage protection for the Y+/Y- pins as per the USB 2.0 specification. With the chip powered on or off if Y+/Y- pins are shorted to VBUS (5V +/- 5%), M+/M- and D+/D- outputs are clamped to provide voltage protection for downstream devices.

The PI3USB102G has a better Y+/Y- power-off leakage current with the voltage range of 0V to 5V versus 0V to 3.3V for the PI3USB102E.

Application

- Routes signals for USB 2.0
- PC, Notebooks and Hand-held devices

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

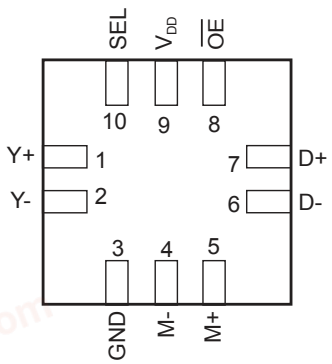
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Truth Table

SEL	$\overline{OE}$	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

Pin Configuration



Pin Description

Pin#	Pin Name	Description
1	Y+	USB Data bus
2	Y-	USB Data bus
3	GND	Ground
4	M-	Multiplexed Source Inputs
5	M+	Multiplexed Source Inputs
6	D-	Multiplexed Source Inputs
7	D+	Multiplexed Source Inputs
8	OE	Switch Enable
9	$\overline{V_{DD}}$	Positive Power Supply
10	SEL	Switch Select

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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Junction Temperature	125°C
Supply Voltage to Ground Potential	–0.5V to +6V
DC Input Voltage	–0.5V to +6V
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for USB 2.0 Switching over Operating Range

(T_A = –40°C to +85°C, V_{DD} = 3.0 - 5.5V)

Parameter	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level	1.4			V
V_{IL}	Input LOW Voltage	Guaranteed LOW level			0.8	
V_{IK}	Clamp Diode Voltage	V_{DD} = Max., I_{IK} = –18mA		-0.7	-1.2	
I_{IH}	Input HIGH Current for SEL and $\overline{OE}$	V_{DD} = Max., V_{IH} = VDD	-100		100	nA
I_{IL}	Input LOW Current for SEL and $\overline{OE}$	V_{DD} = Max., V_{IL} = GND	-100		100	
I_{IH}	Input HIGH Current for Y+/Y-	V_{DD} = 3.3V., V_Y = 5.25V			50	uA
I_{IL}	Input LOW Current for Y+/Y-	V_{DD} = 3.3V., V_Y = 0V			1	
$I_{Leakage}$	Leakage from Y+/Y- to Vdd when $V_{Y+/Y-}$ > Vdd	V_{DD} = 3.3V., $V_{Y+/Y-}$ = 5.25V, $\overline{OE}$ = LOW			200	nA
R_{ON}	Switch On-Resistance(3)	V_{DD} = 3V, 0V ≤ V_{input} ≤ 1.0V, I_{ON} = –40mA		4.0	5.0	Ω
$R_{FLAT(ON)}$	On-Resistance Flatness(3)	V_{DD} = 3V, 0V ≤ V_{input} ≤ 1.0V, I_{ON} = –40mA		1.5		
ΔR_{ON}	On-Resistance match from center ports to any other port(3)	V_{DD} = 3V, 0V ≤ V_{input} ≤ 1.0V, I_{ON} = –40mA		0.9	2.0	
V_{OVP}	Input Over-Voltage Protection Threshold(4)	V_{DD} = 3.0 V	3.1	3.2	3.4	V
		V_{DD} = 3.3 V	3.4	3.5	3.7	
		V_{DD} = 3.6 V	3.7	3.8	4.0	
I_{OZ_M}	Output leakage current on port M when D path is on	$V_{Y+/Y-}$ = 5.25V, V_{DD} = 3.3V SEL = High, $V_{M+/M-}$ = 0V	-200		200	nA
I_{OZ_D}	Output leakage current on port D when M path is on	$V_{Y+/Y-}$ = 5.25V, V_{DD} = 3.3V SEL = Low, $V_{D+/D-}$ = 0V	-200		200	nA
I_{OFF}	Y+/Y- Power-Off Leakage Current	V_{input} = 0V to 5V, V_{DD} = 0V		0.2	1	uA

Power Supply Characteristics

Parameters	Description	Test Conditions(1)	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current	V_{DD} = 3.3V, $\overline{OE}$ = GND, V_{SEL} = GND or V_{DD}		1	2	uA

Notes:

1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. V_{DD} = 3.0 - 5.5V, T_A = 25°C ambient.
3. Measured by the voltage drop between Y+/Y- and the lower of M+/M- and D+/D- at indicated current through the Switch.
4. When the voltage at Y+/Y- is greater than V_{DD} + 0.2V, over-voltage protection limits the output voltage at M+/- and D+/- to protect connected devices from damage.

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Capacitance (T_A = 25°C, V_{DD} = 3.3V, f = 1MHz)

Parameters[3]	Description	Test Conditions[1]	Typ.[2]	Max.	Units
C_{IN}	Input Capacitance		2.2	3.2	pF
$C_{OFF\ (M/D)}$	Switch Off Capacitance for M and D ports	$\overline{OE}$ = High	3.0	4.0	
$C_{OFF\ (Y)}$	Switch Off Capacitance for Y port	$\overline{OE}$ = High	5.0	6.0	
C_{ON}	Switch Capacitance, Switch ON	V_{SEL} = 0V or V_{DD}	6.0	7.0	

Dynamic Electrical Characteristics Over the Operating Range

Parameters[3]	Description	Test Conditions	Min.	Typ.[2]	Max.	Units
X_{TALK}	Crosstalk	R_L = 50Ω, f = 240 MHz		-29		dB
O_{IRR}	OFF Isolation			-28		
-3dB BW	–3dB Bandwidth	R_L = 50Ω		1,000		MHz
-0.5dB BW	–0.5dB Bandwidth	R_L = 50Ω		275		MHz
T_{OVP}	Over-Voltage Response Time[4]	C_L = 10 pF, $V_{Y+/Y-}$ = 5V, V_{DD} = 3.0 to 3.6V [6]		40	100	ns
V_{DSW}	Dynamic Signal Output Swing[5]	C_L = 10 pF, $V_{Y+/Y-}$ = 5V, V_{DD} = 3.0 to 3.6V [6]	2.7	3.0	3.6	V

Notes:
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient.
3. This parameter is determined by device characterization but is not production tested.
4. Time duration for output voltage higher than V_{OVP} when input is connected to 5V.
5. Output voltage observed at M+/M- and D+/D- during over-voltage condition.
6. Tested using a 750 kHz square wave with t_r = 75 ns and t_f = 75 ns.

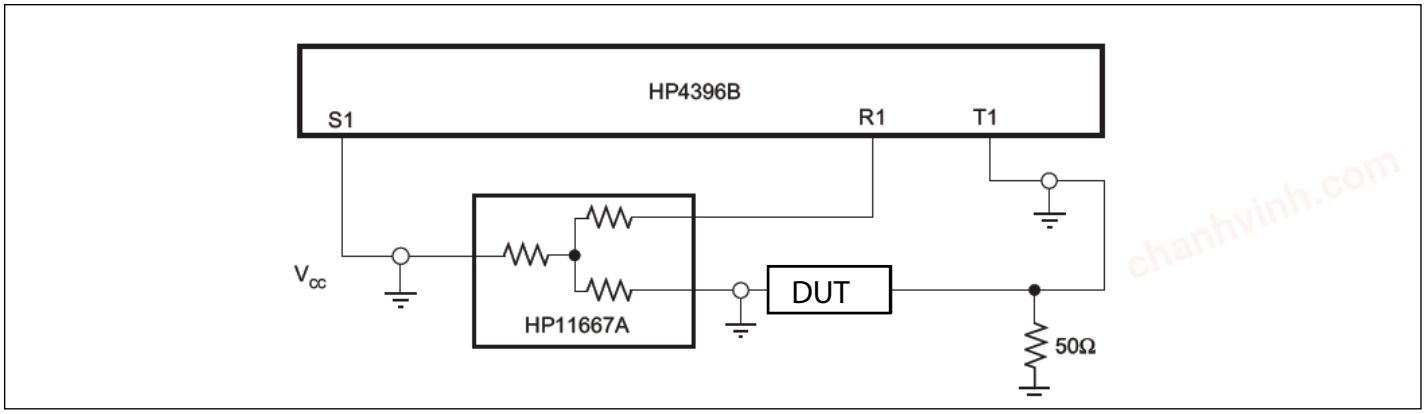
Switching Characteristics

Parameters	Description	Test Conditions [1]	Min.	Typ.	Max.	Units
t_{PD}	Propagation Delay[2,3]	See Test Circuit for Electrical Characteristics		0.25		ns
t_{PZH}, t_{PZL}	Line Enable Time - SEL, $\overline{OE}$ to D(+/-), M(+/-)		0.5		50	
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL, $\overline{OE}$ to D(+/-), M(+/-)		0.5		11.0	
t_{BBM}	Break Before Make Delay			9.0		ns
t_{SKb-b}	Output skew, bit-to-bit (opposite transition of the same output (t_{PHL}-t_{PLH})[2]			8	20	ps

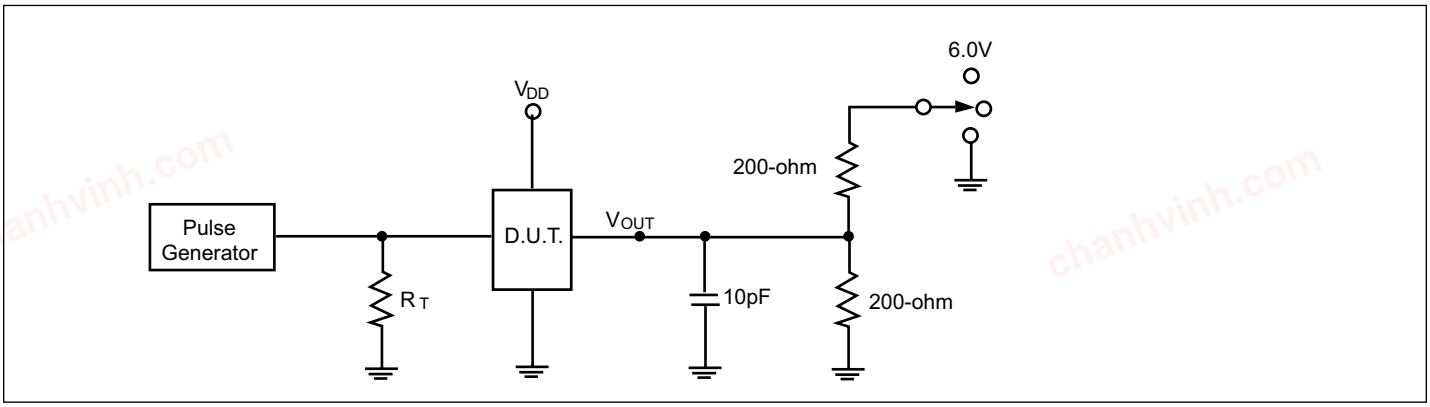
Notes:
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Guaranteed by design.
3. The switch contributes no propagation delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

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Test Circuit for Dynamic Electrical Characteristics



Test Circuit for Electrical Characteristics



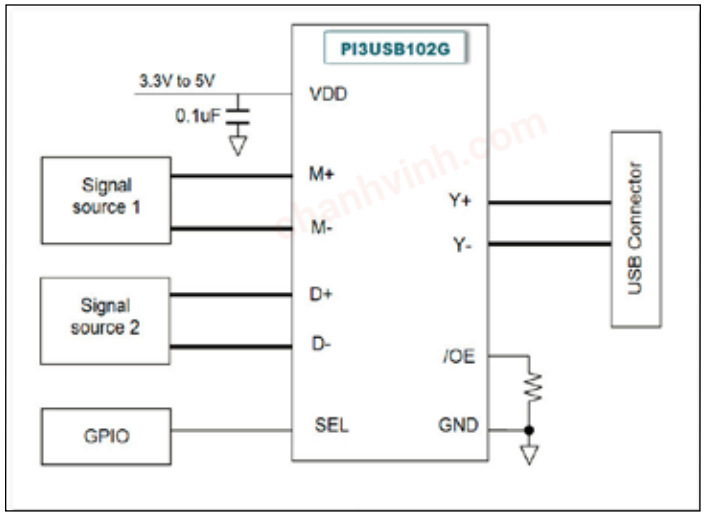
Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. All input impulses are supplied by generators having the following characteristics: $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
4. The outputs are measured one at a time with on transition per measurement.

Switch Positions

Test	Switch
t_{PLZ}, t_{PZL}	6.0V
t_{PHZ}, t_{PZH}	GND
Prop Delay	Open

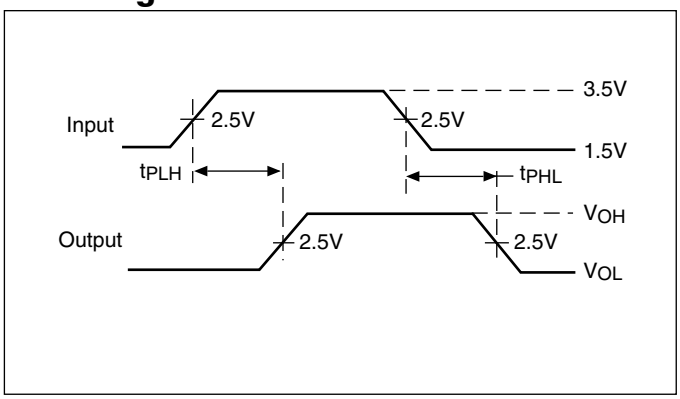
Application Example Diagram



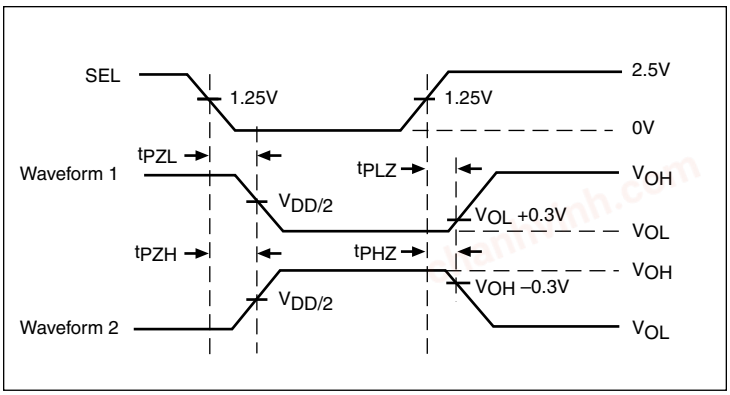
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Switching Waveforms

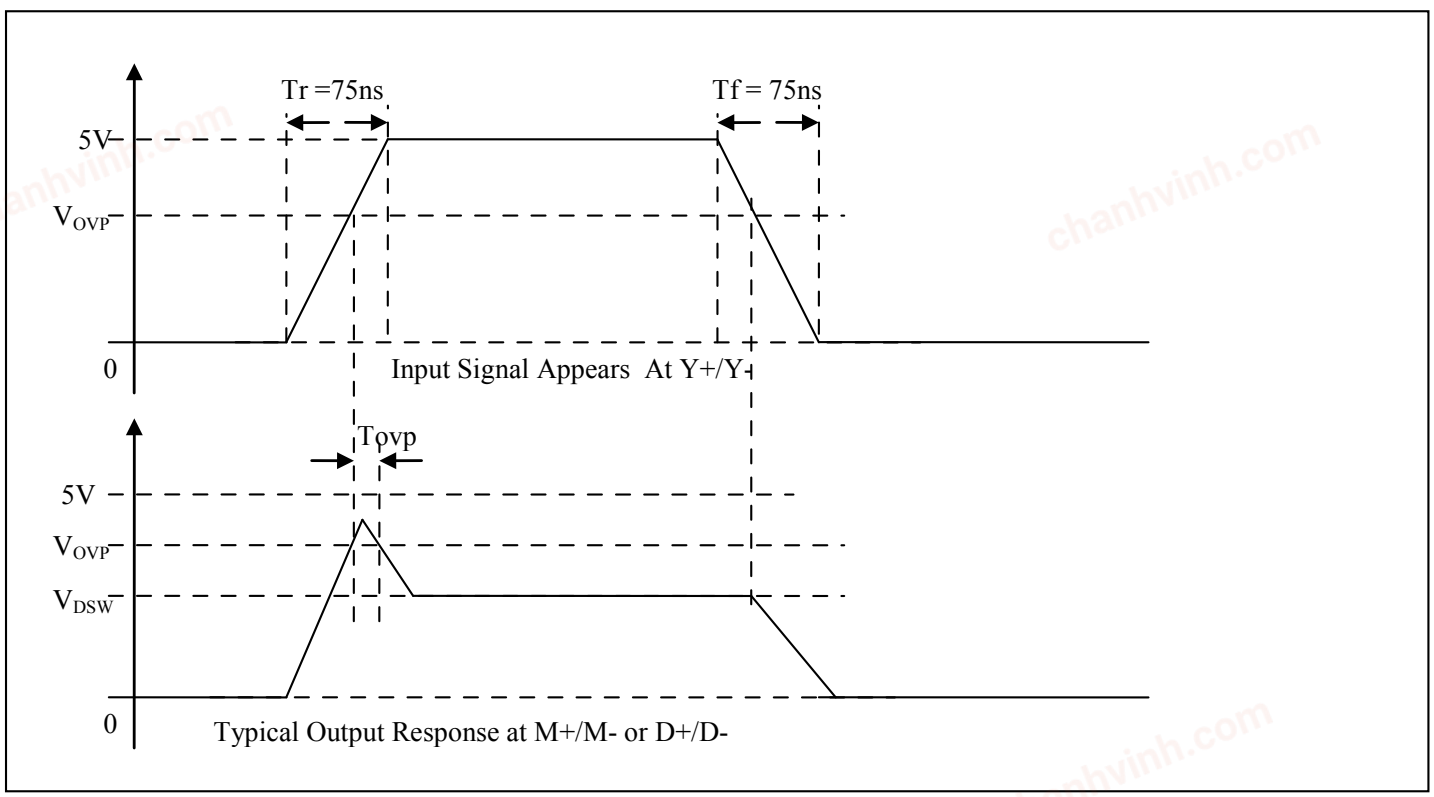


Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Overvoltage Protection Waveforms



The PI3USB102G offers over voltage protection for the Y+/Y- pins to protect from shorts to VBUS (5V). When the voltage on Y+/Y- exceeds V_{OVP}, the voltage at M+/M- and D+/D- is clamped to V_{DSW} within the time T_{OVP}. For rise time of 75 ns (as per USB1.1 and USB2.0 low-speed specifications), T_{OVP} is typically 40 ns. T_{OVP} is smaller for faster risetimes. For example, T_{OVP} is typically 20 ns for rise time of 5 ns.

Part Marking

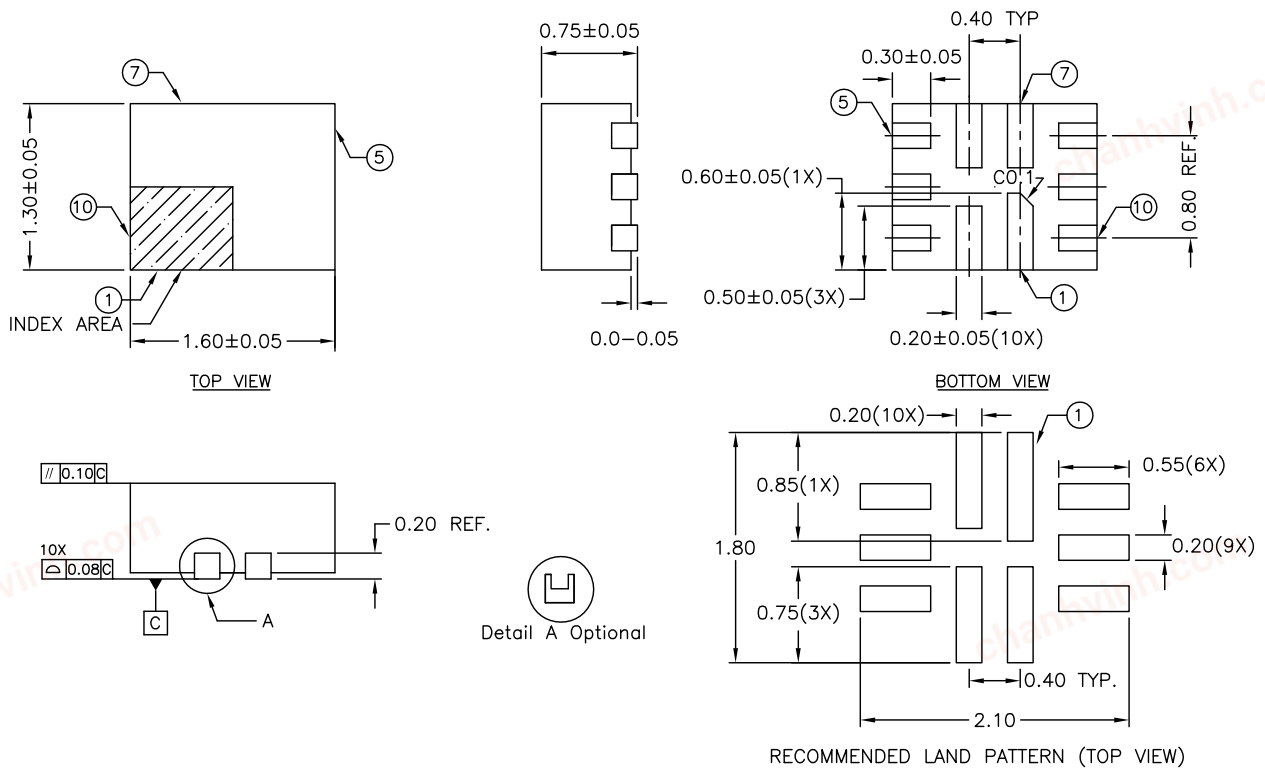
Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

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Packaging Mechanicals

10-TQFN (ZL)



NOTE :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. REFER MO−220.
3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

PERICOM Semiconductor Corporation — DATE: 08/30/13

DESCRIPTION: 10-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL (ZL10)

DOCUMENT CONTROL #: PD-2052 — REVISION: E

13-0175

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description	Top Mark
PI3USB102GZLEX	ZL	10-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)	JW

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
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3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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