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Lead-free Green

**DGD1003**

# HALF-BRIDGE GATE DRIVER IN V-DFN3035-8

## Description

The DGD1003 is a high-voltage / high-speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half-bridge configuration. High voltage processing techniques enable the DGD1003's high side to switch to 150V in a bootstrap operation.

The DGD1003 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver output features high pulse current buffers designed for minimum driver cross conduction. The DGD1003 has a fixed internal deadtime of 420ns (typical).

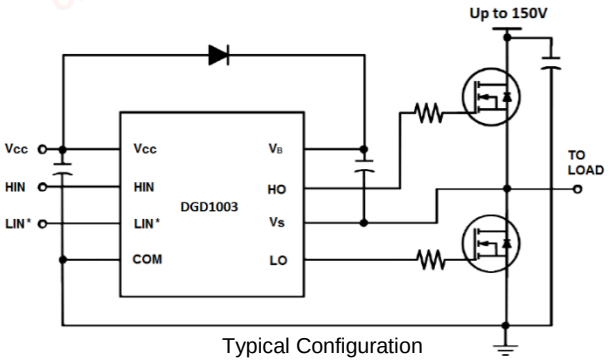
The DGD1003 is offered in the V-DFN3035-8 package and operates over an extended -40°C to +125°C temperature range.

## Features

- Floating High-Side Driver in Bootstrap Operation to 150V
- Drives Two N-Channel MOSFETs or IGBTs in a Half-Bridge Configuration
- 290mA Source/600mA Sink Output Current Capability
- Outputs Tolerant to Negative Transients
- Internal Dead Time of 420ns to Protect MOSFETs
- Wide Low Side Gate Driver Supply Voltage: 10V to 20V
- Logic Input (HIN and LIN*) 3.3V Capability
- Schmitt Triggered Logic Inputs
- Undervoltage Lockout for $V_{CC}$ (Logic and Low Side Supply)
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

## Applications

- DC-DC Converters
- DC-AC Inverters
- AC-DC Power Supplies
- Motor Controls
- Class D Power Amplifiers




Typical Configuration

## Mechanical Data

- Case: V-DFN3035-8
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish—NiPdAu Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.017 grams (Approximate)

V-DFN3035-8



Top View Bottom View

## Ordering Information (Note 4)

| Part Number | Marking | Reel Size (inches) | Tape Width (mm) | Quantity per Reel |
|---|---|---|---|---|
| DGD1003FTA-13 | DGD1003 | 13 | 12 | 5,000 |

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

## Marking Information



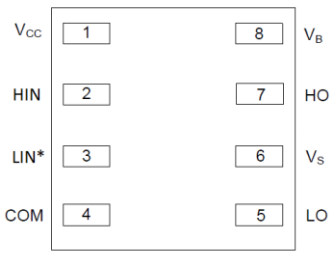

DGD1003 = Product Type Marking Code
YY = Year (ex: 20 = 2020)
WW = Week (01 to 53)


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## Pin Diagrams

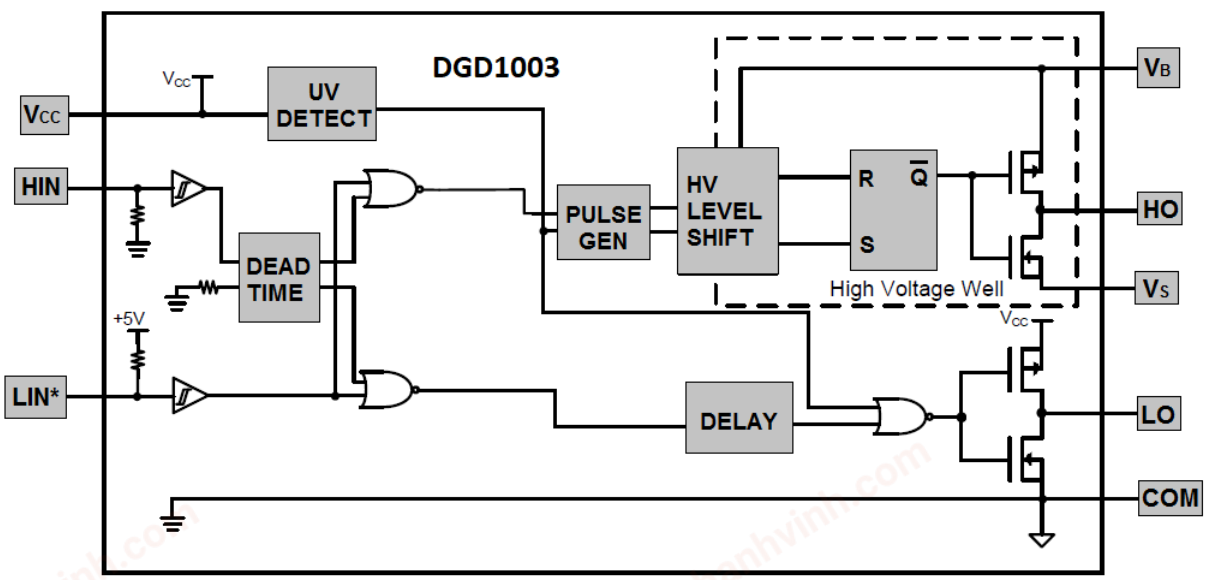



Top View: V-DFN3035-8

## Pin Descriptions

| Pin Number | Pin Name | Function |
|---|---|---|
| 1 | $V_{CC}$ | Logic and Low Side Supply |
| 2 | HIN | Logic Input for High-Side Gate Driver Output in Phase with HO |
| 3 | LIN* | Logic input for Low-Side Gate Driver Output out of Phase with LO |
| 4 | COM | Low-Side and Logic Return |
| 5 | LO | Low-Side Gate Drive Output |
| 6 | $V_S$ | High-Side Floating Supply Return |
| 7 | HO | High-Side Gate Drive Output |
| 8 | $V_B$ | High-Side Floating Supply |

## Functional Block Diagram





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## Absolute Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| High-Side Floating Supply Voltage | $V_B$ | -0.3 to +174 | V |
| High-Side Floating Supply Offset Voltage | $V_S$ | $V_B$-24 to $V_B$+0.3 | V |
| High-Side Floating Output Voltage | $V_{HO}$ | $V_S$-0.3 to $V_B$+0.3 | V |
| Offset Supply Voltage Transient | $dV_S / dt$ | 50 | V/ns |
| Low-Side Fixed Supply Voltage | $V_{CC}$ | -0.3 to +24 | V |
| Low-Side Output Voltage | $V_{LO}$ | -0.3 to $V_{CC}$+0.3 | V |
| Logic Input Voltage (HIN and LIN*) | $V_{IN}$ | -0.3 to $V_{CC}$+0.3 | V |

## Thermal Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Power Dissipation Linear Derating Factor (Note 5) | $P_D$ | 0.44 | W |
| Thermal Resistance, Junction to Ambient (Note 5) | $R_{\theta JA}$ | 231 | °C/W |
| Operating Temperature | $T_J$ | +150 | °C |
| Lead Temperature (Soldering, 10s) | $T_L$ | +300 | |
| Storage Temperature Range | $T_{STG}$ | -55 to +150 | |

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

## Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-Side Floating Supply Absolute Voltage | $V_B$ | $V_S$ + 10 | $V_S$ + 20 | V |
| High-Side Floating Supply Offset Voltage | $V_S$ | (Note 6) | 150 | V |
| High-Side Floating Output Voltage | $V_{HO}$ | $V_S$ | $V_B$ | V |
| Low-Side Supply Voltage | $V_{CC}$ | 10 | 20 | V |
| Low-Side Output Voltage | $V_{LO}$ | 0 | $V_{CC}$ | V |
| Logic Input Voltage (HIN & LIN*) | $V_{IN}$ | 0 | 5 | V |
| Ambient Temperature | $T_A$ | -40 | +125 | °C |

Note: 6. Logic operation for $V_S$ of -5V to +150V.


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## DC Electrical Characteristics ($V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, @$T_A$ = +25°C, unless otherwise specified.) (Note 7)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Logic “1” (HIN) & Logic “0” (LIN*) Input Voltage (Note 8) | $V_{IH}$ | 2.5 | — | — | V | $V_{CC}$ = 10V to 20V |
| Logic “0” (HIN) & Logic “1” (LIN*) Input Voltage (Note 8) | $V_{IL}$ | — | — | 0.8 | V | $V_{CC}$ = 10V to 20V |
| High Level Output Voltage, $V_{BIAS}$ - $V_O$ | $V_{OH}$ | — | 0.05 | 0.2 | V | $I_O$ = 2mA |
| Low Level Output Voltage, $V_O$ | $V_{OL}$ | — | 0.02 | 0.1 | V | $I_O$ = 2mA |
| Offset Supply Leakage Current | $I_{LK}$ | — | — | 50 | µA | $V_B$ = $V_S$ = 150V |
| Quiescent $V_{BS}$ Supply Current | $I_{BSQ}$ | — | 60 | 100 | µA | $V_{IN}$ = 0V or 5V |
| Quiescent $V_{CC}$ Supply Current | $I_{CCQ}$ | — | 350 | 500 | µA | $V_{IN}$ = 0V or 5V |
| Logic “1” Input Bias Current | $I_{IN+}$ | — | 3 | 10 | µA | HIN = 5V, LIN* = 0V |
| Logic “0” Input Bias Current | $I_{IN-}$ | — | — | 5 | µA | HIN = 0V, LIN* = 5V |
| $V_{CC}$ Supply Undervoltage Positive Going Threshold | $V_{CCUV+}$ | 8.0 | 8.9 | 9.8 | V | — |
| $V_{CC}$ Supply Undervoltage Negative Going Threshold | $V_{CCUV-}$ | 7.4 | 8.2 | 9.0 | V | — |
| Output High Short Circuit Pulsed Current | $I_{O+}$ | 130 | 290 | — | mA | $V_O$ = 0V, PW ≤ 10µs |
| Output Low Short Circuit Pulsed Current | $I_{O-}$ | 270 | 600 | — | mA | $V_O$ = 15V, PW ≤ 10µs |

Notes:
7. The $V_{IN}$ and $I_{IN}$ parameters are applicable to the two logic pins: HIN and LIN*. The $V_O$ and $I_O$ parameters are applicable to the respective output pins: HO and LO.
8. For optimal operation, it is recommended that the input pulses (HIN and LIN*) should have a minimum amplitude of 2.5V with a minimum pulse width of 840ns.

## AC Electrical Characteristics ($V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, $C_L$ = 1000pF, @$T_A$ = +25°C, unless otherwise specified.)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Turn-On Propagation Delay | $t_{ON}$ | — | 680 | 820 | ns | $V_S$ = 0V |
| Turn-Off Propagation Delay | $t_{OFF}$ | — | 150 | 220 | ns | $V_S$ = 150V |
| Delay Matching, HO & LO Turn-On/Turn-Off | $t_{DM}$ | — | — | 60 | ns | — |
| Turn-On Rise Time | $t_r$ | — | 70 | 170 | ns | $V_S$ = 0V |
| Turn-Off Fall Time | $t_f$ | — | 35 | 90 | ns | $V_S$ = 0V |
| Deadtime: $t_{DT\ LO-HO}$ & $t_{DT\ HO-LO}$ | $t_{DT}$ | 300 | 420 | 650 | ns | — |


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## Timing Waveforms

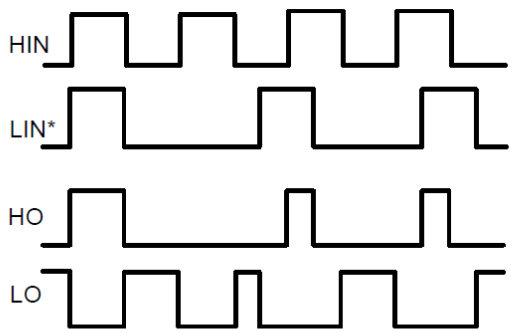



**Figure 1.** Input / Output Timing Diagram

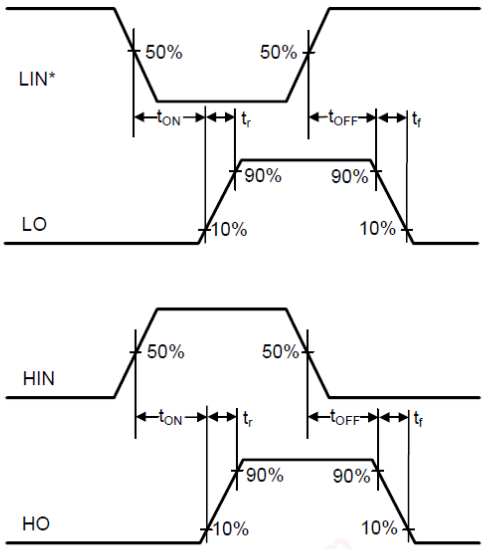



**Figure 2.** Switching Time Waveform Definitions

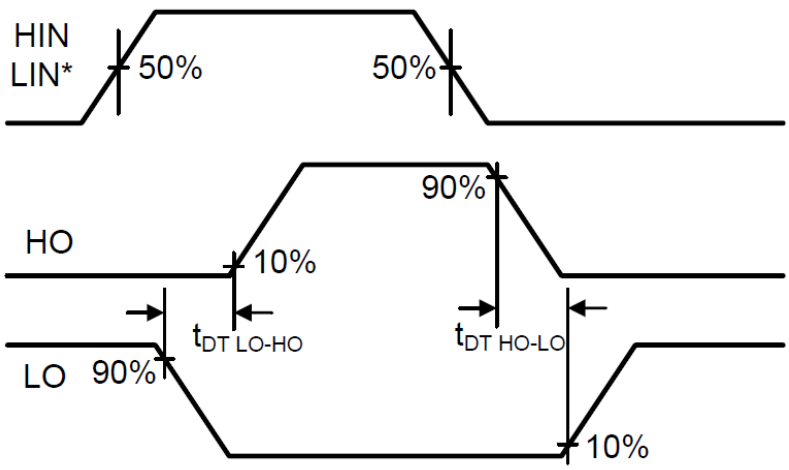



**Figure 3.** Deadtime Waveform Definitions


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## Typical Performance Characteristics ($V_{CC}$ = 15V, @$T_A$ = +25°C, unless otherwise specified.)

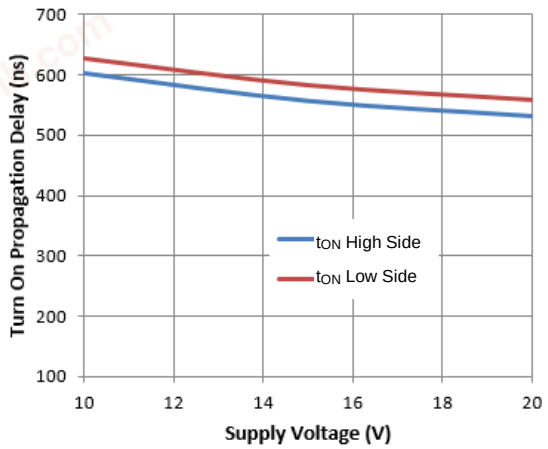



**Figure 4.** Turn-on Propagation Delay vs. Supply Voltage

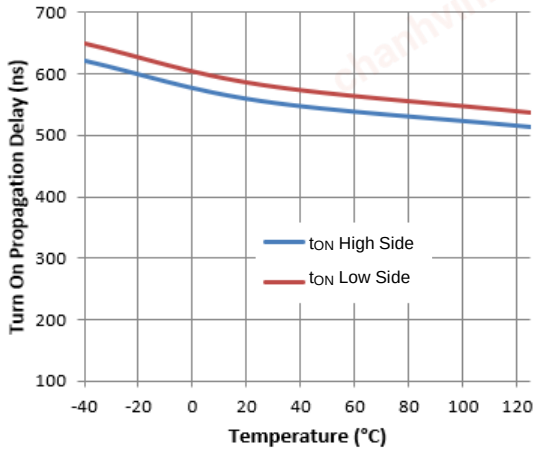



**Figure 5.** Turn-on Propagation Delay vs. Temperature

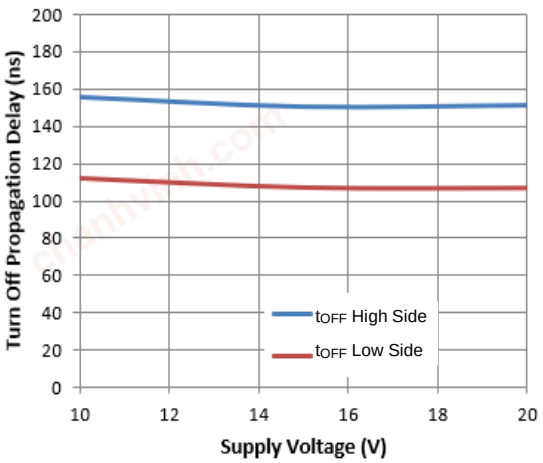



**Figure 6.** Turn-off Propagation Delay vs. Supply Voltage

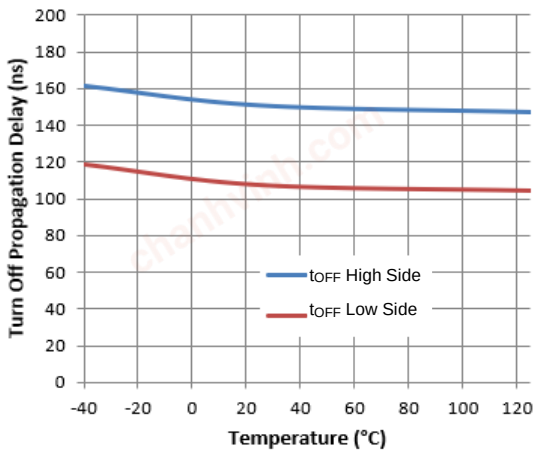



**Figure 7.** Turn-off Propagation Delay vs. Temperature

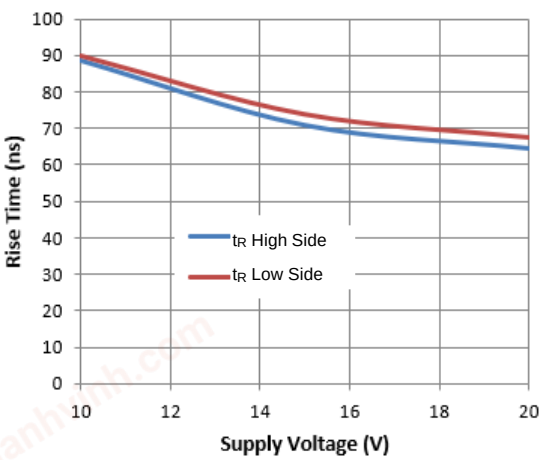



**Figure 8.** Rise Time vs. Supply Voltage

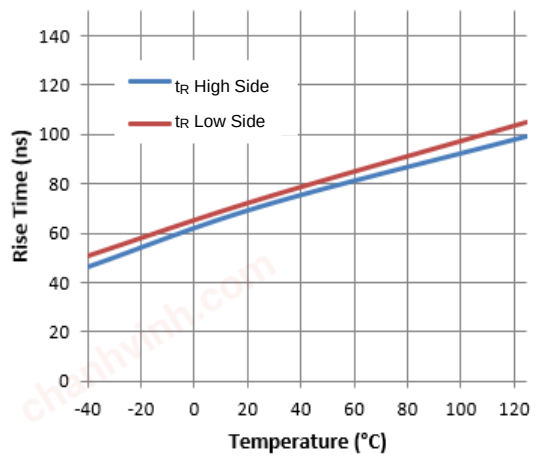



**Figure 9.** Rise Time vs. Temperature


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## Typical Performance Characteristics (continued)

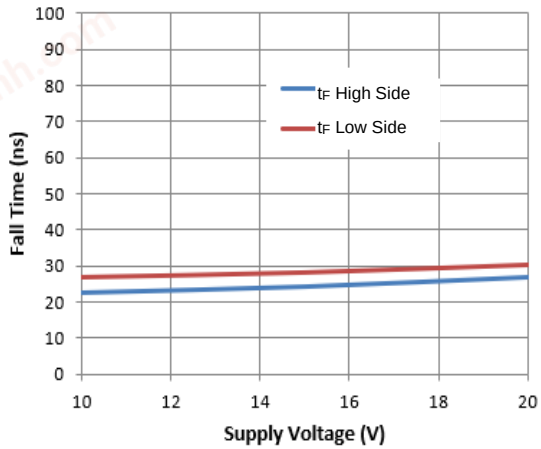



**Figure 10.** Fall Time vs. Supply Voltage

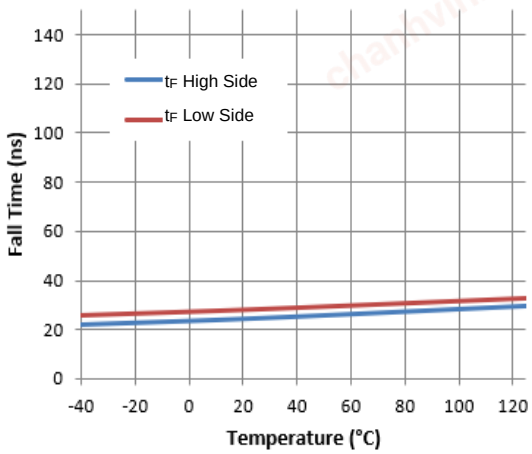



**Figure 11.** Fall Time vs. Temperature

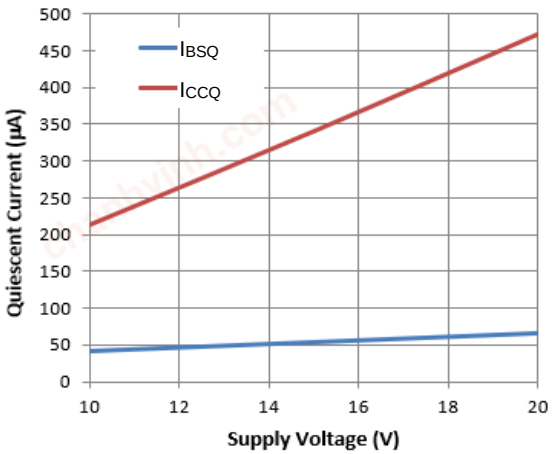



**Figure 12.** Quiescent Current vs. Supply Voltage

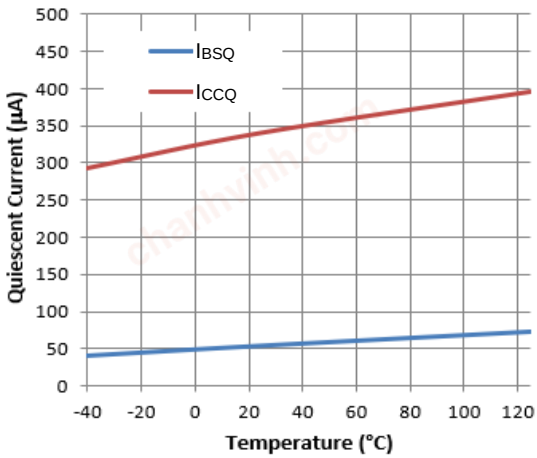



**Figure 13.** Quiescent Current vs. Temperature

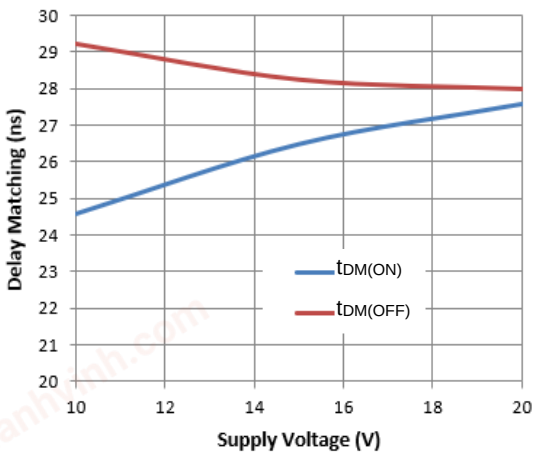



**Figure 14.** Delay Matching vs. Supply Voltage

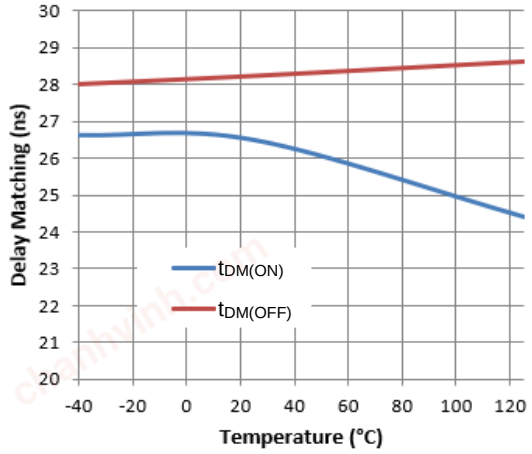



**Figure 15.** Delay Matching vs. Temperature


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## Typical Performance Characteristics (continued)

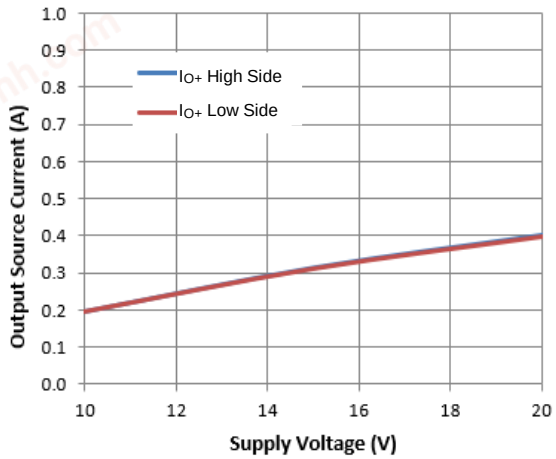



**Figure 16.** Output Source Current vs. Supply Voltage

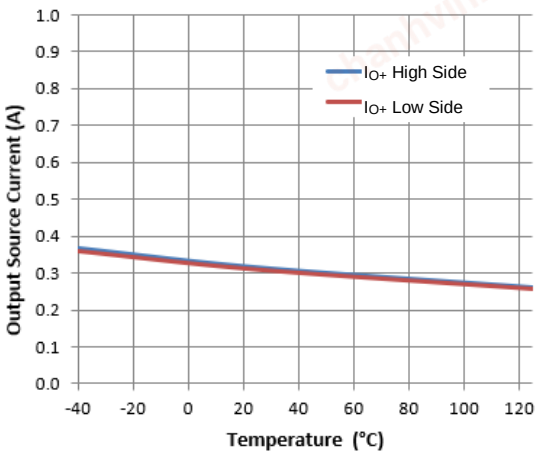



**Figure 17.** Output Source Current vs. Temperature

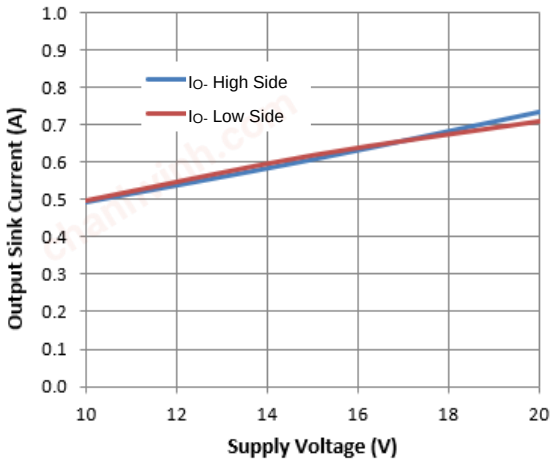



**Figure 18.** Output Sink Current vs. Supply Voltage

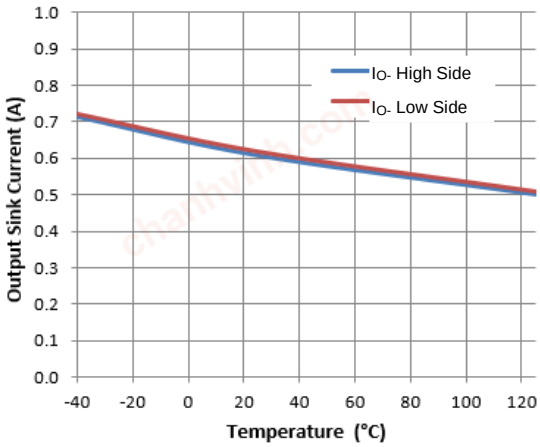



**Figure 19.** Output Sink Current vs. Temperature

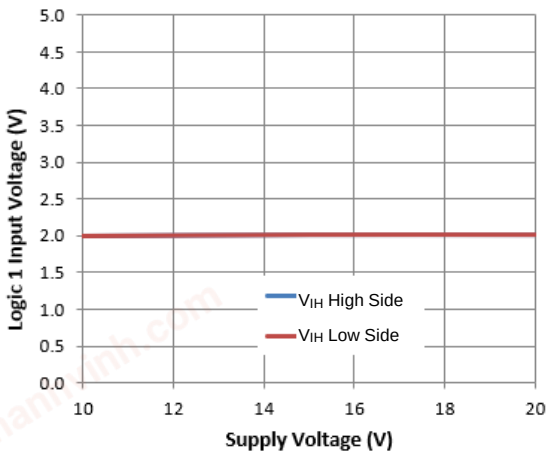



**Figure 20.** Logic 1 Input Voltage vs. Supply Voltage

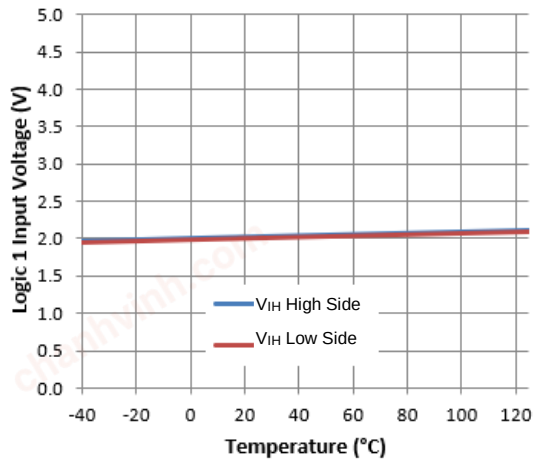



**Figure 21.** Logic 1 Input Voltage vs. Temperature


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## Typical Performance Characteristics (continued)

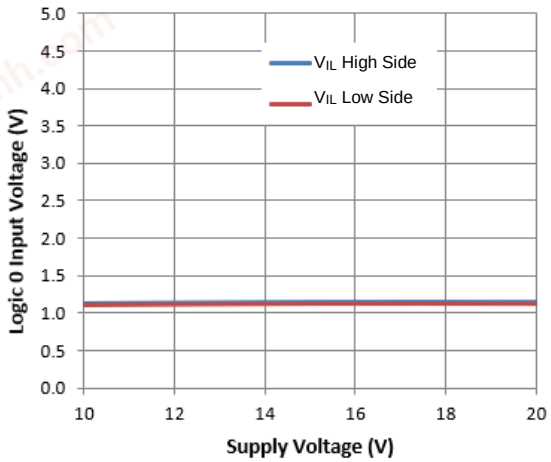



**Figure 22.** Logic 0 Input Voltage vs. Supply Voltage

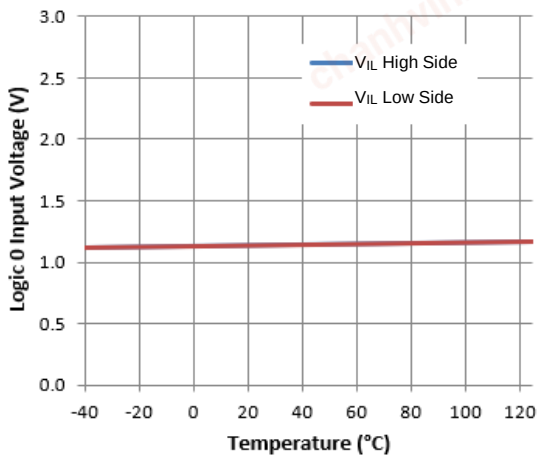



**Figure 23.** Logic 0 Input Voltage vs. Temperature

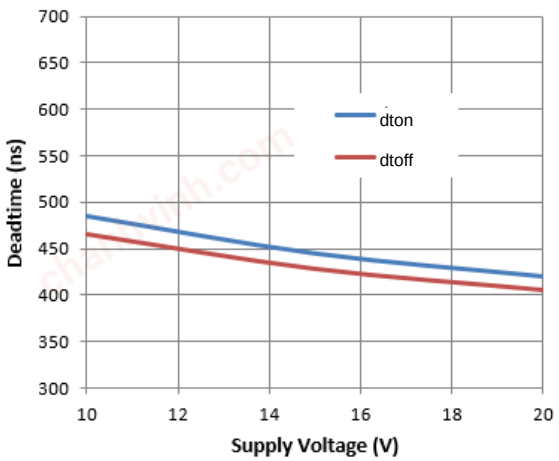



**Figure 24.** Deadtime vs. Supply Voltage

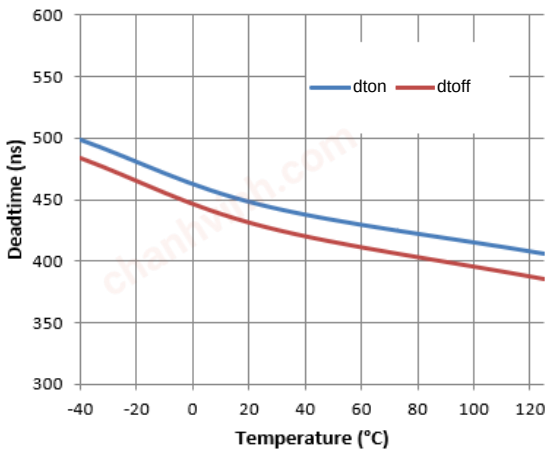



**Figure 25.** Deadtime vs. Temperature

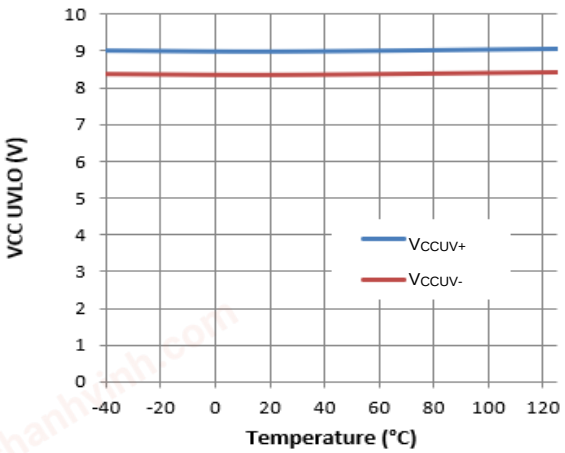



**Figure 26.** VCC UVLO vs. Temperature

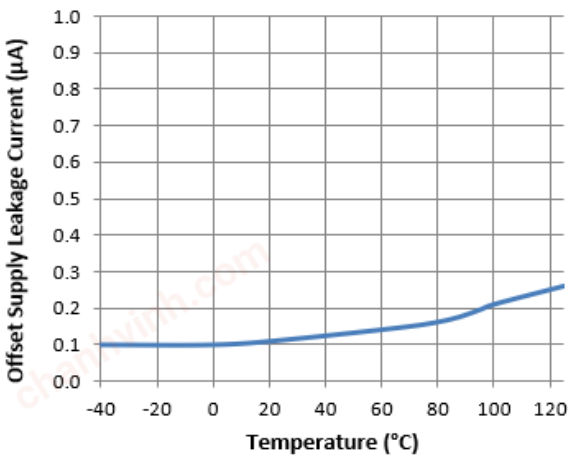



**Figure 27.** Offset Supply Leakage Current vs. Temperature


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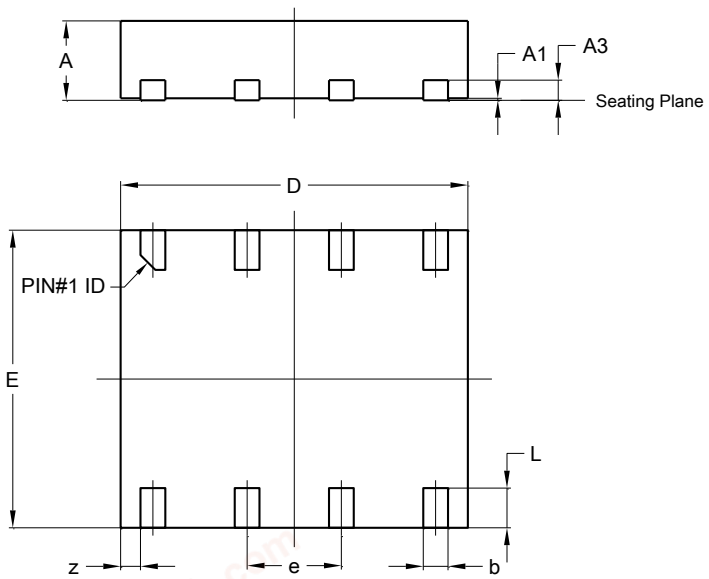
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## Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

**V-DFN3035-8**



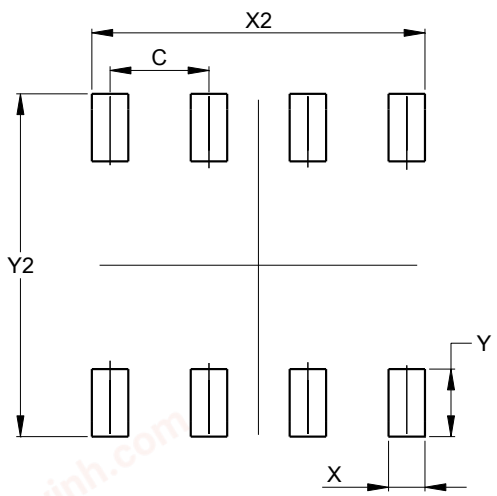

| V-DFN3035-8 | | | |
|---|---|---|---|
| **Dim** | **Min** | **Max** | **Typ** |
| **A** | 0.75 | 0.85 | 0.80 |
| **A1** | 0.00 | 0.05 | 0.03 |
| **A3** | 0.203 REF | | |
| **b** | 0.20 | 0.30 | 0.25 |
| **D** | 3.45 | 3.55 | 3.50 |
| **E** | 2.95 | 3.05 | 3.00 |
| **e** | -- | -- | 0.95 |
| **L** | 0.35 | 0.45 | 0.40 |
| **z** | -- | -- | 0.20 |
| **All Dimensions in mm** | | | |

`

## Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

**V-DFN3035-8**




| Dimensions | Value (in mm) |
|---|---|
| **C** | 0.95 |
| **X** | 0.35 |
| **X2** | 3.20 |
| **Y** | 0.65 |
| **Y2** | 3.30 |


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