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HCPL-2300, HCPL-0300

8 MBd Low Input Current Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

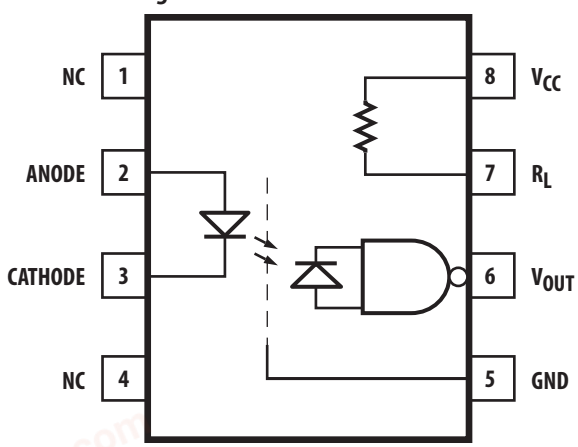
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-2300/HCPL-0300 optocoupler combines an 820 nm AlGaAs photon emitting diode with an integrated high gain photon detector. This combina-tion of Avago designed and manufactured semiconductor devices brings new high performance capabilities to designers of isolated logic and data communication circuits.

The new low current, high speed AlGaAs emitter manufactured with a unique diffused junction, has the virtue of fast rise and fall times at low drive currents. Figure 6 illustrates the propagation delay vs. input current characteristic. These unique characteristics enable this device to be used in an RS-232-C interface with ground loop isolation and improved common mode rejection. As a line receiver, the HCPL-2300/HCPL-0300 will operate over longer line lengths for a given data rate because of lower I_F and V_F specifications.

Functional Diagram



A 0.1 pF bypass capacitor must be connected between pins 5 and 8.

Features

- Guaranteed low thresholds: I_F = 0.5 mA, $V_F \leq$ 1.5 V
- High speed: guaranteed 5 MBd over temperature
- Versatile: compatible with TTL, LSTTL and CMOS
- Efficient 820 nm AlGaAs LED
- Internal shield for guaranteed common mode rejection
- Schottky clamped, open collector output with optional integrated pull-up resistor
- Static and dynamic performance guaranteed from -40°C to 85°C
- Safety approval
  - UL recognized -3750 V rms for 1 minute
  - CSA approved
  - IEC/EN/DIN EN60747-5-5 approved with V_{IORM} = 630 V_{peak} (Option 060)

Applications

- Ground loop elimination
- Computer-peripheral interfaces
- Level shifting
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- RS-232-C interface
- High speed, long distance isolated line receiver

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

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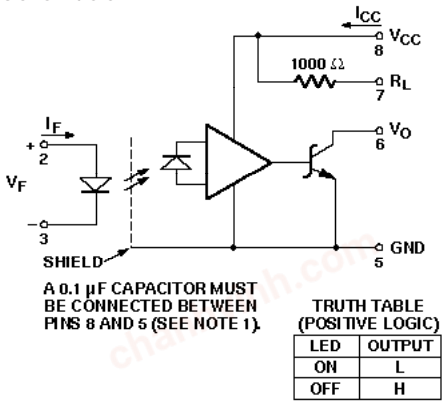
Schematic



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

The output of the shielded integrated detector circuit is an open collector Schottky clamped transistor. The shield, which shunts capacitively coupled common mode noise to ground, provides a guaranteed transient immunity specification of 100 V/µs. The output circuit includes an optional integrated 1000 Ω pull-up resistor for the open collector. This gives designers the flexibility to use the internal resistor for pull-up to five volt logic or to use an external resistor for connection to supply voltages up to 18 V (CMOS logic voltage).

The Electrical and Switching Characteristics of the HCPL-2300/HCPL-0300 are guaranteed over a temperature range of -40°C to 85°C. This enables the user to confidently design a circuit which will operate under a broad range of operating conditions.

Ordering Information

HCPL-xxxx is UL Recognized with 3750 Vrms for 1 minute per UL1577 and are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	non RoHS Compliant							
HCPL-2300	-000E	no option	300 mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-0300	-000E	no option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry. Combination of Option 020 and Option 060 is not available.

Example 1:

HCPL-2300-560E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use '–XXXE.'

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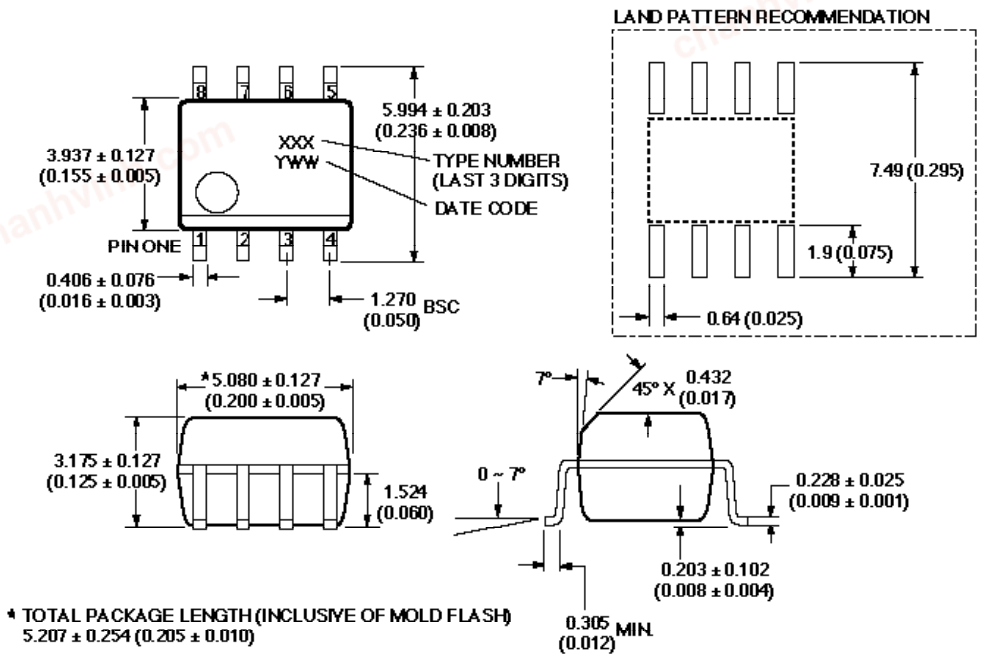
Package Outline Drawings

Small Outline SO-8 Package HCPL-0300



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

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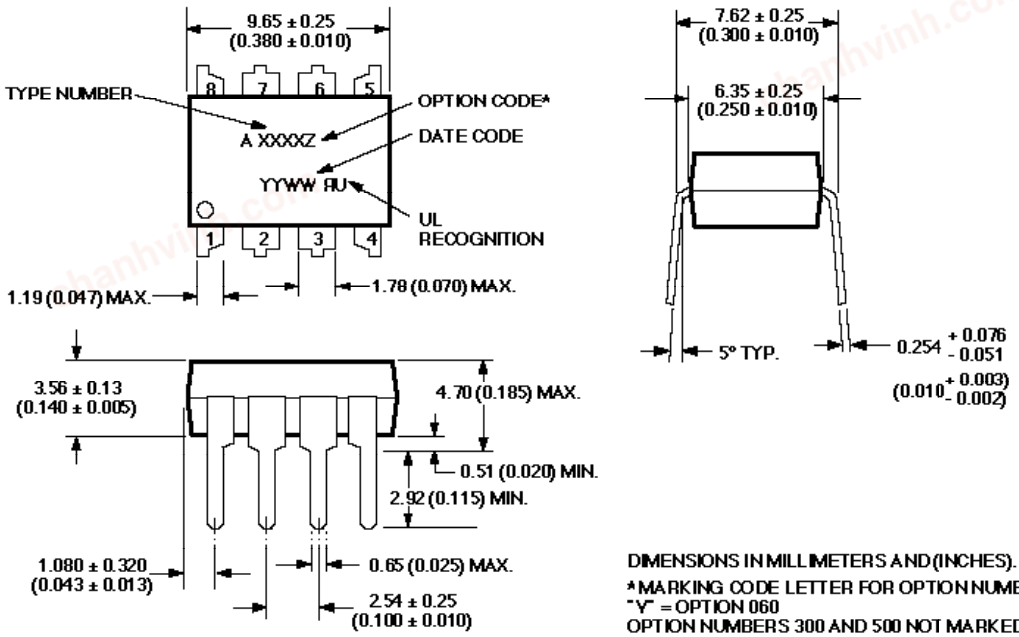
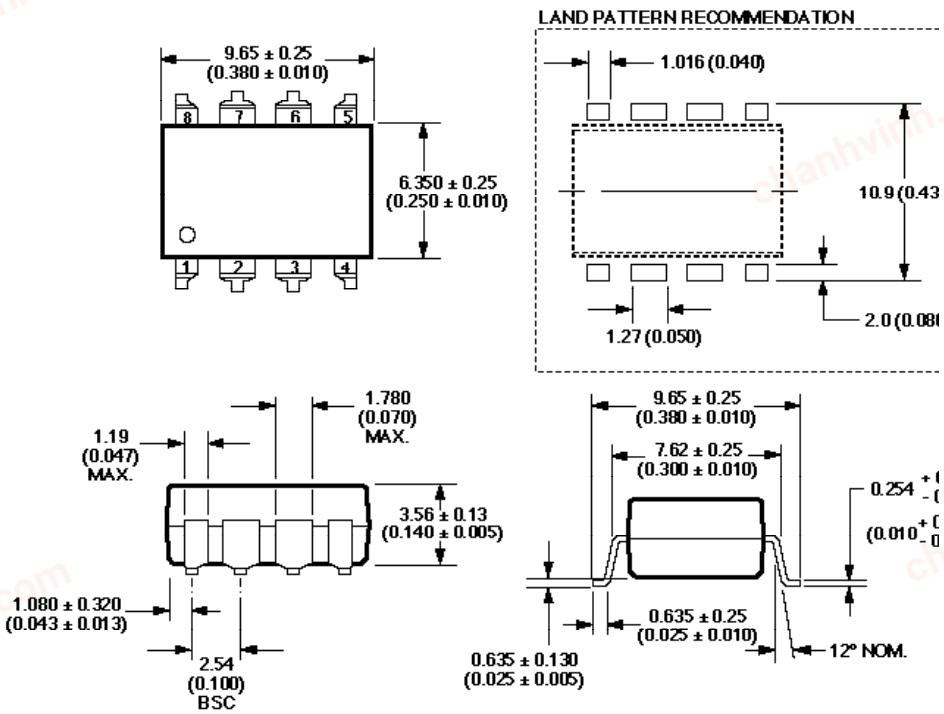
8-Pin DIP Package (HCPL-2300)



DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2300)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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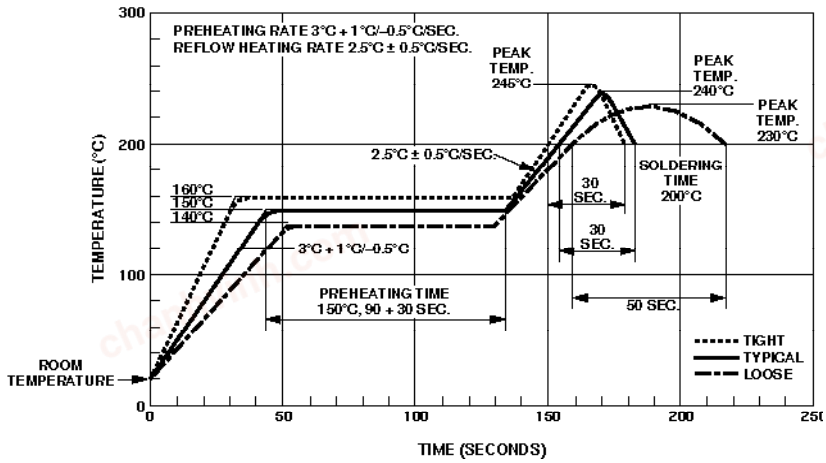
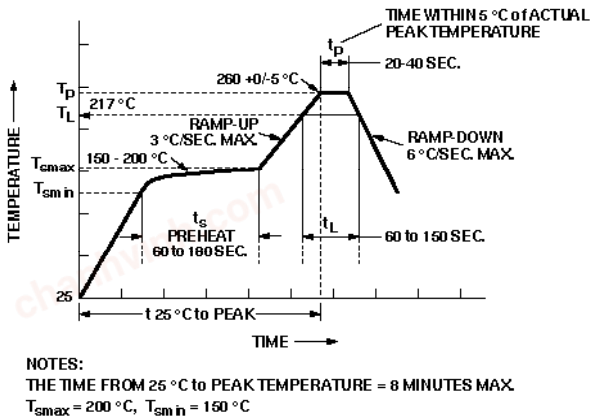
Solder Reflow Temperature Profile



Note: Non-halide flux should be used.

Recommended Pb-Free IR Profile



Note: Non-halide flux should be used.

Regulatory Information

The HCPL-2300 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5

Maximum Working Insulation Voltage V_{IORM} = 630V_{peak}

(Option 060 only)

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

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IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics (HCPL-2300 Option 060 only)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage ≤300 V_{rms} for rated mains voltage ≤600 V_{rms}		 I-IV I-IV	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and sample test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1008	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 11, Thermal Derating curve.) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at TS, VIO = 500 V	RS	≥109	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-5, for a detailed description.

Note:

Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

(No Derating Required up to 55°C)

Description	Min.	Typ.	Max.	Units
Storage Temperature	-55°C		+125°C	T_S
Operating Temperature	-40°C		+85°C	T_A
Lead Solder Temperature (1.6 mm below seating plane)		260°C for 10 s		max
Average Forward Input Current		5 mA [2]		- I_F
Reverse Input Voltage			3.0 V	V_R
Supply Voltage	0 V		7.0 V	V_{CC}
Pull-Up Resistor Voltage	-0.5 V		VCC	V_{RL}
Output Collector Current	-25 mA		25 mA	I_O
Input Power Dissipation		10 mW		P_I
Output Collector Power Dissipation		40 mW		P_O
Output Collector Voltage	-0.5 V		18 V	V_O

Infrared and Vapor Phase Reflow Temperature (Option #300) see Fig. 1, Thermal Profile

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Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units
Input Voltage, Low Level		V_{FL}	-2.5	0.8	V
Input Current High Level	0°C to 85°C	I_{FH}	0.5	1.0	mA
	-40°C to 85°C		0.5	0.75	
Supply Voltage, Output		V_{CC}	4.75	5.25	V
Fan Out (TTL Load)		N		5	
Operating Temperature		T_A	-40	85	°C

DC Electrical Specifications

For -40°C ≤ T_A ≤ 85°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.

All typicals at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified. See note 1.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		0.05	250	µA	V_F = 0.8 V, V_O = 18 V	4	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_F = 0.5 mA I_{OL} (Sinking) = 8 mA		3
High Level Supply Current	I_{CCH}		4.0	6.3	mA	I_F = 0 mA, V_{CC} = 5.25 V		
Low Level Supply Current	I_{CCL}		6.2	10.0	mA	I_F = 1.0 mA, V_{CC} = 5.25 V		
Input Forward Voltage	V_F	1.0	1.3	1.5	V	T_A = 25°C I_F = 1.0 mA	2	
			0.85	1.65				
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 1.0 mA		
Input Reverse Breakdown Voltage	BV_R	3.0			V	I_R = 10 µA		
Input Capacitance	C_{IN}		18		pF	V_F = 0 V, f = 1 MHz		
Internal Pull-up Resistor	R_L	680	1000	1700	Ω	T_A = 25°C		

Switching Specifications

For -40°C ≤ T_A ≤ 85°C, 0.5 mA ≤ I_{FH} ≤ 0.75 mA; For 0°C ≤ T_A ≤ 85°C, 0.5 mA ≤ I_{FH} ≤ 1.0 mA; With 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.

All typicals at T_A = 25°C and V_{CC} = 5 V, I_{FH} = 0.625 mA, unless otherwise specified. See note 1.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time	t_{PLH}		95		ns	C_P = 0 pF	5, 6, 8	4, 8
			85	160		C_P = 20 pF	5, 8	
Propagation Delay Time	t_{PHL}		110		ns	C_P = 0 pF	5, 6, 8	5, 8
			35	200		C_P = 20 pF	5, 8	
Output Rise Time (10-90%)	t_r		40		ns	C_P = 20 pF	7, 8	8
Output Fall Time (90-10%)	t_f		20		ns			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	100	400		V/µs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 560 Ω, I_F = 0 mA	9, 10	6
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	100	400		V/µs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 560 Ω, I_F = 0.5 mA	9, 10	7

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Package Characteristics

For -40°C ≤T_A ≤85°C, unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V_{rms}	RH ≤ 50%, t = 1 min, T_A = 25°C		3, 9
Resistance, Input-Output	R_{I-O}		1012		Ω	V_{I-O} = 500 V		3
Capacitance, Input-Output	C_{I-O}		0.6		pF	f = 1 MHz		3

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), your equipment level safety specification, or Avago Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Bypassing the power supply line is required with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 19. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.5 µF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 100 mA, 500 ns maximum pulse width, provided average current does not exceed 5 mA.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
7. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
8. C_P is the peaking capacitance. Refer to test circuit in Figure 8.
9. In accordance with UL 1577, each optocoupler is momentary withstand proof tested by applying an insulation test voltage ≥4500 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.

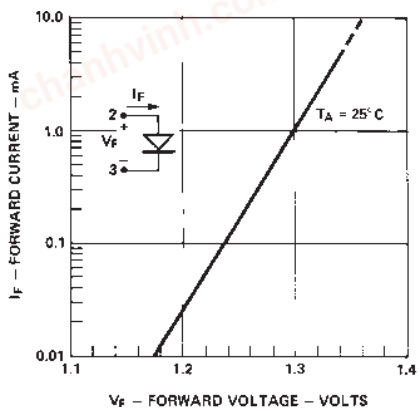

Figure 2. Typical input diode forward characteristics.

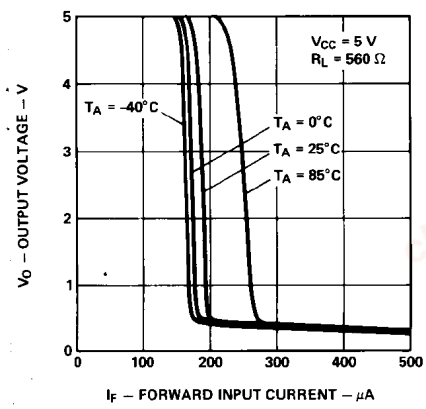

Figure 3. Typical output voltage vs. forward input current vs. temperature.

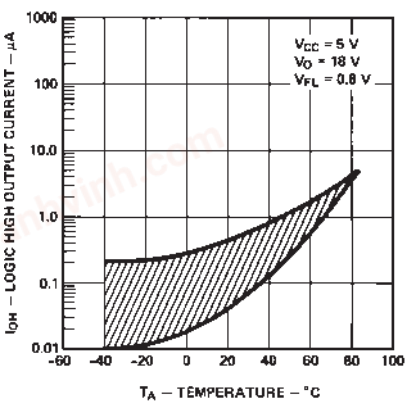

Figure 4. Typical logic high output current vs. temperature.

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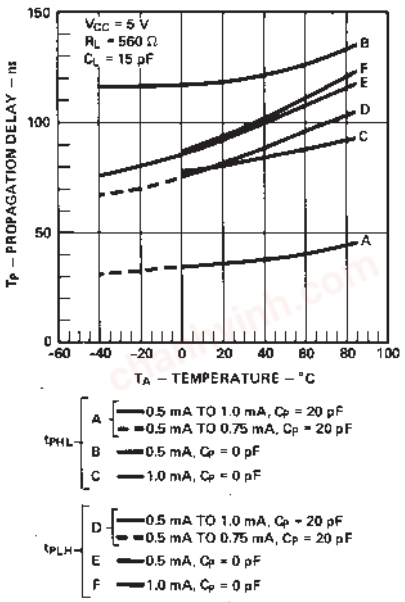

Figure 5. Typical propagation delay vs. temperature and forward current with and without application of a peaking capacitor.

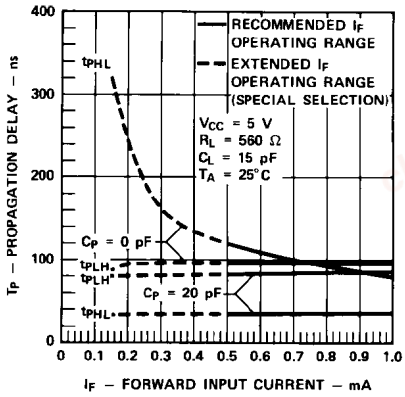

Figure 6. Typical propagation delay vs. forward current.

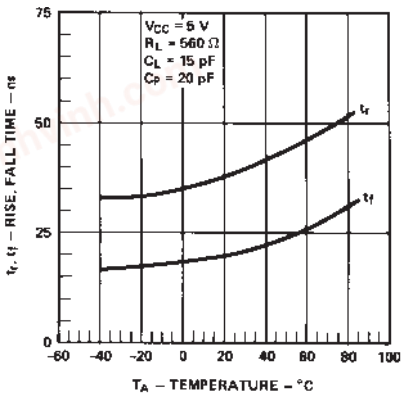

Figure 7. Typical rise, fall time vs. temperature.

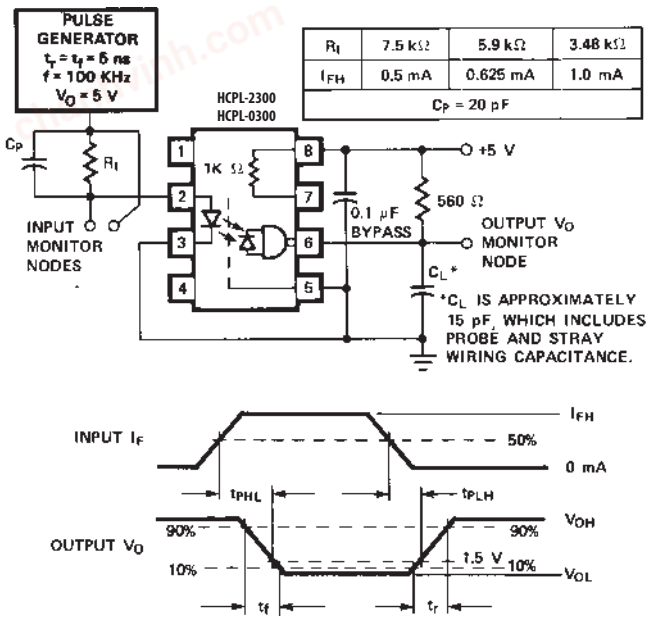

Figure 8. Test Circuit for t_{PHL}, t_{PLH}, t_r, and t_f.

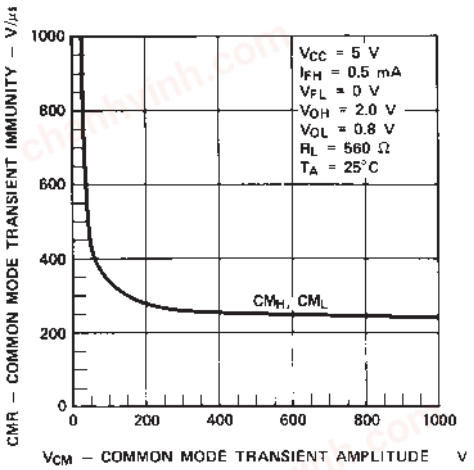

Figure 9. Typical common mode transient immunity vs. common mode transient amplitude.

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Applications

The HCPL-2300/HCPL-0300 optocoupler has the unique combination of low 0.5 mA LED operating drive current at a 5 MBd speed performance. Low power supply current requirement of 10 mA maximum at 5.25 V and the ability to provide isolation between logic systems fulfills numerous applications ranging from logic level translations, line receiver and party line receiver applications, microprocessor I/O port isolation, etc. The open collector output allows for wired-OR arrangement. Specific interface circuits are illustrated in Figures 12-16, and 18 with corresponding component values, performance data and recommended layout in Figures 17 and 19.

For -40°C to 85°C operating temperature range, a mid-range LED forward current (I_F) of 0.625 mA is recommended in order to prevent overdriving the integrated circuit detector due to increased LED efficiency at temperatures between 0°C and -40°C. For narrower temperature range of 0°C to 85°C, a suggested operating LED current of 0.75 mA is recommended for the mid-range operating point and for minimal propagation delay skew.

A peaking capacitance of 20 pF in parallel with the current limiting resistor for the LED shortens t_{PHL} by approximately 33% and t_{PLH} by 13%. Maintaining LED forward voltage (V_F) below 0.8 V will guarantee that the HCPL-2300/HCPL-0300 output is off.

The recommended shunt drive technique for TTL/LSTTL/CMOS of Figure 12 provides for optimal speed performance, no leakage current path through the LED, and reduced common mode influences associated with series switching of a "floating" LED. Alternate series drive techniques with either an active CMOS inverter or an open collector TTL/LSTTL inverter are illustrated in Figures 13 and 14 respectively. Open collector leakage current of 250 µA has been compensated by the 3.16 KΩ resistor (Figure 14) at the expense of twice the operating forward current.

An application of the HCPL-2300/HCPL-0300 as an unbalanced line receiver for use in long line twisted wire pair communication links is shown in Figure 15. Low LED I_F and V_F allow longer line length, higher speed and multiple stations on the line in comparison to higher I_F, V_F optocouplers. Greater speed performance along with nearly infinite common mode immunity are achieved via the balanced split phase circuit of Figure 16. Basic balanced differential line receiver can be accomplished with one HCPL-2300/HCPL-0300 in Figure 16, but with a typical 400 V/µs common mode immunity. Data rate versus distance for both the above unbalanced and balanced line receiver applications are compared in Figure 17. The RS-232-C interface circuit of Figure 18 provides guaranteed minimum common mode immunity of 100 V/µs while maintaining the 2:1 dynamic range of I_F.

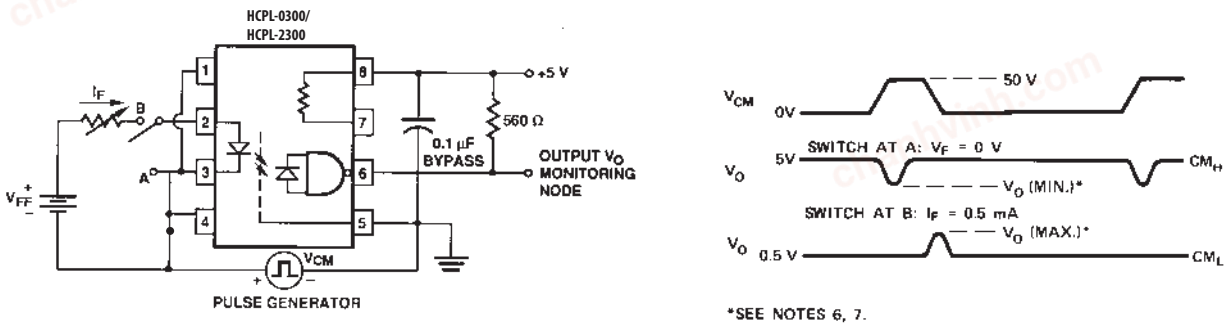

Figure 10. Test circuit for common mode transient immunity and typical waveforms.

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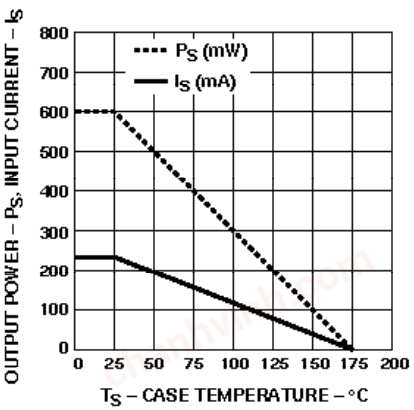
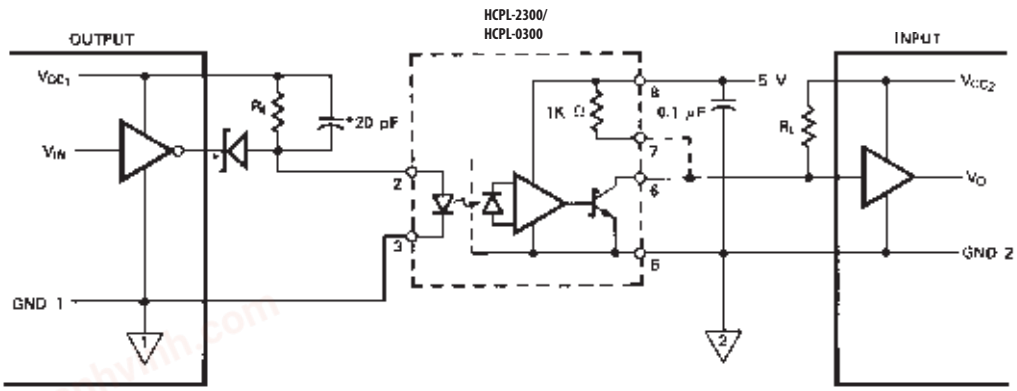


Figure 11. Thermal derating curve, dependence of safety limiting value with case temperature per IEC/EN/DIN EN 60747-5-5.

A recommended layout for use with an internal 1000 Ω resistor or an external pull-up resistor and required V_{CC} bypass capacitor is given in Figure 19. V_{CC1} is used with an external pull-up resistor for output voltage levels (V_O) greater than or equal to 5 V. As illustrated in Figure 19, an optional V_{CC} and GND trace can be located between the input and the output leads of the HCPL-2300/HCPL-0300 to provide additional noise immunity at the compromise of insulation capability (V_{I-O}).



V_{IN} V_{DC}	V_{CC1} V_{DC}	R_I kΩ	R_L kΩ	V_{CC2} V_{DC}
5	5	6.19	↑ (INTERNAL)	5
10	10	14.7	2.37	10
15	15	21.5	3.16	15

*SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT) AND 20 pF CAPACITOR ARE NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 12. Recommended shunt drive circuit for interfacing between TTL/LSTTL/CMOS logic systems.

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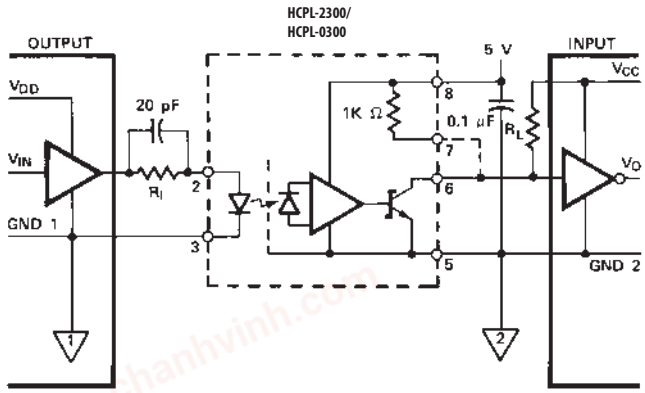


V_{IN} V_{DC}	V_{DD} V_{DC}	R_I kΩ	R_L kΩ	V_{CC} V_{DC}
5	5	5.11	1 (INTERNAL)	5
10	10	13.3	2.37	10
15	15	19.6	3.16	15

Figure 13. Active CMOS series drive circuit.

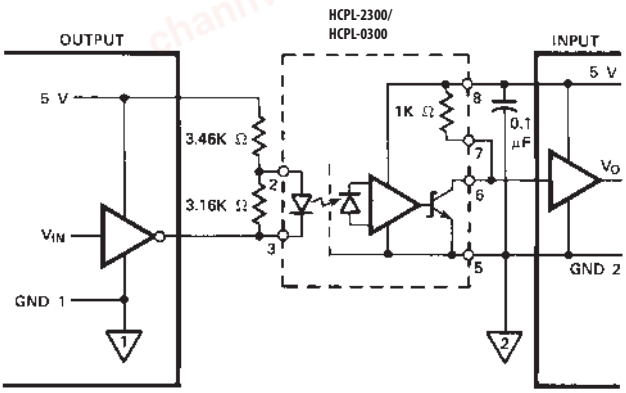
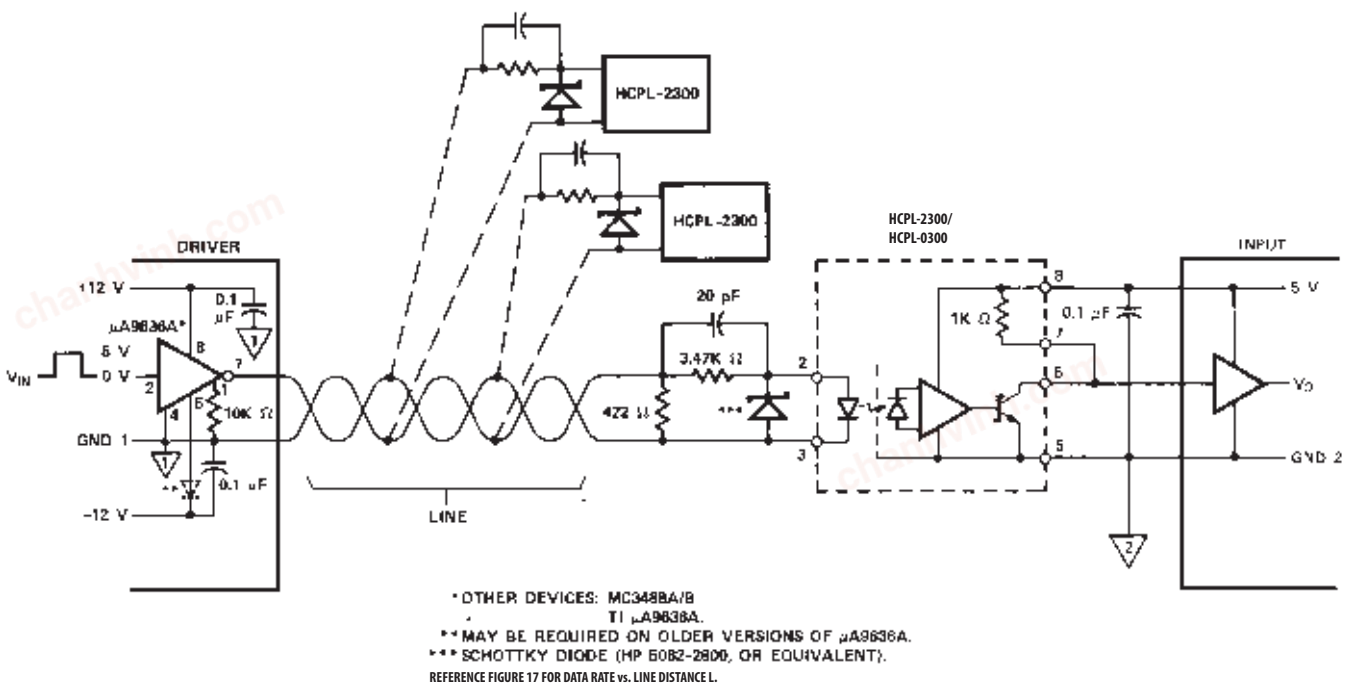


Figure 14. Series drive from open collector TTL/LSTTL units.



*OTHER DEVICES: MC3488A/B
TI μA9636A.
**MAY BE REQUIRED ON OLDER VERSIONS OF μA9636A.
***SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT).
REFERENCE FIGURE 17 FOR DATA RATE vs. LINE DISTANCE L.

Figure 15. Application of HCPL-2300/HCPL-0300 as isolated, unbalanced line receiver(s).

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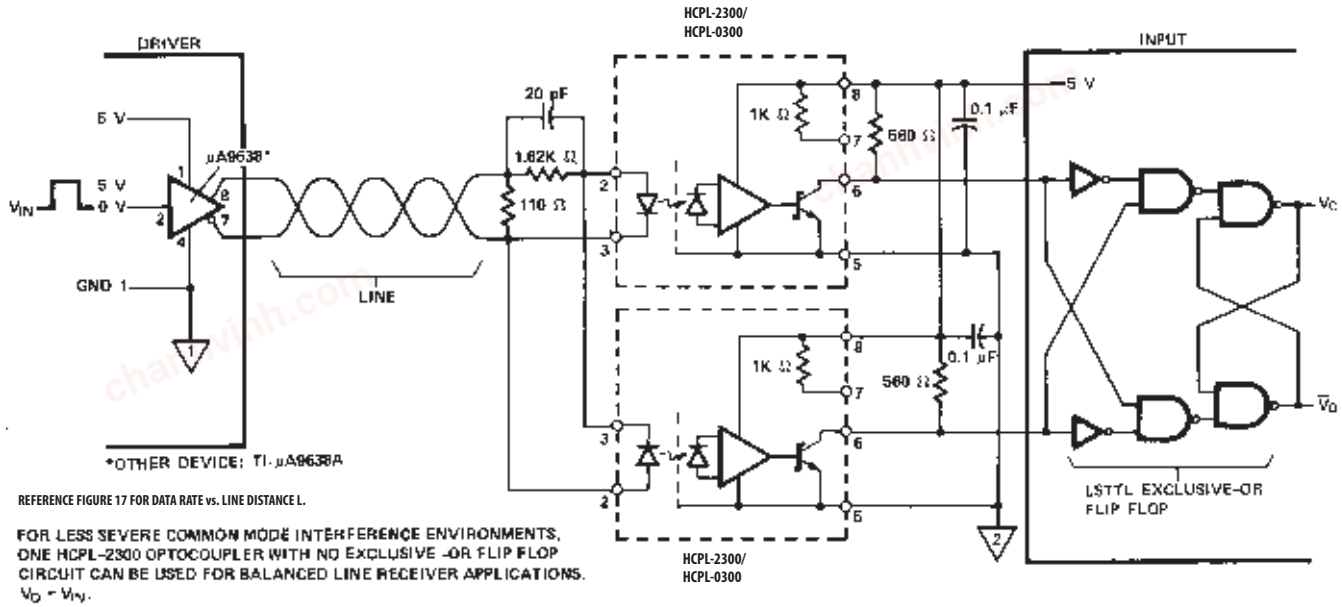

Figure 16. Application of two HCPL-2300/HCPL-0300 units operating as an isolated, high speed, balanced, split phase line receiver with significantly enhanced common mode immunity.

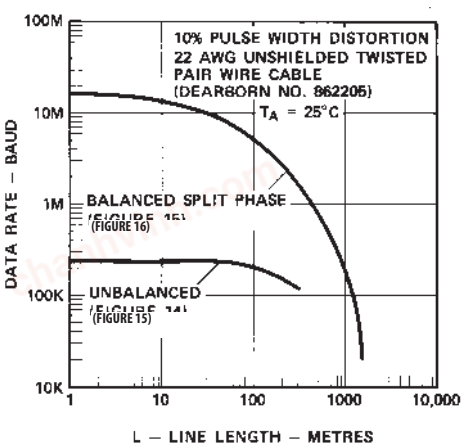

Figure 17. Typical point to point data rate vs. length of line for unbalanced (Figure 15) and balanced (Figure 16) line receivers using HCPL-2300/HCPL-0300 optocouplers.

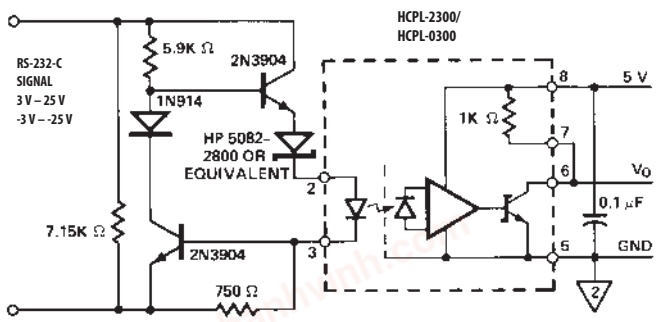

Figure 18. RS-232-C Interface circuit with HCPL-2300/HCPL-0300. 0°C < T_A < 85°C.

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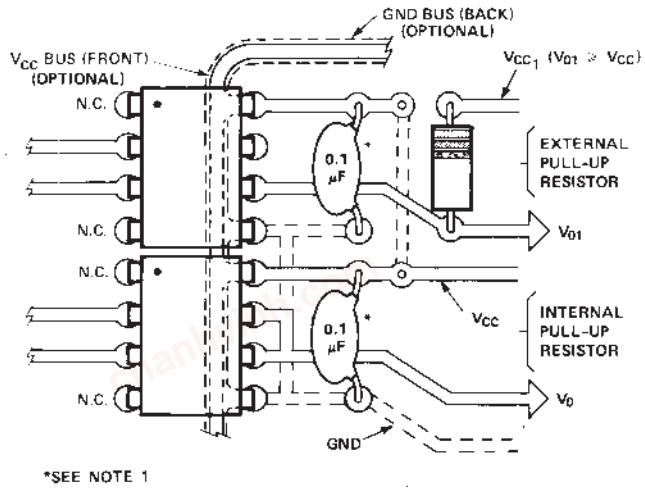

Figure 19. Recommended printed circuit board layout.

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AV02-0919EN March 20, 2013