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HFBR-57E0LZ/ALZ/PZ/APZ

Multimode Small Form Factor Pluggable Transceivers with LC connector for ATM, FDDI, Fast Ethernet and SONET OC-3/SDH STM-1

Data Sheet



Description

The HFBR-57E0 Small Form Factor Pluggable LC transceivers provide the system designer with a product to implement a range of solutions for multimode fiber Fast Ethernet and SONET OC-3 (SDH STM-1) physical layers for ATM and other services.

This transceiver operates at a nominal wavelength of 1300 nm with an LC fiber connector interface with an external connector shield (HFBR-57E0).

Transmitter Section

The transmitter section of the HFBR-57E0 utilizes a 1300 nm InGaAsP LED. This LED is packaged in the optical subassembly portion of the transmitter section. It is driven by a custom silicon IC which converts differential PECL logic signals, ECL referenced (shifted) to a +3.3 V supply, into an analog LED drive current.

Receiver Section

The receiver section of the HFBR-57E0 utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. It is packaged in the optical subassembly portion of the receiver.

This PIN/preamplifier combination is coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Loss of Signal (LOS) function. The data output is differential. The data output is PECL compatible, ECL referenced (shifted) to a +3.3 V power supply. This circuit also includes a loss of signal (LOS) detection circuit which provides an open collector logic high output in the absence of a usable input optical signal. The LOS output is +3.3 V TTL.

Features

- RoHS compliant
- Full compliance with ATM Forum UNI SONET OC-3 multimode fiber physical layer specification
- Full compliance with the optical performance requirements of the FDDI PMD Standard
- Full compliance with the optical performance requirements of 100Base-FX version of IEEE802.3u
- Industry standard Small Form Pluggable (SFP) package
- LC duplex connector optical interface
- Operates with 62.5/125 µm and 50/125 µm multimode fiber
- Single +3.3 V power supply
- +3.3 V TTL LOS output
- Receiver outputs are squelch enabled
- Manufactured in an ISO 9001 certified facility
- Temperature range:
  0 °C to +70° C HFBR-57E0LZ/PZ:
  -40 °C to +85 °C HFBR-57E0ALZ/APZ:
- Bail de-latch option

Applications

- OC-3 SFP transceivers are designed for ATM LAN and WAN applications such as:
  ATM switches and routers
  SONET/SDH switch infrastructure
- Multimode fiber ATM backbone links
- Fast Ethernet

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Loss of Signal

The Loss of Signal (LOS) output indicates that the optical input signal to the receiver does not meet the minimum detectablelevel for FDDI and OC-3 compliant signals. When LOS is high it indicates loss of signal. When LOS is low it indicates normal operation. The LOS thresholds are set to indicate a definite optical fault has occurred (e.g., disconnected or broken fiber connection to receiver, failed transmitter).

Module Package

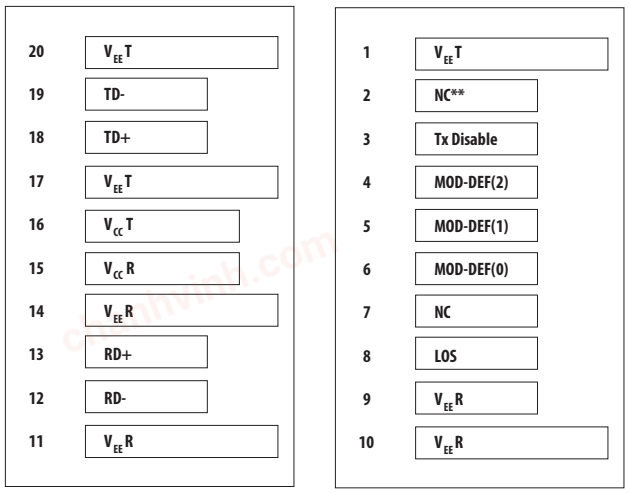
The transceiver meets the Small Form Pluggable (SFP) industry standard package utilizing an integral LC duplex optical interface connector. The hot-pluggable capability of the SFP package allows the module to be installed at any time – even with the host system operating and on-line. This allows for system configuration changes or maintenance without system down time. The HFBR-57E0 uses a reliable 1300 nm LED source and requires a 3.3 V dc power supply for optimal design.

Module Diagrams

Figure 1 illustrates the major functional components of the HFBR-57E0. The connection diagram of the module is shown in Figure 2. Figures 5 and 7 depict the external configuration and dimensions of the module.

Installation

The HFBR-57E0 can be installed in or removed from any MultiSource Agreement (MSA) – compliant Small Form Pluggable port regardless of whether the host equipment is operating or not. The module is simply inserted, electrical interface first, under finger pressure. Controlled hot-plugging is ensured by design and by 3-stage pin sequencing at the electrical interface. The module housing makes initial contact with the host board EMI shield mitigating potential damage due to Electro-Static Discharge (ESD). The 3-stage pin contact sequencing involves (1) Ground, (2) Power, and then (3) Signal pins, making contact with the host board surface mount connector in that order. This printed circuit board card-edge connector is depicted in Figure 2.



** Connect to Internal Ground.

Figure 2. Connection diagram of module printed circuit board.

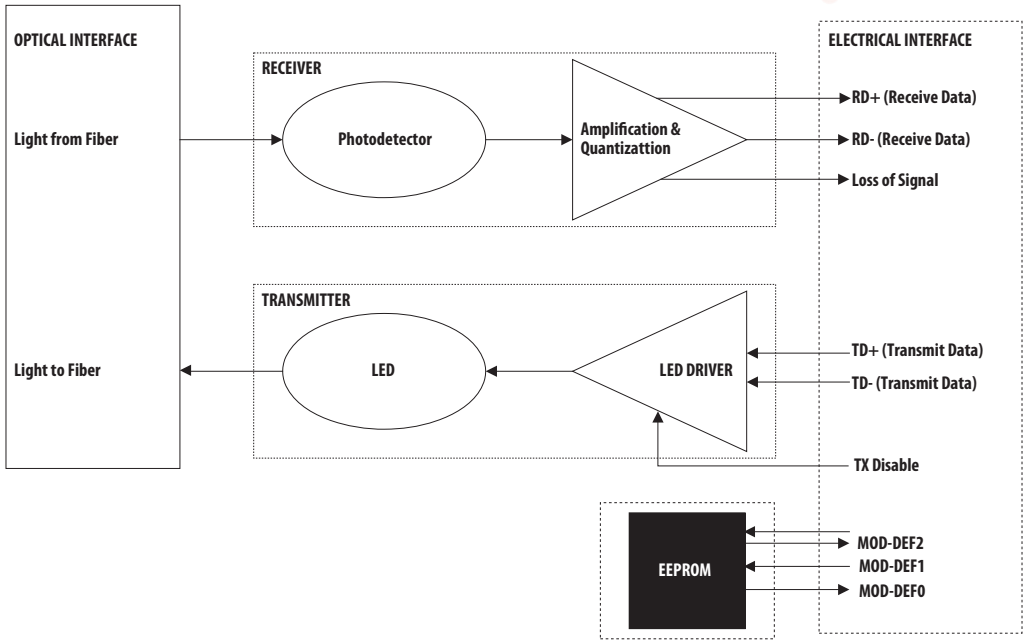


Figure 1. Transceiver functional diagram

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Serial Identification (EEPROM)

The HFBR-57E0 complies with the industry standard MSA that defines the serial identification protocol. This protocol uses the 2-wire serial CMOS E2PROM protocol of the ATMEL AT24C01A or equivalent. The contents of the HFBR-57E0 serial ID memory are defined in Table 3 as specified in the SFP MSA.

Functional Data I/O

The HFBR-57E0 fiberoptic transceiver is designed to accept industry standard differential signals. In order to reduce the number of passive components required on the customer's board, Avago has included the functionality of the transmitter bias resistors and coupling capacitors within the fiberoptic module. The transceiver is compatible with an "ac-coupled" configuration and is internally terminated. Figure 5 depicts the functional diagram of the HFBR-57E0.

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions in which immunity to ESD damage is important. Table 1 documents our immunity to both of these conditions. The first condition is during handling of the transceiver prior to insertion into the transceiver port. To protect the transceiver, it is important to use normal ESD handling precautions.

These precautions include using grounded wrist straps, workbenches, and floor mats in ESD controlled areas. The ESD sensitivity of the HFBR-57E0 is compatible with typical industry production environments. The second condition is static discharges to the exterior of the host equipment chassis after installation. To the extent that the duplex LC optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD requirements. The ESD performance of the HFBR-57E0 exceeds typical industry standards.

Immunity

Equipment hosting the HFBR-57E0 modules will be subjected to radio-frequency electro magnetic fields in some environments. These transceivers have good immunity to such fields due to their shielded design.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C	Meets Class 2 (2000 to 3999 Volts).Withstand up to 2200 V applied between electrical pins.
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 25 kV without damage when the LC connector receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC CEN55022 Class B (CISPR 21) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 450 MHz applied to the transceiver without a chassis enclosure.
Eye Safety	AEL Class 1 EN60825-1 (+A11)	Compliant per Avago testing under single fault conditions. TUV Certification: R 72042022
Component Recognition	Underwriters Laboratories and Canadian Standard Associations Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment	UL File#: E173874
RoHS Compliance		Reference to EU RoHS Directive 2002/95/EC

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Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The metal housing and shielded design of the HFBR-57E0 minimize the EMI challenge facing the host equipment designer. These transceivers provide superior EMI performance. This greatly assists the designer in the management of the overall system EMI performance.

Eye Safety

These transceivers provide Class 1 eye safety by design. Avago has tested the transceiver design for compliance with the requirements listed in Table 1 under normal operating conditions and under a single fault condition.

Flammability

The HFBR-57E0 transceiver housing is made of metal and high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant plastic.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Transceiver Optical Power Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiberoptic link to accommodate fiber cable loses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Avago LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 db aging for 1300 nm LEDs. The 1300 nm Avago LEDs are specified to experience less than 1 db of aging over normal commercial equipment mission life periods. Contact your Avago sales representative for additional details.

Ordering Information

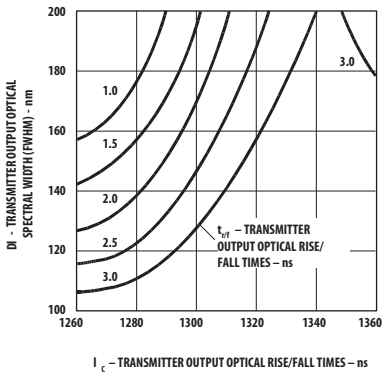
The HFBR-57E0 1300 nm product is available for production orders through the Avago Component Field Sales Offices and Authorized Distributors worldwide.

For technical information regarding this product, please visit the Avago website at www.avagotech.com.

Use the quick search feature to search for this part number. You may also contact the Avago Products Customer Response Centre.

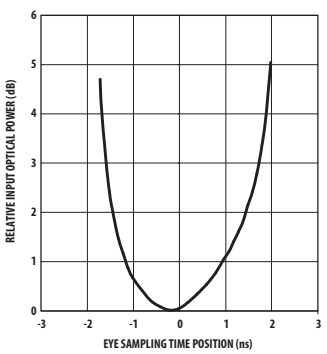
Applications Support Materials

Contact your local Avago Component Field Sales Office for information on how to obtain PCB layouts and evaluation boards for the transceivers.



HFBR-57E0 TRANSMITTER TEST RESULTS OF l_c, Dl AND t_{rf} ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES.

Figure 3. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times



CONDITIONS:
1. T_A = +25 C
2. V_{CC} = 3.3 V dc
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
5. NOTE 13 AND 14 APPLY.

Figure 4. Relative Input Optical Power vs. Eye Sampling Time Position

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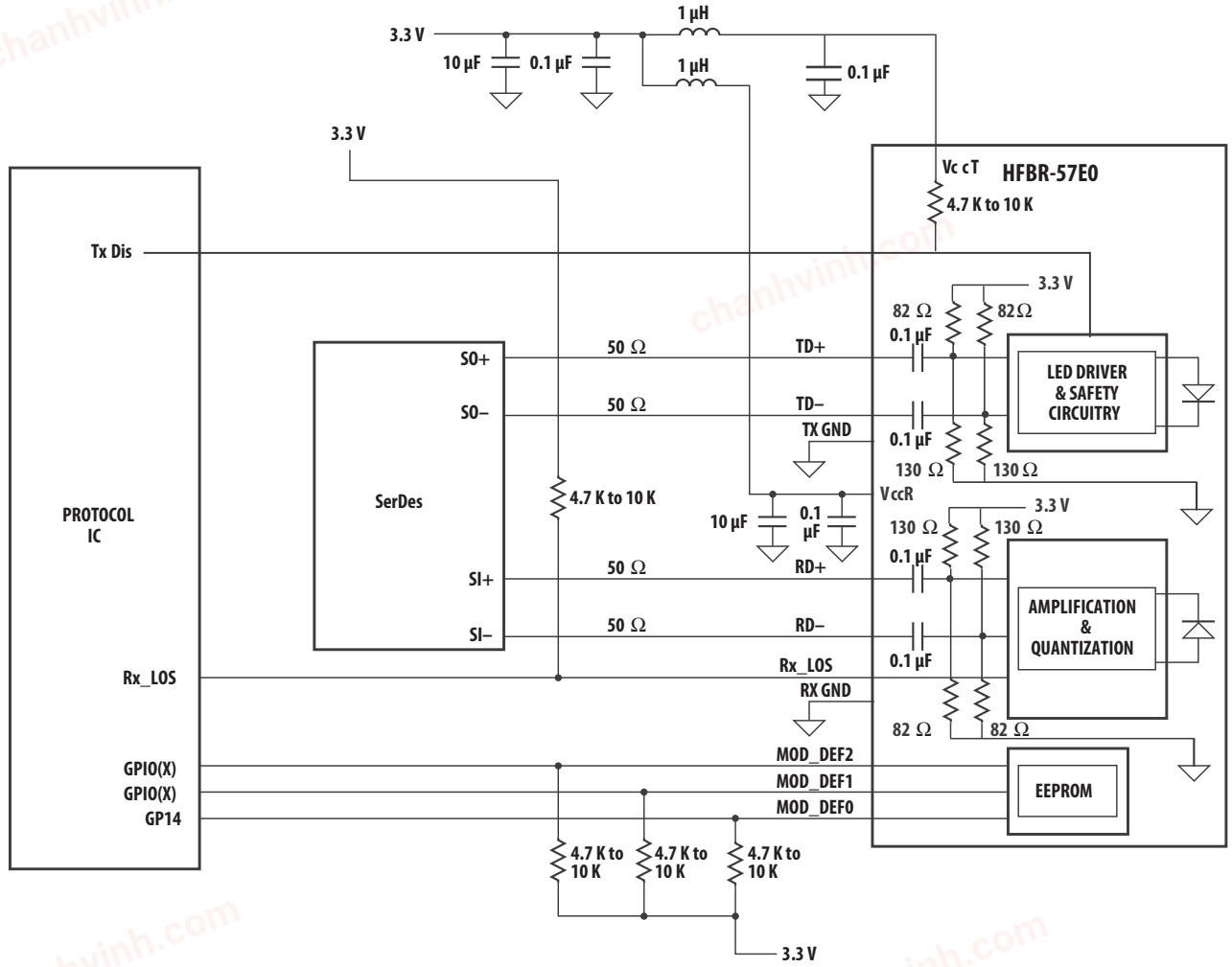
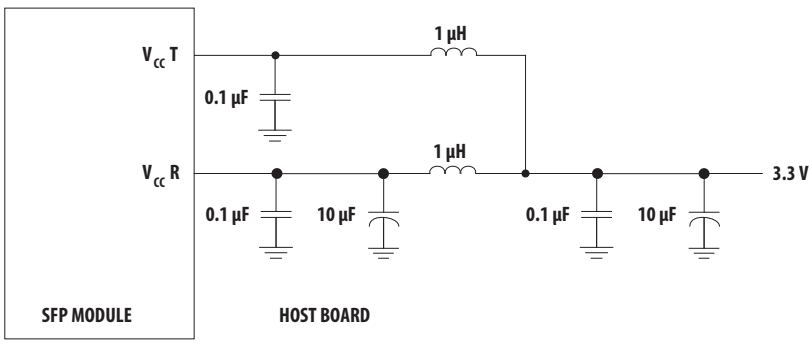


Figure 5. Recommended application configuration



Note: Inductors must have less than 1 ohm series resistance per MSA.

Figure 6. MSA required power supply filter

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Table 2. Pin Description

Pin	Name	Function/Description	MSA Notes
1	$V_{EE}T$	Transmitter Ground	
2	NC	NC	1
3	Tx Disable	Transmitter Disable- Module disables on high or open	
4	MOD-DEF2	Module Definition 2 - Two Wire Serial ID Interface	2
5	MOD-DEF1	Module Definition 1 - Two Wire Serial ID Interface	2
6	MOD-DEF0	Module Definition 0 - grounded in module	2
7	NC	NC	
8	LOS	Loss of Signal - high indicates loss of signal	3
9	$V_{EE}R$	Receiver Ground	
10	$V_{EE}R$	Receiver Ground	
11	$V_{EE}R$	Receiver Ground	
12	RD-	Inverse Received Data Out	4
13	RD+	Received Data Out	4
14	$V_{EE}R$	Receiver Ground	
15	$V_{CC}R$	Receiver Power -3.3 V ± 10%	5
16	$V_{CC}T$	Transmitter Power -3.3 V ± 10%	5
17	$V_{EE}T$	Transmitter Ground	
18	TD+	Transmitter Data In	6
19	TD-	Inverse Transmitter Data In	6
20	$V_{EE}T$	Transmitter Ground	

Notes:

1. Pin 2 connected to internal ground.
2. Mod-Def 0, 1, 2. are the module definition pins. They should be pulled up with a 4.7 K - 10 KΩ resistor on the host board to a supply less than $V_{CC}T$ +0.3 V or $V_{CC}R$ +0.3 V.
   Mod-Def 0 is grounded by the module to indicate that the module is present.
   Mod-Def 1 is clock line of two wire serial interface for optional serial ID.
   Mod-Def 2 is data line of two wire serial interface for optional serial ID.
3. LOS (Loss of Signal) is an open collector/drain output which should be pulled up externally with a 4.7 - 10 KΩ resistor on the host board to a supply < $V_{CC}T$, R +0.3 V. When high, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to <0.8 V.
4. RD-/+: These are the differential receiver outputs. They are ac coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the SERDES. The ac coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 400 and 2000 mV differential (200 - 1000 mV single ended) when properly terminated.
5. $V_{CC}R$ and $V_{CC}T$ are the receiver and transmitter power supplies. They are defined as 2.97 - 3.63 V at the SFP connector pin. The maximum supply current is 230 mA and the associated in-rush current will typically be no more than 30 mA above steady state after 500 nanoseconds.
6. TD-/+: These are the differential transmitter inputs. They are ac coupled differential lines with 100 Ω differential termination inside the module. The ac coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 400 - 2000 mV (200 - 1000 mV single ended), though it is recommended that values between 400 and 1200 mV differential (200 - 600 mV single ended) be used for best EMI performance. These levels are compatible with CML and LVPECL voltage swings.

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Table 3. EEPROM Serial ID Memory Contents

Add	Hex	ASCII	Add	Hex	ASCII	Add	Hex	ASCII	Add	Hex	ASCII
0	03		33	20		63	Note 3		95	Note 3	
1	04		34	20		64	00		96	Note 5	
2	07		35	20		65	12		97	Note 5	
3	00		36	00		66	00		98	Note 5	
4	00		37	00		67	00		99	Note 5	
5	01, Note 6		38	17		68	Note 1		100	Note 5	
6	20, Note 6		39	6A		69	Note 1		101	Note 5	
7	00		40	48	H	70	Note 1		102	Note 5	
8	00		41	46	F	71	Note 1		103	Note 5	
9	00		42	42	B	72	Note 1		104	Note 5	
10	00		43	52	R	73	Note 1		105	Note 5	
11	03, Note 7		44	2D	-	74	Note 1		106	Note 5	
12	02, Note 8		45	35	5	75	Note 1		107	Note 5	
13	00		46	37	7	76	Note 1		108	Note 5	
14	00		47	45	E	77	Note 1		109	Note 5	
15	00		48	30	0	78	Note 1		110	Note 5	
16	C8		49	41, Note 4	A	79	Note 1		111	Note 5	
17	C8		50	50, Note 4	P	80	Note 1		112	Note 5	
18	00		51	5A, Note 4	Z	81	Note 1		113	Note 5	
19	00		52	20, Note 4		82	Note 1		114	Note 5	
20	41	A	53	20, Note 4		83	Note 1		115	Note 5	
21	56	V	54	20		84	Note 2		116	Note 5	
22	41	A	55	20		85	Note 2		117	Note 5	
23	47	G	56	30	0	86	Note 2		118	Note 5	
24	4F	O	57	30	0	87	Note 2		119	Note 5	
25	20		58	30	0	88	Note 2		120	Note 5	
26	20		59	30	0	89	Note 2		121	Note 5	
27	20		60	05		90	Note 2		122	Note 5	
28	20		61	1E		91	Note 2		123	Note 5	
29	20		62	00		92	00		124	Note 5	
30	20					93	00		125	Note 5	
31	20					94	00		126	Note 5	
32	20								127	Note 5	

1. Addresses 68 - 83 specify a unique identifier.
2. Addresses 84 - 91 specify the date code.
3. Addresses 63 and 95 are check sums. Address 63 is the check sum for bytes 0 - 62 and address 95 is the check sum for bytes 64 - 94.
4. Part number options LZ, PZ, ALZ, APZ, etc. Example: for "AP" option, hexes in addresses 49, 50, 51, 52 and 52 will be 41, 50, 5A, 20 and 20 respectively.
5. Addresses 96-127 are vendor specific data.
6. Addresses 5 and 6 specify compliance code. Address 5 with Hex 01 for OC-3 and address 6 with Hex 20 for Fast Ethernet.
7. Address 11 specifies encoding code. Hex 03 for OC-3 and Hex 02 for Fast Ethernet.
8. Address 12 specifies bit rate. Hex 02 for OC-3 and Hex 01 for Fast Ethernet.

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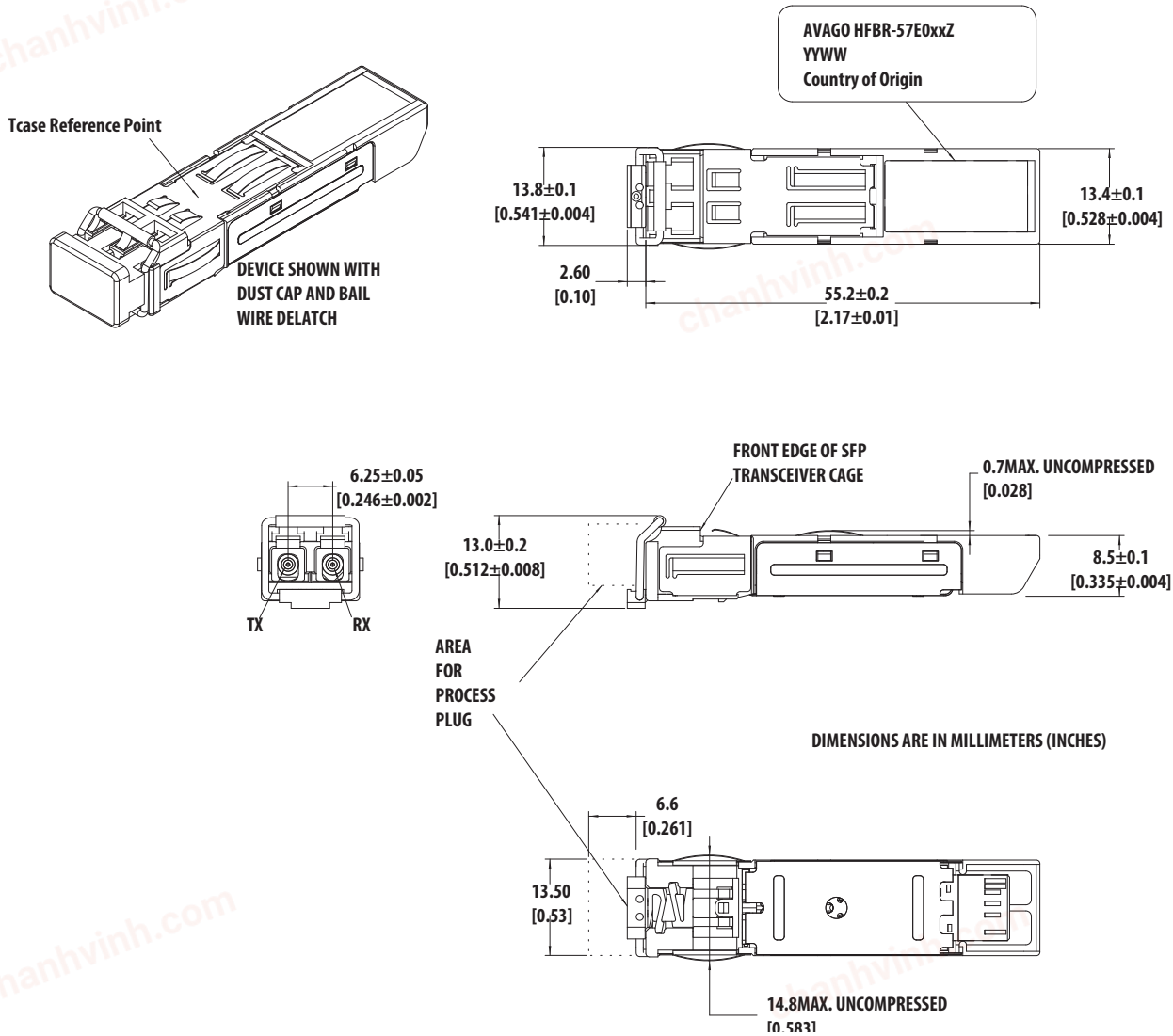
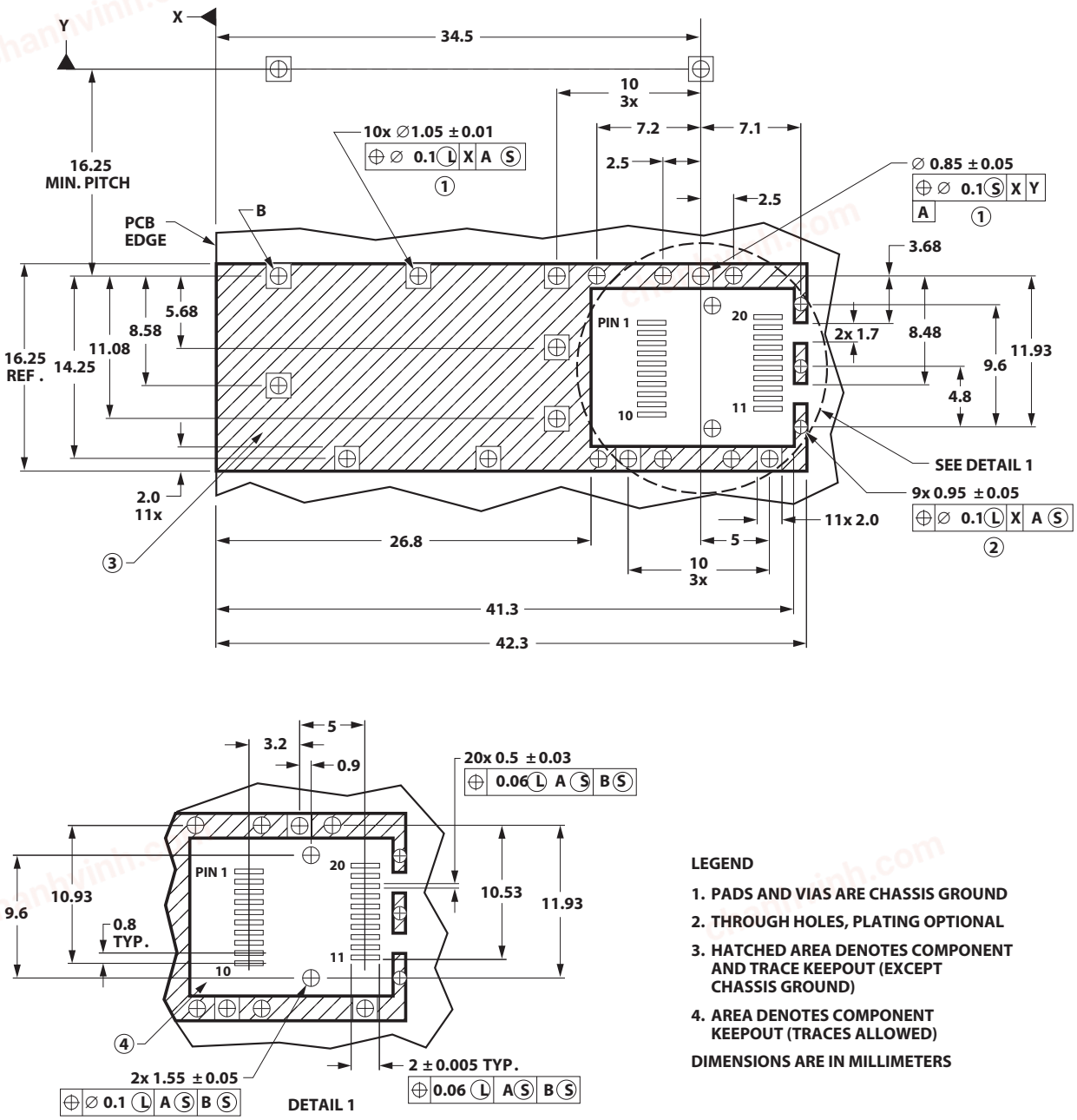


Figure 7. Module Drawing

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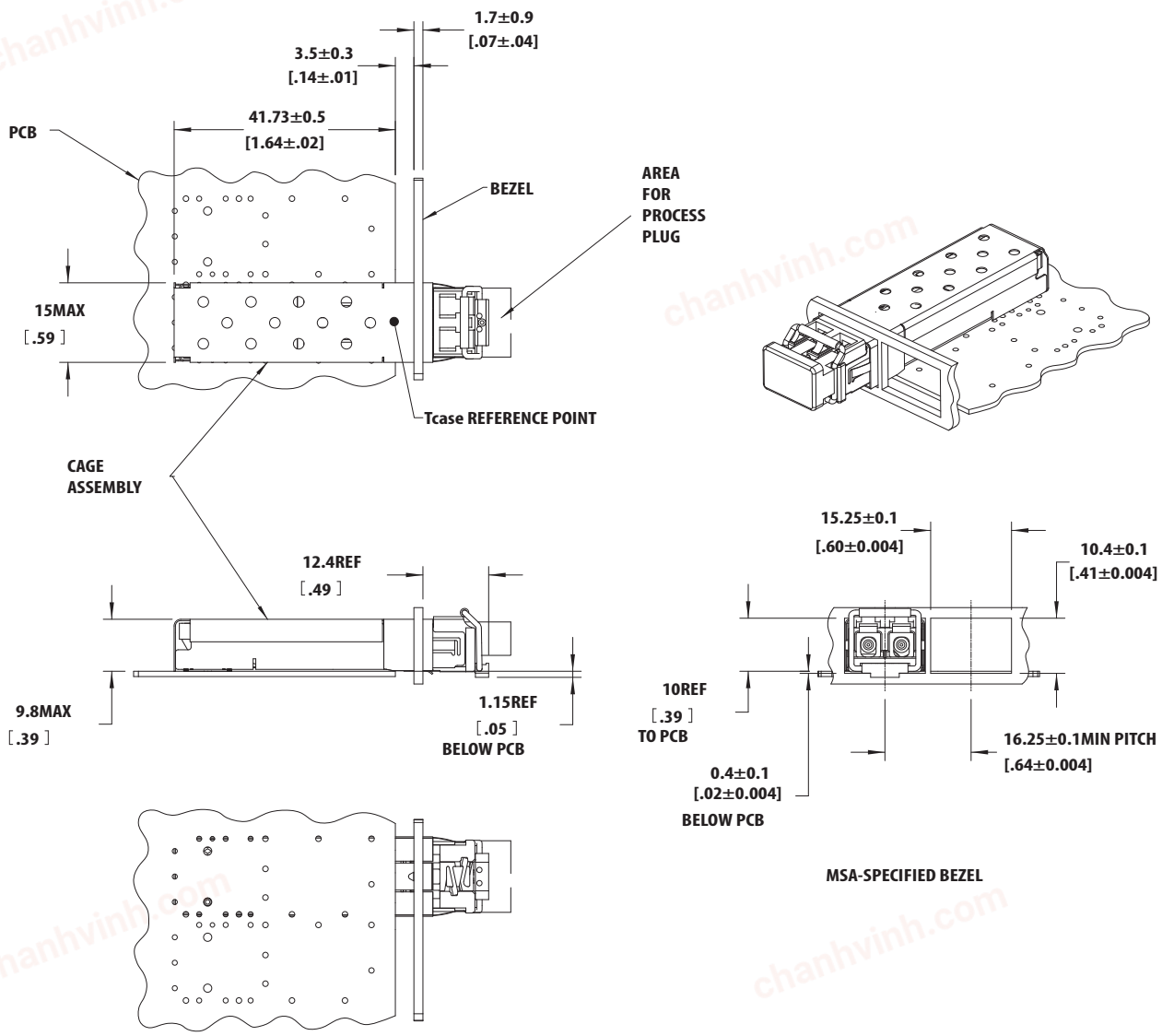
LEGEND

1. PADS AND VIAS ARE CHASSIS GROUND
2. THROUGH HOLES, PLATING OPTIONAL
3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND)
4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED)

DIMENSIONS ARE IN MILLIMETERS

Figure 8. SFP host board mechanical layout

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DIMENSIONS ARE IN MILLIMETERS [INCHES].

Figure 9. SFP Assembly Drawing

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Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Storage Temperature	T_S	-40		+100	°C	
Supply Voltage	V_{CC}	-0.5		3.63	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage (p-p)	V_D			2.4	V	1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Case Operating Temperature						
HFBR-57E0LZ/PZ	T_C	0		+70	°C	
HFBR-57E0ALZ/APZ	T_C	-40		+85	°C	
Supply Voltage	V_{CC}	2.97	3.3	3.63	V	
Data Input: Transmitter Differential Input Voltage (TD+/-)	V_I	0.5	0.8	2.4	V	
Data and Loss of Signal Output Load	R_L		50		Ω	2

Transmitter Electrical Characteristics

HFBR-57E0LZ/PZ (T_C = 0 °C to +70 °C, V_{CC} = 2.97 V to 3.63 V)
HFBR-57E0ALZ/APZ (T_C = -40 °C to +85 °C, V_{CC} = 2.97 V to 3.63 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current	I_{CC}		165	210	mA	3
Power Dissipation	P_{DISS}		0.55	0.80	W	5a
Transmitter Disable (TX Disable) High	V_{IH}	2.0		3.5	V	
Transmitter Disable (TX Disable) Low	V_{IL}	0		0.8	V	

Receiver Electrical Characteristics

HFBR-57E0LZ/PZ (T_C = 0 °C to +70 °C, V_{CC} = 2.97 V to 3.63 V)
HFBR-57E0ALZ/APZ (T_C = -40 °C to +85 °C, V_{CC} = 2.97 V to 3.63 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current	I_{CC}		95	150	mA	4
Power Dissipation	P_{DISS}		0.35	0.55	W	5b
Data Output: Receiver Differential Output Voltage (RD+/-)	V_O	0.4		2.0	V	6a6b
Data Output Rise Time	t_r	0.35		2.2	ns	7
Data Output Fall Time	t_f	0.35		2.2	ns	7
Loss of Signal Output Voltage - Low	$LOSV_{OL}$			0.8	V	6a
Loss of Signal Output Voltage - High	$LOSV_{OH}$	2.0			V	6a
Power Supply Noise Rejection	PSNR		50		mV	

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Notes:
1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The data outputs are terminated with 50Ω .
   The Loss of Signal output is terminated with 50 Ω connected to a pull-up resistor of 4.7 KΩ tied to V_{CC}.
3. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. This is the receiver supply current measured in mA.
5a. The power dissipation of the transmitter is calculated as the sum of the products of supply voltage and current.
5b. The power dissipation of the receiver is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.
6a. Differential Output Voltage is internally ac coupled. The Loss of Signal low and high voltages are measured with load condition as mentioned in note 2.
6b. Data and Data-bar outputs are squelched at LOS assert level. When the received light drops below LOS assert point, it will force receiver data and data-bar to go to steady PECL levels High and Low respectively.
7. The data output rise and fall times are measured between 20% and 80% levels.

Transmitter Optical Characteristics

HFBR-57E0LZ/PZ(T_C = 0 °C to +70 °C, V_{CC} = 2.97 V to 3.63 V)
HFBR-57E0ALZ/APZ (T_C = -40 °C to +85 °C, V_{CC} = 2.97 V to 3.63 V)

Parameter		Symbol	Minimum	Typical	Maximum	Units	Notes
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	BOL EOL	P_O	-19 -20	-15.7	-14	dBm avg	8
Output Optical Power 50/125 µm, NA = 0.20 Fiber	BOL EOL	P_O	-22.5 -23.5		-14	dBm avg	8
Transmitter Disable (High)		$P_{O(off)}$			-45	dBm	
Center Wavelength		λ_C	1270	1308	1380	nm	21, Figure 3
Spectral Width - FWHM Spectral Width - RMS		$\Delta\lambda$		147 63		nm	9, 21, Figure 3
Optical Rise Time		t_r	0.6	1.2	3.0	ns	10, 21, Figure 3
Optical Fall Time		t_f	0.6	2.0	3.0	ns	10, 21, Figure 3
Systematic Jitter Contributed by the Transmitter - OC-3		SJ		0.25	1.2	ns p-p	11a
Duty Cycle Distortion Contributed by the Transmitter - FE		DCD		0.20	0.6	ns p-p	11b
Data Dependent Jitter Contributed by the Transmitter - FE		DDJ		0.07	0.6	ns p-p	11c
Random Jitter Contributed by the Transmitter		RJ					
OC-3				0.10	0.52	ns	12a
FE				0.10	0.69	p-p	12b

Notes:
8. These optical power values are measured with the following conditions:
   The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Avago's 1300 nm LED products is < 1 dB, as specified in this data sheet. Over the specified operating voltage and temperature ranges. With 25 MBd (12.5 MHz square-wave), input signal.
   At the end of one meter of noted optical fiber with cladding modes removed. The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request. Please consult with your local Avago sales representative for further details.
9. The relationship between Full Width Half Maximum and RMS values for Spectral Width is derived from the assumption of a Gaussian shaped spectrum which results in a 2.35 X RMS = FWHM relationship.
10. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by a 25 MBd (12.5 MHz square-wave) input signal. The ANSI T1E1.2 committee has designated the possibility of defining an eye pattern mask for the transmitter optical output as an item for further study. Avago will incorporate this requirement into the specifications for these products if it is defined. The HFBR-57E0 products typically comply with the template requirements of CCITT (now ITU-T) G.957 Section 3.2.5, Figure 2 for the STM- 1 rate, excluding the optical receiver filter normally associated with single mode fiber measurements which is the likely source for the ANSI T1E1.2 committee to follow in this matter.

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Notes:

11a. Systematic Jitter contributed by the transmitter is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. Systematic Jitter is measured at 50% threshold using a 155.52 MBd (77.5 MHz square-wave), 2^{23}- 1 psuedorandom data pattern input signal.

11b. Duty Cycle Distortion contributed by the transmitter is measured at the 50% threshold of the optical output signal using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal.

11c. Data Dependent Jitter contributed by the transmitter is specified with the FDDI test pattern described in FDDI PMD Annex A.5.

12a. Random Jitter contributed by the transmitter is specified with a 155.52 MBd (77.5 MHz square-wave) input signal.

12b. Random Jitter contributed by the transmitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave) input signal. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.

Receiver Optical and Electrical Characteristics

HFBR-57E0LZ /PZ(T_C = 0 °C to +70 °C, V_{CC} = 2.97 V to 3.63 V)
HFBR-57E0ALZ/APZ (T_C = -40 °C to +85 °C, V_{CC} = 2.97 V to 3.63 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Input Optical Power minimum at Window Edge	$P_{IN\ MIN}$ (W)					13a,
OC-3				-30	dBm avg	Figure 4
FE				-31		13b
Input Optical Power at Eye Center	$P_{IN\ MIN}$ (C)				dBm avg	14a,
OC-3				-31		Figure 4
FE				-31.8		14b
Input Optical Power Maximum	$P_{IN\ MAX}$				dBm avg	
OC-3		-14				13a
FE		-14				13b
Operating Wavelength	λ	1270		1380	nm	
Systematic Jitter Contributed by the Receiver OC-3	SJ		0.11	1.2	ns p-p	15a
Duty Cycle Distortion Contributed by the Receiver FE	DCD		0.08	0.4	ns p-p	15b
Data Dependent Jitter Contributed by the Receiver FE	DDJ		0.02	1.0	ns p-p	15c
Random Jitter Contributed by the Receiver	RJ				ns p-p	
OC-3			0.14	1.91		16a
FE			0.14	2.14		16b
Loss of Signal - Deasserted	P_A	P_D +		-31	dBm avg	17
OC-3		1.5 dB		-33		
FE						
Loss of Signal - Asserted	P_D	-45			dBm avg	18
Loss of Signal - Hysteresis	P_A - P_D	1.5			dB	
Loss of Signal Deassert Time (on to off)		0	2	100	µs	19
Loss of Signal Assert Time (off to on)		0	5	350	µs	20

Notes:

13a. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Rate (BER) better than or equal to 1 x 10^{-10}.

- At the Beginning of Life (BOL)
- Over the specified operating temperature and voltage ranges
- Input is a 155.52 MBd, 2^{23}-1 PRBS data pattern with 72 "1" s and 72 "0"s inserted per the CCITT (now ITU-T) recommendation G.958 Appendix I.
- Receiver data window time-width is 1.23 ns or greater for the clock recovery circuit to operate in. The actual test data window time-width is set to simulate the effect of worst case optical input jitter based on the transmitter jitter values from the specification tables. The test window time-width is 3.32 ns.
- Transmitter operating with a 155.52 MBd, 77.5 MHz square-wave, input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.

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13b. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Rate (BER) better than or equal to 2.5×10^{-10}.

- At the Beginning of Life (BOL)
- Over the specified operating temperature and voltage ranges
- Input symbol pattern is the FDDI test pattern defined in FDDI PMD Annex A.5 with 4B/5B NRZI encoded data that contains a duty cycle base-line wander effect of 50 kHz. This sequence causes a near worst case condition for inter-symbol interference.
- Receiver data window time-width is 2.13 ns or greater and centered at mid-symbol. This worst case window time-width is the minimum allowed eye-opening presented to the FDDI PHY PM_Data indication input (PHY input) per the example in FDDI PMD Annex E. This minimum window time-width of 2.13 ns is based upon the worst case FDDI PMD Active Input Interface optical conditions for peak-to-peak DCD (1.0 ns), DDJ (1.2 ns) and RJ (0.76 ns) presented to the receiver.

To test a receiver with the worst case FDDI PMD Active Input jitter condition requires exacting control over DCD, DDJ and RJ jitter components that is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst case FDDI PMD input jitter conditions and meet the minimum output data window time-width of 2.13 ns. This is accomplished by using a nearly ideal input optical signal (no DCD, insignificant DDJ and RJ) and measuring for a wider window time-width of 4.6 ns. This is possible due to the cumulative effect of jitter components through their superposition (DCD and DDJ are directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of DCD (0.4 ns), DDJ (1.0 ns), and RJ (2.14 ns) exist, the minimum window time-width becomes 8.0 ns -0.4 ns - 1.0 ns - 2.14 ns = 4.46 ns, or conservatively 4.6 ns. This wider window time-width of 4.6 ns guarantees the FDDI PMD Annex E minimum window time-width of 2.13 ns under worst case input jitter conditions to the Avago receiver.

- Transmitter operating with an IDLE Line State pattern, 125 MBd (62.5 MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.

14a. All conditions of Note 13a apply except that the measurement is made at the center of the symbol with no window time- width.

14b. All conditions of Note 13b apply except that the measurement is made at the center of the symbol with no window time-width.

15a. Systematic Jitter contributed by the receiver is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. Systematic Jitter is measured at 50% threshold using a 155.52 MBd (77.5 MHz square- wave), 2^{23}-1 psuedorandom data pattern input signal.

15b Duty Cycle Distortion contributed by the receiver is measured at the 50% threshold of the electrical output signal using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is -20 dBm average.

15c. Data Dependent Jitter contributed by the receiver is specified with the FDDI DDJ test pattern described in the FDDI PMD Annex A.5. The input optical power level is -20 dBm average.

16a. Random Jitter contributed by the receiver is specified with a 155.52 MBd (77.5 MHz square- wave) input signal.

16b. Random Jitter contributed by the receiver is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is at maximum "$P_{IN\ MIN}$ (W)". See Application Information - Transceiver Jitter Section for further information.

17. This value is measured during the transition from low to high levels of input optical power.

18. This value is measured during the transition from high to low levels of input optical power. At Loss of Signal assert, the receiver outputs Data Out and Data Out Bar go to steady PECL levels High and Low respectively.

19. The Loss of Signal output shall be de-asserted within 100 µs after a step increase of the Input Optical Power.

20. Loss of Signal output shall be asserted within 350 µs after a step decrease in the Input Optical Power. At Loss of Signal Assert, the receiver outputs Data Out and Data Out Bar go to steady PECL levels High and Low respectively.

21. The HFBR-57E0 transceiver complies with the requirements for the trade-offs between center wavelength, spectral width, and rise/fall times shown in Figure 3. This figure is derived from the FDDI PMD standard (ISO/IEC 9314-3 : 1990 and ANSI X3.166 - 1990) per the description in ANSI T1E1.2 Revision 3. The interpretation of this figure is that values of Center Wavelength and Spectral Width must lie along the appropriate Optical Rise/Fall Time curve.

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Ordering Information

1300 nm LED (Operating Case Temperature 0 to +70 °C)

HFBR-57E0LZ	Standard de-latch
HFBR-57E0PZ	Bail de-latch

1300 nm LED (Operating Case Temperature -40 °C to +85 °C)

HFBR-57E0ALZ	Standard de-latch
HFBR-57E0APZ	Bail de-latch

EEPROM contents and/or label options

HFBR-57E0LZ-YYY	Standard de-latch, 0 to +70°C
HFBR-57E0PZ-YYY	Bail de-latch, 0 to +70°C
HFBR-57E0ALZ-YYY	Standard de-latch, -40°C to +85°C
HFBR-57E0APZ-YYY	Bail de-latch, -40°C to +85°C

Where "YYY" is customer specific.

Handling Precaution

The HFBR-57E0xxZ is a pluggable module and is NOT designed for aqueous wash, IR reflow or wave soldering processes.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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