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HCPL-7860/HCPL-786J
Optically Isolated Sigma-Delta (S-D) Modulator

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-7860/HCPL-786J Optically Isolated Modulator and HCPL-0872 Digital Interface IC or digital filter together form an isolated programmable two-chip analog-to-digital converter. The isolated modulator allows direct measurement of motor phase currents in power inverters.

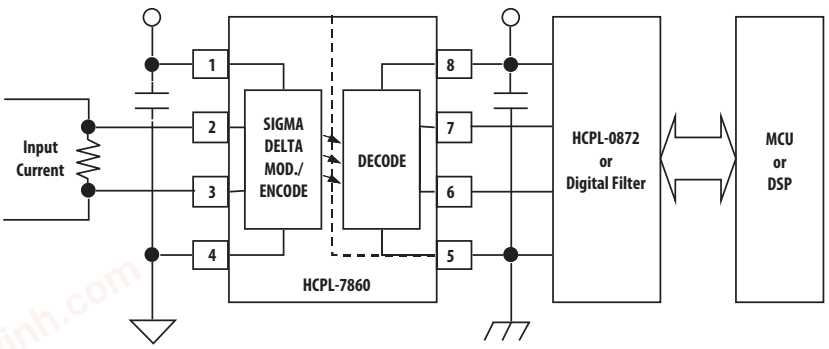
In operation, the HCPL-7860/HCPL-786J Isolated Modulator converts a low-bandwidth analog input into a high-speed one-bit data stream by means of a Sigma-Delta (Σ–Δ) over-sampling modulator. This modulation provides for high noise margins and excellent immunity against isolation-mode transients. The modulator data and on-chip sampling clock are encoded and transmitted across the isolation boundary where they are recovered and decoded into separate high-speed clock and data channels.

Features

- 12-bit Linearity
- 200 ns Conversion Time
  (Pre-Trigger Mode 2 with HCPL-0872)
- 12-bit Effective Resolution with 5 µs Signal Delay
  (14-bit with 102 µs) (with HCPL-0872)
- Fast 3 µs Over-Range Detection (with HCPL-0872)
- ± 200 mV Input Range with Single 5 V Supply
- 1% Internal Reference Voltage Matching
- Offset Calibration (with HCPL-0872)
- -40°C to +85°C Operating Temperature Range
- 15 kV/µs Isolation Transient Immunity
- Safety Approval: UL 1577, CSA and IEC/EN/DIN EN 60747-5-2

Applications

- Motor Phase and Rail Current Sensing
- Data Acquisition Systems
- Industrial Process Control
- Inverter Current Sensing
- General Purpose Current Sensing and Monitoring

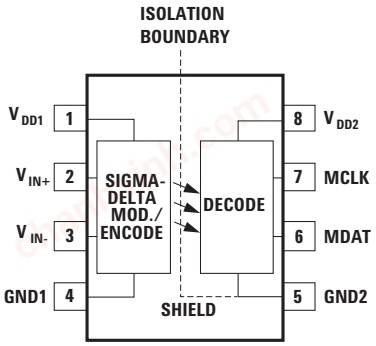


NOTE: A 0.1 µF bypass capacitor must be connected between pins VDD1 and GND1 and between pins VDD2 and GND2.

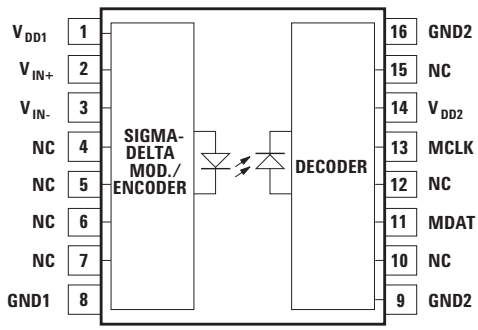
CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.

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Pin Description



HCPL-7860



HCPL-786J

Symbol	Description
V_{DD1}	Supply voltage input (4.5 V to 5.5 V)
V_{IN+}	Positive input (± 200 mV recommended)
V_{IN-}	Negative input (normally connected to GND1)
GND1	Input ground

Symbol	Description
V_{DD2}	Supply voltage input (4.5 V to 5.5 V)
MCLK	Clock output (10 MHz typical)
MDAT	Serial data output
GND2	Output ground

Note: NC = No connection. Leave floating.

Ordering Information

HCPL-7860 is UL Recognized with 3750 Vrms for 1 minute per UL1577. HCPL-786J is UL Recognized with 5000 Vrms for 1 minute per UL1577.

	Option							
Part number	RoHS Compliant	Non-RoHS Compliant	Package	Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
HCPL-7860	-000E	No option	300 mil DIP-8				X	50 per tube
	-300E	#300		X	X		X	50 per tube
	-500E	#500		X	X	X	X	1000 per reel
HCPL-786J	-000E	No option	SO-16				X	45 per tube
	-500E	#500		X		X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-7860-500E to order product of Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

Example 2:

HCPL-786J to order product of SO-16 package in tube packaging and non-RoHS compliant.

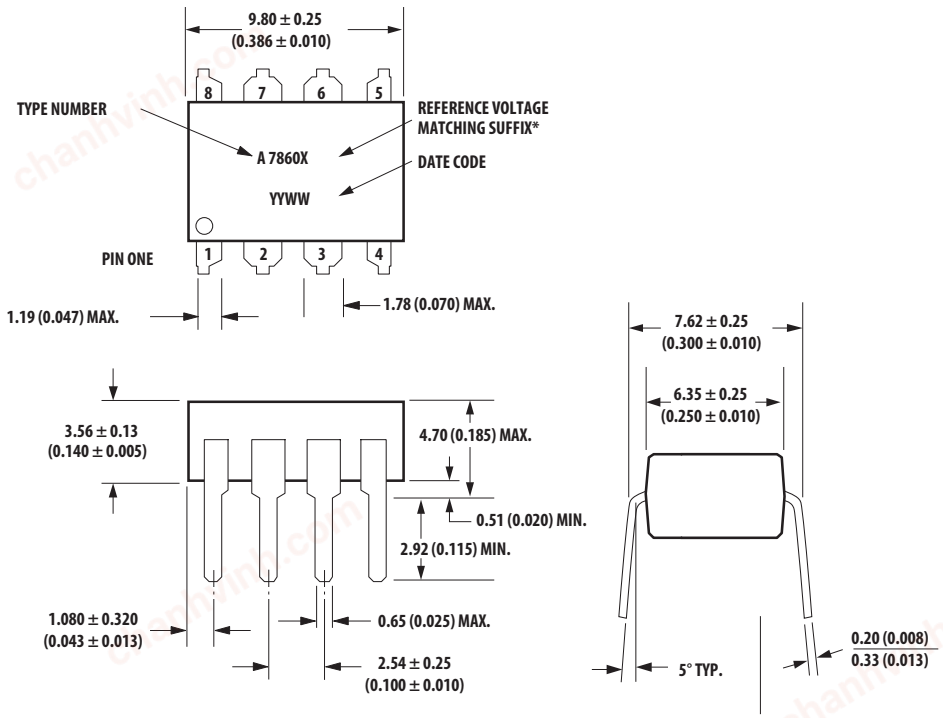
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

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Package Outline Drawings

8-pin DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

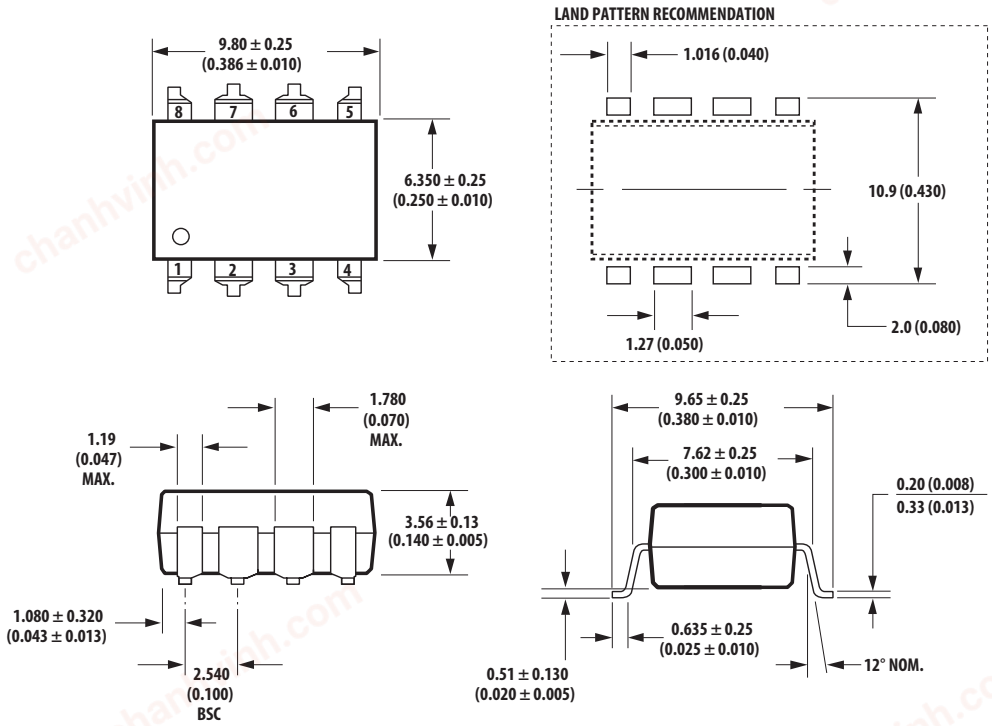
NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20mils) MAX.

NOTE: INITIAL OR CONTINUED VARIATION IN THE COLOUR OF THE HCPL-7860/HCPL-786J'S WHITE MOLD COMPOUND ISNORMAL AND DOES NOT AFFECT DEVICE PERFORMANCE OR RELIABILITY.

*ALL UNITS WITHIN EACH HCPL-7860 STANDARD PACKAGING INCREMENT (EITHER 50 PER TUBE OR 1000 PER REEL) HAVEA COMMON MARKING SUFFIX TO REPRESENT A REFERENCE VOLTAGE MATCHING OF ± 1%. AN ABSOLUTEREFERENCE VOLTAGE TOLERANCE OF ± 4% IS GUARANTEED BETWEEN STANDARD PACKAGING INCREMENTS.

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8-pin Gull Wing Surface Mount Option 300

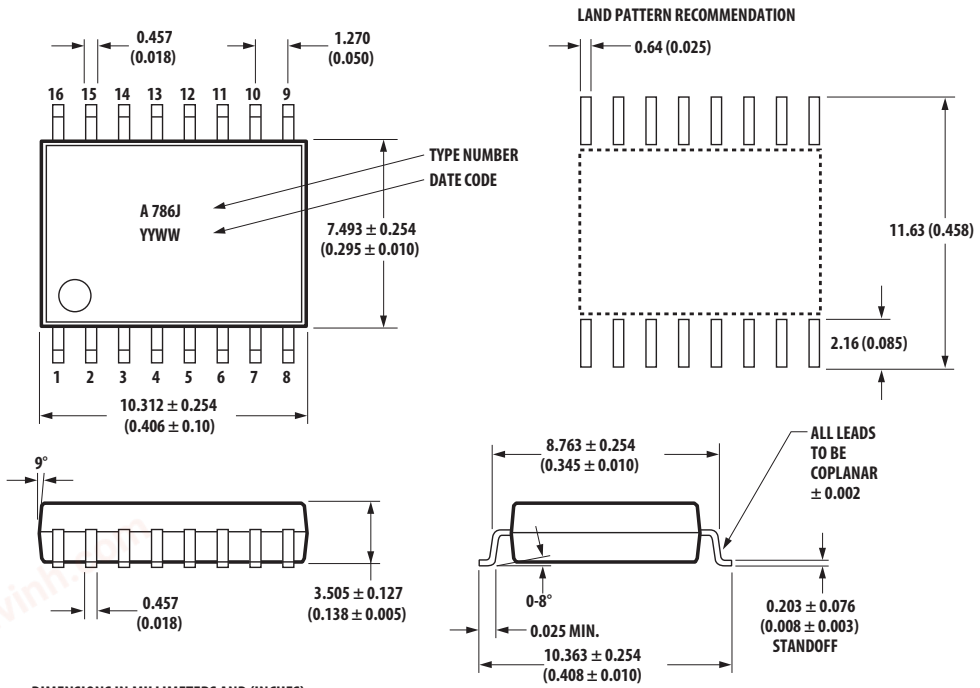


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

16-Lead Surface Mount



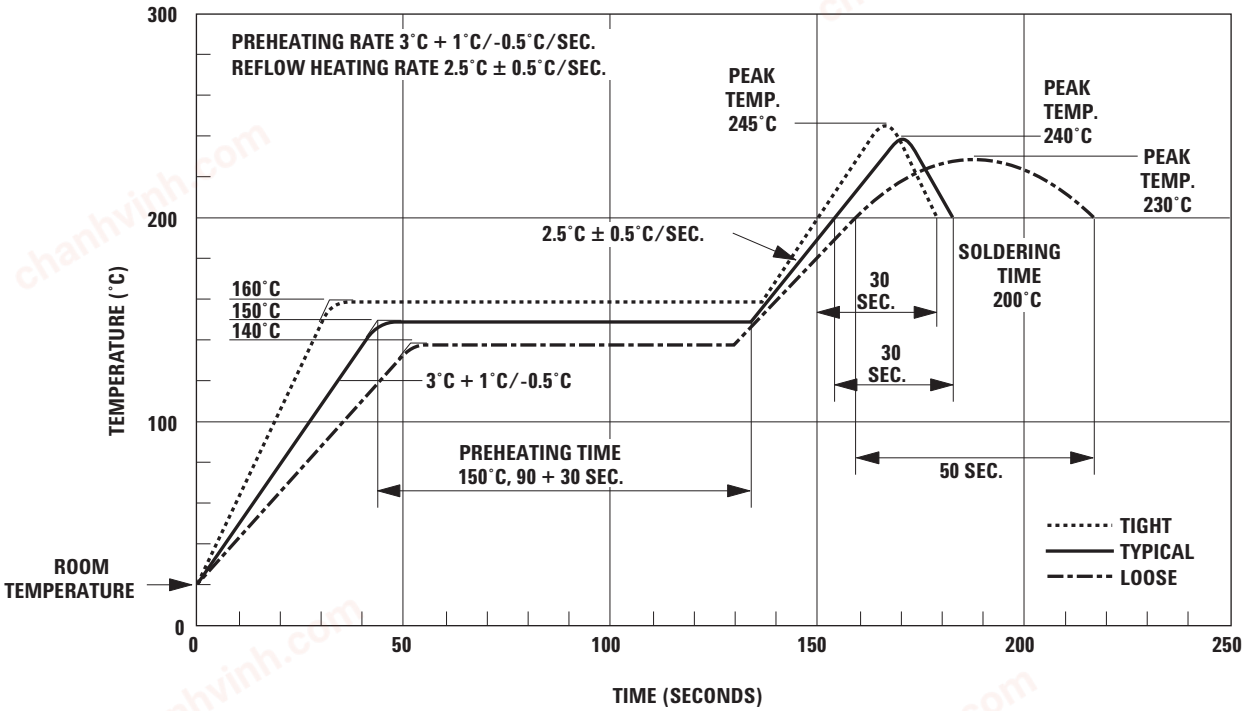
DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: Initial and continued variation in the color of the HCPL-786J's white mold compound is normal and does not affect device performance or reliability.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

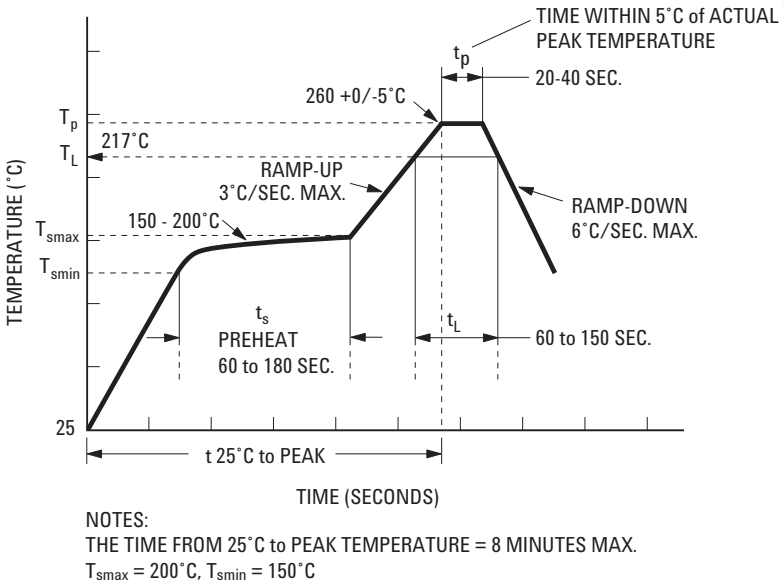
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Solder Reflow Temperature Profile



Note: Use of non-chlorine-activated fluxes is highly recommended.

Recommended Lead Free IR Profile



NOTES:
THE TIME FROM 25˚C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200˚C, T_{smin} = 150˚C

Note: Use of non-chlorine-activated fluxes is highly recommended.

Regulatory Information

The HCPL-7860/HCPL-786J has been approved by the following organizations:

IEC/EN/DIN EN 60747-5-2

Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2
(VDE 0884 Teil 2):2003-01.

UL

Approval under UL 1577, component recognition program. File E55361.

CSA

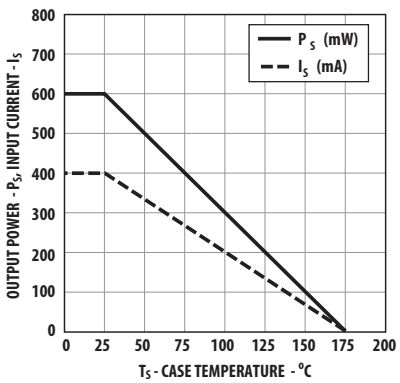
Approval under CSA Component Acceptance Notice #5, File CA 88324.

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IEC/EN/DIN EN 60747-5-2 Insulation Characteristics[1]

Description	Symbol	HCPL-7860	HCPL-786J	Unit
Installation classification per DIN VDE 0110/1.89, Table 1				
for rated mains voltage ≤ 300 Vrms		I - IV	I - IV	
for rated mains voltage ≤ 450 Vrms		I - III	I - IV	
for rated mains voltage ≤ 600 Vrms		I - III	I - IV	
for rated mains voltage ≤ 1000 Vrms		I - II	I - III	
Climatic Classification		40/85/21	40/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1230	Vpeak
Input to Output Test Voltage, Method b [2] V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1670	2306	Vpeak
Input to Output Test Voltage, Method a[2] V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1425	1968	Vpeak
Highest Allowable Overvoltage(Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	8000	Vpeak
Safety-limiting values - maximum values allowed in the event of a failure.				
Case Temperature	T_S	175	175	°C
Input Current [3]	$I_{S, INPUT}$	400	400	mA
Output Power [3]	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

Notes:
1. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application. Surface Mount Classifications is Class A in accordance with CECC00802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.
3. Refer to the following figure for dependence of P_S and I_S on ambient temperature.



Insulation and Safety Related Specifications

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Parameter	Symbol	DIP-8	SO-16	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.4	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Ambient Operating Temperature	T_A	-40	85	°C	
Supply Voltages	V_{DD1}, V_{DD2}	0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} + 0.5	V	1
Two Second Transient Input Voltage		-6.0			
Output Voltages	MCLK, MDAT	-0.5	V_{DD2} + 0.5	V	
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Maximum Solder Reflow Thermal Profile section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Ambient Operating Temperature	T_A	-40	+85	°C	
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	
Input Voltage	V_{IN+}, V_{IN-}	-200	+200	mV	1

Electrical Specifications (DC)

Unless otherwise noted, all specifications are at V_{IN+} = 0 V and V_{IN-} = 0 V, all Typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V, and all Minimum and Maximum specifications apply over the following ranges: T_A = -40°C to +85°C, V_{DD1} = 4.5 to 5.5 V and V_{DD2} = 4.5 to 5.5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Average Input Bias Current	I_{IN}		-0.8		µA		1	3
Average Input Resistance	R_{IN}		450		k Ω			3
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		60		dB			4
Output Logic High Voltage	V_{OH}	3.9	4.9		V	I_{OUT} = -100 µA		
Output Logic Low Voltage	V_{OL}		0.1	0.6	V	I_{OUT} = 1.6 mA		
Output Short Circuit Current	$\|I_{OSC}\|$		30		mA	V_{OUT} = V_{DD2} or GND2		5
Input Supply Current	I_{DD1}		10	15	mA	V_{IN+} = -350 mV to +350 mV	2	
Output Supply Current	I_{DD2}		10	15	mA		3	
Output Clock Frequency	f_{CLK}	8.2	10	13.2	MHz		4	
Data Hold Time	t_{HDDAT}		15		ns			6

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Electrical Specifications (Tested with HCPL-0872 or Sinc^3 Filter)

Unless otherwise noted, all specifications are at V_{IN+} = -200 mV to +200 mV and V_{IN-} = 0 V; all Typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V, and all Minimum and Maximum specifications apply over the following ranges: T_A = -40°C to +85°C, V_{DD1} = 4.5 to 5.5 V and V_{DD2} = 4.5 to 5.5 V.

STATIC CHARACTERISTICS

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Resolution			15			bits			7
Integral Nonlinearity		INL		3	30	LSB		5	8
				0.01	0.14	%		6	8
Differential Nonlinearity		DNL			1	LSB			9
Uncalibrated Input Offset		V_{OS}	-3	0	3	mV	V_{IN+} = 0 V	7	
Offset Drift vs. Temperature		dV_{OS}/dT_A		2	10	µV/°C	V_{IN+} = 0 V	7	10
Offset drift vs. VDD1		dV_{OS}/dV_{DD1}		0.12		mV/V	V_{IN+} = 0 V	7	
Internal Reference Voltage		V_{REF}		320		mV		8	
Absolute Reference Voltage Tolerance			-4		4	%		8	2
Reference Voltage Matching	HCPL-7860		-1		1	%	T_A = 25°C.	8	2
	HCPL-786J		-2		2	%			
V_{REF} Drift vs. Temperature		dV_{REF}/dT_A		60		ppm/°C.		8	
V_{REF} Drift vs. VDD1		dV_{REF}/dV_{DD1}		0.2		%		8	
Full Scale Input Range			$-V_{REF}$		$+V_{REF}$	mV			11
Recommended Input Voltage Range			-200		+200	mV			

DYNAMIC CHARACTERISTICS (Digital Interface IC HCPL-0872 is set to Conversion Mode 3.)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Signal-to-Noise Ratio	SNR	62	73		dB	V_{IN+} = 35 Hz, 400 mV_{pk-pk} (141 mV_{rms}) sine wave.	9,10	
Total Harmonic Distortion	THD		-67		dB			
Signal-to-(Noise + Distortion)	SND		66		dB			
Effective Number of Bits	ENOB	10	12		bits		11	12
Conversion Time	t_{C2}		0.2	0.8	µs	Pre-Trigger Mode 2	1,12	13
	t_{C1}		19	23	µs	Pre-Trigger Mode 1	1,12	13
	t_{C0}		39	47	µs	Pre-Trigger Mode 0	1,12	
Signal Delay	t_{DSIG}		19	23	µs		13	14
Over-Range Detect Time	t_{OVR1}	2.0	3.0	4.2	µs	V_{IN+} = 0 to 400mV step waveform	14	15
Threshold Detect Time (default configuration)	t_{THR1}		10		µs			16
Signal Bandwidth	BW	18	22		kHz		15	17
Isolation Transient Immunity	CMR	15	20		kV/µs	V_{ISO} = 1 kV		18

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Package Characteristics

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Conditions	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	HCPL-7860	3750			Vrms	RH ≤ 50%, t = 1 min; T_A = 25°C	19, 20
		HCPL-786J	5000					
Input-Output Resistance	R_{I-O}		10^{12}	10^{13}		Ω	V_{I-O} = 500 Vdc	20
			10^{11}				T_A = 100°C	
Input-Output Capacitance	C_{I-O}			1.4		pF	f = 1 MHz	20
Input IC Junction-to-Case Thermal Resistance	θ_{jci}			96		°C/W	Thermocouple located at center underside of package	
Output IC Junction-to-Case Thermal Resistance	θ_{jco}			114		°C/W		

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification, or Avago Technologies Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. If V_{IN-} (pin 3) is brought above V_{DD1} - 2 V with respect to GND1 an internal optical-coupling test mode may be activated. This test mode is not intended for customer use.
2. All units within each HCPL-7860 standard packaging increment (either 50 per tube or 1000 per reel) have a Reference Voltage Matching of ± 1%. An Absolute Reference Voltage Tolerance of ± 4% is guaranteed between standard packaging increments.
3. Because of the switched-capacitor nature of the isolated modulator, time averaged values are shown.
4. $CMRR_{IN}$ is defined as the ratio of the gain for differential inputs applied between V_{IN+} and V_{IN-} to the gain for common-mode inputs applied to both V_{IN+} and V_{IN-} with respect to input ground GND1.
5. Short-circuit current is the amount of output current generated when either output is shorted to V_{DD2} or GND2. Use under these conditions is not recommended.
6. Data hold time is amount of time that the data output MDAT will stay stable following the rising edge of output clock MCLK.
7. Resolution is defined as the total number of output bits. The useable accuracy of any A/D converter is a function of its linearity and signal-to-noise ratio, rather than how many total bits it has.
8. Integral nonlinearity is defined as one-half the peak-to-peak deviation of the best-fit line through the transfer curve for V_{IN+} = -200 mV to +200 mV, expressed either as the number of LSBs or as a percent of measured input range (400 mV).
9. Differential nonlinearity is defined as the deviation of the actual difference from the ideal difference between midpoints of successive output codes, expressed in LSBs.
10. Data sheet value is the average magnitude of the difference in offset voltage from T_A =25°C to T_A= 85°C, expressed in microvolts per °C. Three standard deviation from typical value is less than 6 µV/°C.
11. Beyond the full-scale input range the output is either all zeroes or all ones.
12. The effective number of bits (or effective resolution) is defined by the equation ENOB = (SNR-1.76)/6.02 and represents the resolution of an ideal, quantization-noise limited A/D converter with the same SNR.
13. Conversion time is defined as the time from when the convert start signal CS is brought low to when SDAT goes high, indicating that output data is ready to be clocked out. This can be as small as a few cycles of the isolated modulator clock and is determined by the frequency of the isolated modulator clock and the selected Conversion and Pre-Trigger modes. For determining the true signal delay characteristics of the A/D converter for closed-loop phase margin calculations, the signal delay specification should be used.
14. Signal delay is defined as the effective delay of the input signal through the Isolated A/D converter. It can be measured by applying a -200 mV to ± 200 mV step at the input of modulator and adjusting the relative delay of the convert start signal CS so that the output of the converter is at mid scale. The signal delay is the elapsed time from when the step signal is applied at the input to when output data is ready at the end of the conversion cycle. The signal delay is the most important specification for determining the true signal delay characteristics of the A/D converter and should be used for determining phase margins in closed-loop applications. The signal delay is determined by the frequency of the modulator clock and which Conversion Mode is selected, and is independent of the selected Pre-Trigger Mode and, therefore, conversion time.
15. The minimum and maximum overrange detection time is determined by the frequency of the channel 1 isolated modulator clock.
16. The minimum and maximum threshold detection time is determined by the user-defined configuration of the adjustable threshold detection circuit and the frequency of the channel 1 isolated modulator clock. See the Applications Information section for further detail. The specified times apply for the default configuration.
17. The signal bandwidth is the frequency at which the magnitude of the output signal has decreased 3 dB below its low-frequency value. The signal bandwidth is determined by the frequency of the modulator clock and the selected Conversion Mode.
18. The isolation transient immunity (also known as Common-Mode Rejection) specifies the minimum rate-of-rise of an isolation-mode signal applied across the isolation boundary beyond which the modulator clock or data signals are corrupted.
19. In accordance with UL1577, for devices with minimum V_{ISO} specified at 3750 Vrms(HCPL-7860) or 5000 Vmrs (HCPL-786J) , each isolated modulator (optocoupler) is proof-tested by applying an insulation test voltage greater than 4500 Vrms (HCPL-7860) or 6000 Vrms (HCPl-786J) for one second. This test is performed before the Method b, 100% production test for partial discharge shown in IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table.
20. This is a two-terminal measurement: pins 1-4 are shorted together and pins 5-8 are shorted together.

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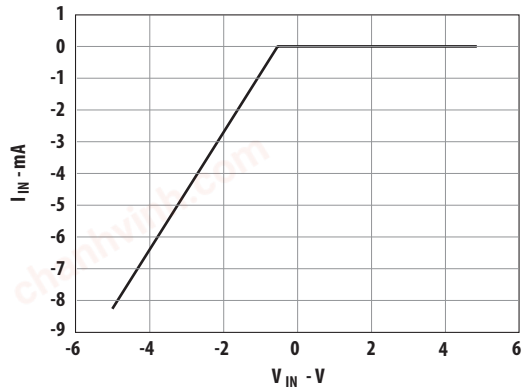


Figure 1. I_{IN} vs. V_{IN}.

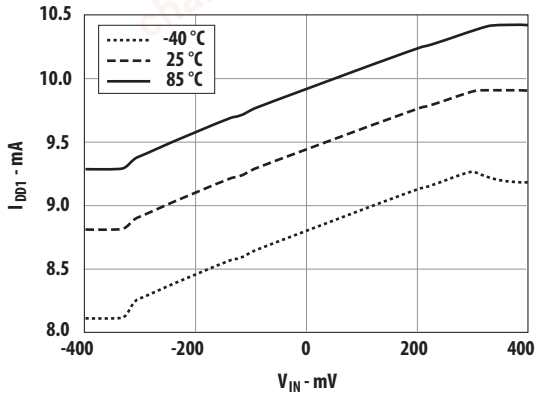


Figure 2. I_{DD1} vs. V_{IN}.

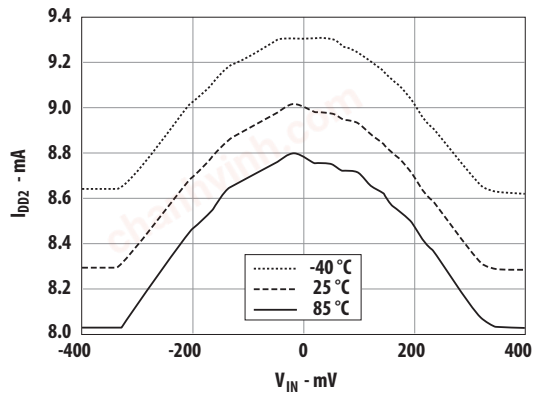


Figure 3. I_{DD2} vs. V_{IN}.

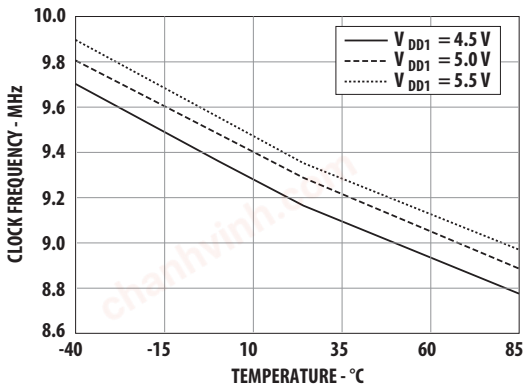


Figure 4. Clock Frequency vs. Temperature.

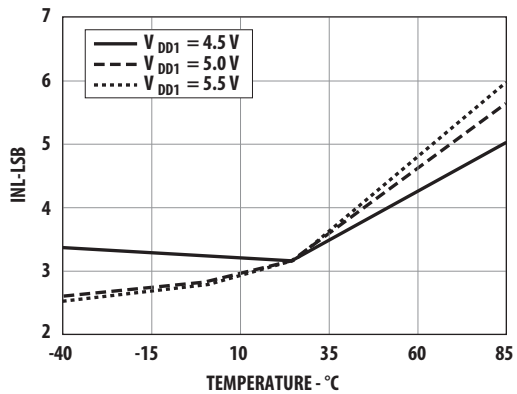


Figure 5. INL (Bits) vs. Temperature

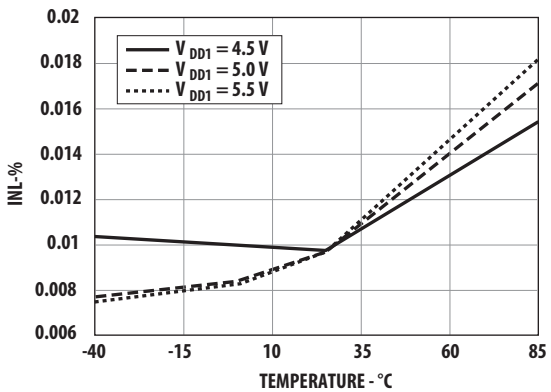


Figure 6. INL (%) vs. Temperature

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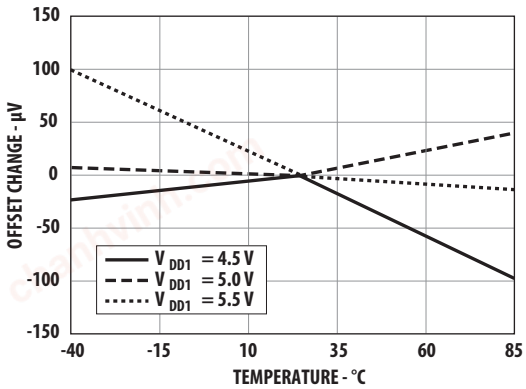


Figure 7. Offset Change vs. Temperature

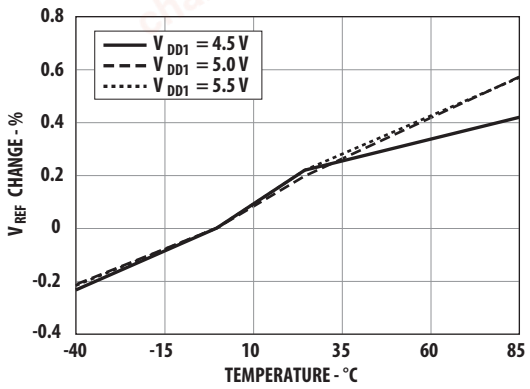


Figure 8. V_{REF} Change vs. Temperature

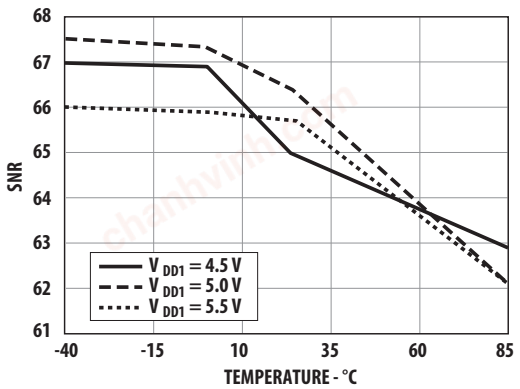


Figure 9. SNR vs. Temperature

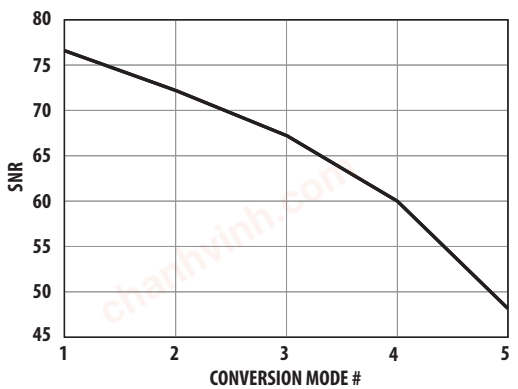


Figure 10. SNR vs. Conversion Mode.

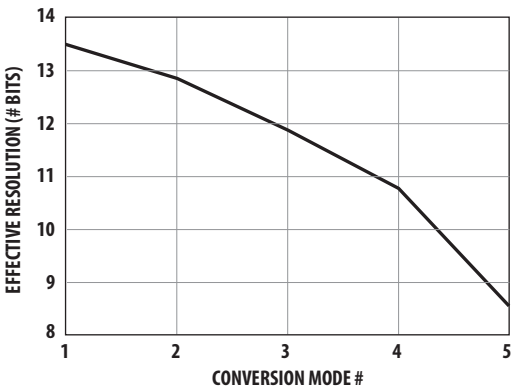


Figure 11. Effective Resolution vs. Conversion Mode.

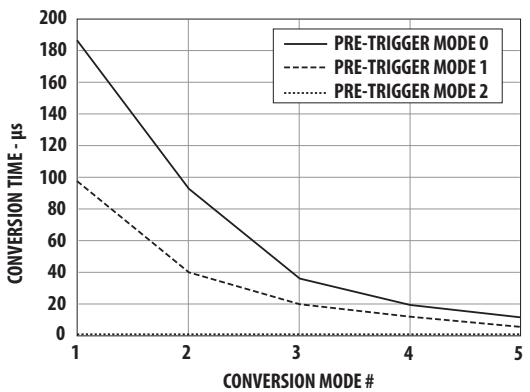


Figure 12. Conversion Time vs. Conversion Mode.

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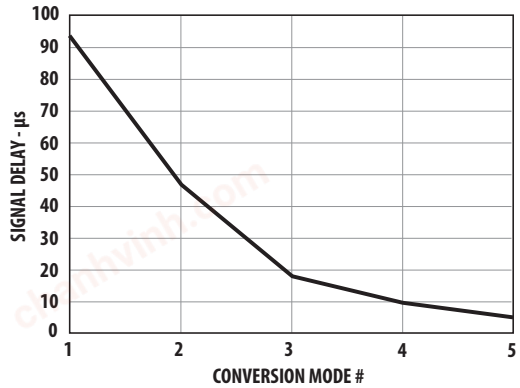


Figure 13. Signal Delay vs. Conversion Mode.

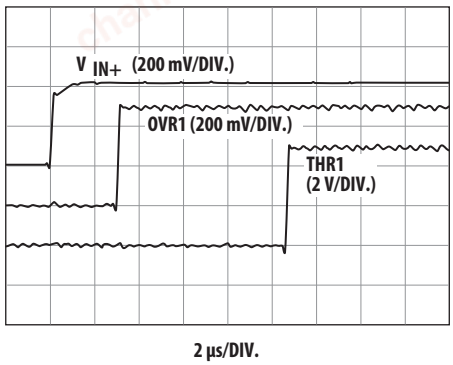


Figure 14. Over-Range and Threshold Detect Times.

Application Information

Digital Current Sensing

As shown in Figure 16, using the Isolated 2-chip A/D converter to sense current can be as simple as connecting a current-sensing resistor, or shunt, to the input and reading output data through the 3-wire serial output interface. By choosing the appropriate shunt resistance, any range of current can be monitored, from less than 1 A to more than 100 A.

Even better performance can be achieved by fully utilizing the more advanced features of the Isolated A/D converter, such as the pre-trigger circuit, which can reduce conversion time to less than 1 µs, the fast over-range detector for quickly detecting short circuits, different conversion modes giving various resolution/speed trade-offs, offset calibration mode to eliminate initial offset from measurements, and an adjustable threshold detector for detecting non-short circuit overload conditions.

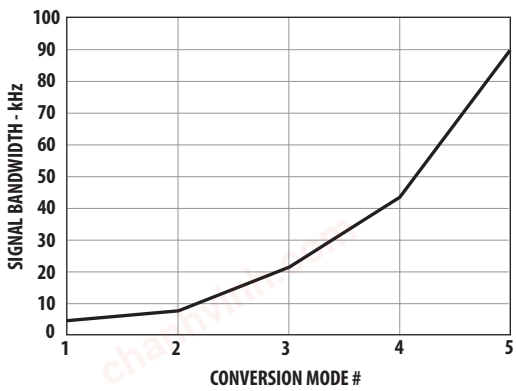


Figure 15. Signal Bandwidth vs. Conversion Mode.

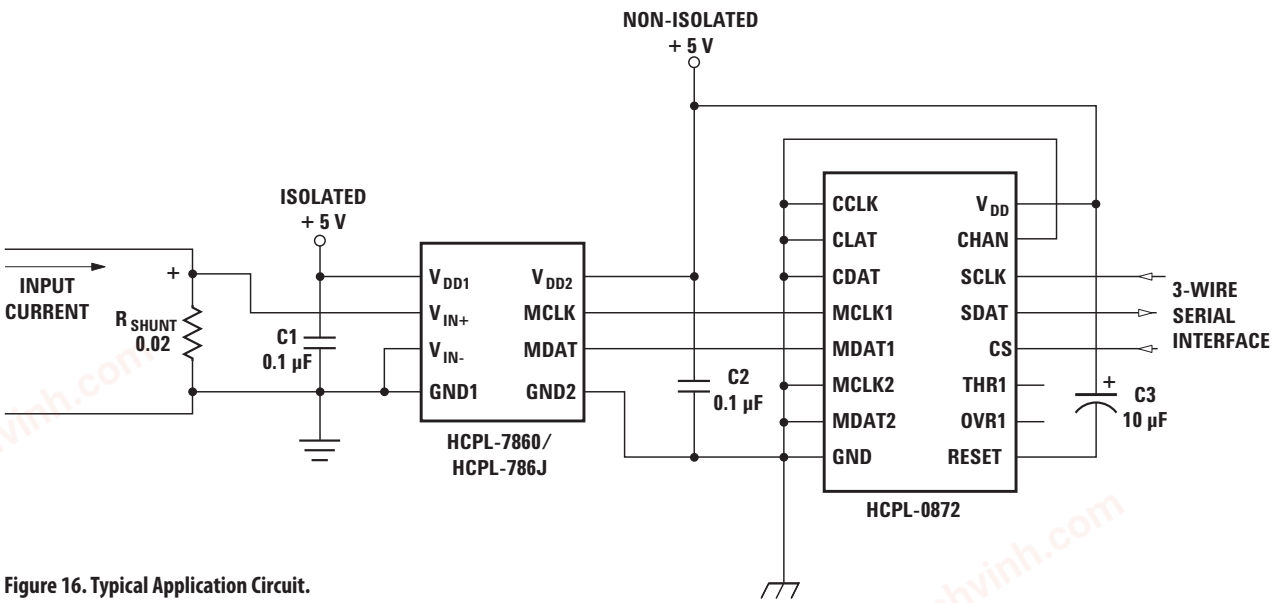


Figure 16. Typical Application Circuit.

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Product Description

The HCPL-7860/HCPL-786J Isolated Modulator (optocoupler) uses sigma-delta modulation to convert an analog input signal into a high-speed (10 MHz) single-bit digital data stream; the time average of the modulator's single-bit data is directly proportional to the input signal. The isolated modulator's other main function is to provide galvanic isolation between the analog input and the digital output. An internal voltage reference determines the full-scale analog input range of the modulator (approximately ± 320 mV); an input range of ± 200 mV is recommended to achieve optimal performance.

HCPL-7860/HCPL-786J can be used together with HCPL-0872, Digital Interface IC or a digital filter. The primary functions of the HCPL-0872 Digital Interface IC are to derive a multi-bit output signal by averaging the single-bit modulator data, as well as to provide a direct microcontroller interface. The effective resolution of the multi-bit output signal is a function of the length of time (measured in modulator clock cycles) over which the average is taken; averaging over longer periods of time results in higher resolution. The Digital Interface IC can be configured for five conversion modes, which have different combinations of speed and resolution to achieve the desired level of performance. Other functions of the HCPL-0872 Digital Interface IC include a Phase Locked Loop based pre-trigger circuit that can either give more precise control of the effective sampling time or reduce conversion time to less than 1 µs, a fast over-range detection circuit that rapidly indicates when the magnitude of the input signal is beyond full-scale, an adjustable threshold detection circuit that indicates when the magnitude of the input signal is above a user adjustable threshold level, an offset calibration circuit, and a second multiplexed input that allows a second Isolated Modulator to be used with a single Digital Interface IC.

The digital output format of the Isolated A/D Converter is 15 bits of unsigned binary data. The input full-scale range and code assignment is shown in Table 1 below. Although the output contains 15 bits of data, the effective resolution is lower and is determined by selected conversion mode as shown in Table 2 below.

Table 1. Input Full-Scale Range and Code Assignment.

Analog Input	Voltage Input	Digital Output
Full Scale Range	640 mV	32768 LSBs
Minimum Step Size	20 µV	1 LSB
+Full Scale	+320 mV	111111111111111
Zero	0 mV	100000000000000
-Full Scale	-320 mV	000000000000000

Table 2. Isolated A/D Converter Typical Performance Characteristics.

Conversion Mode	Signal-to-Noise Ratio (dB)	Effective Resolution (bits)	Conversion Time (µs)			Signal Delay(µs)	Signal Bandwidth (kHz)
			Pre-Trigger Mode				
			0	1	2		
1	83	13.5	205	102		102	3.4
2	79	12.8	103	51		51	6.9
3	73	11.9	39	19	0.2	19	22
4	***66***	***10.7***	***20***	10		***10***	***45***
5	53	8.5	10	5		5	90

Notes: Bold italic type indicates Default values.

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Power Supplies and Bypassing

The recommended application circuit is shown in Figure 17. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple zener diode (D1); the value of resistor R1 should be chosen to supply sufficient current from the existing floating supply. The voltage from the current sensing resistor or shunt (Rsense) is applied to the input of the HCPL-7860/HCPL-786J (U2) through an RC anti-aliasing filter (R2 and C2). And finally, the output clock and data of the isolated modulator are connected to the digital interface IC. Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

The power supply for the isolated modulator is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

An inexpensive 78L05 three-terminal regulator can also be used to reduce the floating supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 17, 0.1 µF bypass capacitors (C1 and C3) should be located as close as possible to the input and output power-supply pins of the isolated modulator (U2). The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolated modulator. A 0.01 µF bypass capacitor (C2) is also recommended at the input due to the switched-capacitor nature of the input circuit. The input bypass capacitor also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal.

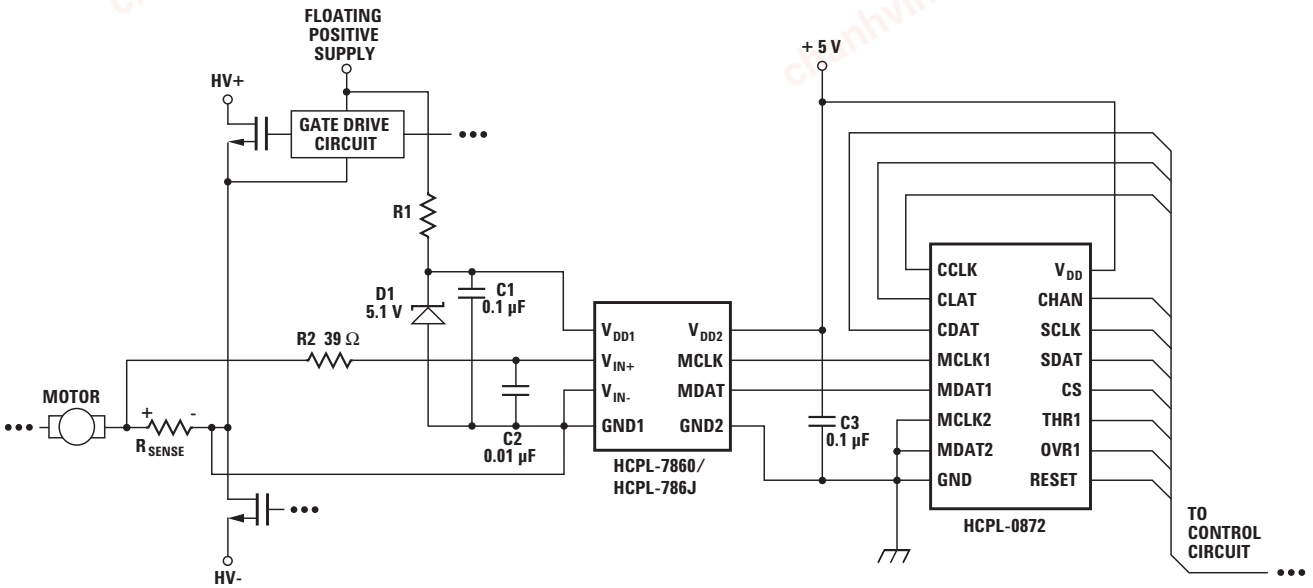


Figure 17. Recommended Application Circuit.

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PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. In addition, the layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

Shunt Resistors

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, while larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolated modulator. The first step in selecting a shunt is determining how much current the shunt will be sensing. The graph in Figure 18 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolated modulator. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the shunt should see during normal operation. For example, if a motor will have a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (= 10 x 1.414 x 1.5). Assuming a maximum input voltage of 200 mV, the maximum value of shunt resistance in this case would be about 10 mΩ.

The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 1 W in the previous example.

If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum value to decrease power dissipation. The minimum value of the shunt is limited by precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. The effect increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal resistance of the shunt or by using a shunt with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the shunt on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

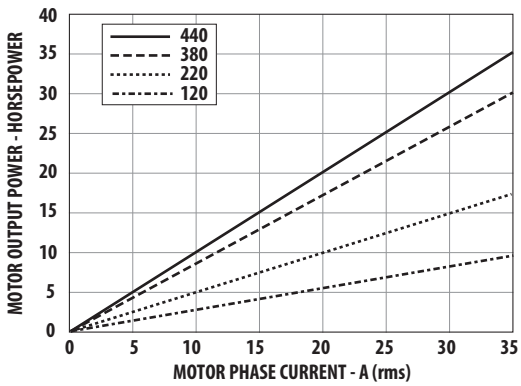


Figure 18. Motor Output Horsepower vs. Motor Phase Current and Supply Voltage.

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For a two-terminal shunt, as the value of shunt resistance decreases, the resistance of the leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the lead during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall. Both of these effects are eliminated when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

Several four-terminal shunts from Isotek (Isabellenhütte) suitable for sensing currents in motor drives up to 71 Arms (71 hp or 53 kW) are shown in Table 3; the maximum current and motor power range for each of the PBV series shunts are indicated. For shunt resistances from 50 mΩ down to 10 mΩ, the maximum current is limited by the input voltage range of the isolated modulator. For the 5 mΩ and 2 mΩ shunts, a heat sink may be required due to the increased power dissipation at higher currents.

When laying out a PC board for the shunts, a couple of points should be kept in mind. The Kelvin connections to the shunt should be brought together under the body of the shunt and then run very close to each other to the input of the isolated modulator; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the shunt is not located on the same PC board as the isolated modulator circuit, a tightly twisted pair of wires can accomplish the same thing.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the shunt to help distribute the current between the layers of the PC board. The PC board should use 2 or 4 oz. copper for the layers, resulting in a current carrying capacity in excess of 20 A. Making the current carrying traces on the PC board fairly large can also improve the shunt's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

Table 3. Isotek (Isabellenhütte) Four-Terminal Shunt Summary.

Shunt Resistor Part Number	Shunt Resistance	Tol.	Maximum RMS Current	Motor Power Range 120 V_{AC} - 440 V_{AC}	
	mΩ	%	A	hp	kW
PBV-R050-0.5	50	0.5	3	0.8 - 3	0.6 - 2
PBV-R020-0.5	20	0.5	7	2 - 7	0.6 - 2
PBV-R010-0.5	10	0.5	14	4 - 14	3 - 10
PBV-R005-0.5	5	0.5	25 [28]	7 - 25 [8 - 28]	5 - 19 [6 - 21]
PBV-R002-0.5	2	0.5	39 [71]	11 - 39 [19 - 71]	8 - 29 [14 - 53]

Note: Values in brackets are with a heatsink for the shunt.

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Shunt Connections

The recommended method for connecting the isolated modulator to the shunt resistor is shown in Figure 17. V_{IN+} (pin 2 of the HPCL-7860/HCPL-786J) is connected to the positive terminal of the shunt resistor, while V_{IN-} (pin 3) is shorted to GND1 with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolated modulator circuit to the shunt resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the shunt are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current shunt.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the isolated modulator to the sense resistor be the only return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolated modulator circuit and the gate drive circuit should be the positive power supply line.

In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting V_{IN+} and V_{IN-} directly across the shunt resistor with two conductors, and connecting GND1 to the shunt resistor with a third conductor for the power-supply return path, as shown in Figure 19. When connected this way, both input pins should be bypassed. To minimize electromagnetic interference of the sense signal, all of the conductors (whether two or three are used) connecting the isolated modulator to the sense resistor should be either twisted pair wire or closely spaced traces on a PC board.

The 39 Ω resistor in series with the input lead (R2) forms a lowpass anti-aliasing filter with the 0.01 µF input bypass capacitor (C2) with a 400 kHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the inductance of wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

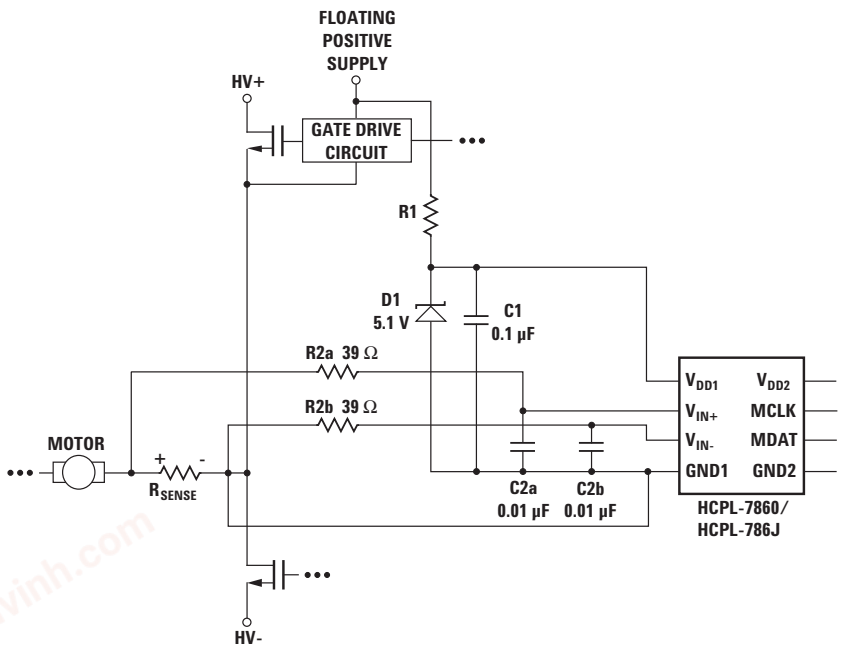


Figure 19. Schematic for Three Conductor Shunt Connection.

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Voltage Sensing

The HCPL-7860/HCPL-786J Isolated Modulator can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (280 kΩ) and input bias current (1 μA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 39 Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth. To obtain higher bandwidth, the input bypass capacitor (C2) can be reduced, but it should not be reduced much below 1000 pF to maintain adequate input bypassing of the isolated modulator.

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