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High CMR Isolation Amplifiers

Technical Data

HCPL-7800
HCPL-7800A
HCPL-7800B

Features

- **15 kV/μs Common-Mode Rejection at V_{CM} = 1000 V***
- **Compact, Auto-Insertable Standard 8-pin DIP Package**
- **4.6 μV/°C Offset Drift vs. Temperature**
- **0.9 mV Input Offset Voltage**
- **85 kHz Bandwidth**
- **0.1% Nonlinearity**
- **Worldwide Safety Approval: UL 1577 (3750 V rms/1 min), VDE 0884 and CSA**
- **Advanced Sigma-Delta (ΣΔ) A/D Converter Technology**
- **Fully Differential Circuit Topology**
- **1 μm CMOS IC Technology**

Applications

- **Motor Phase Current Sensing**
- **General Purpose Current Sensing**
- **High-Voltage Power Source Voltage Monitoring**
- **Switch-Mode Power Supply Signal Isolation**
- **General Purpose Analog Signal Isolation**
- **Transducer Isolation**

*The terms common-mode rejection (CMR) and isolation-mode rejection (IMR) are used interchangeably throughout this data sheet.

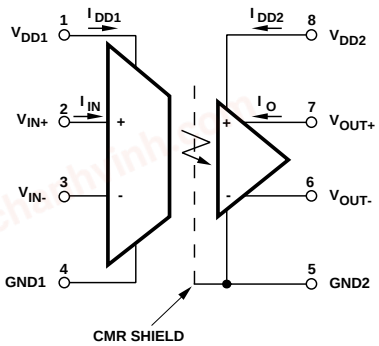
Description

The HCPL-7800 high CMR isolation amplifier provides a unique combination of features ideally suited for motor control circuit designers. The product provides the precision and stability needed to accurately monitor motor current in high-noise motor control environments, providing for smoother control (less "torque ripple") in various types of motor control applications.

This product paves the way for a smaller, lighter, easier to produce, high noise rejection, low cost solution to motor current sensing. The product can also be used for general analog signal isolation applications requiring high accuracy, stability and linearity under similarly severe noise conditions. For general applications, we recommend the HCPL-7800 which exhibits a part-to-part gain tolerance of ± 5%. For precision applications, HP offers the HCPL-7800A and HCPL-7800B, each with part-to-part gain tolerances of ± 1%.

The HCPL-7800 utilizes sigma-delta (ΣΔ) analog-to-digital converter technology, chopper stabilized amplifiers, and a fully differential circuit topology fabricated using HP's 1 μm CMOS IC process. The part also couples our high-efficiency, high-speed AlGaAs LED to a high-speed, noise-shielded detector

Functional Diagram



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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using our patented “light-pipe” optocoupler packaging technology.

Together, these features deliver unequaled isolation-mode noise rejection, as well as excellent offset and gain accuracy and stability over time and temperature. This performance is delivered in a compact, auto-insertable, industry standard 8-pin DIP package that meets worldwide regulatory safety standards (gull-wing surface mount option #300 also available).

Ordering Information:

HCPL-7800x

- No Specifier = ± 5% Gain Tol.; Mean Gain Value = 8.00
- A = ± 1% Gain Tol.; Mean Gain Value = 7.93
- B = ± 1% Gain Tol.; Mean Gain Value = 8.07

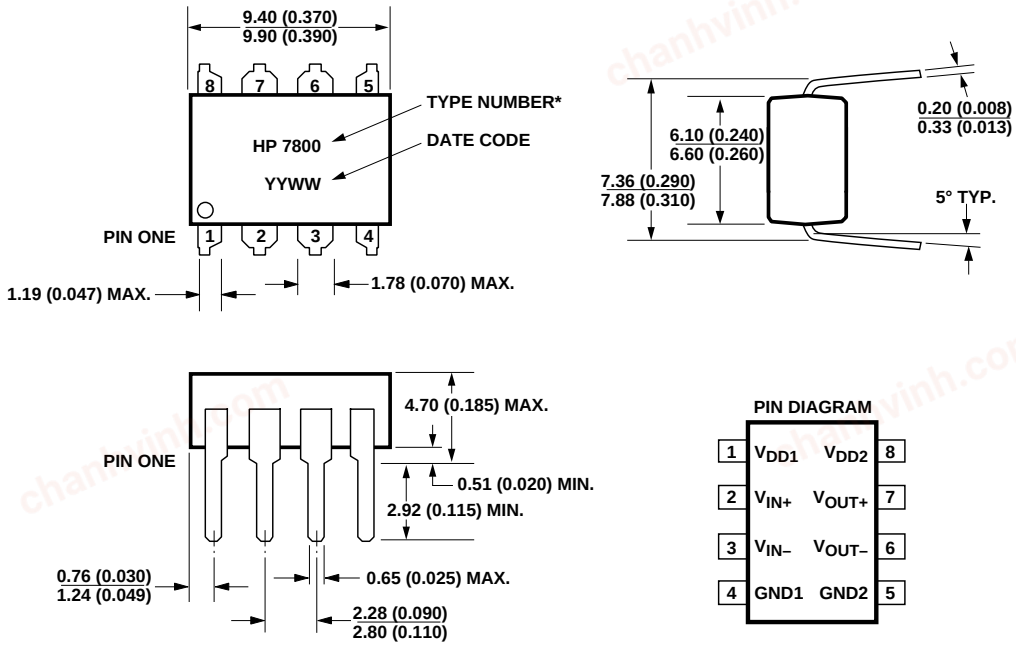
Option yyy

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

Option datasheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings

Standard DIP Package

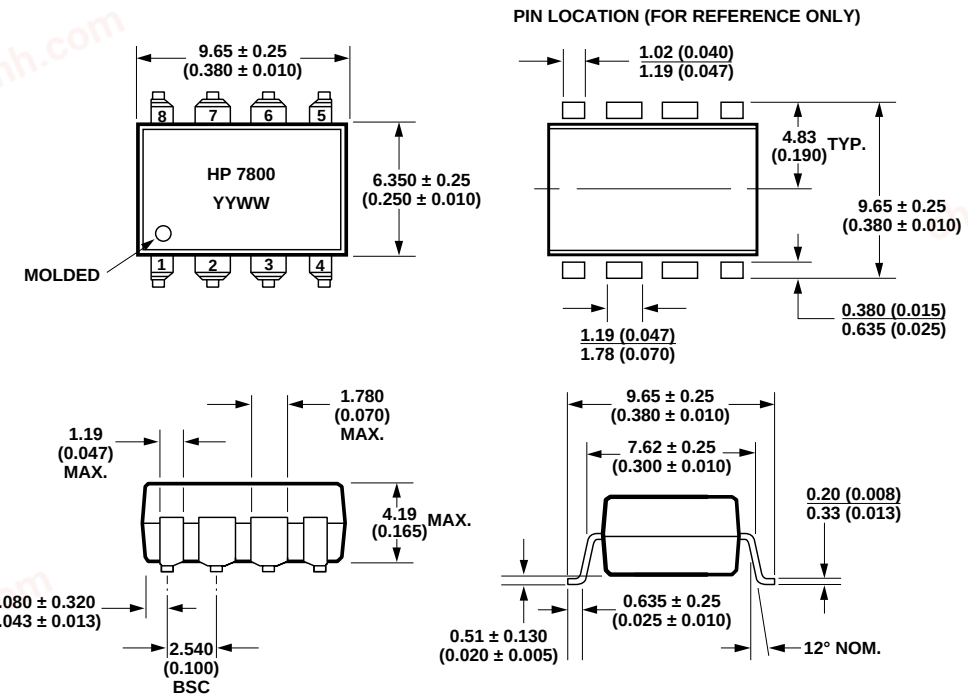


DIMENSIONS IN MILLIMETERS AND (INCHES).

* TYPE NUMBER FOR: HCPL-7800 = 7800
HCPL-7800A = 7800A
HCPL-7800B = 7800B

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Gull Wing Surface Mount Option 300*

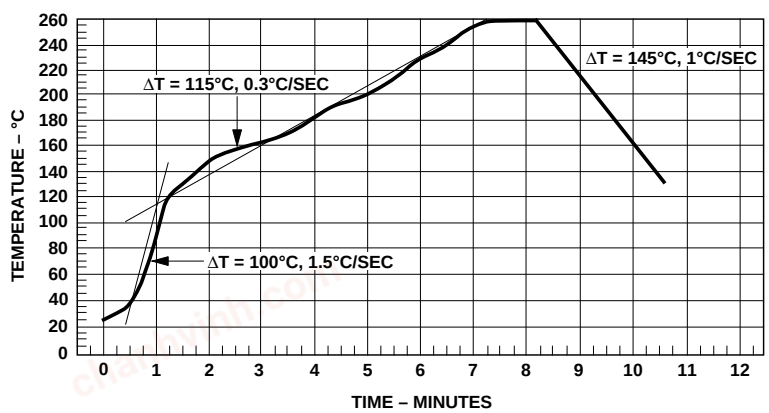


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

* REFER TO OPTION 300 DATA SHEET FOR MORE INFORMATION.

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

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Regulatory Information

The HCPL-7800 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		III a		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 (06.92) Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 600 V rms		 I-IV I-III	
Climatic Classification		40/100/21	
Pollution Degree (DIN VDE 0110, Table 1)*		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V peak
Input to Output Test Voltage, Method b** V_{PR} = 1.875 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	1591	V peak
Input to Output Test Voltage, Method a** V_{PR} = 1.5 x V_{IORM}, Type and sample test with t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	1273	V peak
Highest Allowable Overvoltage** (Transient Overvoltage t_{TR} = 10 sec)	V_{TR}	6000	V peak
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 27) Case Temperature Input Power Output Power	 T_S $P_{S,Input}$ $P_{S,Output}$	 175 80 250	 °C mW mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 1×10^{12}	Ω

*This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V rms (per DIN VDE 0110).
**Refer to the front of the optocoupler section of the current catalog for a more detailed description of VDE 0884 and other product safety requirements.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	℃	
Ambient Operating Temperature	T_A	-40	100	℃	
Supply Voltages	V_{DD1}, V_{DD2}	0.0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} +0.5	V	
Two Second Transient Input Voltage		-6.0			
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2} +0.5	V	
Lead Solder Temperature (1.6 mm below seating plane, 10 sec.)	T_{LS}		260	℃	1
Reflow Temperature Profile	See **Package Outline Drawings** Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40	85	℃	2
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	3
Input Voltage	V_{IN+}, V_{IN-}	-200	200	mV	4
Output Current	$\|I_O\|$		1	mA	5

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DC Electrical Specifications

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-1.8	-0.9	0.0	mV		1	
Input Offset Drift vs. Temperature	dV_{OS}/dT		-2.1		µV/°C		1, 2	6
Abs. Value of Input Offset Drift vs. Temperature	$\lvert dV_{OS}/dT \rvert$		4.6		µV/°C		1	7
Input Offset Drift vs. V_{DD1}	dV_{OS}/dV_{DD1}		30		µV/V		1, 3	8
Input Offset Drift vs. V_{DD2}	dV_{OS}/dV_{DD2}		-40		µV/V		1, 4	9
Gain (± 5% Tol.)	G	7.61	8.00	8.40		-200 mV < V_{IN+} < 200 mV	1, 5	10
Gain - A Version (± 1% Tol.)	G_A	7.85	7.93	8.01				
Gain - B Version (± 1% Tol.)	G_B	7.99	8.07	8.15				
Gain Drift vs. Temperature	dG/dT		0.001		%/°C		5, 6	11
Abs. Value of Gain Drift vs. Temperature	$\lvert dG/dT \rvert$		0.001		%/°C		5	12
Gain Drift vs. V_{DD1}	dG/dV_{DD1}		0.21		%/V		5, 7	13
Gain Drift vs. V_{DD2}	dG/dV_{DD2}		-0.06		%/V		5, 8	14
200 mV Nonlinearity	NL_{200}		0.2	0.35	%		5, 9	15
200 mV Nonlinearity Drift vs. Temperature	dNL_{200}/dT		-0.001		% pts/°C		5, 10	16
200 mV Nonlinearity Drift vs. V_{DD1}	dNL_{200}/dV_{DD1}		-0.005		% pts/V		5, 11	17
200 mV Nonlinearity Drift vs. V_{DD2}	dNL_{200}/dV_{DD2}		-0.007		% pts/V		5, 12	18
100 mV Nonlinearity	NL_{100}		0.1	0.25	%	-100 mV< V_{IN+} < 100 mV	5, 13	19
Maximum Input Voltage Before Output Clipping	$\lvert V_{IN+} \rvert_{max}$		300		mV		14	
Average Input Bias Current	I_{IN}		-670		nA		15, 16	20
Input Bias Current Temperature Coefficient	dI_{IN}/dT		3		nA/°C			
Average Input Resistance	R_{IN}		530		kΩ		15	20
Input Resistance Temperature Coefficient	dR_{IN}/dT		0.38		%/°C			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		72		dB			21
Output Resistance	R_O		11		Ω			5
Output Resistance Temperature Coefficient	dR_O/dT		0.6		%/°C			
Output Low Voltage	V_{OL}		1.18		V	$\lvert V_{IN+} \rvert$ = 500 mV I_{OUT+} = 0 A, I_{OUT-} = 0 A	14	22
Output High Voltage	V_{OH}		3.61		V			
Output Common-Mode Voltage	V_{OCM}	2.20	2.39	2.60	V	-40°C < T_A < 85°C 4.5 V < V_{DD1} < 5.5 V	14	
Input Supply Current	I_{DD1}		10.7	15.5	mA		17	23
Output Supply Current	I_{DD2}		11.6	14.5	mA	V_{IN+} = 200 mV, -40°C < T_A < 85°C 4.5 V < V_{DD2} < 5.5 V	18	24
Output Short-Circuit Current	$\lvert I_{OSC} \rvert$		9.3		mA	V_{OUT} = 0 V or V_{DD2}		25

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AC Electrical Specifications

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Rising Edge Isolation Mode Rejection	IMR_R	10	25		kV/µs	V_{IM} = 1 kV	19, 20	26
Falling Edge Isolation Mode Rejection	IMR_F	10	15		kV/µs			
Isolation Mode Rejection Ratio at 60 Hz	IMRR		>140		dB		19	27
Propagation Delay to 10%	t_{PD10}		2.0	3.3	µs	-40°C < T_A < 85°C	21, 22	
Propagation Delay to 50%	t_{PD50}		3.4	5.6	µs			
Propagation Delay to 90%	t_{PD90}		6.3	9.9	µs			
Rise/Fall Time (10%-90%)	$t_{R/F}$		4.3	6.6	µs			
Bandwidth (-3 dB)	f_{-3dB}	50	85		kHz		23, 24	
Bandwidth (-45°)	$f_{-45°}$		35		kHz			
RMS Input-Referred Noise	V_N		300		µV rms	Bandwidth = 100 kHz	25, 26	28
Power Supply Rejection	PSR		5		mV_{p-p}			29

Package Characteristics

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	t = 1 min., RH ≤ 50%			30, 31
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C	V_{I-O} = 500 Vdc		30
		10^{11}				T_A = 100°C			
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz			30
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		96		°C/W				32
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		114		°C/W				

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

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Notes:
General Note: Typical values represent the mean value of all characterization units at the nominal operating conditions. Typical drift specifications are determined by calculating the rate of change of the specified parameter versus the drift parameter (at nominal operating conditions) for each characterization unit, and then averaging the individual unit rates. The corresponding drift figures are normalized to the nominal operating conditions and show how much drift occurs as the particular drift parameter is varied from its nominal value, with all other parameters held at their nominal operating values. Figures show the mean drift of all characterization units as a group, as well as the ± 2-sigma statistical limits. Note that the typical drift specifications in the tables below may differ from the slopes of the mean curves shown in the corresponding figures.

1. HP recommends the use of non-chlorine activated fluxes.
2. The HCPL-7800 will operate properly at ambient temperatures up to 100°C but may not meet published specifications under these conditions.
3. DC performance can be best maintained by keeping V_{DD1} and V_{DD2} as close as possible to 5 V. See application section for circuit recommendations.
4. HP recommends operation with V_{IN-} = 0 V (tied to GND1). Limiting V_{IN+} to 100 mV will improve DC nonlinearity and nonlinearity drift. If V_{IN-} is brought above 800 mV with respect to GND1, an internal test mode may be activated. This test mode is not intended for customer use.
5. Although, statistically, the average difference in the output resistance of pins 6 and 7 is near zero, the standard deviation of the difference is 1.3 Ω due to normal process variations. Consequently, keeping the output current below 1 mA will ensure the best offset performance.
6. Data sheet value is the average change in offset voltage versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the change in offset voltage per °C change in temperature.
7. Data sheet value is the average magnitude of the change in offset voltage versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the change in magnitude per °C change in temperature.
8. Data sheet value is the average change in offset voltage versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the change in offset voltage per volt change of the input supply voltage.
9. Data sheet value is the average change in offset voltage versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the change in offset voltage per volt change of the output supply voltage.
10. Gain is defined as the slope of the best-fit line of differential output voltage (V_{OUT+} - V_{OUT-}) versus differential input voltage (V_{IN+} -V_{IN-}) over the specified input range.
11. Data sheet value is the average change in gain versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the percentage change in gain per °C change in temperature.
12. Data sheet value is the average magnitude of the change in gain versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the percentage change in magnitude per °C change in temperature.
13. Data sheet value is the average change in gain versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the percentage change in gain per volt change of the input supply voltage.
14. Data sheet value is the average change in gain versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the percentage change in gain per volt change of the output supply voltage.
15. Nonlinearity is defined as the maximum deviation of the output voltage from the best-fit gain line (see Note 10), expressed as a percentage of the full-scale differential output voltage range. For example, an input range of ± 200 mV generates a full-scale differential output range of 3.2 V (± 1.6 V); a maximum output deviation of 6.4 mV would therefore correspond to a nonlinearity of 0.2%.
16. Data sheet value is the average change in nonlinearity versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per °C change in temperature. For example, if the temperature is increased from 25°C to 35°C, the nonlinearity typically will decrease by 0.01 percentage points (10°C times -0.001 % pts/°C) from 0.2% to 0.19%.
17. Data sheet value is the average change in nonlinearity versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per volt change of the input supply voltage.
18. Data sheet value is the average change in nonlinearity versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per volt change of the output supply voltage.
19. NL_{100} is the nonlinearity specified over an input voltage range of ± 100 mV.
20. Because of the switched-capacitor nature of the input sigma-delta converter, time-averaged values are shown.
21. This parameter is defined as the ratio of the differential signal gain (signal applied differentially between pins 2 and 3) to the common-mode gain (input pins tied together and the signal applied to both inputs at the same time), expressed in dB.
22. When the differential input signal exceeds approximately 300 mV, the outputs will limit at the typical values shown.
23. The maximum specified input supply current occurs when the differential input voltage (V_{IN+} - V_{IN-}) = 0 V. The input supply current decreases approximately 1.3 mA per 1 V decrease in V_{DD1}.
24. The maximum specified output supply current occurs when the differential input voltage (V_{IN+} - V_{IN-}) = 200 mV, the maximum recommended operating input voltage. However, the output supply current will continue to rise for differential input voltages up to approximately 300 mV, beyond which the output supply current remains constant.

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25. Short circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground.
26. IMR (also known as CMR or Common Mode Rejection) specifies the minimum rate of rise of an isolation mode noise signal at which small output perturbations begin to appear. These output perturbations can occur with both the rising and falling edges of the isolation-mode wave form and may be of either polarity. When the perturbations first appear, they occur only occasionally and with relatively small peak amplitudes (typically 20-30 mV at the output of the recommended application circuit). As the magnitude of the isolation mode transients increase, the regularity and amplitude of the perturbations also increase. See applications section for more information.
27. IMRR is defined as the ratio of differential signal gain (signal applied differentially between pins 2 and 3) to the isolation mode gain (input pins tied to pin 4 and the signal applied between the input and the output of the isolation amplifier) at 60 Hz, expressed in dB.
28. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 200 kHz at room temperature), and is not attenuated by the internal output filter. A filter circuit can be easily added to the external post-amplifier to reduce the total rms output noise. The internal output filter does eliminate most, but not all, of the sigma-delta quantization noise. The magnitude of the output quantization noise is very small at lower frequencies (below 10 kHz) and increases with increasing frequency. See applications section for more information.
29. Data sheet value is the differential amplitude of the transient at the output of the HCPL-7800 when a 1 V_{pk-pk}, 1 MHz square wave with 5 ns rise and fall times is applied to both V_{DD1} and V_{DD2}.
30. This is a two-terminal measurement: pins 1-4 are shorted together and pins 5-8 are shorted together.
31. In accordance with UL1577, for devices with minimum V_{ISO} specified at 3750 V_{rms}, each optocoupler is proof-tested by applying an insulation test voltage greater-than-or-equal-to 4500 V_{rms} for one second (leak current detection limit, $I_{I-O} < 5$ µA). This test is performed before the method b, 100% production test for partial discharge shown in the VDE 0884 Insulation Characteristics Table.
32. Case temperature was measured with a thermocouple located in the center of the underside of the package.

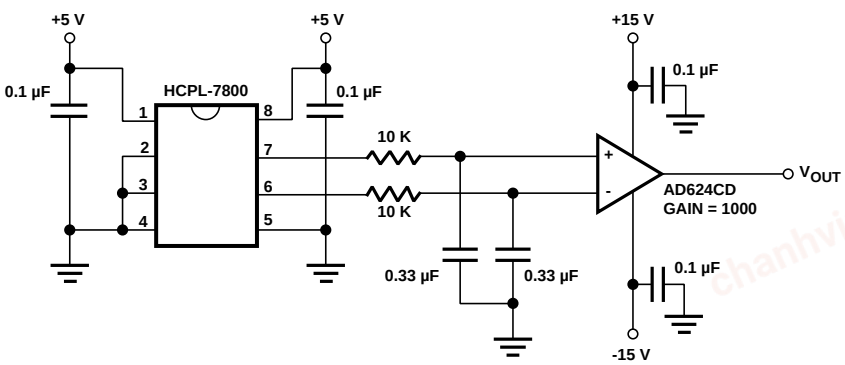


Figure 1. Input Offset Voltage Test Circuit.

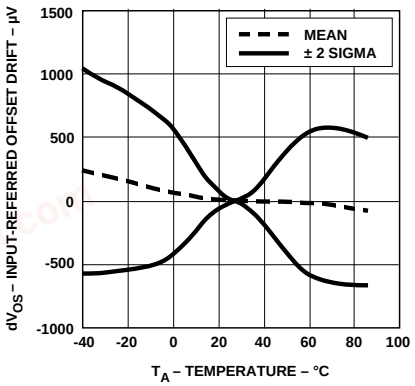


Figure 2. Input-Referred Offset Drift vs. Temperature.

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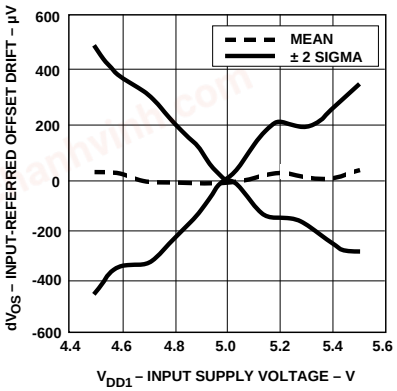


Figure 3. Input-Referred Offset Drift vs. V_{DD1} (V_{DD2} = 5 V).

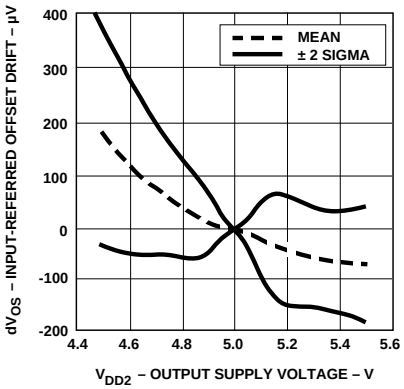


Figure 4. Input-Referred Offset Drift vs. V_{DD2} (V_{DD1} = 5 V).

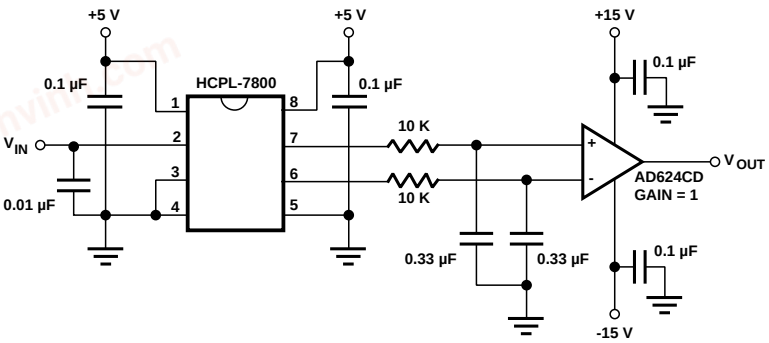


Figure 5. Gain and Nonlinearity Test Circuit.

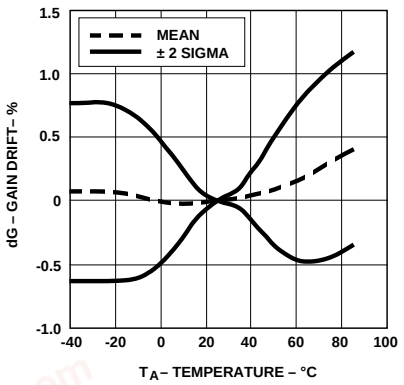


Figure 6. Gain Drift vs. Temperature.

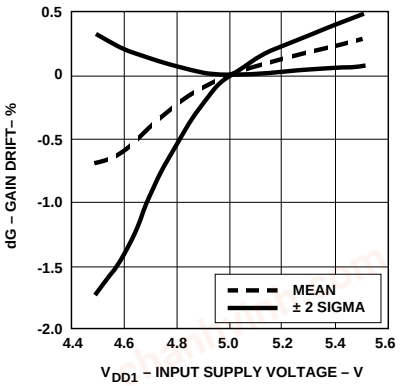


Figure 7. Gain Drift vs. V_{DD1} (V_{DD2} = 5 V).

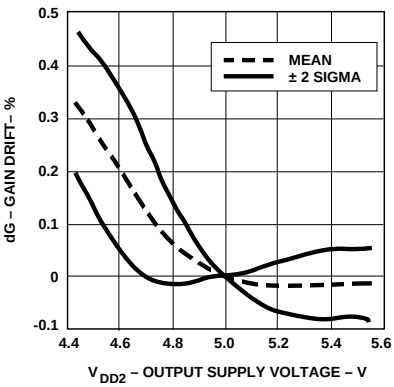


Figure 8. Gain Drift vs. V_{DD2} (V_{DD1} = 5 V).

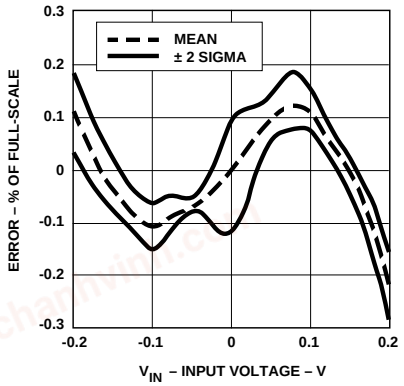


Figure 9. 200 mV Nonlinearity Error Plot.

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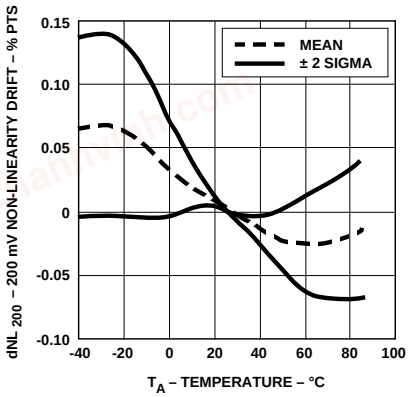


Figure 10. 200 mV Nonlinearity Drift vs. Temperature.

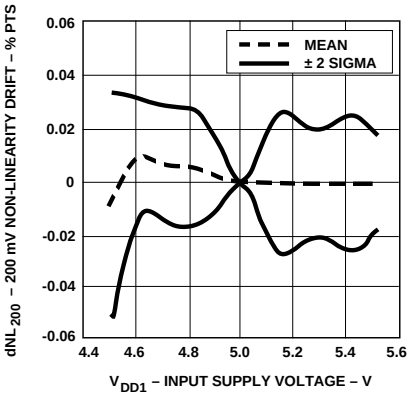


Figure 11. 200 mV Nonlinearity Drift vs. V_{DD1} (V_{DD2} = 5 V).

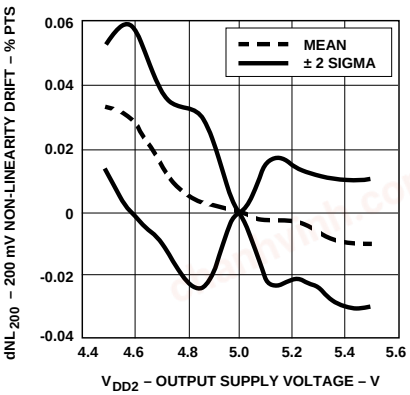


Figure 12. 200 mV Nonlinearity Drift vs. V_{DD2} (V_{DD1} = 5 V).

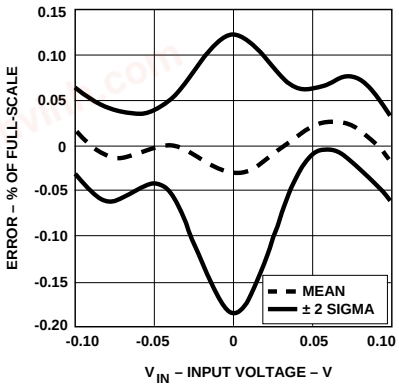


Figure 13. 100 mV Nonlinearity Error Plot.

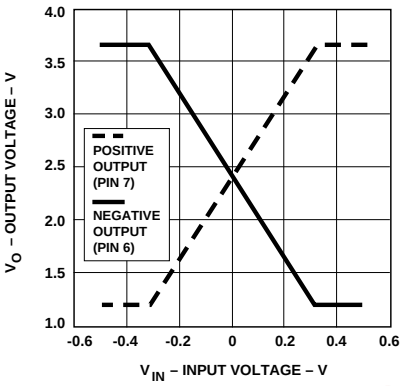


Figure 14. Typical Output Voltages vs. Input Voltage.

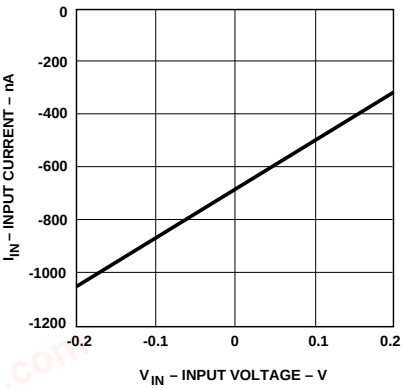


Figure 15. Typical Input Current vs. Input Voltage.

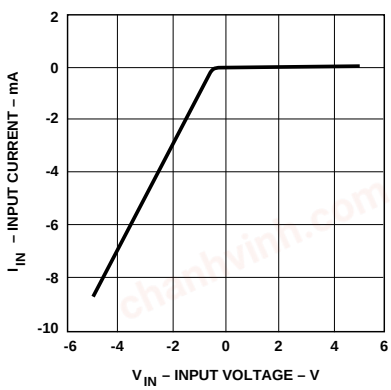


Figure 16. Typical Input Current vs. Input Voltage.

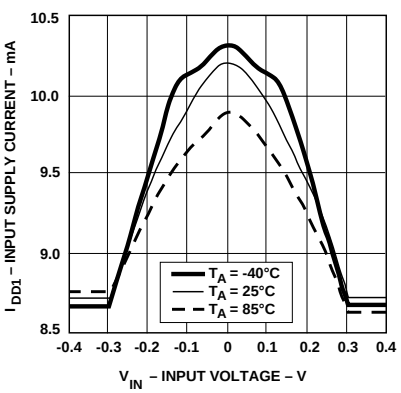


Figure 17. Typical Input Supply Current vs. Input Voltage.

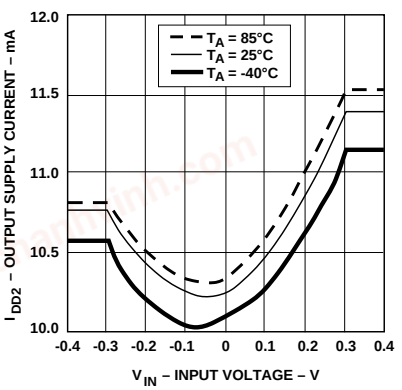


Figure 18. Typical Output Supply Current vs. Input Voltage.

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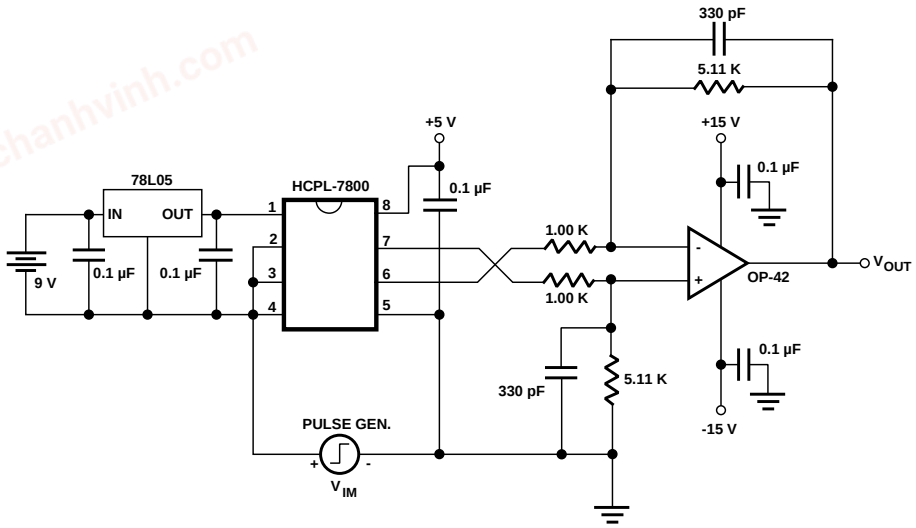


Figure 19. Isolation Mode Rejection Test Circuit.

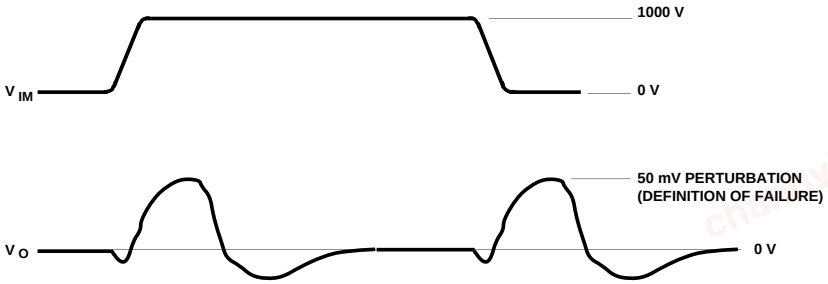


Figure 20. Typical IMR Failure Waveform.

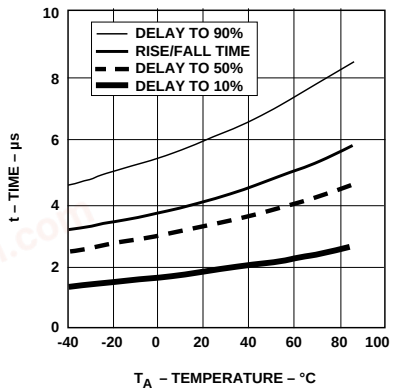


Figure 21. Typical Propagation Delays and Rise/Fall Time vs. Temperature.

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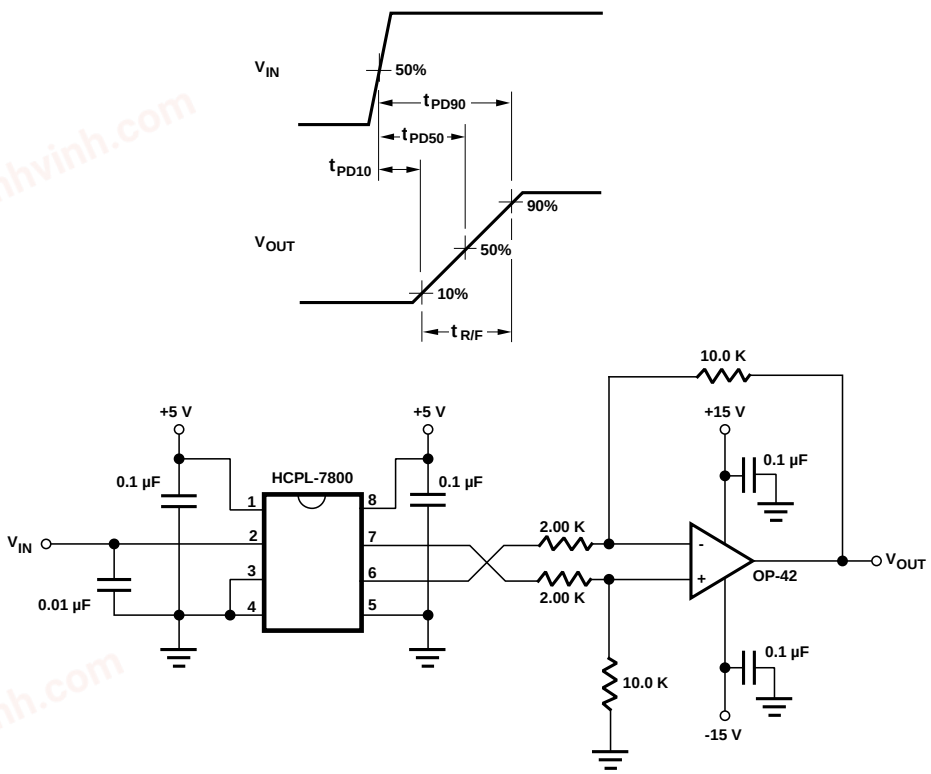


Figure 22. Propagation Delay and Rise/Fall Time Test Circuit.

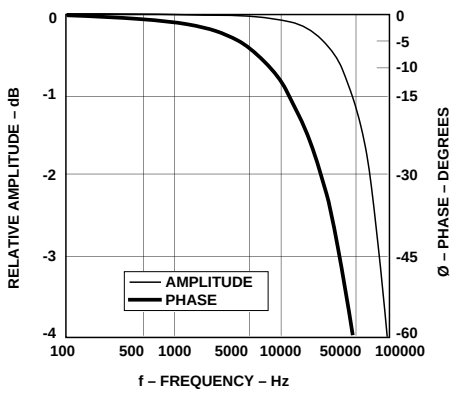


Figure 23. Typical Amplitude and Phase Response vs. Frequency.

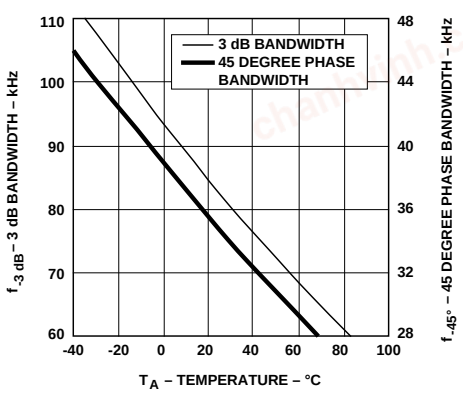


Figure 24. Typical 3 dB and 45° Bandwidths vs. Temperature.

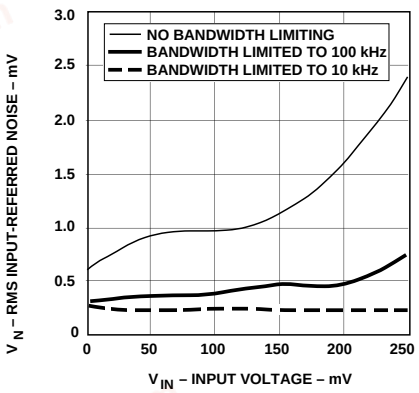


Figure 25. Typical RMS Input-Referred Noise vs. Input Voltage.

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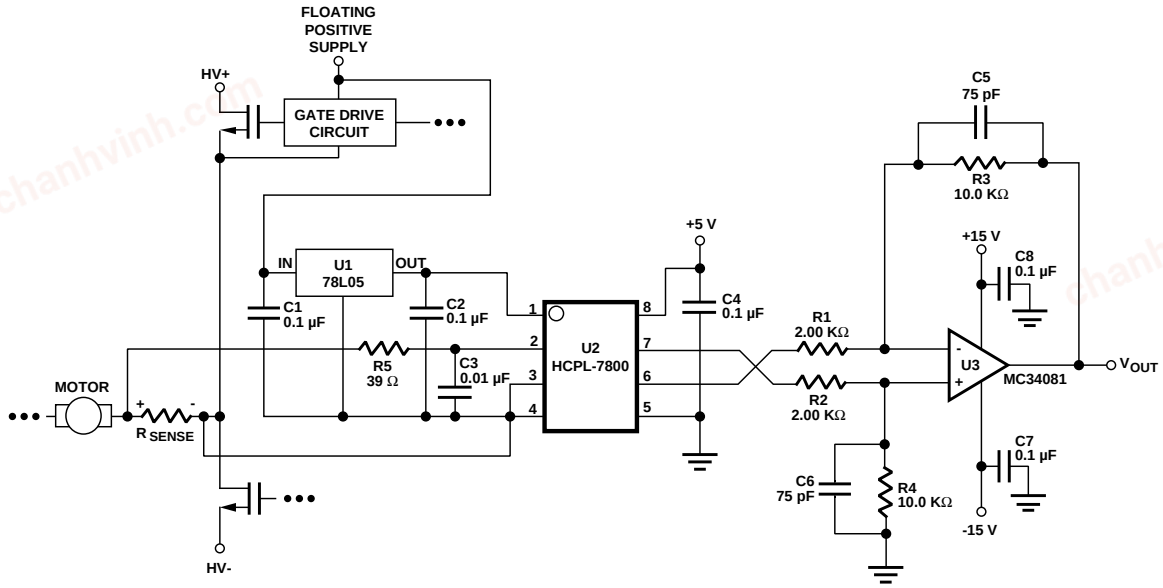


Figure 26. Recommended Application Circuit.

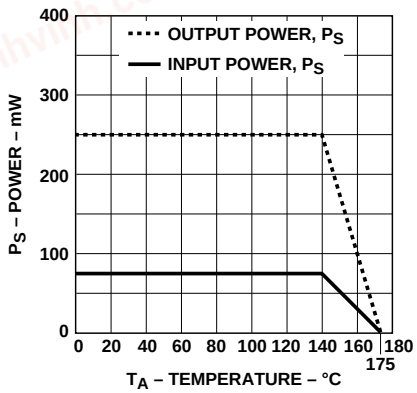


Figure 27. Dependence of Safety-Limiting Parameters on Ambient Temperature.

Applications Information

Functional Description

Figure 28 shows the primary functional blocks of the HCPL-7800. In operation, the sigma-delta analog-to-digital converter converts the analog input signal into a high-speed serial bit stream, the time average of which is directly proportional to the input signal. This high speed stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted into accurate analog voltage levels, which are then filtered to produce the final output signal.

To help maintain device accuracy over time and temperature, internal amplifiers are chopper-stabilized. Additionally, the encoder circuit eliminates the effects of pulse-width distortion of the optically transmitted data by generating one pulse for every edge (both rising and falling) of the converter data to be transmitted, essentially converting the *widths* of the sigma-delta output pulses into the *positions* of the encoder output pulses. A significant benefit of this coding scheme is that any non-ideal characteristics of the LED (such as non-linearity and drift over time and temperature) have little, if any, effect on the performance of the HCPL-7800.

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Circuit Information

The recommended application circuit is shown in Figure 26. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator. The input of the HCPL-7800 is connected directly to the current sensing resistor. The differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit. Although the application circuit is relatively simple, a few general recommendations should be followed to ensure optimal performance.

As shown in Figure 26, 0.1 µF bypass capacitors should be located as close as possible to the input and output power supply pins of the HCPL-7800. Notice that pin 2 (V_{IN+}) is bypassed with a 0.01 µF capacitor to reduce input offset voltage that can be caused by the combination of long input leads and the switched-capacitor nature of the input circuit.

With pin 3 (V_{IN-}) tied directly to pin 4 (GND1), the power-supply return line also functions as the sense line for the negative side of the current-sensing resistor; this allows a single twisted pair of wire to connect the isolation amplifier to the sense resistor. In some applications, however, better performance may be obtained by connecting pins 2 and 3 (V_{IN+} and V_{IN-}) directly across the sense resistor with twisted pair wire and using a separate wire for the power supply return line. Both input pins should be bypassed with 0.01 µF capacitors close to the isolation amplifier. In either case, it is recommended that twisted-pair wire be used to connect the isolation amplifier to the current-sensing resistor to minimize electro-magnetic interference of the sense signal.

To obtain optimal CMR performance, the layout of the printed circuit board (PCB) should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the PCB does not pass directly below the HCPL-7800. An example single-sided PCB layout for the recommended application circuit is shown in Figure 29. The trace pattern is shown in "X-ray" view as it would be seen from the top of the PCB; a mirror image of this layout can be used to generate a PCB.

An inexpensive 78L05 three-terminal regulator is shown in the recommended application circuit. Because the performance of the isolation amplifier can be affected by changes in the power supply voltages, using regulators with tighter output voltage tolerances will result in better overall circuit performance. Many different regulators that provide tighter output voltage tolerances than the 78L05 can be used, including: TL780-05 (Texas Instruments), LM340LAZ-5.0 and LP2950CZ-5.0 (National Semiconductor).

The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier. Many different op-amps could be used in the circuit, including: MC34082A (Motorola), TL032A, TLO52A, and TLC277 (Texas Instruments), LF412A (National Semiconductor).

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

The current-sensing resistor should have a relatively low value of resistance to minimize power dissipation, a fairly low inductance to accurately reflect high-frequency signal components, and a reasonably tight tolerance to maintain overall circuit accuracy. Although decreasing the value of the sense resistor decreases power dissipation, it also decreases the full-scale input voltage making iso-amp offset voltage effects more significant. These two

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conflicting considerations, therefore, must be weighed against each other in selecting an appropriate sense resistor for a particular application. To maintain circuit accuracy, it is recommended that the sense resistor and the isolation amplifier circuit be located as close as possible to one another. Although it is possible to buy current-sensing resistors from established vendors (e.g., the LVR-1, -3 and -5 resistors from Dale), it is also possible to make a sense resistor using a short piece of wire or even a trace on a PC board.

Figures 30 and 31 illustrate the response of the overall isolation amplifier circuit shown in Figure 26. Figure 30 shows the response of the circuit to a ± 200 mV 20 kHz sine wave input and Figure 31 the response of the circuit to a ± 200 mV 20 kHz square wave input. Both figures demonstrate the fast, well-behaved response of the HCPL-7800.

Figure 32 shows how quickly the isolation amplifier recovers from an overdrive condition generated by a 2 kHz square wave swinging between 0 and 500 mV (note that the time scale is different from the previous figures). The first wave form is the output of the application circuit with the filter capacitors removed to show the actual response of the isolation amplifier. The second wave form is the response of the same circuit with the capacitors installed. The recovery time and overshoot are relatively independent of the amplitude and polarity of the overdrive signal, as well as its duration.

For more information, refer to Application Note 1059.

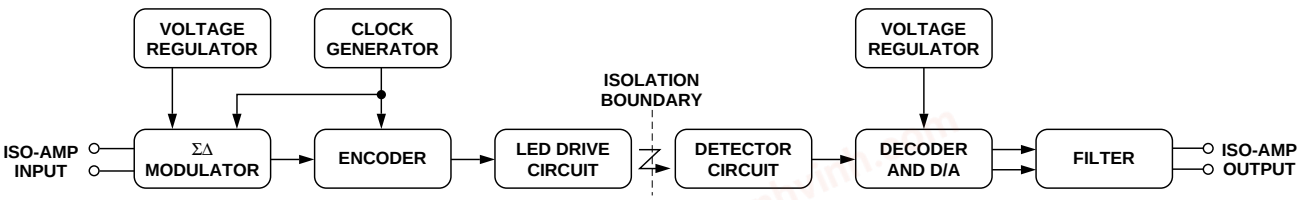


Figure 28. HCPL-7800 Block Diagram.

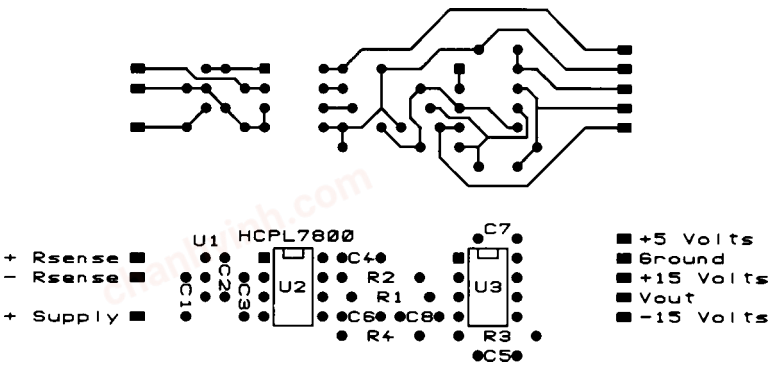


Figure 29. PC Board Trace Pattern and Loading Diagram Example.

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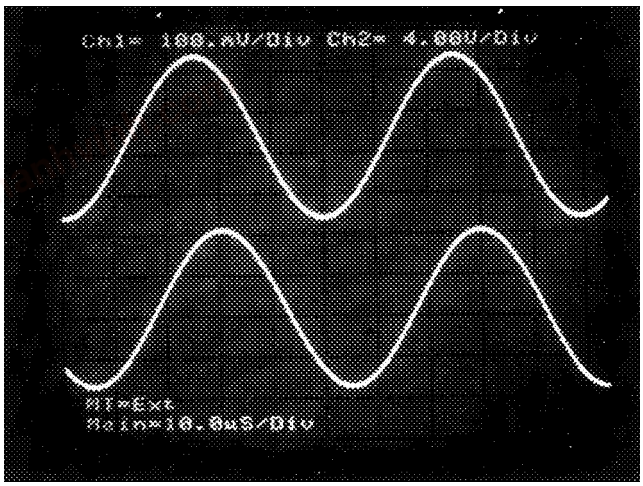


Figure 30. Application Circuit Sine Wave Response.

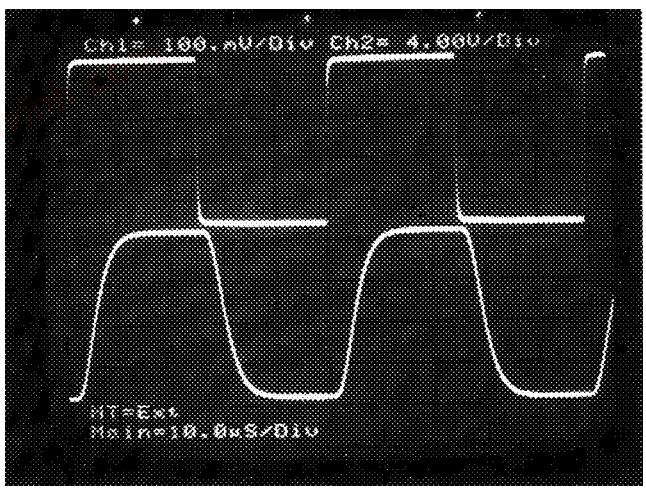


Figure 31. Application Circuit Square Wave Response.

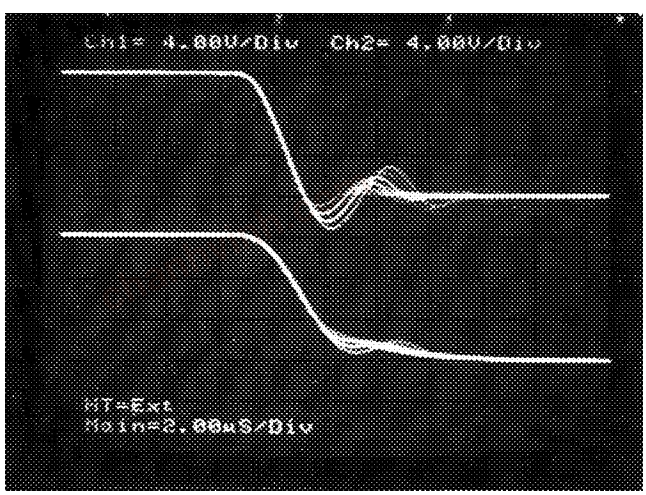


Figure 32. Application Circuit Overload Recovery Waveform.