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HCPL-7710/0710

40 ns Propagation Delay, CMOS Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

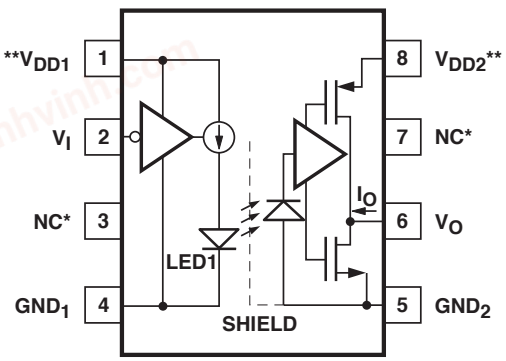
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

Available in either an 8-pin DIP or SO-8 package style respectively, the HCPL-7710 or HCPL-0710 optocouplers utilize the latest CMOS IC technology to achieve outstanding performance with very low power consumption. The HCPL-x710 require only two bypass capacitors for complete CMOS compatibility.

Basic building blocks of the HCPL-x710 are a CMOS LED driver IC, a high speed LED and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC, which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



* Pin 3 is the anode of the internal LED and must be left unconnected for guaranteed data sheet performance. Pin 7 is not connected internally.

** A 0.1 µF bypass capacitor must be connected between pins 1 and 4, and 5 and 8.

TRUTH TABLE (POSITIVE LOGIC)

V_I, INPUT	LED1	V_O, OUTPUT
H	OFF	H
L	ON	L

Features

- +5 V CMOS compatibility
- 8 ns maximum pulse width distortion
- 20 ns maximum prop. delay skew
- High speed: 12 Mbd
- 40 ns maximum prop. delay
- 10 kV/µs minimum common mode rejection
- -40°C to 100°C temperature range
- Safety and regulatory approvals
  UL Recognized
  3750 V_{rms} for 1 min. per UL 1577
  5000 V_{rms} for 1 min. per UL 1577 (for HCPL-7710 option 020)
  CSA Component Acceptance Notice #5
  IEC/EN/DIN EN 60747-5-5
  – V_{IORM} = 630 V_{peak} for HCPL-7710 Option 060
  – V_{IORM} = 567 V_{peak} for HCPL-0710 Option 060

Applications

- Digital fieldbus isolation: DeviceNet, SDS, Profibus
- AC plasma display panel level shifting
- Multiplexed data transmission
- Computer peripheral interface
- Microprocessor system interface

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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Selection Guide

8-Pin DIP (300 Mil)	Small Outline SO-8
HCPL-7710	HCPL-0710

Ordering Information

HCPL-0710 and HCPL-7710 are UL Recognized with 3750 V_{rms} for 1 minute per UL1577.

Part number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 V_{rms}/ 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Non RoHS Compliant							
HCPL-7710	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	-020					X		50 per tube
	-320E	-320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-0710	-000E	No option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
	-060E	#060		X				X	100 per tube
	-560E	#560		X		X		X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-7710-560E to order product of Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

HCPL-0710 to order product of Small Outline SO-8 package in tube packaging and non RoHS compliant.

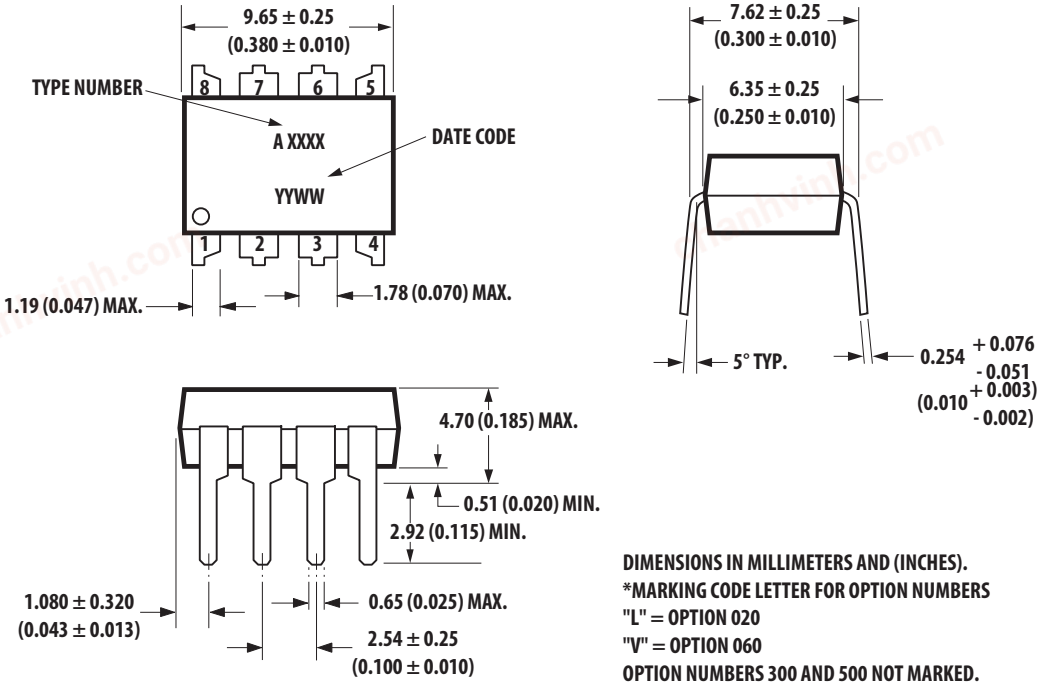
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

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Package Outline Drawing

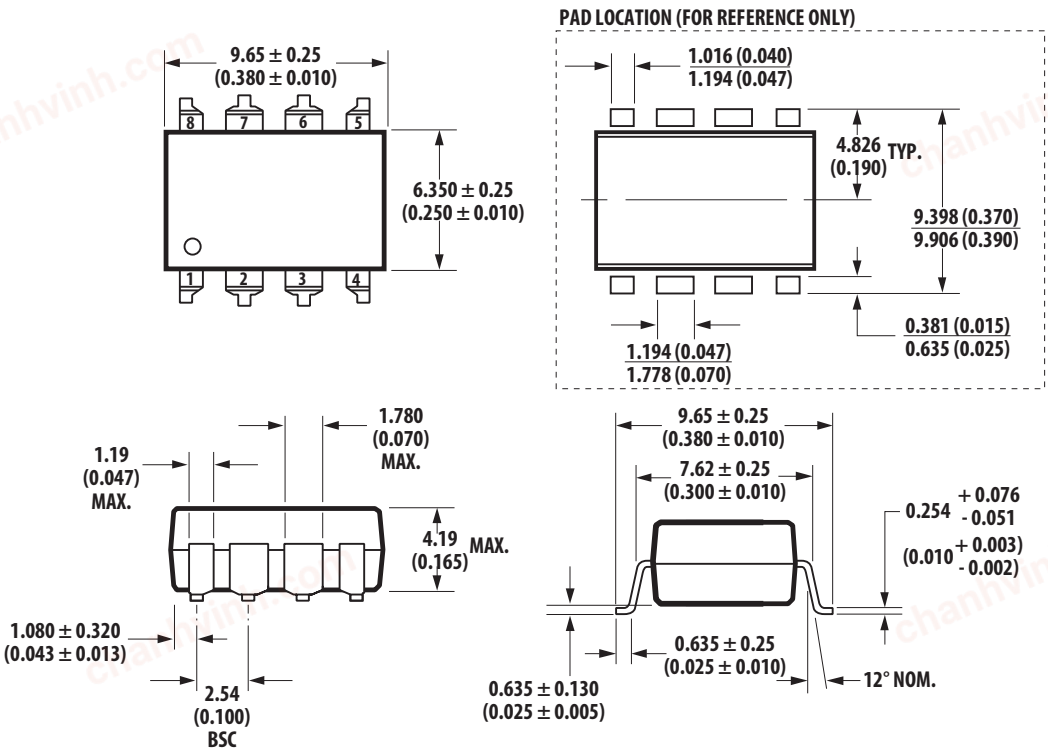
HCPL-7710 8-Pin DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

Package Outline Drawing

HCPL-7710 Package with Gull Wing Surface Mount Option 300

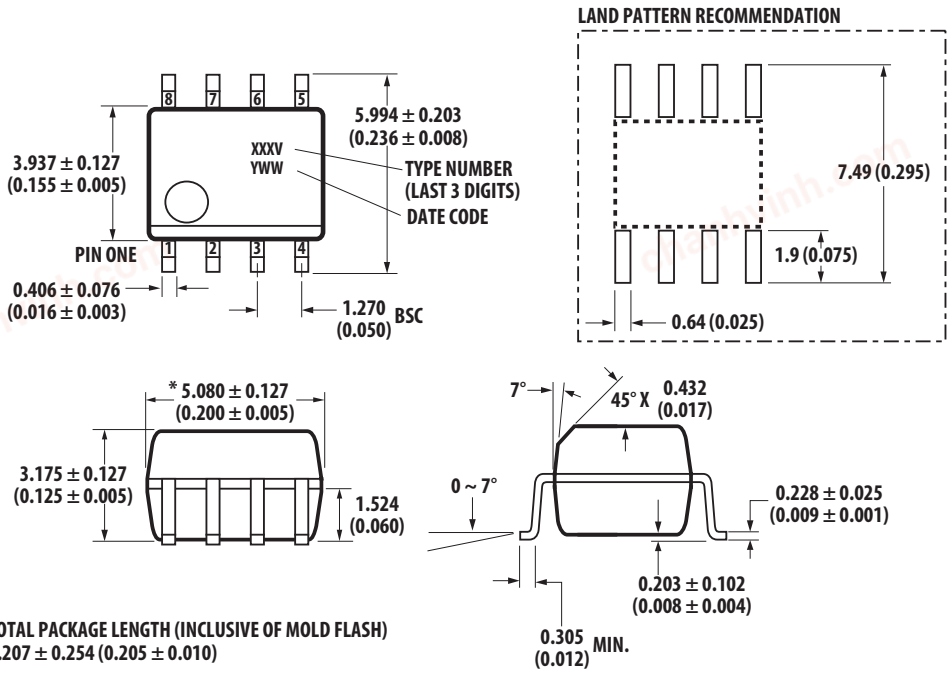


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

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Package Outline Drawing

HCPL-0710 Outline Drawing (Small Outline SO-8 Package)



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

OPTION NUMBER 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Solder Reflow Thermal Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The HCPL-x710 have been approved by the following organizations:

UL

Recognized under UL 1577, component recognition program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5

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Insulation and Safety Related Specifications

Parameter	Symbol	Value 7710	Value 0710	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	≥175	≥175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs, which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

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IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics* (Option 060)

Description	Symbol	Characteristic HCPL-7710	Characteristic HCPL-0710	Units
Installation classification per DIN VDE 0110, Table 1				
for rated mains voltage ≤ 150 V_{rms}		I-IV	I-IV	
for rated mains voltage ≤ 300 V_{rms}		I-IV	I-III	
for rated mains voltage ≤ 600 V_{rms}		I-IV	I-III	
Climatic Classification		55/85/21	55/85/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	567	V_{peak}
Input-to-Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	1063	V_{peak}
Input-to-Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1008	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	8000	6000	V_{peak}
Safety Limiting Values - maximum values allowed in the event of a failure				
Case Temperature	T_S	175	150	°C
Input Current	$I_{S,INPUT}$	230	150	mA
Output Power	$P_{S,OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{10} = 500 V	R_{IO}	$\geq 10^9$	$\geq 10^9$	Ω

* Refer to the front of the optocoupler section of the Isolation and Control Component Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Note: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Note: The surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	125	°C
Ambient Operating Temperature	T_A	–40	+100	°C
Supply Voltages	V_{DD1}, V_{DD2}	0	6.0	Volts
Input Voltage	V_I	–0.5	V_{DD1} +0.5	Volts
Output Voltage	V_O	–0.5	V_{DD2} +0.5	Volts
Input Current	I_I	–10	+10	mA
Average Output Current	I_O		10	mA
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane			
Solder Reflow Temperature Profile	See Solder Reflow Temperature Profile Section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+100	°C
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V
Logic High Input Voltage	V_{IH}	2.0	V_{DD1}	V
Logic Low Input Voltage	V_{IL}	0.0	0.8	V
Input Signal Rise and Fall Times	t_r, t_f		1.0	ms

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Electrical Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.
All typical specifications are at T_A = +25 °C, V_{DD1} = V_{DD2} = +5 V.

DC Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Logic Low Input Supply Current [1]	I_{DD1L}		6.0	10.0	mA	V_I = 0 V
Logic High Input Supply Current	I_{DD1H}		1.5	3.0	mA	$V_I = V_{DDI}$
Input Supply Current	I_{DD1}			13.0	mA	
Output Supply Current	I_{DD2}		5.5	11.0	mA	
Input Current	I_I	-10		10	µA	
Logic High Output Voltage	V_{OH}	4.4 4.0	5.0 4.8		V	I_O = -20 µA, $V_I = V_{IH}$ I_O = -4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0 0.5	0.1 1.0	V	I_O = -20 µA, $V_I = V_{IL}$ I_O = -4 mA, $V_I = V_{IL}$

Switching Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Time to Logic Low Output [2]	t_{PHL}		20	40	ns	C_L = 15 pF CMOS Signal Levels
Propagation Delay Time to Logic High Output	t_{PLH}		23	40	ns	C_L = 15 pF CMOS Signal Levels
Pulse Width [3]	PW	80			ns	C_L = 15 pF CMOS Signal Levels
Data Rate [3]				12.5	MBd	C_L = 15 pF CMOS Signal Levels
Pulse Width Distortion [4] $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		3	8	ns	C_L = 15 pF CMOS Signal Levels
Propagation Delay Skew [5]	t_{PSK}			20	ns	C_L = 15 pF
Output Rise Time (10 - 90%)	t_R		9		ns	C_L = 15 pF CMOS Signal Levels
Output Fall Time (90 - 10%)	t_F		8		ns	C_L = 15 pF CMOS Signal Levels
Common Mode Transient Immunity at Logic High Output [6]	$\lvert CM_H \rvert$	10	20		kV/µs	$V_I = V_{DD1}$, $V_O > 0.8\ V_{DD1}$, V_{CM} = 1000 V
Common Mode Transient Immunity at Logic Low Output [6]	$\lvert CM_L \rvert$	10	20		kV/µs	V_I = 0 V, V_O > 0.8 V, V_{CM} = 1000 V
Input Dynamic Power Dissipation Capacitance [7]	C_{PD1}		60		pF	
Output Dynamic Power Dissipation Capacitance [7]	C_{PD2}		10		pF	

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Package Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage [8, 9, 10]	0710	V_{ISO}	3750			Vrms	RH = 50%, t = 1 min., T_A = 25 °C
	7710		3750				
	Option 020		5000				
Resistance (Input-Output) [8]		R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V_{dc}
Capacitance (Input-Output) [8]		C_{I-O}		0.6		pF	f = 1 MHz
Input Capacitance [11]		C_I		3.0			
Input IC Junction-to-Case Thermal Resistance	-7710	θ_{jci}		145		°C/W	Thermocouple located at center underside of package
	-0710			160			
Output IC Junction-to-Case Thermal Resistance	-7710	θ_{jco}		140			
	-0710			135			
Package Power Dissipation		P_{PD}			150	mW	

Notes:

1. The LED is ON when V_I is low and OFF when V_I is high.
2. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.
3. Mimimum Pulse Width is the shortest pulse width at which 10% maximum, Pulse Width Distortion can be guaranteed. Maximum Data Rate is the inverse of Minimum Pulse Width. Operating the HCPL-x710 at data rates above 12.5 MBd is possible provided PWD and data dependent jitter increases and relaxed noise margins are tolerable within the application. For instance, if the maximum allowable variation of bit width is 30%, the maximum data rate becomes 37.5 MBd. Note: HCPL-x710 performances above 12.5 MBd are not guaranteed by Avago.
4. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD (percent pulse width distortion) is equal to the PWD divided by pulse width.
5. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
6. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\,V_{DD2}$. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O < 0.8\,V$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
7. Unloaded dynamic power dissipation is calculated as follows: $C_{PD} * V_{DD2} * f + I_{DD} * V_{DD}$, where f is switching frequency in MHz.
8. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
9. In accordance with UL1577, each HCPL-0710 is proof tested by applying an insulation test voltage ≥4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤5 μA). Each HCPL-7710 is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).
10. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
11. C_I is the capacitance measured at pin 2 (V_I).

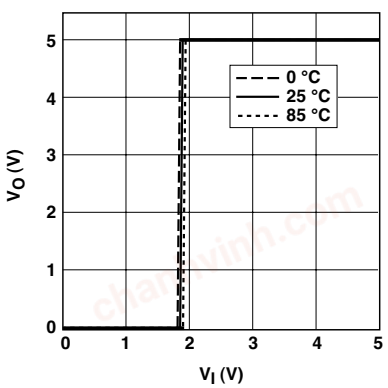


Figure 1. Typical output voltage vs. input voltage

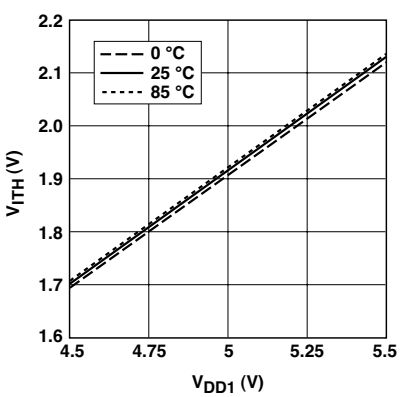


Figure 2. Typical input voltage switching threshold vs. input supply voltage

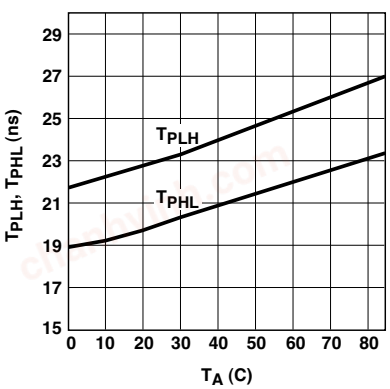


Figure 3. Typical propagation delays vs. temperature

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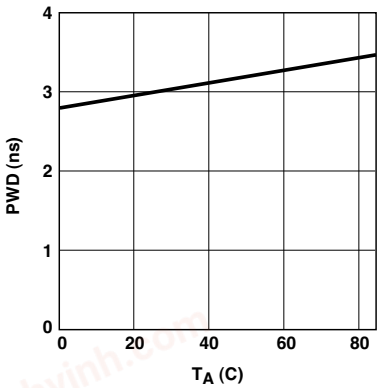


Figure 4. Typical pulse width distortion vs. temperature

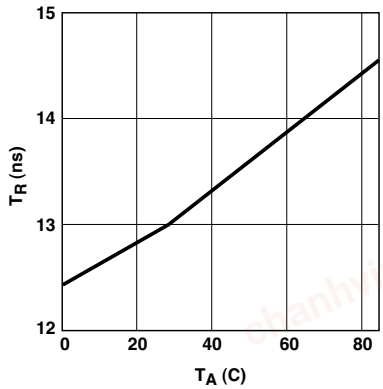


Figure 5. Typical rise time vs. temperature

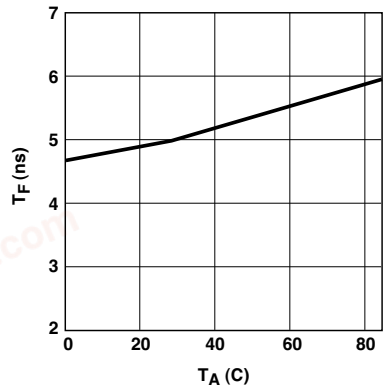


Figure 6. Typical fall time vs. temperature

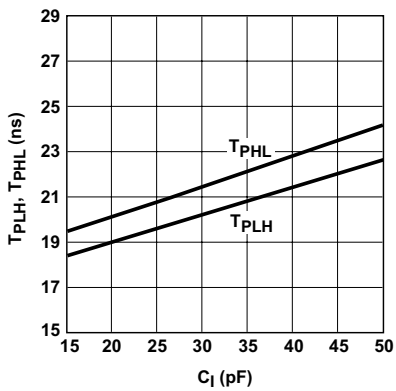


Figure 7. Typical propagation delays vs. output load capacitance

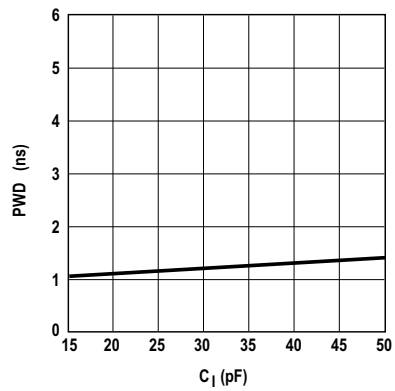


Figure 8. Typical pulse width distortion vs. output load capacitance

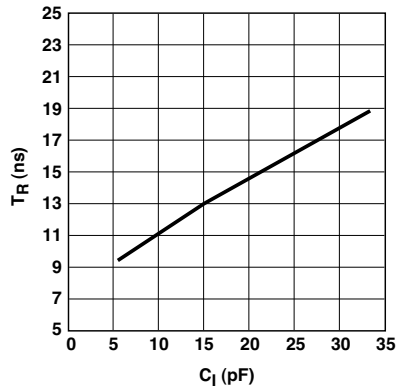


Figure 9. Typical rise time vs. load capacitance

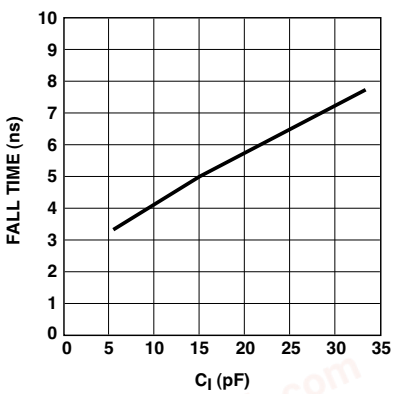
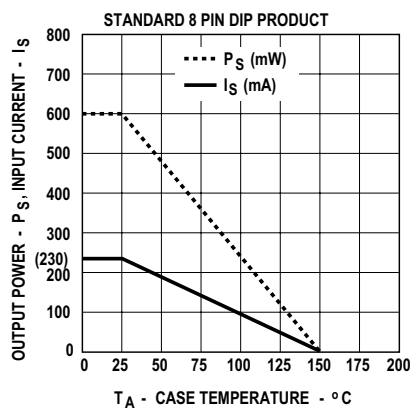


Figure 10. Typical fall time vs. load capacitance



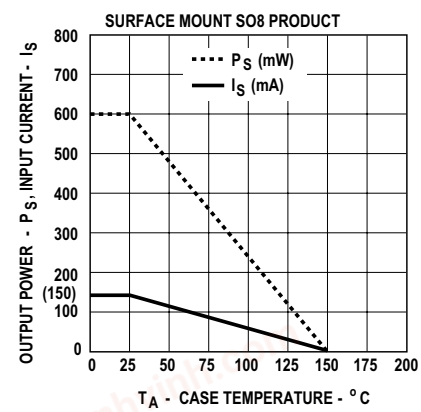


Figure 11. Thermal derating curve, dependence of Safety Limiting Value with case temperature per IEC/EN/DIN EN 60747-5-5

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Application Information

Bypassing and PC Board Layout

The HCPL-x710 optocouplers are extremely easy to use. No external interface circuitry is required because the HCPL-x710 use high-speed CMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in Figure 12, the only external components required for proper operation are two bypass capacitors. Capacitor values should be between 0.01 µF and 0.1 µF. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 13 illustrates the recommended printed circuit board layout for the HPCL-x710.

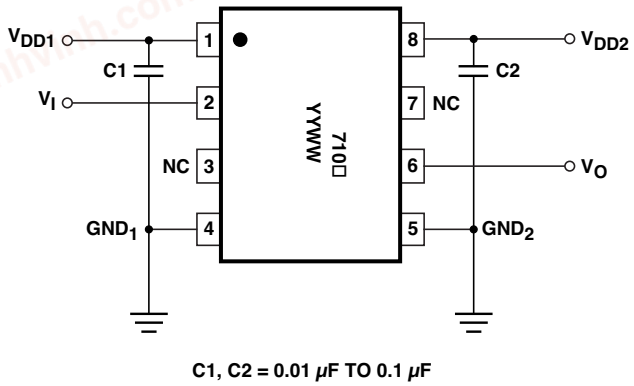


Figure 12. Recommended Printed Circuit Board layout.

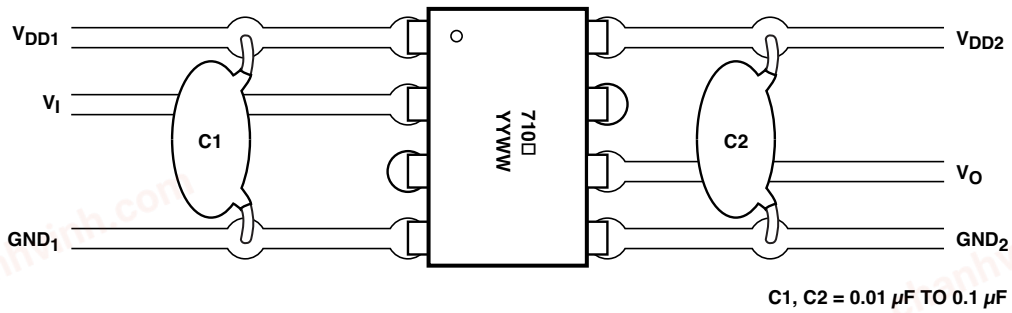


Figure 13. Recommended Printed Circuit Board layout.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation Delay is a figure of merit that describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low. See Figure 14.

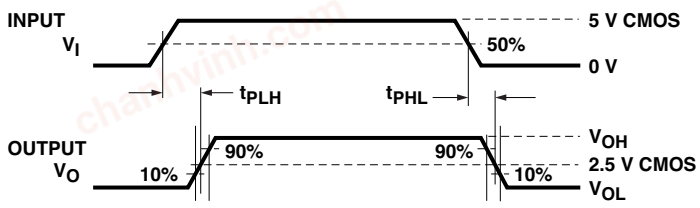


Figure 14.

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Pulse-width distortion (PWD) is the difference between t_{PHL} and t_{PLH} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20 - 30% of the minimum pulse width is tolerable. The PWD specification for the HCPL-x710 is 8 ns (10%) maximum across recommended operating conditions. 10% maximum is dictated by the most stringent of the three fieldbus standards, PROFIBUS.

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delay is large enough it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers that are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 15, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 16 is the timing diagram of a typical parallel data application with both the clock and data lines being sent through the optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. In this case, the data is assumed to be clocked off of the rising edge of the clock.

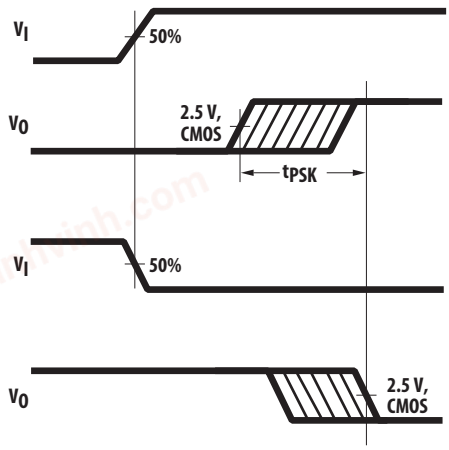


Figure 15. Propagation delay skew waveform

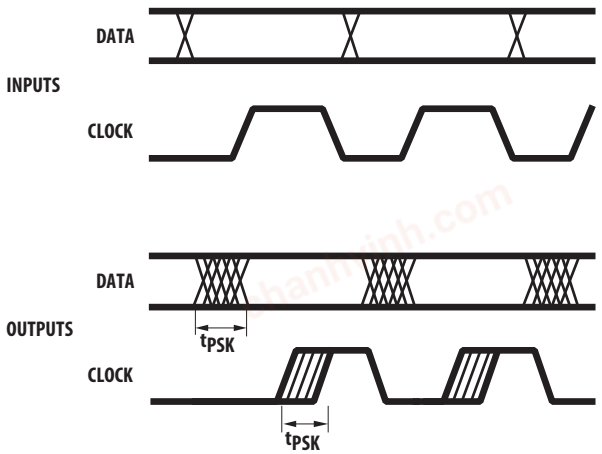


Figure 16. Parallel data transmission example

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 16 shows that there will be uncertainty in both the data and clock lines. These two areas of uncertainty must not overlap; otherwise, the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-x710 optocouplers offer the advantage of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature, and power supply ranges.

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Digital Field Bus Communication Networks

To date, despite its many drawbacks, the 4 - 20 mA analog current loop has been the most widely accepted standard for implementing process control systems. In today's manufacturing environment, however, automated systems are expected to help manage the process, not merely monitor it. With the advent of digital field bus communication networks such as DeviceNet, PROFIBUS, and Smart Distributed Systems (SDS), gone are the days of constrained information. Controllers can now receive multiple readings from field devices (sensors, actuators, etc.) in addition to diagnostic information.

The physical model for each of these digital field bus communication networks is very similar as shown in Figure 17. Each includes one or more buses, an interface unit, optical isolation, transceiver, and sensing and/or actuating devices.

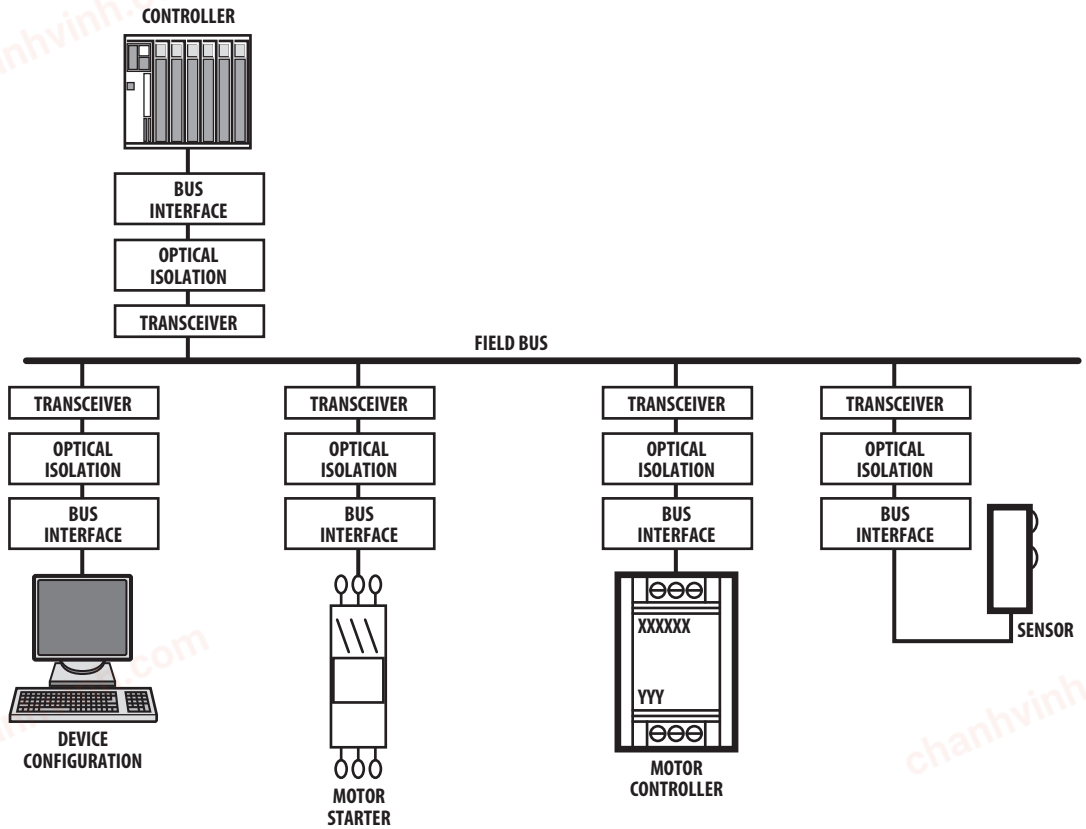


Figure 17. Typical field bus communication physical model

Optical Isolation for Field Bus Networks

To recognize the full benefits of these networks, Avago optocouplers are recommended to provide galvanic isolation. As network communication is bi-directional (involving receiving data from and transmitting data onto the network), two Avago optocouplers are needed. By providing galvanic isolation, data integrity is retained via noise reduction and the elimination of false signals. In addition, the network receives maximum protection from power system faults and ground loops.

Within an **isolated node**, such as the DeviceNet Node shown in Figure 18, *some* of the node's components are referenced to a ground other than V- of the network. These components could include such things as devices with serial ports, parallel ports, RS-232 and RS-485 type ports. As shown in Figure 18, power from the network is used only for the transceiver and input (network) side of the optocouplers.

Isolation of nodes connected to any of the three types of digital field bus networks is best achieved by using the HCPL-x710 optocouplers. For each network, the HCPL-x710 satisify the critical propagation delay and pulse width distortion requirements over the temperature range of 0 °C to +85 °C, and power supply voltage range of 4.5 V to 5.5 V.

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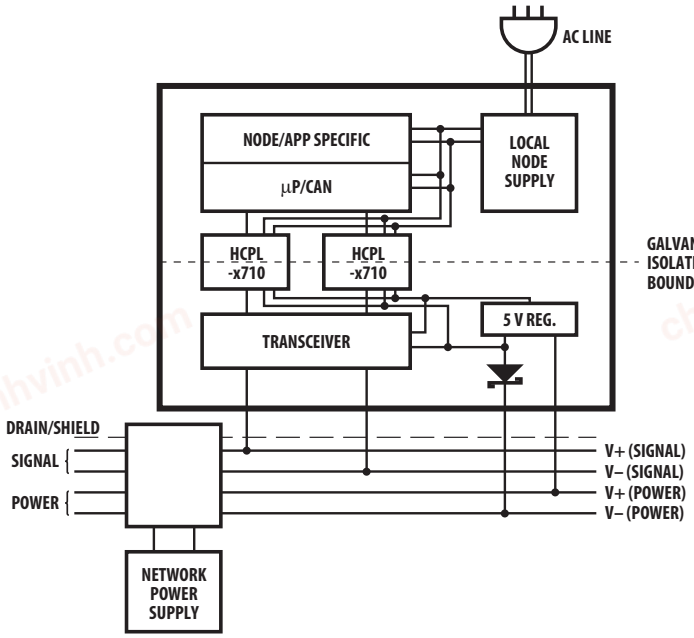


Figure 18. Typical DeviceNet node.

Implementing DeviceNet and SDS with the HCPL-x710

With transmission rates up to 1 Mbit/s, both DeviceNet and SDS are based upon the same broadcast-oriented, communications protocol — the Controller Area Network (CAN). Three types of isolated nodes are recommended for use on these networks: Isolated Node Powered by the Network (Figure 19), Isolated Node with Transceiver Powered by the Network (Figure 20), and Isolated Node Providing Power to the Network (Figure 21).

Isolated Node Powered by the Network

This type of node is very flexible and as can be seen in Figure 19, is regarded as "isolated" because not all of its components have the same ground reference. Yet, all components are still powered by the network. This node contains two regulators: one is isolated and powers the CAN controller, node-specific application and isolated (node) side of the two optocouplers while the other is non-isolated. The non-isolated regulator supplies the transceiver and the non-isolated (network) half of the two optocouplers.

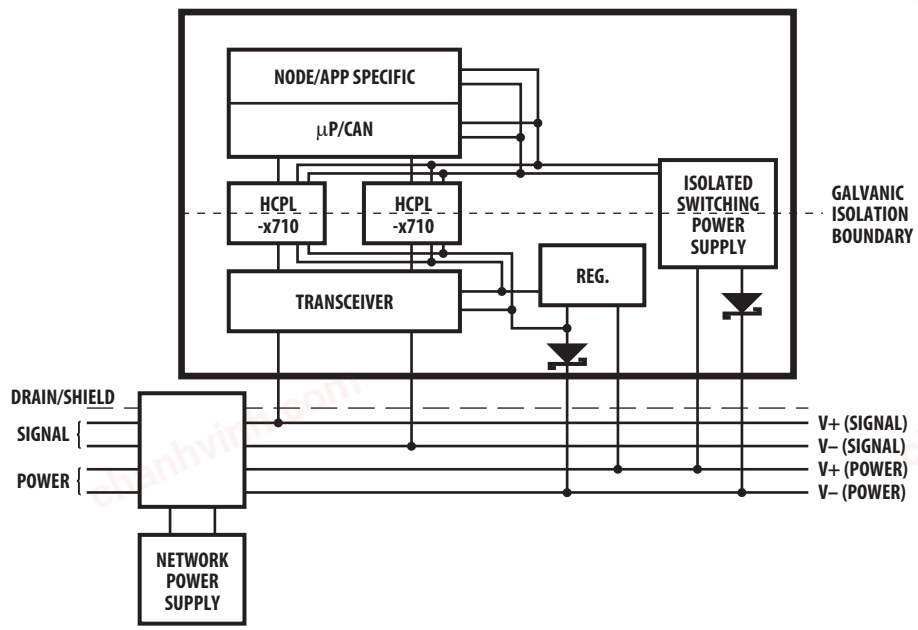


Figure 19. Isolated node powered by the network

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Isolated Node with Transceiver Powered by the Network

Figure 20 shows a node powered by both the network and another source. In this case, the transceiver and isolated (network) side of the two optocouplers are powered by the network. The rest of the node is powered by the AC line which is very beneficial when an application requires a significant amount of power. This method is also desirable as it does not heavily load the network.

More importantly, the unique "dual-inverting" design of the HCPL-x710 ensure the network will not "lock-up" if either AC line power to the node is lost or the node powered-off. Specifically, when input power (V_{DD1}) to the HCPL-x710 located in the transmit path is eliminated, a RECESSIVE bus state is ensured as the HCPL-x710 output voltage (V_O) go HIGH.

*Bus V+ Sensing

It is suggested that the Bus V+ sense block shown in Figure 20 be implemented. A locally powered node with an un-powered isolated Physical Layer will accumulate errors and become bus-off if it attempts to transmit. The Bus V+ sense signal would be used to change the BOI attribute of the DeviceNet Object to the "auto-reset" (01) value. Refer to Volume 1, Section 5.5.3. This would cause the node to continually reset until bus power was detected. Once power was detected, the BOI attribute would be returned to the "hold in bus-off" (00) value. The BOI attribute should not be left in the "auto-reset" (01) value since this defeats the jabber protection capability of the CAN error confinement. Any inexpensive low frequency optical isolator can be used to implement this feature.

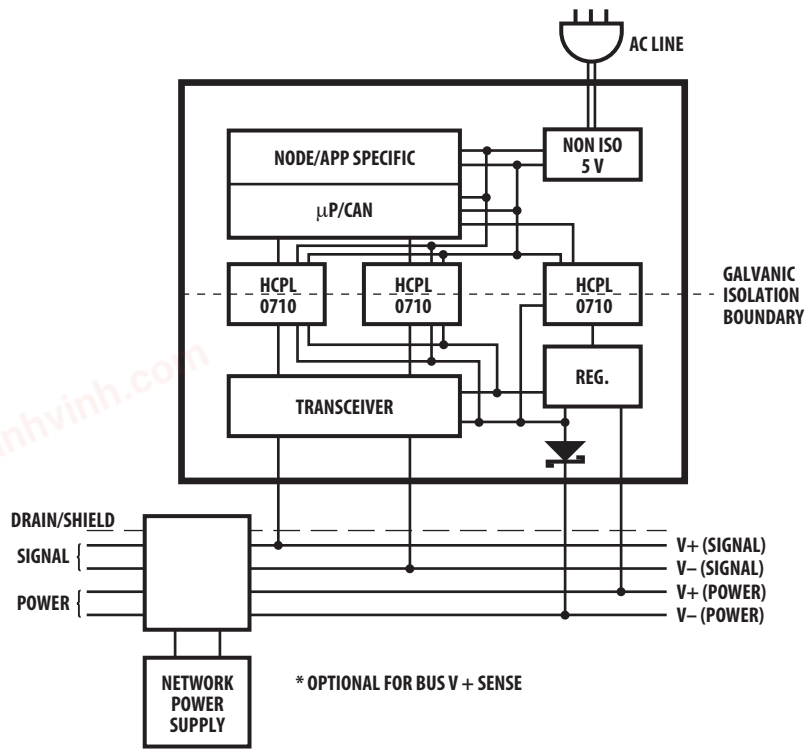


Figure 20. Isolated node with transceiver powered by the network

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Isolated Node Providing Power to the Network

Figure 21 shows a node providing power to the network. The AC line powers a regulator which provides 5 V locally. The AC line also powers a 24 V isolated supply, which powers the network, and another 5 V regulator, which, in turn, powers the transceiver and isolated (network) side of the two optocouplers. This method is recommended when there are a limited number of devices on the network that do not require much power, thus eliminating the need for separate power supplies.

More importantly, the unique "dual-inverting" design of the HCPL-x710 ensure the network will not "lock-up" if either AC line power to the node is lost or the node powered-off. Specifically, when input power (V_{DD1}) to the HCPL-x710 located in the transmit path is eliminated, a RECESSIVE bus state is ensured as the HCPL-x710 output voltage (V_O) go HIGH.

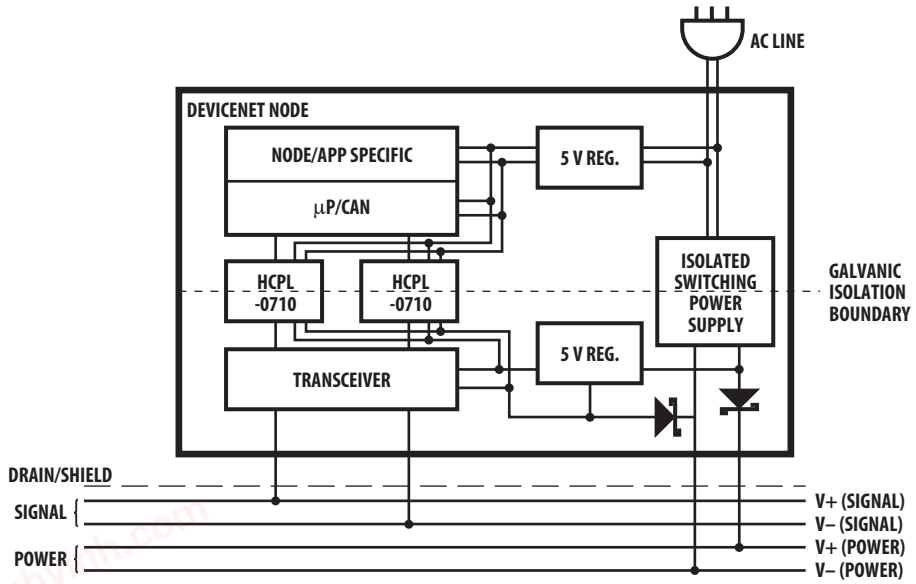


Figure 21. Isolated node providing power to the network

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Power Supplies and Bypassing

The recommended DeviceNet application circuit is shown in Figure 22. As the HCPL-x710 are fully compatible with CMOS logic level signals, the optocoupler is connected directly to the CAN transceiver. Two bypass capacitors (with values between 0.01 and 0.1 µF) are required and should be located as close as possible to the input and output power-supply pins of the HCPL-x710. For each capacitor, the total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm. The bypass capacitors are required because of the high-speed digital nature of the signals inside the optocoupler.

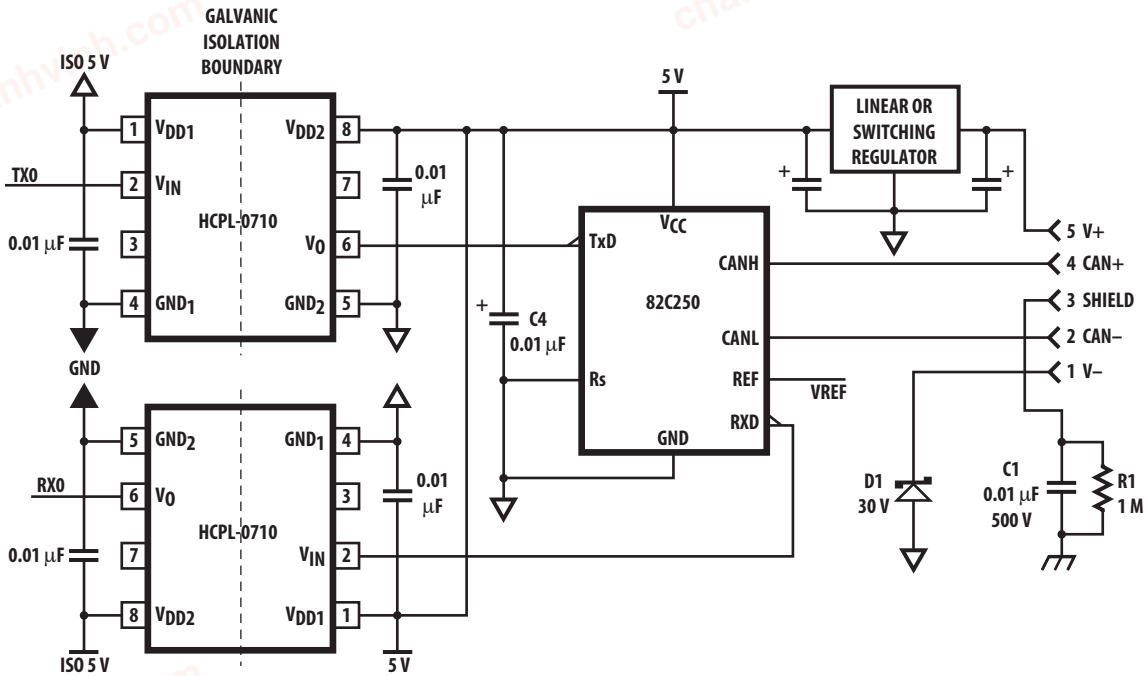


Figure 22. Recommended DeviceNet application circuit

Implementing PROFIBUS with the HCPL-x710

An acronym for Process Fieldbus, PROFIBUS is essentially a twisted-pair serial link very similar to RS-485 capable of achieving high-speed communication up to 12 MBd. As shown in Figure 23, a PROFIBUS Controller (PBC) establishes the connection of a field automation unit (control or central processing station) or a field device to the transmission medium. The PBC consists of the line transceiver, optical isolation, frame character transmitter/receiver (UART), and the FDL/APP processor with the interface to the PROFIBUS user.

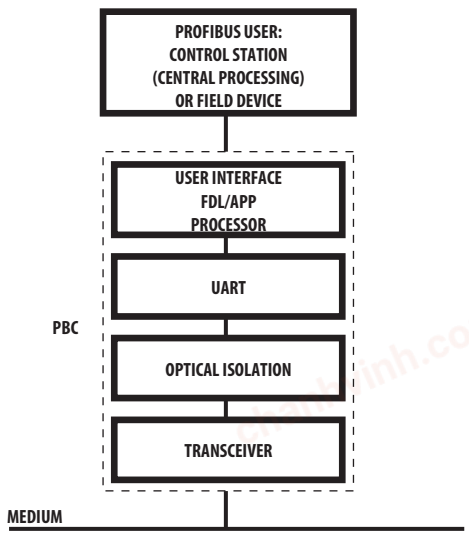


Figure 23. PROFIBUS Controller (PBC)

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Power Supplies and Bypassing

The recommended PROFIBUS application circuit is shown in Figure 24. Since the HCPL-x710 are fully compatible with CMOS logic level signals, the optocoupler is connected directly to the transceiver. Two bypass capacitors (with values between 0.01 and 0.1 µF) are required and should be located as close as possible to the input and output power-supply pins of the HCPL-x710. For each capacitor, the total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm. The bypass capacitors are required because of the high-speed digital nature of the signals inside the optocoupler.

Being very similar to multi-station RS485 systems, the HCPL-061N optocoupler provides a transmit disable function that is necessary to make the bus free after each master/slave transmission cycle. Specifically, the HCPL-061N disables the transmitter of the line driver by putting it into a high state mode. In addition, the HCPL-061N switches the RX/TX driver IC into the listen mode. The HCPL-061N offers HCMOS compatibility and the high CMR performance (1 kV/µs at V_{CM} = 1000 V) essential in industrial communication interfaces.

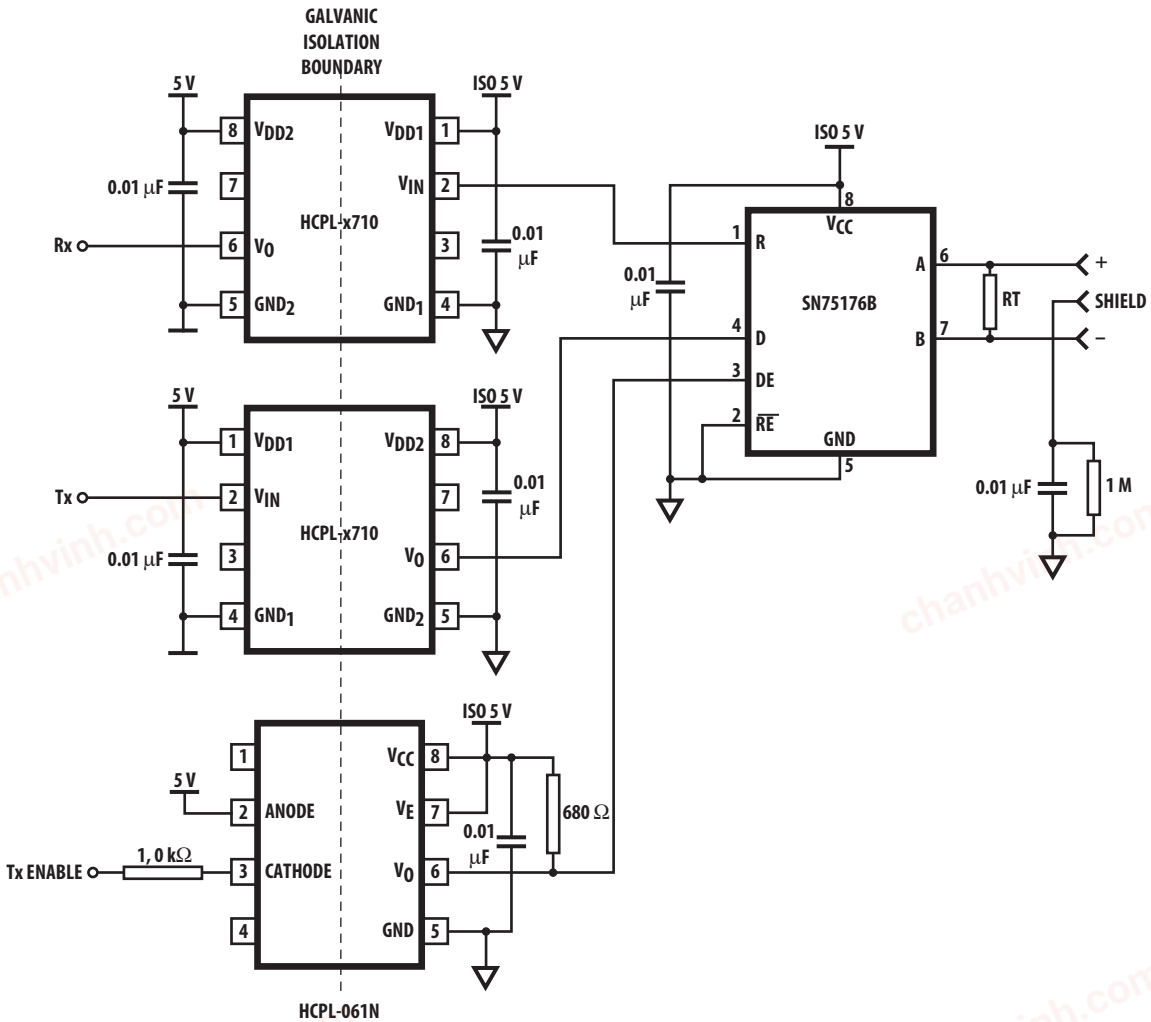


Figure 24. Recommended PROFIBUS application circuit

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