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6N137, HCNW137, HCNW2601, HCNW2611, HCPL-0600, HCPL-0601, HCPL-0611, HCPL-0630, HCPL-0631, HCPL-0661, HCPL-2601, HCPL-2611, HCPL-2630, HCPL-2631, HCPL-4661

High CMR, High Speed TTL Compatible Optocouplers

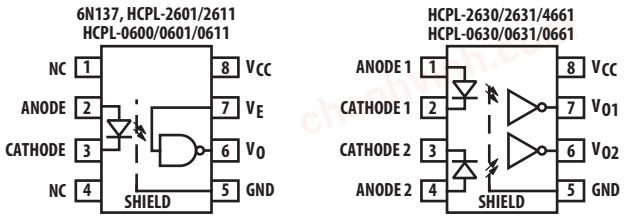
Data Sheet

Description

The 6N137, HCPL-26xx/06xx/4661, HCNW137/26x1 are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification up to 15,000 V/µs at Vcm = 1000 V.

This unique design provides maximum AC and DC circuit isolation while achieving TTL compatibility. The optocoupler AC and DC operational parameters are guaranteed from –40 °C to +85 °C allowing troublefree system performance.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Features

- 15 kV/µs minimum Common Mode Rejection (CMR) at VCM= 1 kV for HCNW2611, HCPL-2611, HCPL-4661, HCPL-0611, HCPL-0661
- High speed: 10 MBd typical
- LSTTL/TTL compatible
- Low input current capability: 5 mA
- Guaranteed AC and DC performance over temperature: –40 °C to +85 °C
- Available in 8-Pin DIP, SOIC-8, widebody packages
- Strobable output (single channel products only)
- Safety approval
  - UL recognized - 3750 V_{rms} for 1 minute and 5000 V_{rms} for 1 minute per UL1577 CSA approved (5000 V_{rms}/1 Minute rating is for HCNW137/26X1 and Option 020 [6N137, HCPL-2601/11/30/31, HCPL-4661] products only)
  - IEC/EN/DIN EN 60747-5-5 approved with
    - V_{IORM}= 567 V_{peak} for 06xx Option 060
    - V_{IORM}= 630 V_{peak} for 6N137/26xx Option 060
    - V_{IORM}=1414 V_{peak} for HCNW137/26x1
- MIL-PRF-38534 hermetic version available (HCPL-56xx/66xx)

Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Power transistor isolation in motor drives
- Isolation of high speed logic systems

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The 6N137, HCPL-26xx, HCPL-06xx, HCPL-4661, HCNW137, and HCNW26x1 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Selection Guide

Minimum CMR		Input On-Current (mA)	Output Enable	8-Pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/µs)	V_{CM} (V)			Single Channel Package	Dual Channel Package	Single Channel Package	Dual Channel Package	Single Channel Package	Single and Dual Channel Packages
1000	10	5	YES	6N137					
5,000	1,000	5	YES			HCPL-0600		HCNW137	
			NO		HCPL-2630		HCPL-0630		
10,000	1,000		YES	HCPL-2601		HCPL-0601		HCNW2601	
			NO		HCPL-2631		HCPL-0631		
15,000	1,000		YES	HCPL-2611		HCPL-0611		HCNW2611	
			NO		HCPL-4661		HCPL-0661		
1,000	50		YES	HCPL-2602[a]					
3, 500	300		YES	HCPL-2612[a]					
1,000	50	3	YES	HCPL-261A[a]		HCPL-061A[a]			
			NO		HCPL-263A[a]		HCPL-063A[a]		
1,000[b]	1,000		YES	HCPL-261N[a]		HCPL-061N[a]			
			NO		HCPL-263N[a]		HCPL-063N[a]		
1,000	50	12.5	[c]						HCPL-193x[a] HCPL-56xx[a] HCPL-66xx[a]

a. Technical data are on separate Avago publications.

b. 15 kV/µs with V_{CM} = 1 kV can be achieved using Avago application circuit.3

c. Enable is available for single channel products only, except for HCPL-193x devices.

Ordering Information

HCPL-xxxx is UL Recognized with 3750 V_{rms} for 1 minute per UL1577.

HCNWxxxx is UL Recognized with 5000 V_{rms} for 1 minute per UL1577.

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Table 1 Ordering Information

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/ 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Non RoHS Compliant							
6N137	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-560E	-560		X	X	X		X	1000 per reel
HCPL-2601	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	-		X	X			X	50 per tube
HCPL-2611	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-2630	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
HCPL-2631 HCPL-4661	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel

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Table 1 Ordering Information (Continued)

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/ 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Non RoHS Compliant							
HCPL-0600 HCPL-0601 HCPL-0611	-000E	No option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
	-060E	#060		X				X	100 per tube
	-560E	#560		X		X		X	1500 per reel
HCPL-0630 HCPL-0631 HCPL-0661	-000E	No option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
HCNW137 HCNW2601 HCNW2611	-000E	No option	400 mil DIP-8				X	X	42 per tube
	-300E	#300		X	X		X	X	42 per tube
	-500E	#500		X	X	X	X	X	750 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry. Combinations of Option 020 and Option 060 are not available.

Example 1:

HCPL-2611-560E to order product of 300-mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

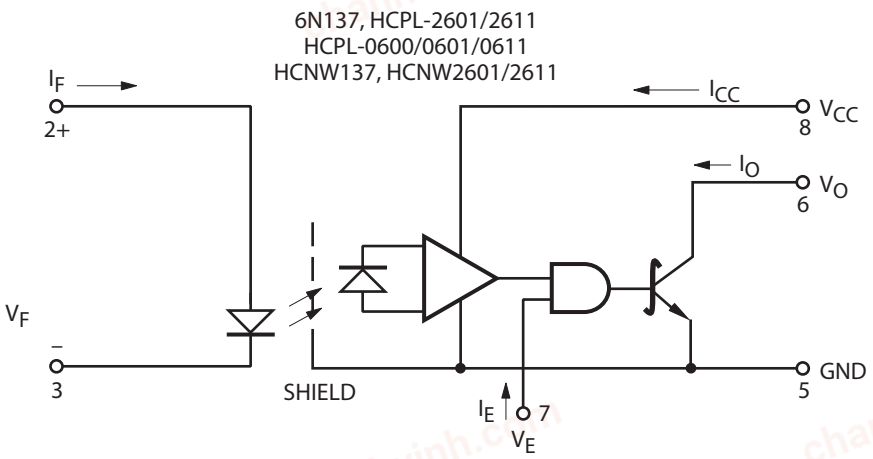
Example 2:

HCPL-2630 to order product of 300-mil DIP package in tube packaging and non RoHS compliant.

Option data sheets are available. Contact your Avago sales representative or authorized distributor for information.

NOTE The notation '#xxx' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant option will use '-xxxE'.

Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 5).

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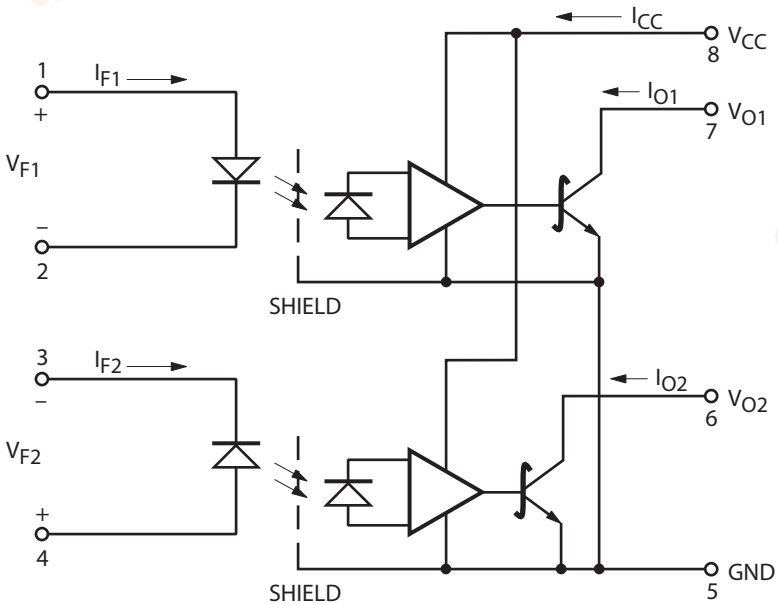
HCPL-2630/2631/4661
HCPL-0630/0631/0661



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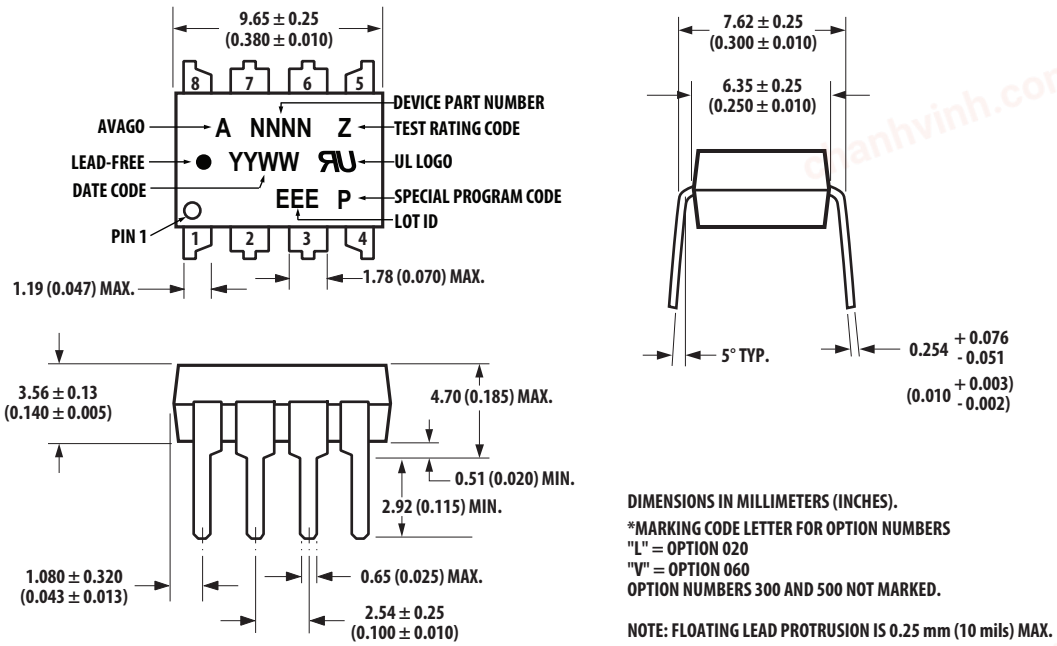
Package Outline Drawings

8-pin DIP Package[1] (6N137, HCPL-2601/11/30/31, HCPL-4661)



DIMENSIONS IN MILLIMETERS (INCHES).

*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

1. JEDEC Registered Data (for 6N137 only).

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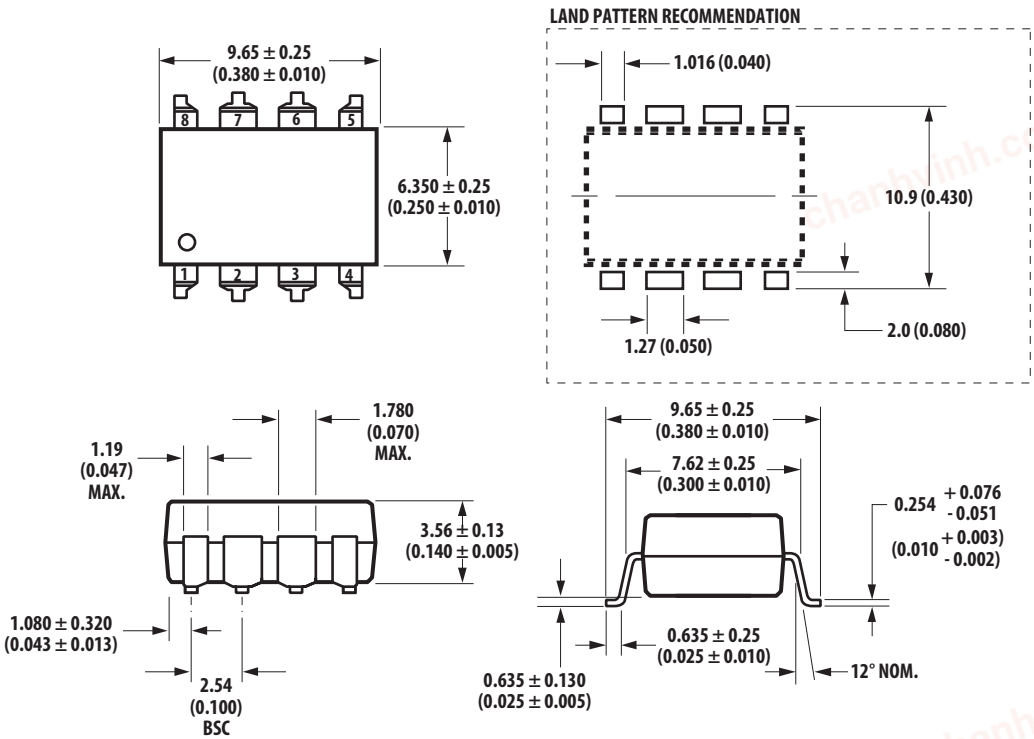
8-pin DIP Package with Gull Wing Surface Mount Option 300 (6N137, HCPL-2601/11/30/31, HCPL-4661)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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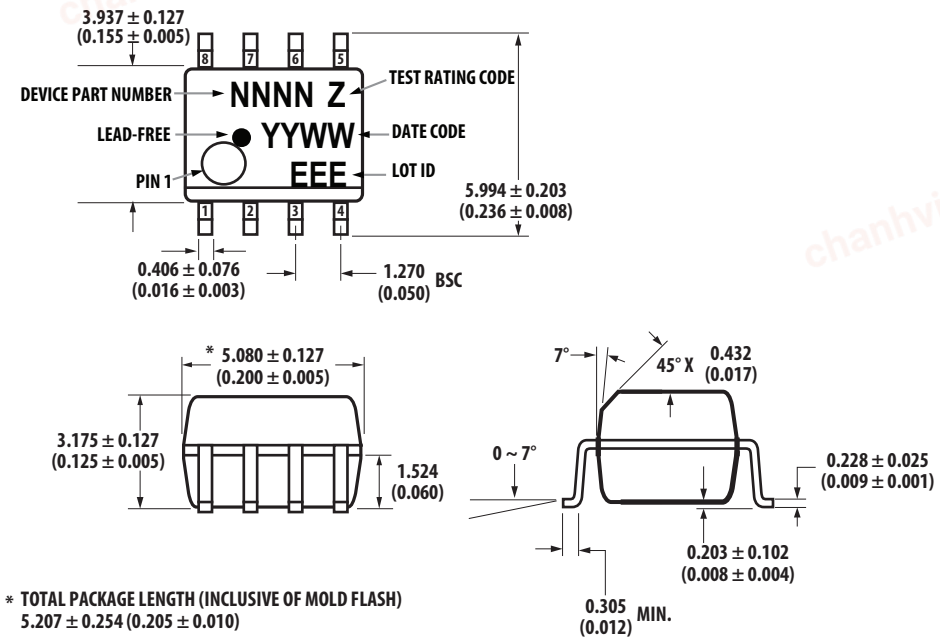
Small-Outline SO-8 Package (HCPL-0600/01/11/30/31/61)

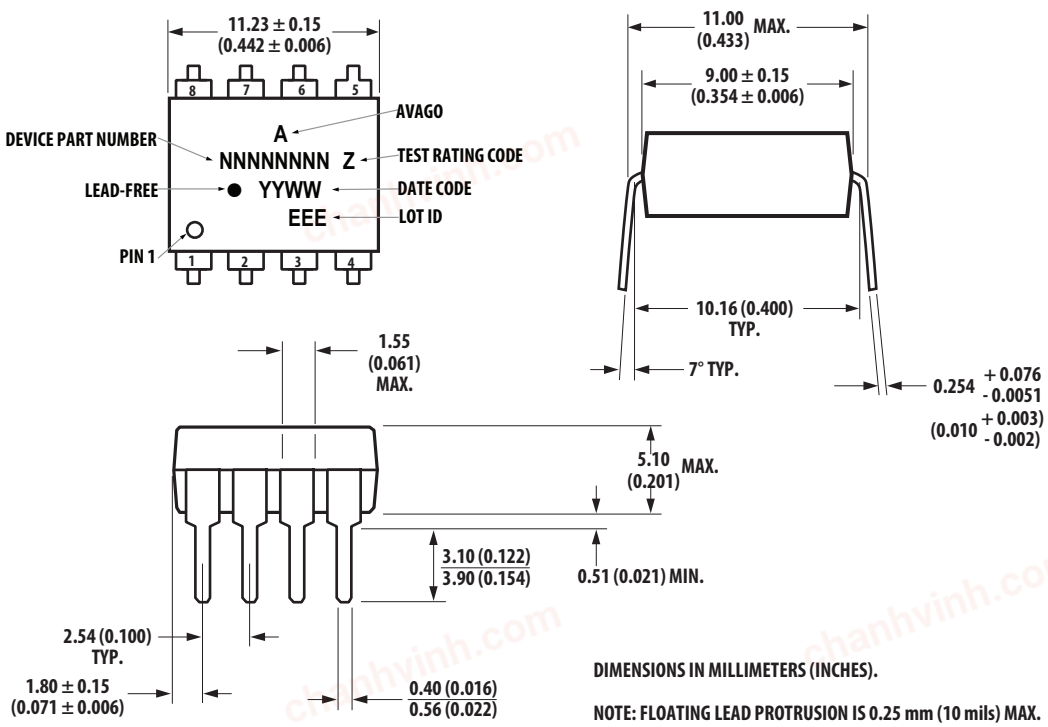


* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

8-Pin Widebody DIP Package (HCNW137, HCNW2601/11)



DIMENSIONS IN MILLIMETERS (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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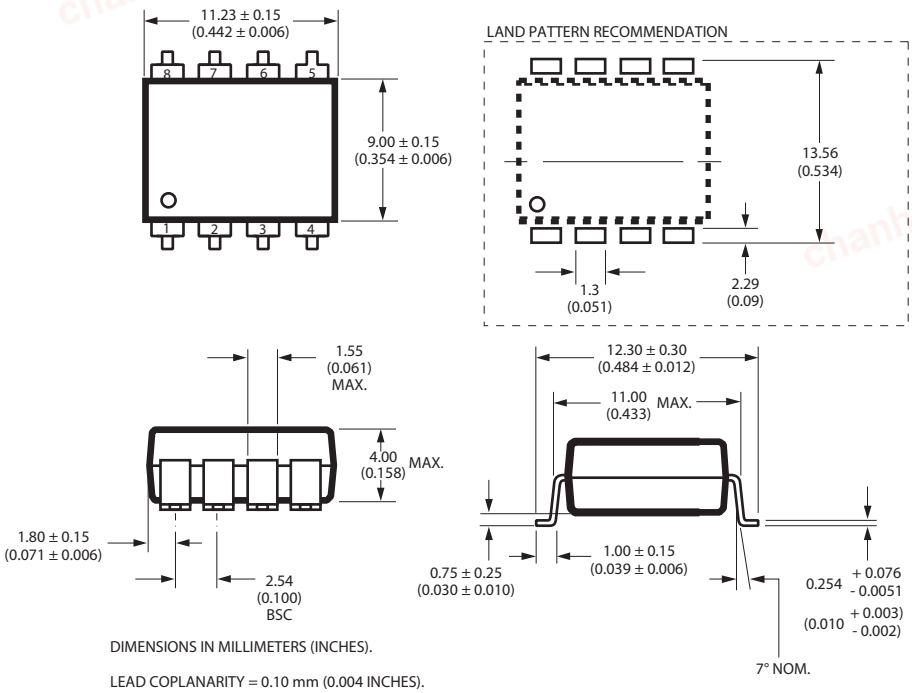
8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW137, HCNW2601/11)



DIMENSIONS IN MILLIMETERS (INCHES).

LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Test Rating Code, Z	Optional Identification Code
L – Option x2x	A – Avago
V – Option x5x or x6x	– UL Logo
	P – Special Program Code

Reflow Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The 6N137, HCPL-26xx/06xx/46xx, and HCNW137/26xx have been approved by the following organizations:

UL Recognized under UL 1577, Component Recognition Program, File E55361.

IEC/EN/DIN EN 60747-5-5

CSA Approved under CSA Component Acceptance Notice #5, File CA 88324.

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Insulation and Safety Related Specifications

Parameter	Symbol	8-pin DIP (300 Mil) Value	SO-8 Value	Widebod (400 Mil) Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – Surface mount classification is Class A in accordance with CECC 00802.

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IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[1] (HCPL-06xx Option 060 Only)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 150 V_{rms} for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 600 V_{rms}		 I-IV I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{peak}
Input-to-Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1063	V_{peak}
Input-to-Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure) Case Temperature Input Current[b] Output Power[b]	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 150 150 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	RS	$\geq 10^9$	Ω

a. Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-5, for a detailed description.

b. Ratings apply to all devices except otherwise noted in the Package column.

1. Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

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IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[1] (HCPL-26xx; 46xx; 6N13x Option 060 Only)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 450 V_{rms}		 I-IV I-IV	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and sample test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1008	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at TS, VIO = 500 V	R_S	≥ 10^9	Ω

a. Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-5, for a detailed description.

1. Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application

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IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[1] (HCNW137/2601/2611 Only)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 600 V_{rms} for rated mains voltage ≤ 1000 V_{rms}		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2651	V_{peak}
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and sample test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 150 400 700	 °C mA mW
Insulation Resistance at TS, VIO = 500 V	R_S	$\geq 10^9$	Ω

a. Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-5, for a detailed description.

1. Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application.

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Absolute Maximum Ratings[1] (No Derating Required up to 85 °C)

Parameter	Symbol	Package[a]	Min.	Max.	Units	Note
Storage Temperature	T_S		–55	125	°C	
Operating Temperature[b]	T_A		–40	85	°C	
Average Forward Input Current	I_F	Single 8-Pin DIP Single SO-8 Widebody		20	mA	c
		Dual 8-Pin DIP Dual SO-8		15		d, e
Reverse Input Voltage	V_R	8-Pin DIP, SO-8		5	V	d
		Widebody		3		
Input Power Dissipation	P_I	Widebody		40	mW	
		Single 8-Pin DIP		36		
Supply Voltage (1 Minute Maximum)	V_{CC}			7	V	
Enable Input Voltage (Not to Exceed VCC by more than 500 mV)	V_E	Single 8-Pin DIP Single SO-8 Widebody		VCC + 0.5	V	
Enable Input Current	I_E			5	mA	
Output Collector Current	I_O			50	mA	d
Output Collector Voltage	V_O			7	V	d
Output Collector Power Dissipation	P_O	Single 8-Pin DIP Single SO-8 Widebody		85	mW	
		Dual 8-Pin DIP Dual SO-8		60		d, f
Lead Solder Temperature (Through Hole Parts Only)	T_{LS}	8-Pin DIP		260 °C for 10 sec., 1.6 mm below seating plane		
		Widebody		260 °C for 10 sec., up to seating plane		
Solder Reflow Temperature Profile (Surface Mount Parts Only)		SO-8 and Option 300		See Package Outline Drawings section		

a. Ratings apply to all devices except otherwise noted in the Package column.

b. 0 °C to 70 °C on JEDEC Registration.

c. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.

d. Each channel.

e. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.

f. Derate linearly above 80 °C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.

1. JEDEC Registered Data (for 6N137 only).

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Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}[a]	0	250	µA
Input Current, High Level[b]	I_{FH}[c]	5	15	mA
Power Supply Voltage	V_{CC}	4.5	5.5	V
Low Level Enable Voltage[d]	V_{EL}	0	0.8	V
High Level Enable Voltage[d]	V_{EH}	2.0	VCC	V
Operating Temperature	T_A	–40	85	°C
Fan Out (at RL = 1 kΩ)[b]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

a. The off condition can also be guaranteed by ensuring that VFL ≤ 0.8 V.

b. Each channel.

c. The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.

d. For single channel products only.

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Electrical Specifications

Over recommended temperature (T_A =–40 °C to +85 °C) unless otherwise specified. All Typicals at V_{CC} = 5 V, T_A = 25 °C.

All enable test conditions apply to single channel products only. See note.

NOTE Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 17. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.

Table 2 Electrical Specifications

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}[a]	All		5.5	100	µA	V_{CC} = 5.5 V, V_E = 2.0 V,	1	b, c, d
							V_O = 5.5 V, I_F = 250 mA		
Input Threshold Current	I_{TH}	Single Channel Widebody		2.0	5.0	mA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2, 3	d
		Dual Channel		2.5					
Low Level Output Voltage	V_{OL}[a]	8-Pin DIP, SO-8		0.35	0.6	V	VCC = 5.5 V, VE = 2.0 V, IF = 5 mA, IOL (Sinking) = 13 mA	2, 3, 4, 5	b, d
		Widebody		0.4					
High Level Supply Current	I_{CCH}	Single Channel		7.0	10.0*	mA	V_E = 0.5 V V_{CC} = 5.5 V, I_F = 0 mA		e
				6.5			V_E = V_{CC}, V_{CC} = 5.5 V, I_F = 0 mA		
		Dual Channel		10	15		Both Channels		
Low Level Supply Current	I_{CCL}	Single Channel		9.0	13.0*	mA	V_E = 0.5 V V_{CC} = 5.5 V, I_F = 10 mA		f
				8.5			V_E = V_{CC}, V_{CC} = 5.5 V I_F = 10 mA		
		Dual Channel		13	21		Both Channels		
High Level Enable Current	I_{EH}	Single Channel		–0.7	–1.6	mA	VCC = 5.5 V, VE = 2.0 V		
Low Level Enable Current	I_{EL}[a]			–0.9	–1.6	mA	VCC = 5.5 V, VE = 0.5 V		g
High Level Enable Voltage	V_{EH}		2.0			V			d
Low Level Enable Voltage	V_{EL}				0.8	V			
Input Forward Voltage	V_F	8-Pin DIP	1.4	1.5	1.75[a]	V	T_A = 25 °C, I_F = 10 mA	6, 7	b
		SO-8	1.3		1.80		I_F = 10 mA		
		Widebody	1.25	1.64	1.85		T_A = 25 °C, I_F = 10 mA		
			1.2		2.05		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R[a]	8-Pin DIP, SO-8	5			V	I_R = 10 A		b
		Widebody	3				I_R = 100 A, T_A = 25°C		

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Table 2 Electrical Specifications (Continued)

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	8-Pin DIP, SO-8		–1.6		mV/°C	I_F = 10 mA	7	b
		Widebody		–1.9					
Input Capacitance	C_{IN}	8-Pin DIP, SO-8		60		pF	f = 1 MHz, V_F = 0 V		b
		Widebody		70					

a. JEDEC registered data for the 6N137. The JEDEC Registration specifies 0 °C to +70 °C. Avago specifies –40 °C to +85 °C.

b. Each channel.

c. The JEDEC registration for the 6N137 specifies a maximum I_{OH} of 250 µA. Avago guarantees a maximum I_{OH} of 100 µA.

d. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance. For single channel products only.

e. The JEDEC registration for the 6N137 specifies a maximum I_{CCH} of 15 mA. Avago guarantees a maximum I_{CCH} of 10 mA.

f. The JEDEC registration for the 6N137 specifies a maximum I_{CCL} of 18 mA. Avago guarantees a maximum I_{CCL} of 13 mA.

g. The JEDEC registration for the 6N137 specifies a maximum I_{EL} of –2.0 mA. Avago guarantees a maximum I_{EL} of –1.6 mA.

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Switching Specifications (AC)

Over Recommended Temperature (T_A = –40 °C to + 85 °C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified.

All Typicals at T_A = 25 °C, V_{CC} = 5 V.

Parameter	Sym.	Package[a]	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75[b]	ns	T_A = 25°C R_L = 350 Ω	8, 9, 10	c, d, f
					100		R_L = 350 Ω C_L = 15 pF		
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75*	ns	T_A = 25°C R_L = 350 Ω C_L = 15 pF		c, e, f
					100		R_L = 350 Ω C_L = 15 pF		
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	8-Pin DIP SO-8		3.5	35	ns	R_L = 350 Ω C_L = 15 pF	8, 9, 10, 11	g, f
		Widebody			40				
Propagation Delay Skew	t_{PSK}				40	ns	R_L = 350 Ω C_L = 15 pF		h, g, f
Output Rise Time (10-90%)	t_r			24		ns	R_L = 350 Ω C_L = 15 pF	12	c, f
Output Fall Time (90-10%)	t_f			10		ns	R_L = 350 Ω C_L = 15 pF	12	c, f
Propagation Delay Time of Enable from VEH to VEL	t_{ELH}	Single Channel		30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	13, 14	i
Propagation Delay Time of Enable from VEL to VEH	t_{EHL}	Single Channel		20		ns			j

a. Ratings apply to all devices except otherwise noted in the Package column.

b. JEDEC registered data for the 6N137.

c. Each channel.

d. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.

e. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.

f. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance. For single channel products only.

g. See application section titled “Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew” for more information.

h. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.

i. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.

j. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.

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Parameter	Sym.	Device	Min.	Typ.	Units		Test Conditions	Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	6N137	1,000	10,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 5 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25 °C	15	a, b, c, d
		HCPL-2630 HCPL-0600/0630 HCNW137	5,000	10,000		$\|V_{CM}\|$ = 1 kV			
		HCPL-2601/2631 HCPL-0601/0631 HCNW2601	10,000	15,000		$\|V_{CM}\|$ = 1 kV			
		HCPL-2611/4661 HCPL-0611/0661 HCNW2611	15,000	25,000		$\|V_{CM}\|$ = 1 kV			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	6N137	1,000	10,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 5 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω,, T_A = 25°C	15	a, e, c, d
		HCPL-2630 HCPL-0600/0630 HCNW137	5,000	10,000		$\|V_{CM}\|$ = 1 kV			
		HCPL-2601/2631 HCPL-0601/0631 HCNW2601	10,000	15,000		$\|V_{CM}\|$ = 1 kV			
		HCPL-2611/4661 HCPL-0611/0661 HCNW2611	15,000	25,000		$\|V_{CM}\|$ = 1 kV			

a. Each channel.

b. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).

c. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM}(p\text{-}p)$.

d. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance. For single channel products only.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).

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Package Characteristics

All Typicals at T_A = 25 °C.

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Insulation	I_{I-O} [a]	Single 8-Pin DIP Single SO-8			1	µA	45% RH, t = 5 s, V_{I-O} = 3 kV dc, T_A = 25 °		b, c
Input-Output Momentary With-stand Voltage[d]	V_{ISO}	8-Pin DIP, SO-8	3750			V rms	RH 50%, t = 1 min, T_A = 25 °C		b, c
		Widebody	5000						b, e
		OPT 020[f]	5000						
Input-Output Resistance	R_{I-O}	8-Pin DIP, SO-8		10^{12}		Ω	V_{I-O} = 500 V_{dc},		g, b, h
		Widebody	10^{12}	10^{13}			V_{I-O} = 500 V_{dc}, T_A = 25 °C		
			10^{11}				V_{I-O} = 500 V_{dc}, T_A = 100 °C		
Input-Output Capacitance	C_{I-O}	8-Pin DIP, SO-8		0.6		pF	f = 1 MHz, T_A = 25 °C		g, b, h
		Widebody		0.5	0.6				
Input-Input Insulation Leakage Current	I_{I-I}	Dual Channel		0.005		µA	RH 45%, t = 5 s, V_{I-I} = 500 V		i
Resistance (Input-Input)	R_{I-I}	Dual Channel		1011		Ω	RH 45%, t = 5 s, V_{I-I} = 500 V		i
Capacitance (Input-Input)	C_{I-I}	Dual 8-Pin DIP		0.03		pF	f = 1 MHz		i
		Dual SO-8		0.25					

a. JEDEC registered data for the 6N137. The JEDEC Registration specifies 0 °C to 70 °C. Avago specifies –40 °C to 85 °C.

b. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.

c. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{rms} for one second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.

d. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

e. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for one second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.

f. For 6N137, HCPL-2601/2611/2630/2631/4661 only.

g. Each channel.

h. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together. For dual channel products only.

i. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual channel products only.

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Figure 1 Typical High Level Output Current vs. Temperature

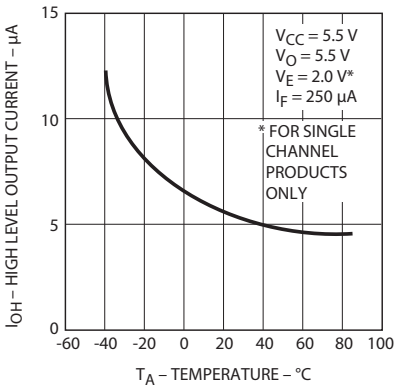

Figure 2 Typical Output Voltage vs. Forward Input Current

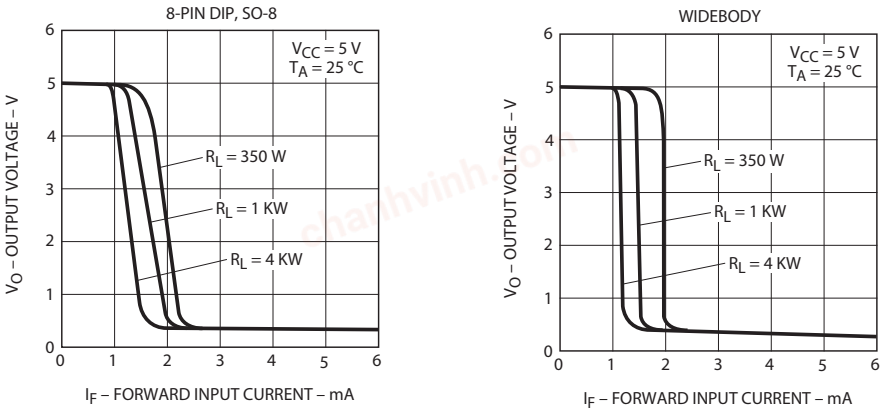

Figure 3 Typical Input Threshold Current vs. Temperature

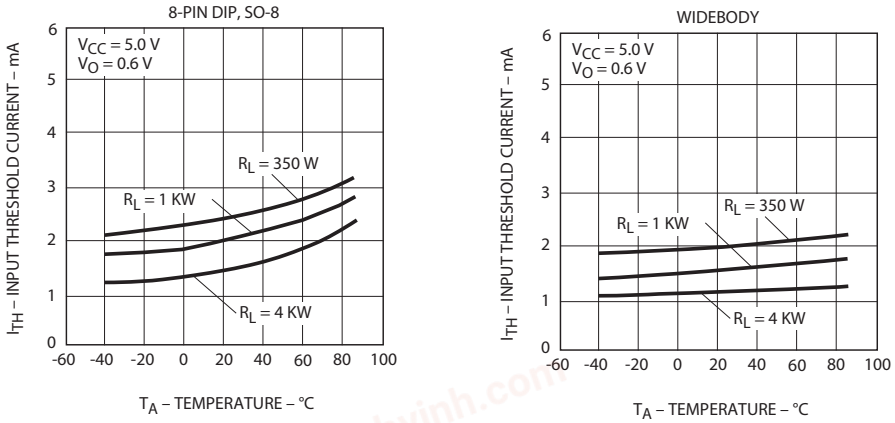

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Figure 4 Typical Low Level Output Voltage vs. Temperature

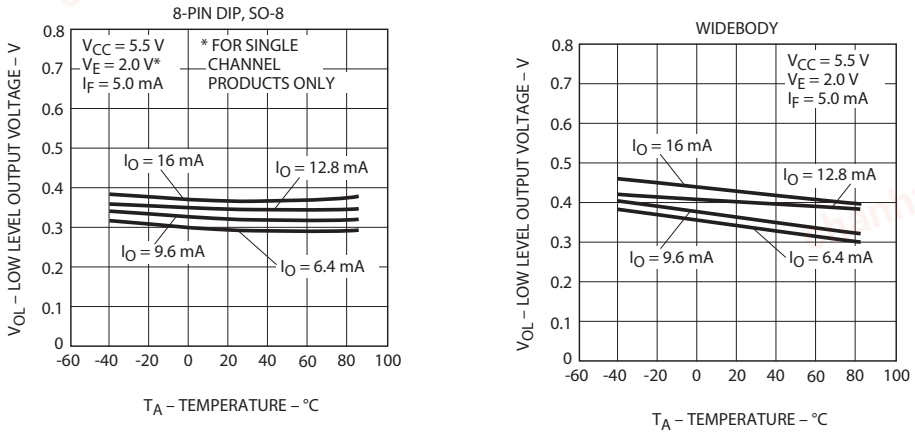

Figure 5 Typical Low Level Output Current vs. Temperature

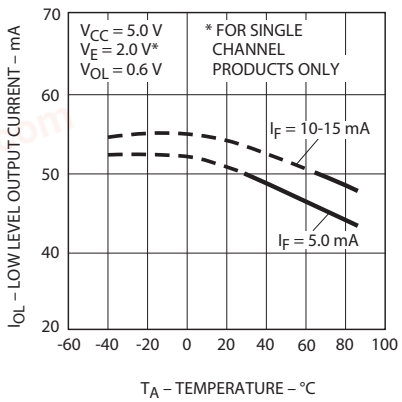

Figure 6 Typical Input Diode Forward Characteristic

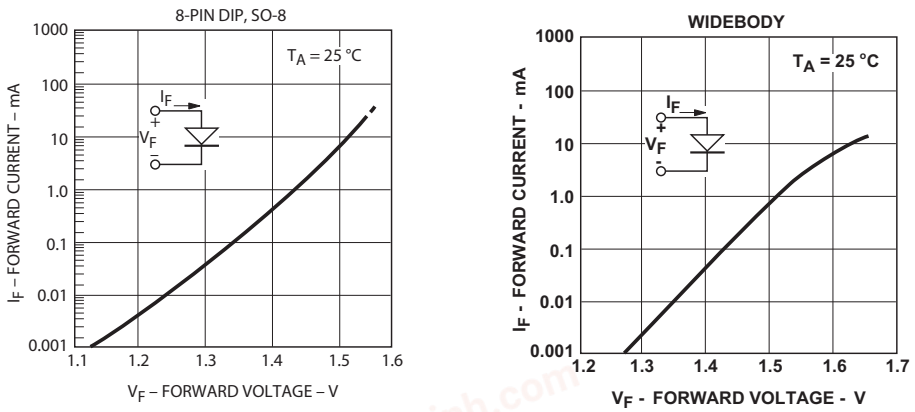

Figure 7 Typical Temperature Coefficient of Forward Voltage vs. Input Current

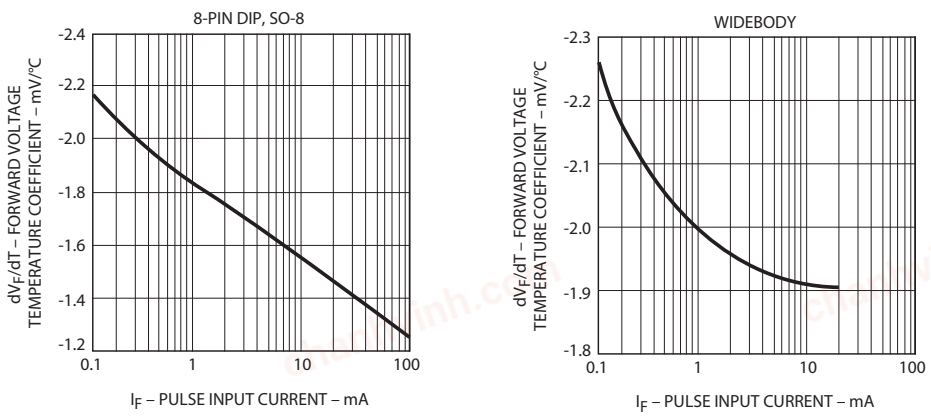

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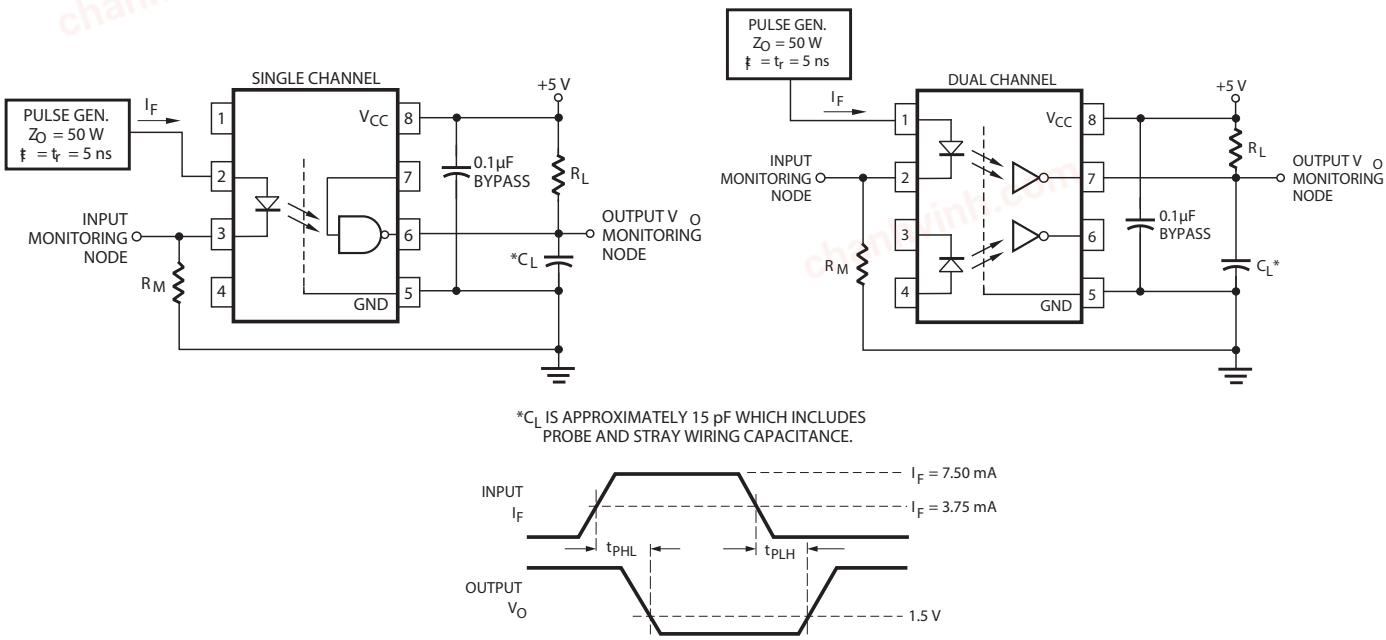
Figure 8 Test Circuit for T_{PHL} and T_{PLH}



*C_L IS APPROXIMATELY 15 pF WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

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Figure 9 Typical Propagation Delay vs. Temperature

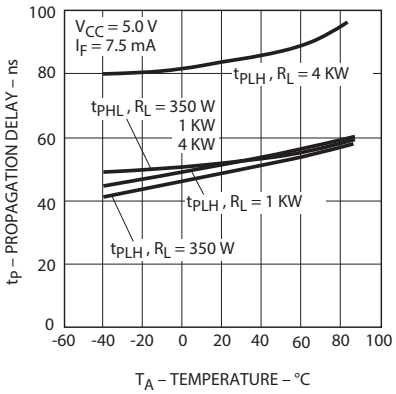

Figure 10 Typical Propagation Delay vs. Pulse Input Current

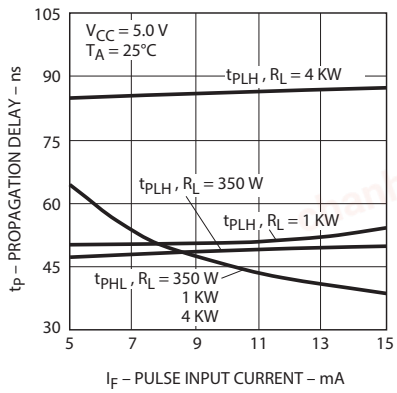

Figure 11 Typical Pulse Width Distortion vs. Temperature

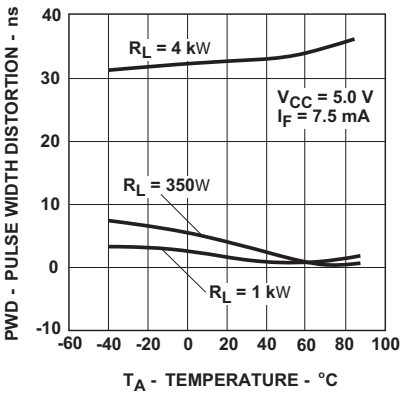

Figure 12 Typical Rise and Fall Time vs. Temperature

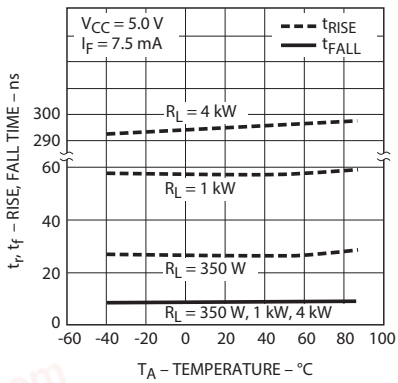

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Figure 13 Test Circuit for t_{EHL} and t_{ELH}

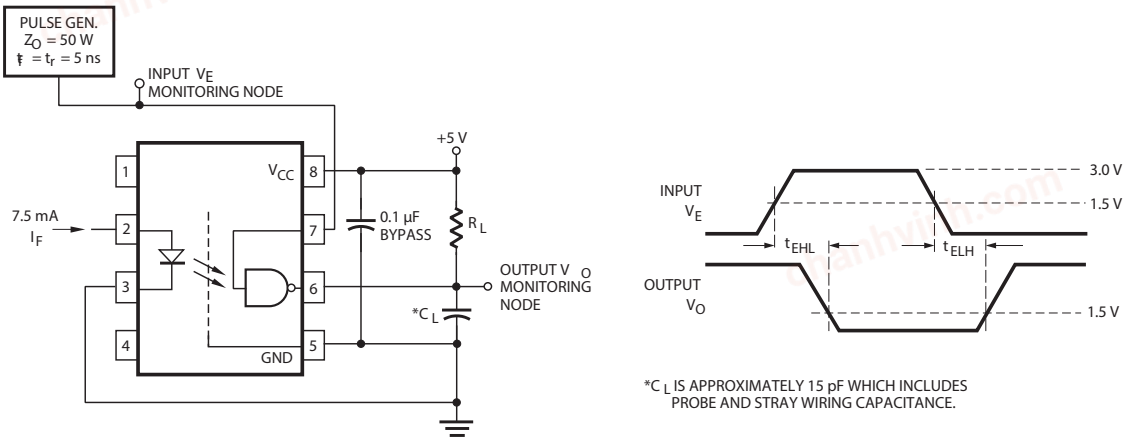

Figure 14 Typical Enable Propagation Delay vs. Temperature

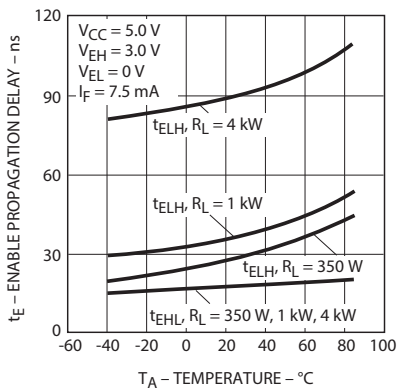

Figure 15 Test Circuit for Common Mode Transient Immunity and Typical Waveforms

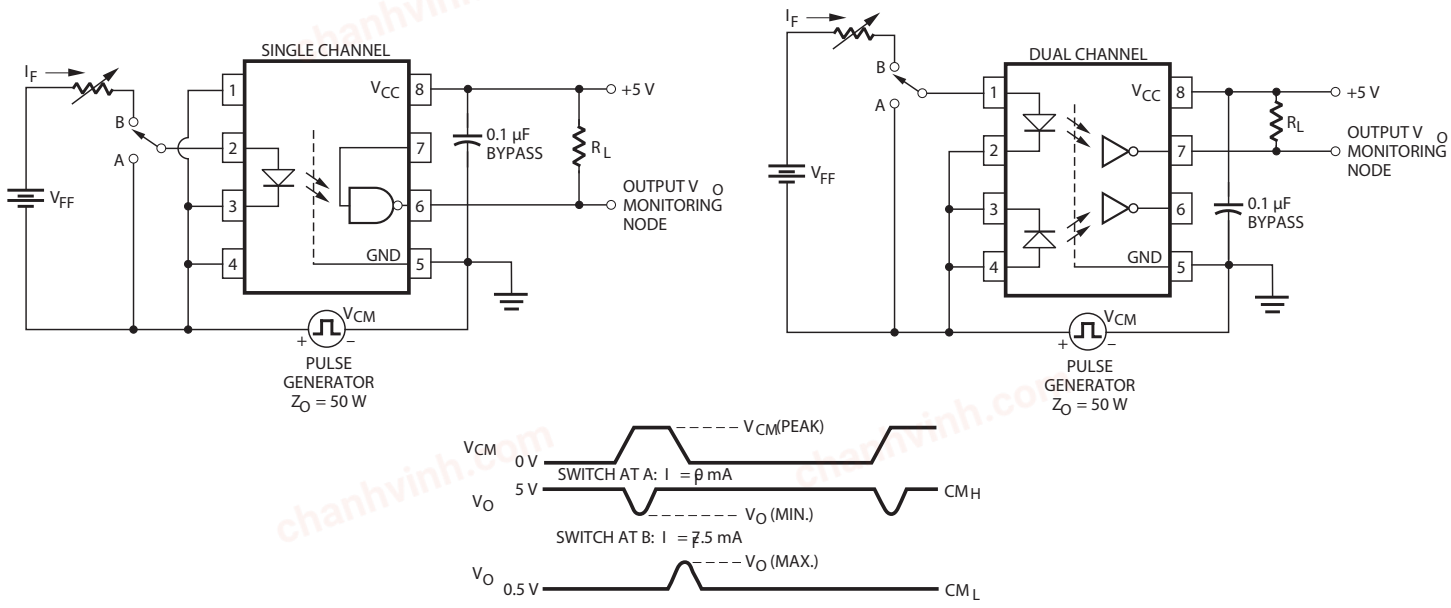

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Figure 16 Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747 5-5

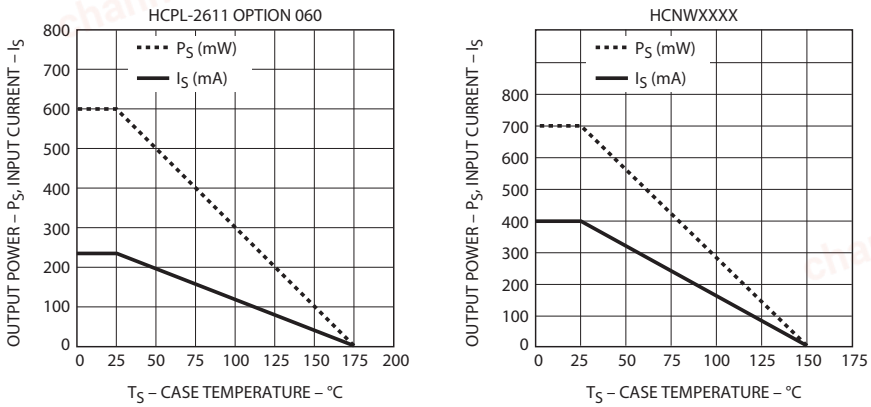

Figure 17 Recommended Printed Circuit Board Layout

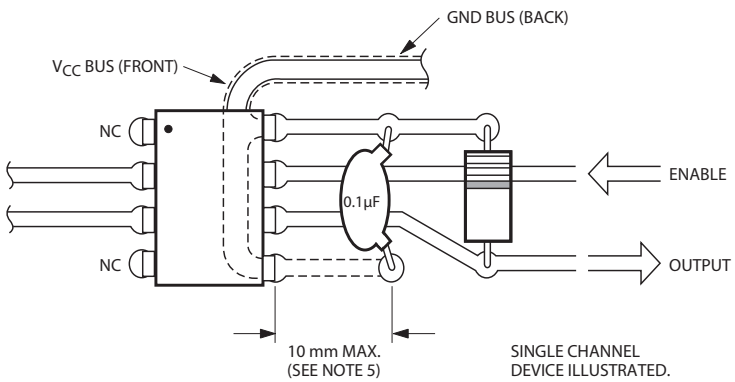

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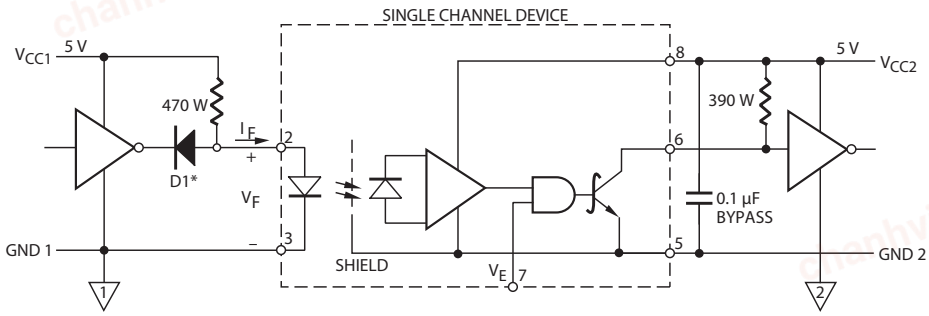
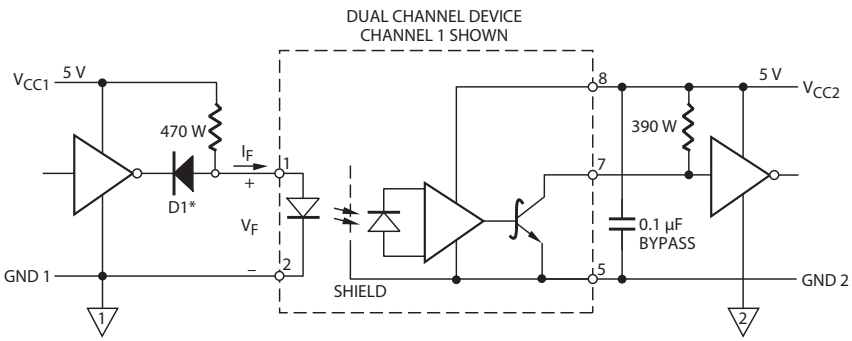
Figure 18 Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.



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Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output causing the output to change from high to low (see Figure 8).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and $t_{PH}L$ and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-l, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 19, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 20 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 20 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulsewidth distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

Figure 19 Illustration of Propagation Delay Skew – tPSK

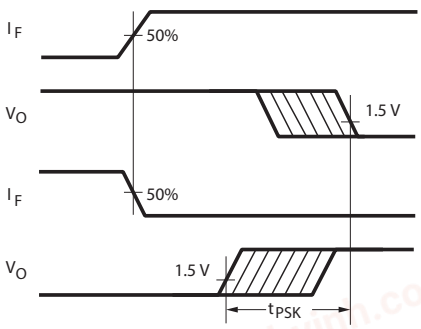
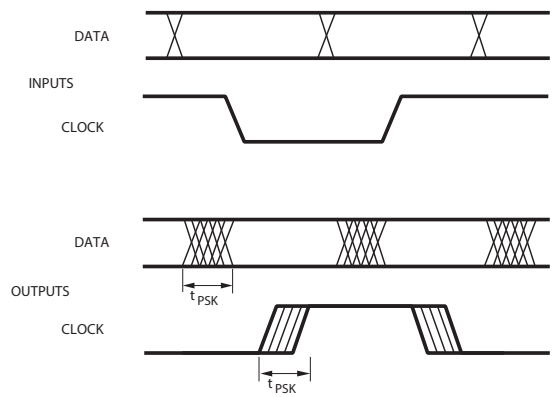


Figure 20 Parallel Data Transmission Example



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AV02-0940EN – March 23, 2016

Lead (Pb) Free
RoHS 6 fully compliant
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product