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HCPL-2400, HCPL-2430

20 MBd High CMR Logic Gate Optocouplers

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

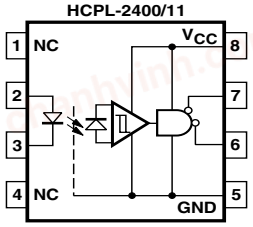
The HCPL-2400 and HCPL-2430 high speed opto-couplers combine an 820 nm AlGaAs light emitting diode with a high speed photodetector. This combina-tion results in very high data rate capability and low input current. The totem pole output (HCPL-2430) or three state output (HCPL-2400) eliminates the need for a pull up resistor and allows for direct drive of data buses.

The detector has optical receiver input stage with built-in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional waveshaping. The hysteresis provides differential mode noise immunity and minimizes the potential for output signal chatter.

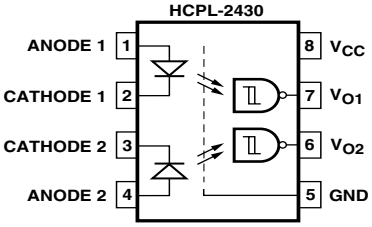
The electrical and switching characteristics of the HCPL-2400 and HCPL-2430 are guaranteed over the temperature range of 0°C to 70°C.

Functional Diagram

HCPL-2400/11



HCPL-2430



TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	L	L
OFF	L	H
ON	H	Z
OFF	H	Z

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

Features

- High speed: 40 MBd typical data rate
- High common mode rejection:
  HCPL-2400: 10 kV/µs at V_{CM} = 300 V (typical)
- AC performance guaranteed over temperature
- High speed AlGaAs emitter
- Compatible with TTL, STTL, LSTTL, and HCMOS logic families
- Totem pole and tri state output (no pull up resistor required)
- Safety approval
  - UL recognized – 3750 V rms for 1 minute per UL1577
  - IEC/EN/DIN EN 60747-5-2 approved with V_{IORM} = 630 V_{peak} (Option 060) for HCPL-2400
  - CSA approved
- High power supply noise immunity
- MIL-PRF-38534 hermetic version available (HCPL-5400/1 and HCPL-5430/1)

Applications

- Isolation of high speed logic systems
- Computer-peripheral interfaces
- Switching power supplies
- Isolated bus driver (networking applications)
- Ground loop elimination
- High speed disk drive I/O
- Digital isolation for A/D, D/A conversion
- Pulse transformer replacement

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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These optocouplers are compatible with TTL, STTL, LSTTL, and HCMOS logic families. When Schottky type TTL devices (STTL) are used, a data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 13. Typical data rates are 40 MBd.

Selection Guide

8-Pin DIP (300 Mil)		Minimum CMR				
Single Channel Package	Dual Channel Package	dV/dt (V/µs)	V_{CM} (V)	Minimum Input On Current (mA)	Maximum Propagation Delay (ns)	Hermetic Package
HCPL-2400		1000	300	4	60	
	HCPL-2430	1000	50	4	60	
		500	50	6	60	HCPL-540X*
		500	50	6	60	HCPL-543X*
		500	50	6	60	HCPL-643X*

*Technical data for the Hermetic HCPL-5400/01, HCPL-5430/31, and HCPL-6430/31 are on separate Avago publications.

Ordering Information

HCPL-2400 and HCPL-2430 are UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
	RoHS Compliant	Non RoHS Compliant							
HCPL-2400	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-060E	#060						X	50 per tube
	-360E	-360		X	X			X	50 per reel
HCPL-2430	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	-					X		50 per tube
	-060E	-						X	50 per tube

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-2430-500E to order product of Gull Wing Surface Mount package in Tape in RoHS compliant.

Example 2:

HCPl-2400 to order product of 8-Pin DIP package in tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

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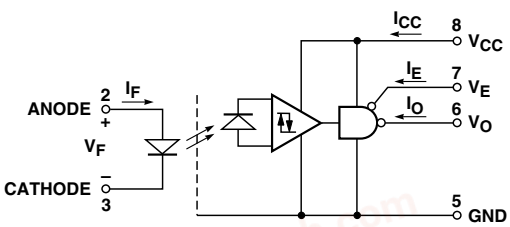
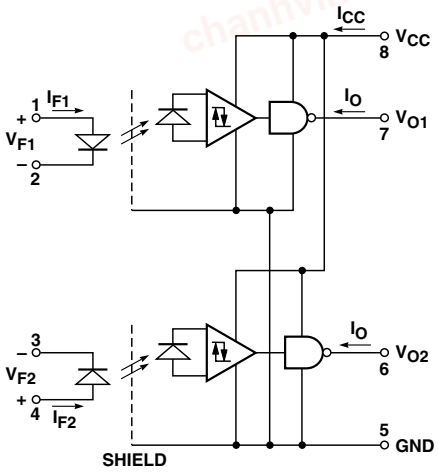
Schematic



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	L	L
OFF	L	H
ON	H	Z
OFF	H	Z



TRUTH TABLE
(POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

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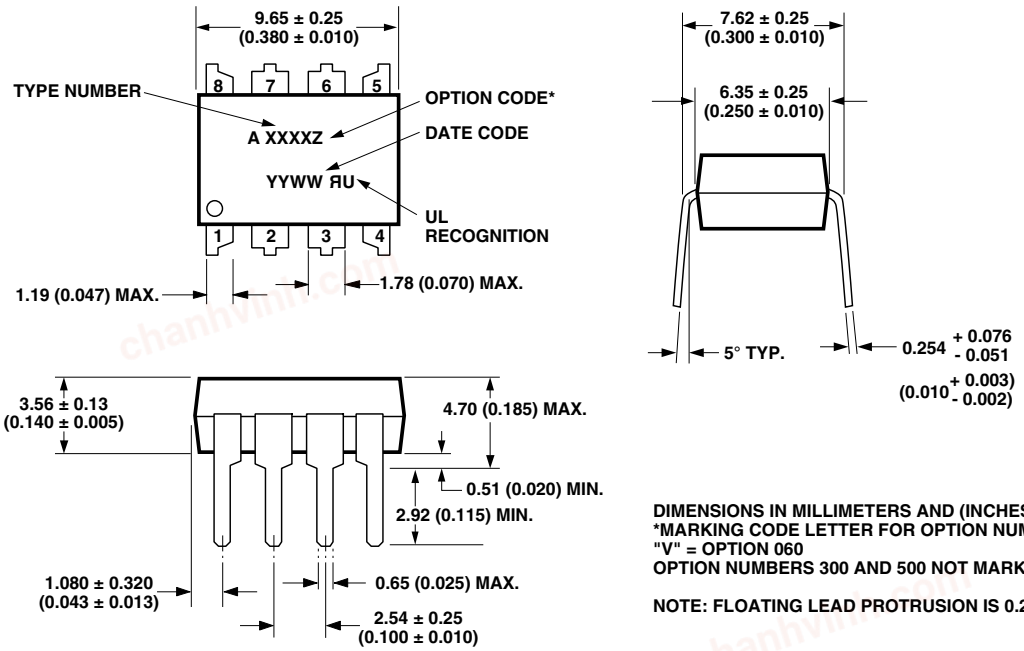
Package Outline Drawings

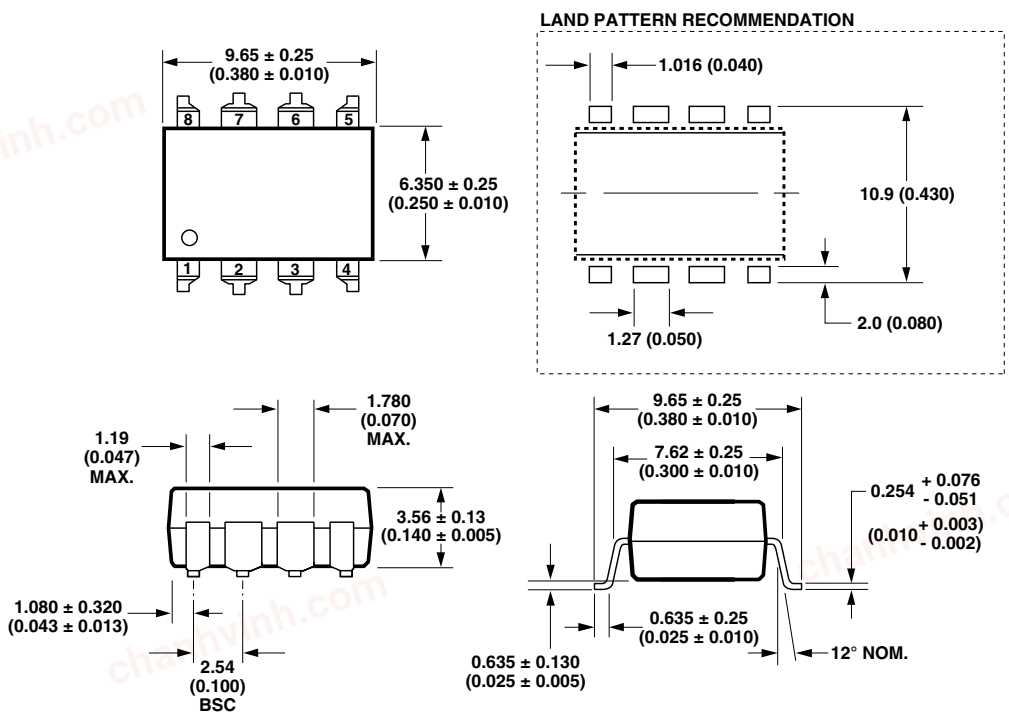
8-Pin DIP Package (HCPL-2400, HCPL-2430)



DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2400, HCPL-2430)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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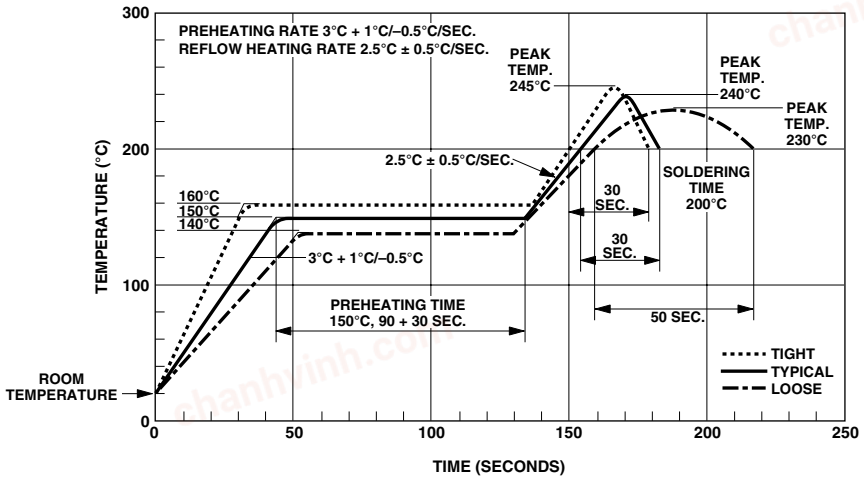
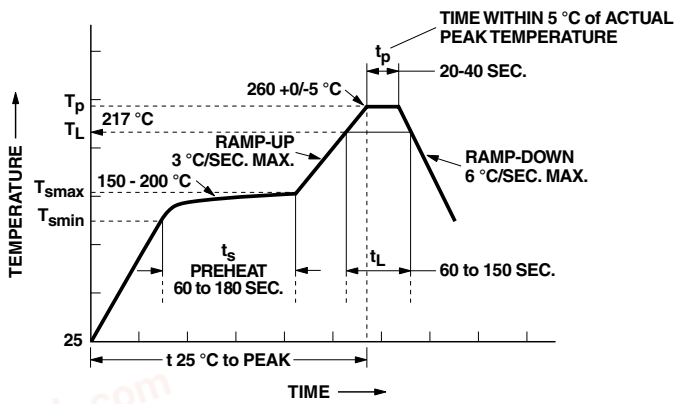
Solder Reflow Thermal Profile



Note: Non-halide flux should be used.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Regulatory Information

The HCPL-24XX has been approved by the following organizations:

VDE

Approved according to VDE 0884/06.92 (Option 060 only).

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

IEC/EN/DIN EN 60747-5-2

Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01.
(Option 060 only)

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Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics
(HCPL-2400 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤300 V rms		I-IV	
for rated mains voltage ≤450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 12, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2 for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must ben ensured by protective circuits in application.

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Absolute Maximum Ratings

(No derating required up to 70°C)

Parameter	Symbol	Minimum	Maximum	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Average Forward Input Current	$I_{F(AVG)}$		10	mA	
Peak Forward Input Current	I_{FPK}		20	mA	12
Reverse Input Voltage	V_R		2	V	
Three State Enable Voltage (HCPL-2400 Only)	V_E	-0.5	10	V	
Supply Voltage	V_{CC}	0	7	V	
Average Output Collector Current	I_O	-25	25	mA	
Output Collector Voltage	V_O	-0.5	10	V	
Output Voltage	V_O	-0.5	18	V	
Output Collector Power Dissipation (Each Channel)	P_O		40	mW	
Total Package Power Dissipation (Each Channel)	P_T		350	mW	
Lead Solder Temperature (for Through Hole Devices)	260°C for 10 sec., 1.6 mm below seating plane				
Reflow Temperature Profile (Option #300)	See **Package Outline Drawings** section				

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Power Supply Voltage	V_{CC}	4.75	5.25	V
Forward Input Current (ON)	$I_{F(ON)}$	4	8	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$		0.8	V
Fan Out	N		5	TTL Loads
Enable Voltage (Low) HCPL-2400 Only)	V_{EL}	0	0.8	V
Enable Voltage (High) HCPL-2400 Only)	V_{EH}	2	V_{CC}	V
Operating Temperature	T_A	0	70	°C

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Electrical Specifications

0°C ≤T_A ≤70°C, 4.75 V ≤V_{CC} ≤5.25 V, 4 mA ≤$I_{F(ON)}$ ≤8 mA, 0 V ≤$V_{F(OFF)}$ ≤0.8 V. All typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 6.0 mA, $V_{F(OFF)}$ = 0 V, except where noted. See Note 11.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}				0.5	V	I_{OL} = 8.0 mA (5 TTL Loads)	1	
Logic High Output Voltage	V_{OH}		2.4 2.7			V	I_{OH} = -4.0 mA I_{OH} = -0.4 mA	2	
Output Leakage Current	I_{OHH}				100	µA	V_O = 5.25 V, V_F = 0.8 V		
Logic High Enable Current	V_{EH}	2400	2.0			V			
Logic Low Enable Voltage	V_{EL}	2400			0.8	V			
Logic High Enable Current	I_{EH}	2400			20	µA	V_E = 2.4 V		
					100		V_E = 5.25 V		
Logic Low Enable Current	I_{EL}	2400		-0.28	-0.4	mA	V_E = 0.4 V		
Logic Low Supply Current	I_{CCL}	2400		19	26	mA	V_{CC} = 5.25 V, V_E = 0 V, I_O = Open		
		2430		34	46		V_{CC} = 5.25 V, I_O = Open		
Logic High Supply Current	I_{CCH}	2400		17	26	mA	V_{CC} = 5.25 V, V_E = 0 V, I_O = Open		
		2430		32	42		V_{CC} = 5.25 V, I_O = Open		
High Impedance State Supply Current	I_{CCZ}	2400		22	28	mA	V_{CC} = 5.25 V, V_E = 5.25 V		
High Impedance State Output Current	I_{OZL}	2400			20	µA	V_O = 0.4 V, V_E = 2 V		
	I_{OZH}				20	µA	V_O = 2.4 V		
	I_{OZH}				100	µA	V_O = 5.25 V		
Logic Low Short Circuit Output Current	I_{OSL}			52		mA	V_O = V_{CC} = 5.25 V, I_F = 8 mA	2	
Logic High Short Circuit Output Current	I_{OSH}			-45		mA	V_{CC} = 5.25 V, I_F = 0 mA, V_O = GND		2
Input Current Hysteresis	I_{HYS}		0.25			mA	V_{CC} = 5 V	3	
Input Forward Voltage	V_F		1.1	1.3	1.5		T_A = 25°C, I_F = 8 mA		
			1.0		1.55			4	
Input Reverse Breakdown Voltage	BV_R		3.0	5.0		V	T_A = 25°C, I_R = 10 µA		
			2.0						
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.44		mV/°C	I_F = 6 mA	4	
Input Capacitance	C_{IN}			20		pF	f = 1 MHz, V_F = 0 V		

*All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

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Switching Specifications

0°C ≤ T_A ≤ 70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, 4 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V. All typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 6.0 mA, $V_{F(OFF)}$ = 0 V, except where noted. See Note 11.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}				55	ns	$I_{F(ON)}$ = 7 mA	5, 6, 7	1, 4, 5, 6
			15	33	60				
Propagation Delay Time to Logic High Output Level	t_{PLH}				55	ns	$I_{F(ON)}$ = 7 mA	5, 6, 7	1, 4, 5, 6
			15	30	60				
Pulse Width Distortion	$\|t_{PHL}-t_{PLH}\|$			2	15	ns	$I_{F(ON)}$ = 7 mA	5, 8	6
				5	25				
Propagation Delay Skew	t_{PSK}				35	ns	Per Notes & Text	15, 16	7
Output Rise Time	t_r			20		ns		5	
Output Fall Time	t_f			10		ns		5	
Output Enable Time to Logic High	t_{PZH}	2400		15		ns		9, 10	
Output Enable Time to Logic Low	t_{PZL}	2400		30		ns		9, 10	
Output Disable Time from Logic High	t_{PHZ}	2400		20		ns		9, 10	
Output Disable Time from Logic Low	t_{PLZ}	2400		15		ns		9, 10	
Logic High Common Mode Transient Immunity	$\|CM_H\|$		1000	10,000		V/µs	V_{CM} = 300 V, T_A = 25°C, I_F = 0 mA	11	9
Logic Low Common Mode Transient Immunity	$\|CM_L\|$		1000	10,000		V/µs	V_{CM} = 300 V, T_A = 25°C, I_F = 4 mA	11	9
Power Supply Noise Immunity	PSNI			0.5		V_{p-p}	V_{CC} = 5.0 V, 48 Hz ≤ = F_{AC} ≤50 MHz		10

*All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

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Package Characteristics

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		3750			V rms	RH ≤50%, t = 1 min., T_A = 25°C		3, 13
Input-Output Resistance	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		3
Input-Output Capacitance	C_{I-O}			0.6		pF	f = 1 MHz V_{I-O} = 0 Vdc		
Input-Input Insulation Leakage Current	I_{I-I}	2430		0.005		μA	RH ≤45% t = 5 s, V_{I-I} = 500 Vdc		8
Resistance (Input-Input)	R_{I-I}	2430		10^{11}		Ω	V_{I-I} = 500 Vdc		8
Capacitance (Input-Input)	C_{I-I}	2430		0.25		pF	f = 1 MHz		8

*All typical values are at T_A = 25°C.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Each channel.
2. Duration of output short circuit time not to exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse.
5. The typical data shown is indicative of what can be expected using the application circuit in Figure 13.
6. This specification simulates the worst case operating conditions of the HCPL-2400 over the recommended operating temperature and V_{CC} range with the suggested application circuit of Figure 13.
7. Propagation delay skew is discussed later in this data sheet.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
10. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)}$ > 2.0 V, and for desired logic low state, $V_{OL(MAX)}$ < 0.8 V.
11. Use of a 0.1 μF bypass capacitor connected between pins 8 and 5 adjacent to the device is required.
12. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V rms for one second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% Production test shown in the IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics Table, if applicable.

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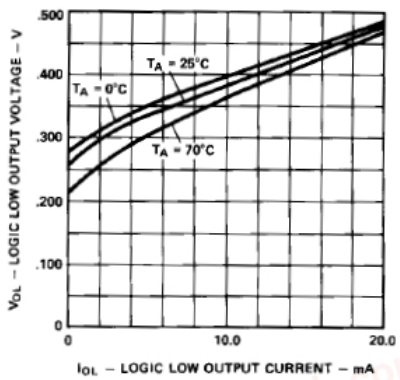

Figure 1. Typical logic low output voltage vs. logic low output current.

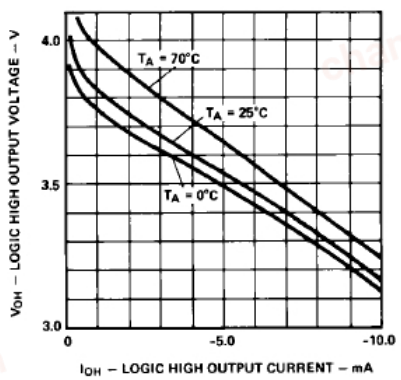

Figure 2. Typical logic high output voltage vs. logic high output current.

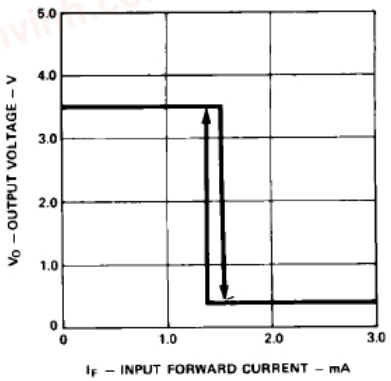

Figure 3. Typical output voltage vs. input forward current.

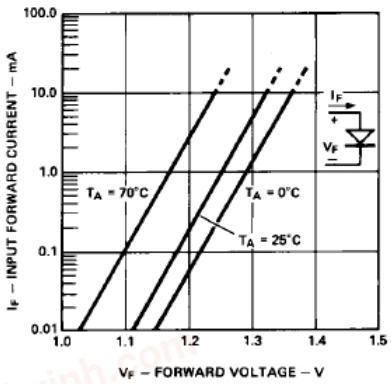

Figure 4. Typical diode input forward current characteristic.

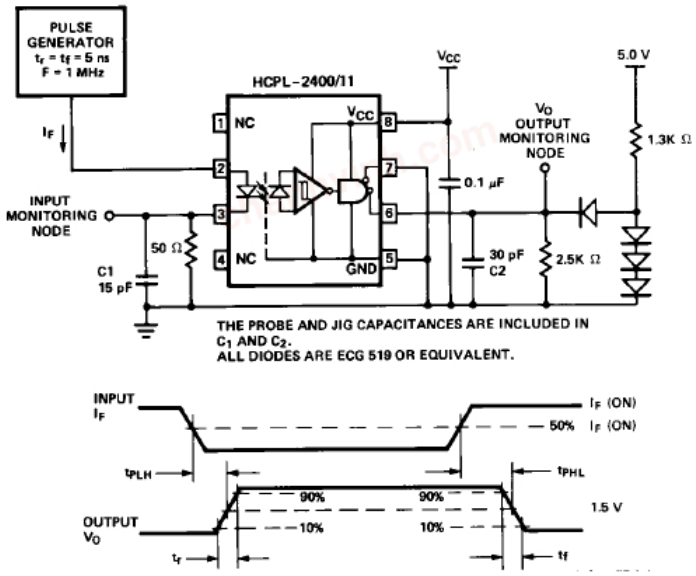

Figure 5. Test circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

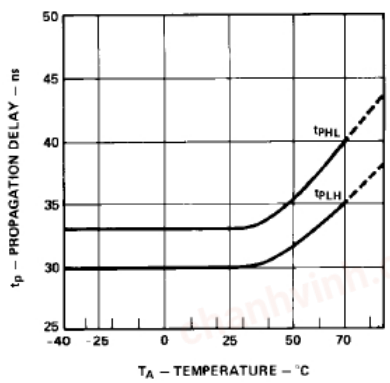

Figure 6. Typical propagation delay vs. ambient temperature.

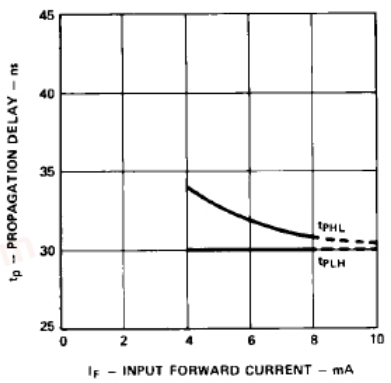

Figure 7. Typical propagation delay vs. input forward current.

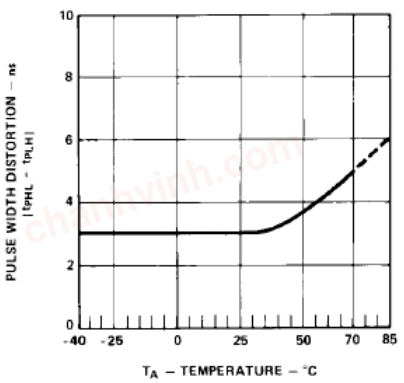

Figure 8. Typical pulse width distortion vs. ambient temperature.

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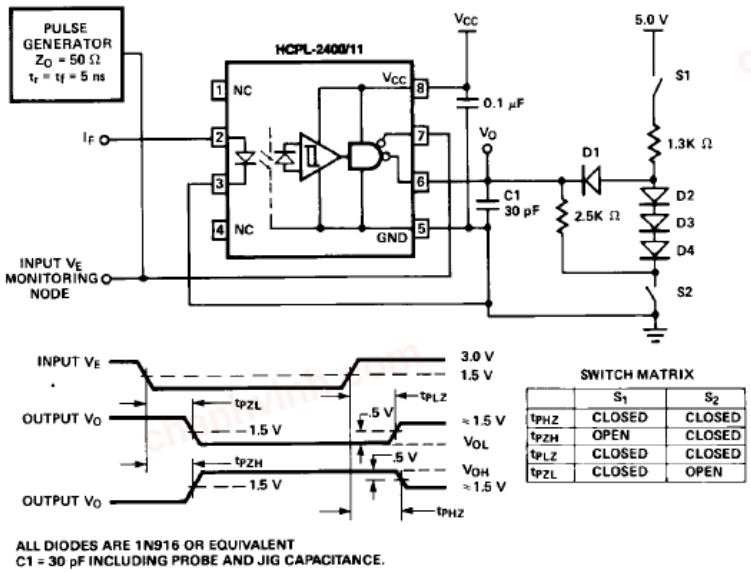

	S_1	S_2
t_{PHZ}	CLOSED	CLOSED
t_{PZH}	OPEN	CLOSED
t_{PLZ}	CLOSED	CLOSED
t_{PZL}	CLOSED	OPEN

Figure 9. Test circuit for t_{PHZ}, t_{PZH}, t_{PLZ} and t_{PZL}.

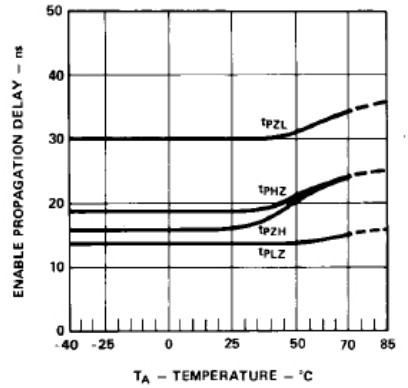

Figure 10. Typical enable propagation delay vs. ambient temperature.

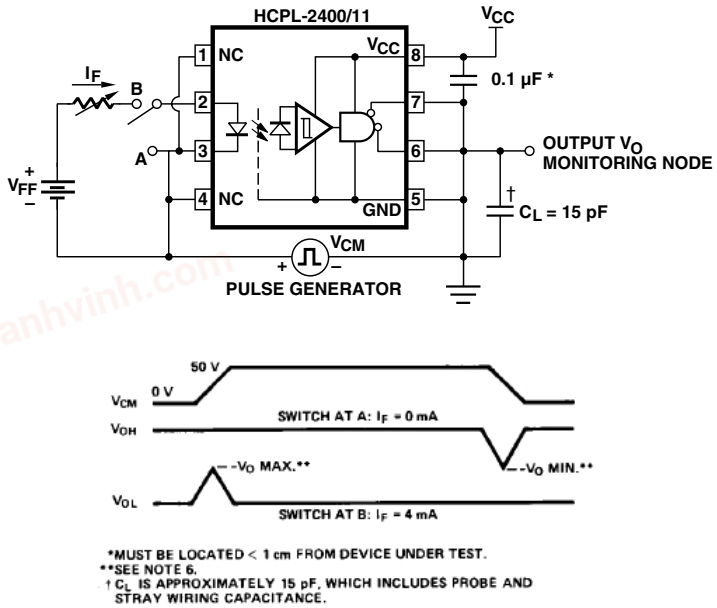

Figure 11. Test diagram for common mode transient immunity and typical waveforms.

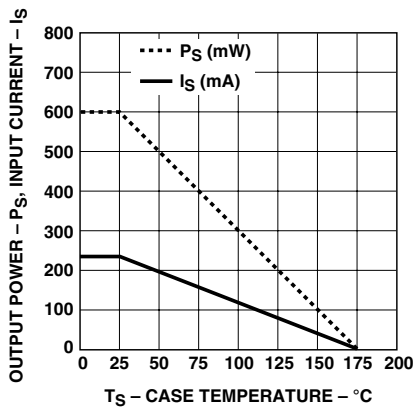

Figure 12. Thermal derating curve, dependence of safety limiting value with case temperature per IEC/EN/DIN EN 60747-5-2.

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Applications

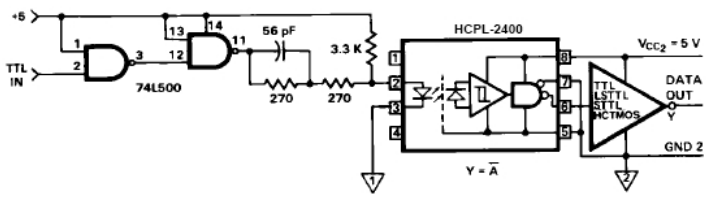

Figure 13. Recommended 20 MBd HCPL-2400/30 interface circuit.

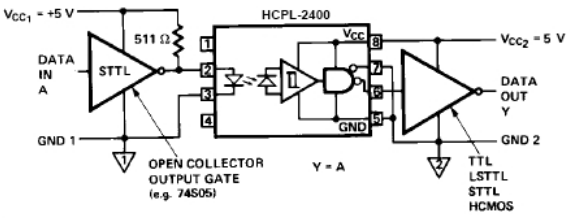

Figure 14. Alternative HCPL-2400/30 interface circuit.

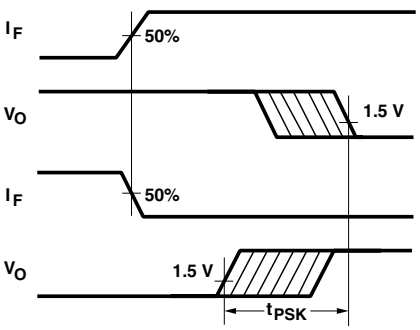

Figure 15. Illustration of propagation delay skew – t_{PSK}.

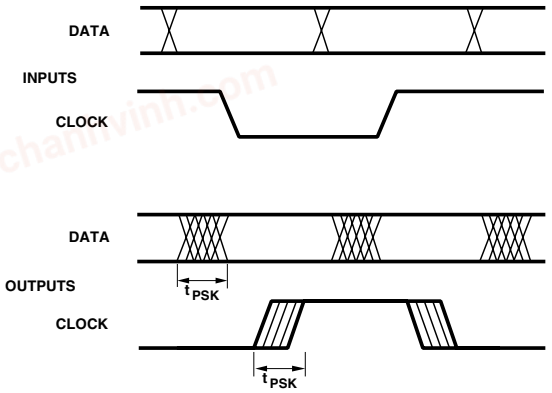

Figure 16. Parallel data transmission example.

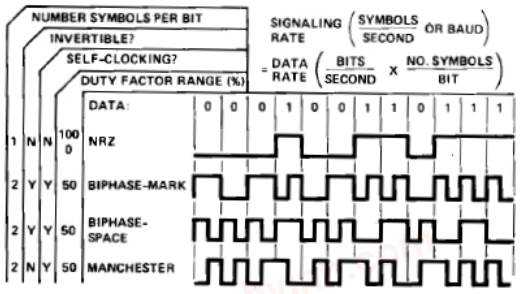

Figure 17. Modulation code selections.

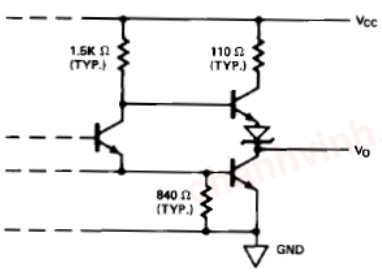

Figure 18. Typical HCPL-2400/30 output schematic.

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Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 5).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 15, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest pro-pagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 16 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signals are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 16 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PHZ}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-2400/30 optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature, input current, and power supply ranges.

Application Circuit

A recommended LED drive circuit is shown in Figure 13. This circuit utilizes several techniques to minimize the total pulse-width distortion at the output of the optocoupler. By using two inverting TTL gates connected in series, the inherent pulse-width distortion of each gate cancels the distortion of the other gate. For best results, the two series-connected gates should be from the same package.

The circuit in Figure 13 also uses techniques known as prebias and peaking to enhance the performance of the optocoupler LED. Prebias is a small forward voltage applied to the LED when the LED is off. This small prebias voltage partially charges the junction capacitance of the LED, allowing the LED to turn on more quickly. The speed of the LED is further increased by applying momentary current peaks to the LED during the turn-on and turn-off transitions of the drive current. These peak currents help to charge and discharge the capacitances of the LED more quickly, shortening the time required for the LED to turn on and off.

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Switching performance of the HCPL-2400/30 optocouplers is not sensitive to the TTL logic family used in the recommended drive circuit. The typical and worst-case switching parameters given in the data sheet can be met using common 74LS TTL inverting gates or buffers. Use of faster TTL families will slightly reduce the overall propagation delays from the input of the drive circuit to the output of the optocoupler, but will not necessarily result in lower pulse-width distortion or propagation delay skew. This reduction in overall propagation delay is due to shorter delays in the drive circuit, not to changes in the propagation delays of the optocoupler; optocoupler propagation delays are not affected by the speed of the logic used in the drive circuit.

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