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BROADCOM®

Data Sheet

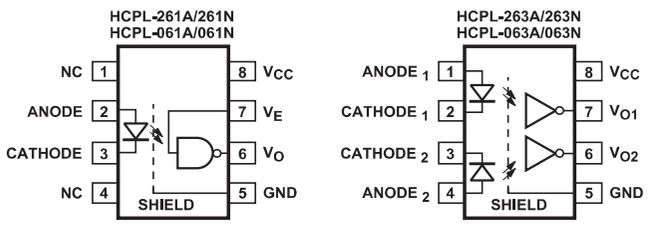
HCPL-261A, HCPL-061A, HCPL-263A, HCPL-063A, HCPL-261N, HCPL-061N, HCPL-263N, HCPL-063N

HCMOS Compatible, High CMR, 10-MBd Optocouplers

Description

The Broadcom® HCPL-261A family of optically coupled gates provide all the benefits of the industry-standard 6N137 family with the added benefit of HCMOS compatible input current. This allows direct interface to all common circuit topologies without additional LED buffer or drive components. The Al-GaAs LED used allows lower drive currents and reduces degradation by using the latest LED technology. On the single-channel parts, an enable output allows the detector to be strobed. The output of the detector IC is an open collector schottky-clamped transistor. The internal shield provides a minimum common mode transient immunity of 1000 V/µs for the HCPL-261A family and 15000 V/µs for the HCPL-261N family.

Figure 1: Functional Diagram



NOTE: The connection of a 0.1-µF bypass capacitor between pins 5 and 8 is required.

TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

Features

- HCMOS/LSTTL/TTL performance compatible
- 1000 V/µs minimum Common Mode Rejection (CMR) at V_{CM} = 50V (HCPL-261A family) and 15 kV/µs minimum CMR at V_{CM} = 1000V (HCPL-261N family)
- High speed: 10 MBd typical
- AC and DC performance specified over industrial temperature range –40°C to +85°C
- Available in 8-pin DIP, SOIC-8 packages
- Safety approval:
  - UL recognized per UL1577 3750 V_{rms} for 1 minute and 5000 V_{rms} for 1 minute (Option 020)
  - CSA approved
  - IEC/EN/DIN EN 60747-5-5 approved

Applications

- Low input current (3.0 mA) HCMOS compatible version of 6N137 optocoupler
- Isolated line receiver
- Simplex/multiplex data transmission
- Computer-peripheral interface
- Digital isolation for A/D, D/A conversion
- Switching power supplies
- Instrumentation input/output isolation
- Ground loop elimination
- Pulse transformer replacement

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage and/or degradation that might be induced by electrostatic discharge (ESD). The components featured in this data sheet are not to be used in military or aerospace applications or environments.

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Selection Guide

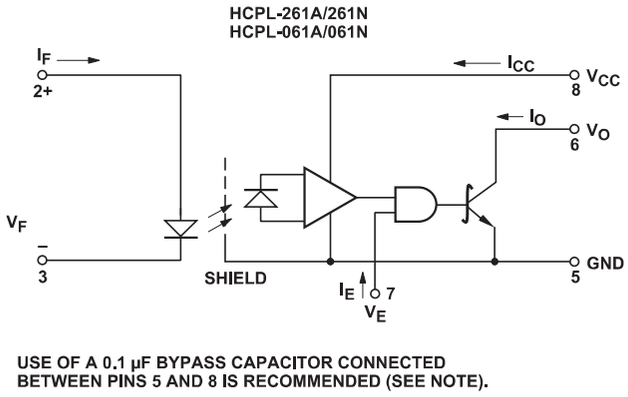
Minimum CMR		Input		8-Pin DIP (300 Mil)		Small-Outline SO-8 (400 Mil)		Wide Body	Hermetic
dV/dt (V/µs)	V_{CM} (V)	On-Current (mA)	Output Enable	Single-Channel Package	Dual-Channel Package	Single-Channel Package	Dual-Channel Package	Single-Channel Package	Single- and Dual-Channel Packages
NA	NA	5	YES	6N137[a]		HCPL-0600[a]		HCNW137[a]	
			NO		HCPL-2630[a]		HCPL-0630[a]		
5,000	50		YES	HCPL-2601[a]		HCPL-0601[a]		HCNW2601[a]	
			NO		HCPL-2631[a]		HCPL-0631[a]		
10,000	1,000		YES	HCPL-2611[a]		HCPL-0611[a]		HCNW2611[a]	
			NO		HCPL-4661[a]		HCPL-0661[a]		
1,000	50		YES	HCPL-2602[a]					
3,500	300		YES	HCPL-2612[a]					
1,000	50	3	YES	HCPL-261A		HCPL-061A			
			NO		HCPL-263A		HCPL-063A		
1,000[b]	1,000		YES	HCPL-261N		HCPL-061N			
			NO		HCPL-263N		HCPL-063N		
1,000	50	12.5	c						HCPL-193x[a]
									HCPL-56xx[a]
									HCPL-66xx[a]

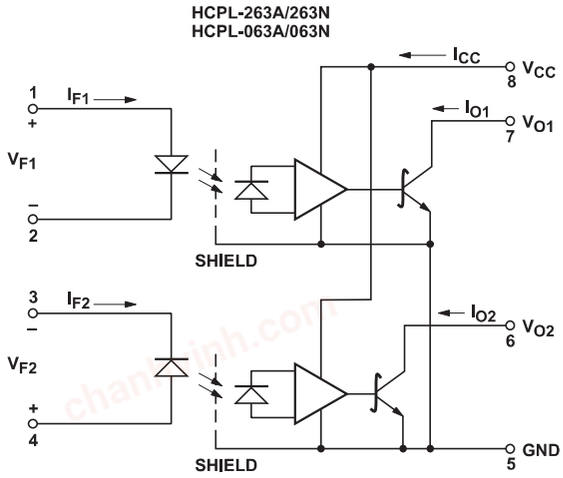
a. Technical data are on separate Broadcom publications.

b. 15 kV/µs with V_{CM} = 1 kV can be achieved using a Broadcom application circuit.

c. Enable is available for single-channel products only, except for HCPL-193x devices.

Schematic





Note: Bypassing of the power supply line is required with a 0.1-µF ceramic disc capacitor adjacent to each optocoupler as shown in Figure 20. The total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.

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Ordering Information

HCPL-xxxx is UL recognized with 3750 V_{rms} for 1 minute per UL1577.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape and Reel	UL 5000 V_{rms}/1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Non-RoHS Compliant							
HCPL-261A	-000E	No option	300-mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	-320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-261N	-000E	No option	300-mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	—		X	X	X		X	1000 per reel
HCPL-263A	-000E	No option	300-mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
HCPL-263N	-000E	No option	300-mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
HCPL-061A HCPL-061N	-000E	No option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
	-060E	#060		X				X	100 per tube
	-560E	#560		X		X		X	1500 per reel
HCPL-063A HCPL-063N	-000E	No option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel

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To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry. The combination of Option 020 and Option 060 is not available.

Example:

HCPL-261A-560E to order product of 300-mil DIP Gull Wing Surface-Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

NOTE: The notation #XXX is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant option will use -XXXE.

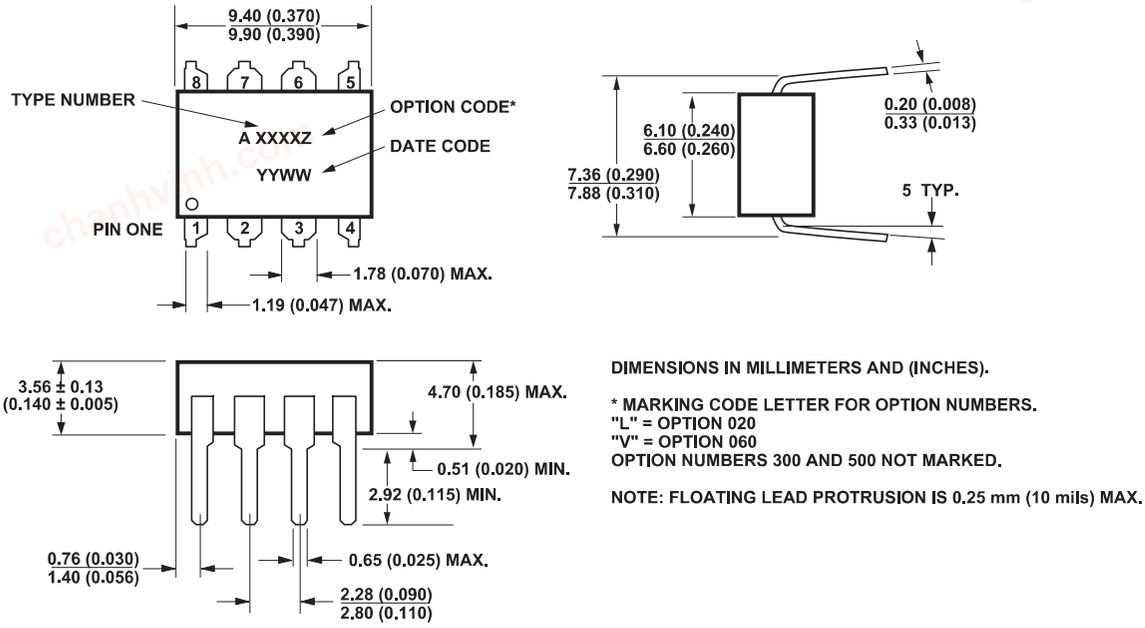
Package Outline Drawings

NOTE: Pin locations are for reference only.

HCPL-261A/261N/263A/263N Outline Drawings

NOTE: Pin location for reference only.

Figure 2: 8-Pin Dual In-Line Package Device Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS.
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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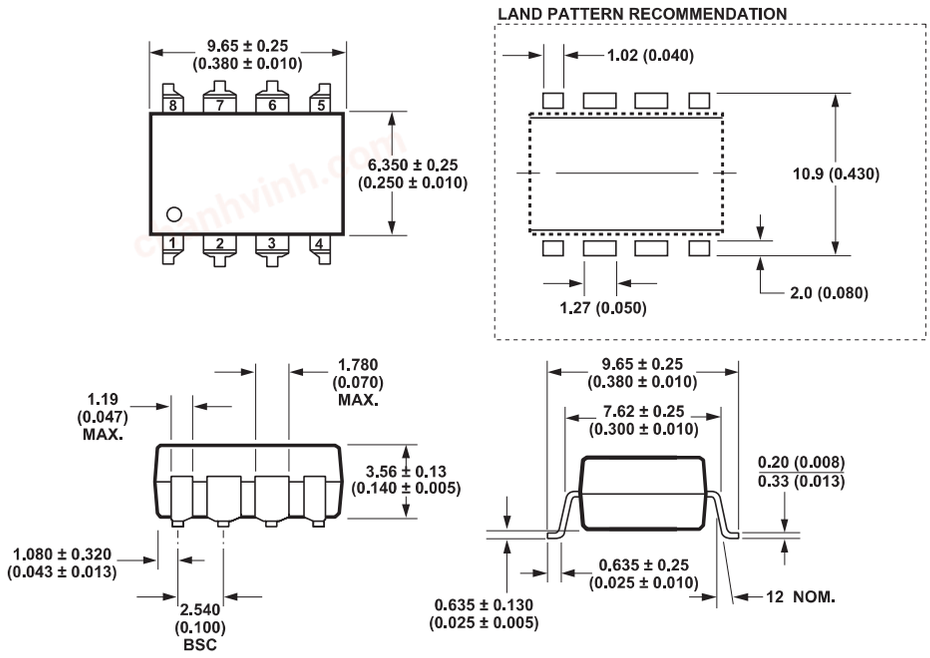
Figure 3: Gull Wing Surface-Mount Option #300 Package Device Outline Drawing



DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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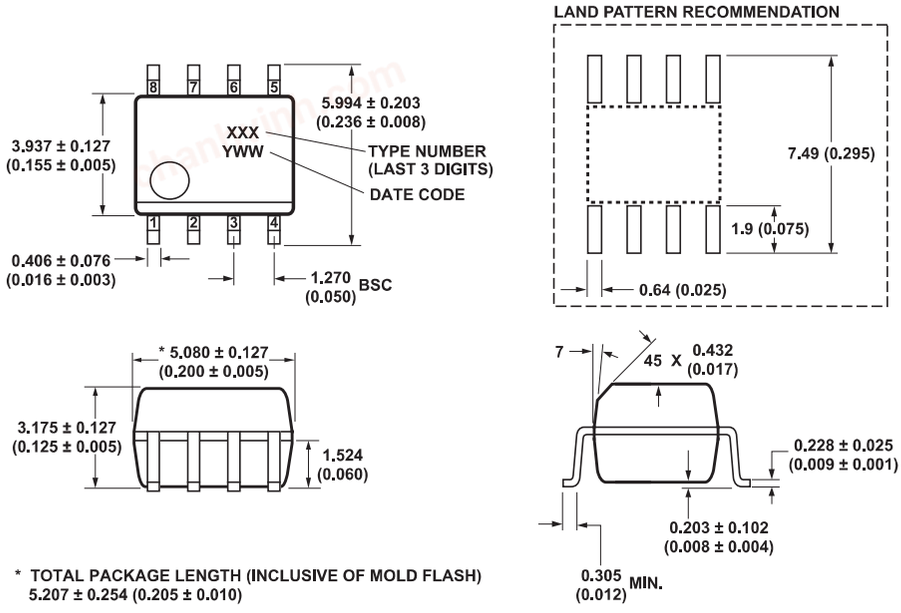
HCPL-061A/061N/063A/063N Outline Drawing

Figure 4: 8-Pin Small Outline Package Device Drawing



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The HCPL-261A and HCPL-261N families have been approved by the following organizations:

UL	Recognized under UL 1577, Component Recognition Program, File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.
IEC/EN/DIN EN 60747-5-5	

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Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	L (101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L (102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

NOTE: Option 300 – Surface-mount classification is Class A in accordance with CECC 00802.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[a]

Description	Symbol	PDIP Option 060	SO-8 Option 060	Unit
Installation classification per DIN VDE 0110, Table 1				
For Rated Mains Voltage ≤ 150 V_{rms}		I-IV	I-IV	
For Rated Mains Voltage ≤ 300 V_{rms}		I-IV	I-IV	
For Rated Mains Voltage ≤ 600 V_{rms}		I-III	I-III	
Climatic Classification		40/85/21	40/85/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	567	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m= 1s, Partial Discharge < 5 pC	V_{PR}	1181	1063	V_{peak}
Input to Output Test Voltage, Method a[a] V_{IOR}M × 1.6 = V_{PR}, Type and Sample Test, t_m= 10s, Partial Discharge < 5 pC	V_{PR}	1008	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	6000	6000	V_{peak}
Safety-Limiting Values – maximum values allowed in the event of a failure.				
Case Temperature	T_S	175	150	°C
Input Current	$I_{S, INPUT}$	230	150	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$\geq 10^9$	$\geq 10^9$	Ω

a. Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-5, for a detailed description.

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	–40	+85	°C	
Average Input Current	$I_{F(AVG)}$	—	10	mA	a
Reverse Input Voltage	V_R	—	3	V	
Supply Voltage	V_{CC}	–0.5	7	V	b
Enable Input Voltage	V_E	–0.5	5.5	V	
Output Collector Current (Each Channel)	I_O	—	50	mA	
Output Power Dissipation (Each Channel)	P_O	—	60	mW	c
Output Voltage (Each Channel)	V_O	–0.5	7	V	
Lead Solder Temperature (Through-Hole Parts Only)		260°C for 10s, 1.6-mm below seating plane.			
Solder Reflow Temperature Profile (Surface-Mount Parts Only)		See Package Outline Drawings section.			

a. Peaking circuits can be used, which produce transient input currents up to 30 mA, 50-ns maximum pulse width, provided the average current does not exceed 10 mA.

b. 1 minute maximum.

c. Derate linearly above 80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Input Voltage, Low Level	V_{FL}	–3	0.8	V
Input Current, High Level	I_{FH}	3.0	10	mA
Power Supply Voltage	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (at R_L = 1 kΩ)	N	—	5	TTL Loads
Output Pull-up Resistor	R_L	330	4k	Ω
Operating Temperature	T_A	–40	85	°C

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Electrical Specifications

Over recommended operating temperature (T_A = –40°C to +85°C) unless otherwise specified.
All typical values at T_A = 25°C, V_{CC} = 5V.

Parameter	Symbol	Device[a]	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		—	3.1	100	µA	V_{CC} = 5.5V, V_O = 5.5V, V_F = 0.8V, V_E = 2.0V	5	b
Low Level Output Voltage	V_{OL}		—	0.4	0.6	V	V_{CC} = 5.5V, I_{OL} = 13 mA (sinking), I_F = 3.0 mA, V_E = 2.0V	6, 9	b, c
High Level Supply Current	I_{CCH}	Single	—	7	10	mA	V_E = 0.5V, V_{CC} = 5.5V, I_F = 0 mA		c
		Dual	—	9	15	mA	V_{CC} = 5.5V, I_F = 0 mA		
Low Level Supply Current	I_{CCL}	Single	—	8	13	mA	V_E = 0.5V, V_{CC} = 5.5V, I_F = 3.0 mA		
		Dual	—	12	21	mA	V_{CC} = 5.5V, I_F = 3.0 mA		
High Level Enable Current	I_{EH}	Single	—	–0.6	–1.6	mA	V_{CC} = 5.5V, V_E = 2.0V		
Low Level Enable Current	I_{EL}	Single	—	–0.9	–1.6	mA	V_{CC} = 5.5V, V_E = 0.5V		
Input Forward Voltage	V_F		1.0	1.3	1.6	V	I_F = 4 mA	7	c
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		—	–1.25	—	mV/°C	I_F = 4 mA		c
Input Reverse Breakdown Voltage	BV_R		3	5	—	V	I_R = 100 µA		c
Input Capacitance	C_{IN}		—	60	—	pF	f = 1 MHz, V_F = 0V		

a. Single-channel products = HCPL-261A/261N/061A/061N only. Dual-channel products = HCPL-263A/263N/063A/063N only.

b. No external pull-up is required for a high logic state on the enable input of a single-channel product. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.

c. Each channel.

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Switching Specifications

Over recommended operating conditions (T_A = –40°C to +85°C) unless otherwise specified.
All typical values at T_A = 25°C, V_{CC} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Current Threshold High to Low	I_{THL}	—	1.5	3	mA	V_{CC} = 5.5V, V_O = 0.6V, I_O > 13 mA (sinking)	8, 11	a
Propagation Delay Time to High Output Level	t_{PLH}	—	52	100	ns	I_F = 3.5 mA, V_{CC} = 5.0V, V_E = Open, C_L = 15 pF, R_L = 350Ω	10, 12, 13	a, b, c
Propagation Delay Time to Low Output Level	t_{PHL}	—	53	100	ns		10, 12, 13	a, b, d
Pulse Width Distortion	PWD $\lvert t_{PHL} - t_{PLH} \rvert$	—	11	45	ns		10, 14	a, e
Propagation Delay Skew	t_{PSK}	—	—	60	ns		26	a, f
Output Rise Time	t_R	—	42	—	ns		10, 15	a, b
Output Fall Time	t_F	—	12	—	ns		10, 15	a, b
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{EHL}	—	19	—	ns	I_F = 3.5 mA, V_{CC} = 5.0V, V_{EL} = 0V, V_{EH} = 3V,	16, 17	g
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{ELH}	—	30	—	ns	C_L = 15 pF, R_L = 350Ω	16, 17	g

a. No external pull-up is required for a high logic state on the enable input of a single-channel product. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.

b. Each channel.

c. The t_{PLH} propagation delay is measured from the 1.75-mA point on the falling edge of the input pulse to the 1.5V point on the rising edge of the output pulse.

d. The t_{PHL} propagation delay is measured from the 1.75-mA point on the rising edge of the input pulse to the 1.5V point on the falling edge of the output pulse.

e. Pulse width distortion (PWD) is defined as the difference between t_{PLH} and t_{PHL} for any given device.

f. Propagation delay skew (t_{PSK}) is equal to the worst-case difference in t_{PLH} and/or t_{PHL} that will be seen between any two units under the same test conditions and operating temperature.

g. Single-channel products only (HCPL-261A/261N/061A/061N).

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Common Mode Transient Immunity Specifications

All values at T_A = 25°C.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	HCPL-261A HCPL-061A HCPL-263A HCPL-063A	1	5	—	kV/µs	V_{CM} = 50V V_{CC} = 5.0V, R_L = 350Ω, I_F = 0 mA, T_A = 25°C, $V_{O(MIN)}$ = 2V	18	a, b, c, d
		HCPL-261N HCPL-061N HCPL-263N HCPL-063N	1	5	—	kV/µs	V_{CM} = 1000V V_{CC} = 5V, R_L = 350Ω, I_F = 0 mA, T_A = 25°C, $V_{O(MIN)}$ = 2V		
			15	25	—	kV/µs	V_{CM} = 1000V Using Broadcom application circuit	21	a, b, c
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	HCPL-261A HCPL-061A HCPL-263A HCPL-063A	1	5	—	kV/µs	V_{CM} = 50V V_{CC} = 5.0V, R_L = 350Ω, I_F = 3.5 mA, T_A = 25°C, $V_{O(MAX)}$ = 0.8V	18	a, c, d, e
		HCPL-261N HCPL-061N HCPL-263N HCPL-063N	1	5	—	kV/µs	V_{CM} = 1000V V_{CC} = 5.0V, R_L = 350Ω, I_F = 3.5 mA, T_A = 25°C, $V_{O(MAX)}$ = 0.8V		
			15	25	—	kV/µs	V_{CM} = 1000V Using Broadcom application circuit	21	a, c, e

a. Each channel.

b. Common mode transient immunity in a Logic High level is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to ensure that the output will remain in a Logic High state (that is, V_O > 2.0V).

c. For sinusoidal voltages, $(|dV_{CM}|/dt)_{max} = \pi f_{CM} V_{CM(p-p)}$.

d. No external pull-up is required for a high logic state on the enable input of a single-channel product. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.

e. Common mode transient immunity in a Logic Low level is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to ensure that the output will remain in a Logic Low state (that is, V_O < 0.8V).

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Package Characteristics

All typical values at T_A = 25°C.

Parameter	Sym.	Package[a]	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage[b]	V_{ISO}		3750	—	—	V_{rms}	RH ≤ 50%, T_A = 25°C, t = 1 minute		c, d
		OPT 020[e]	5000	—	—				c, f
Input-Output Resistance	R_{I-O}		—	10^{12}	—	Ω	V_{I-O} = 500 Vdc		g, h
Input-Output Capacitance	C_{I-O}		—	0.6	—	pF	f = 1 MHz, T_A = 25°C		g, h
Input-Input Insulation Leakage Current	I_{I-I}	Dual Channel	—	0.005	—	μA	RH ≤ 45%, t = 5s, V_{I-I} = 500V		i
Resistance (Input-Input)	R_{I-I}	Dual Channel	—	10^{11}	—	Ω			i
Capacitance (Input-Input)	C_{I-I}	Dual 8-Pin Dip	—	0.03	—	pF	f = 1 MHz		i
		Dual SO-8	—	0.25	—				

a. Ratings apply to all devices except otherwise noted in the Package column

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), your equipment level safety specification.

c. The device is considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.

d. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 4500 V_{rms} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.

e. For 8-pin DIP package devices (HCPL-261A/261N/263A/263N) only.

f. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).

g. Each channel.

h. Measured between the LED anode and cathode shorted together, and pins 5 through 8 shorted together.

i. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual-channel products only.

Figure 5: Typical High Level Output Current vs. Temperature

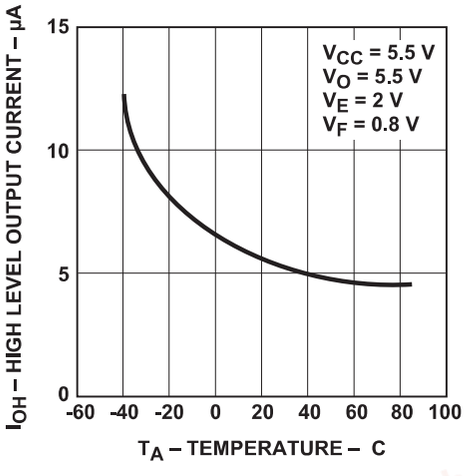

Figure 6: Low Level Output Current vs. Temperature

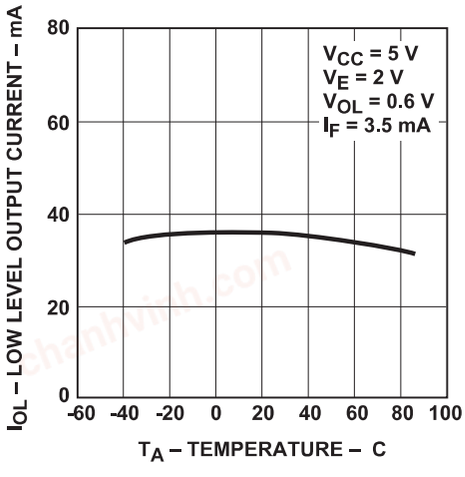

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Figure 7: Typical Diode Input Forward Current Characteristic

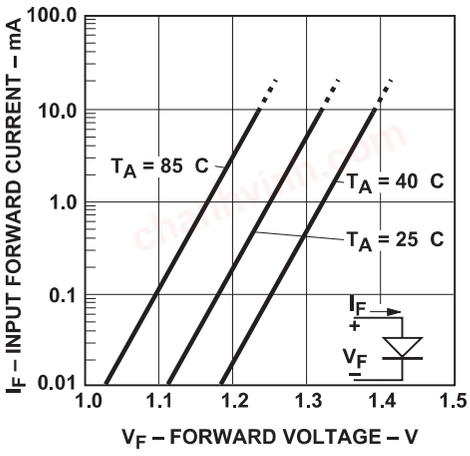

Figure 8: Typical Output Voltage vs. Forward Input Current

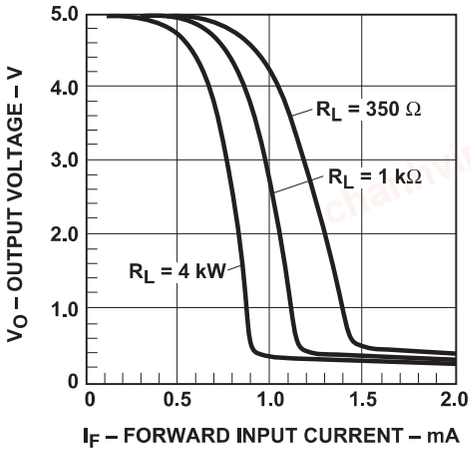

Figure 9: Typical Low Level Output Voltage vs. Temperature

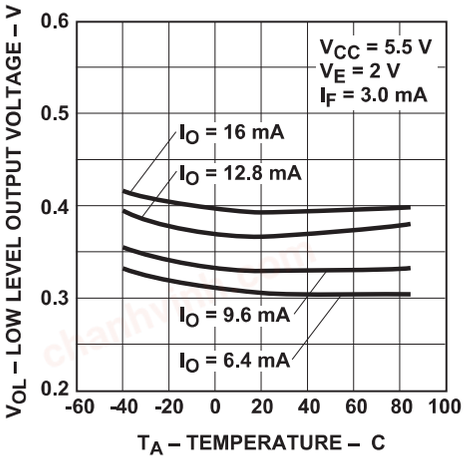

Figure 10: Test Circuit for t_{PHL} and t_{PLH}

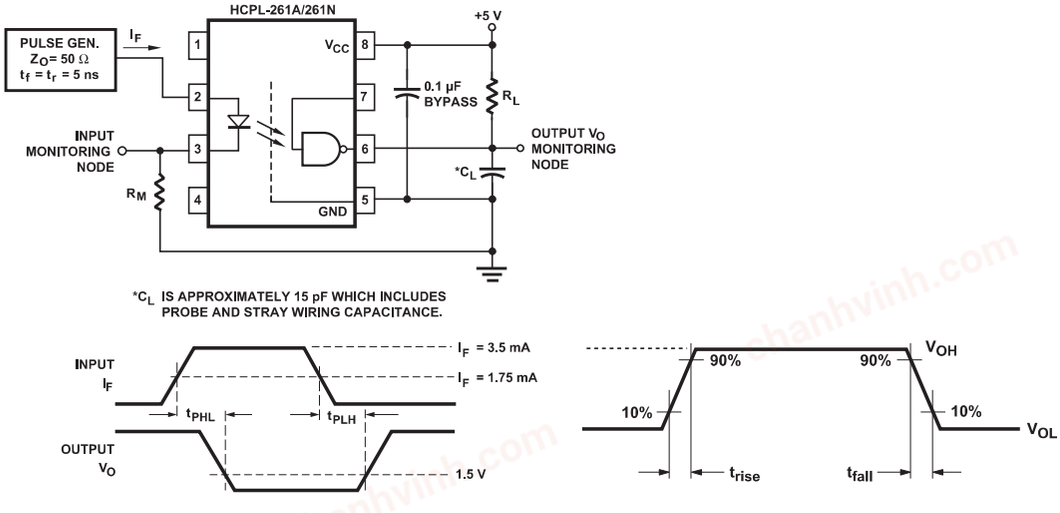

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Figure 11: Typical Input Threshold Current vs. Temperature

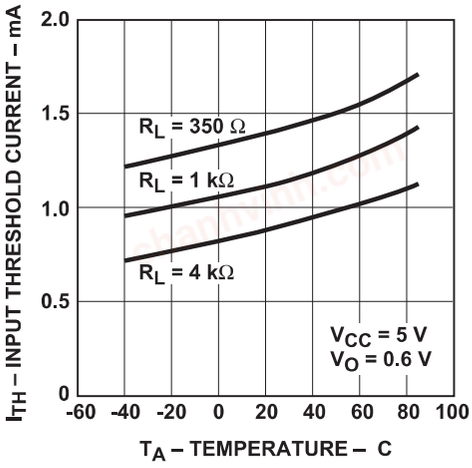

Figure 12: Typical Propagation Delay vs. Temperature

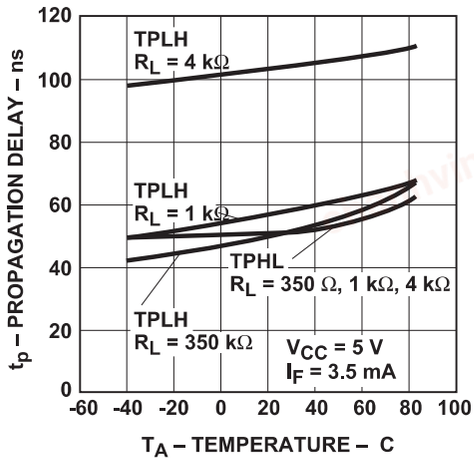

Figure 13: Typical Propagation Delay vs. Pulse Input Current

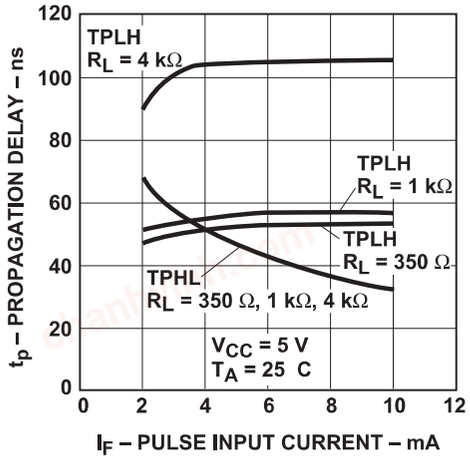

Figure 14: Typical Pulse Width Distortion vs. Temperature

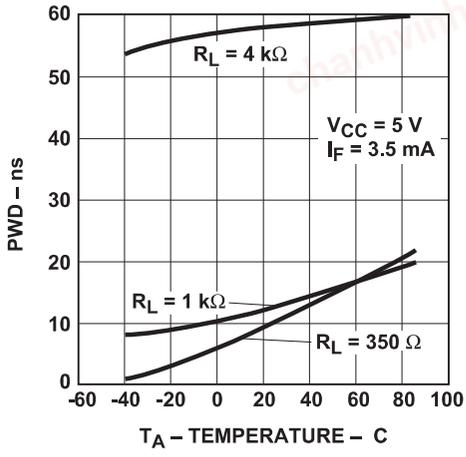

Figure 15: Typical Rise and Fall Time vs. Temperature

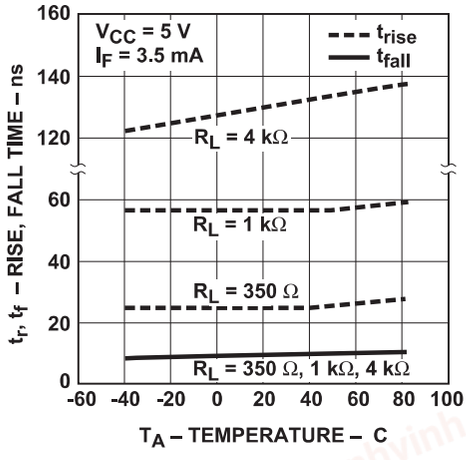

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Figure 16: Test Circuit for t_{EHL} and t_{ELH}

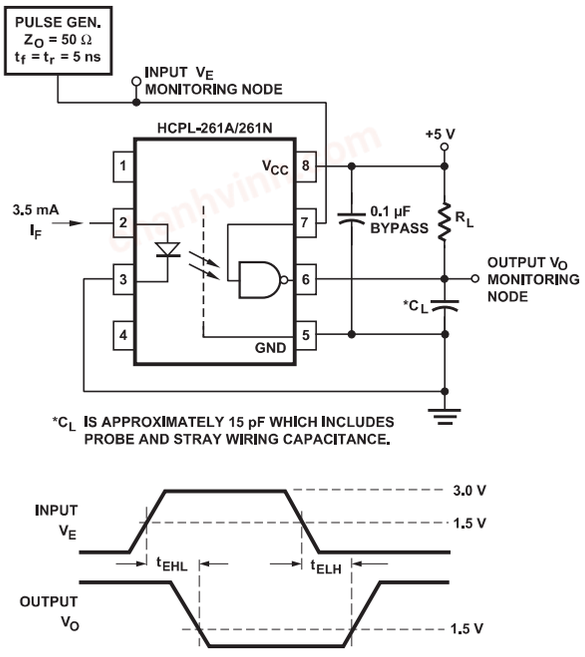

Figure 17: Typical Enable Propagation Delay vs. Temperature (HCPL-261A/-261N/-061A/-061N Only)

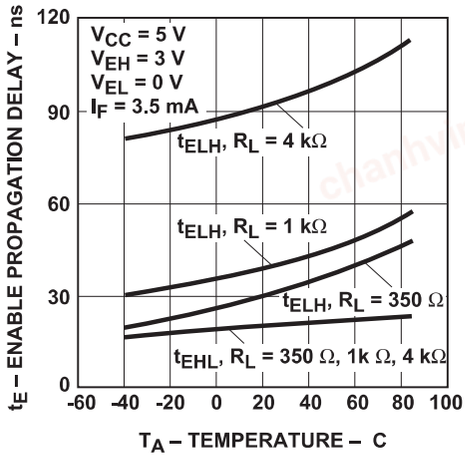

Figure 18: Test Circuit for Common Mode Transient Immunity and Typical Waveforms

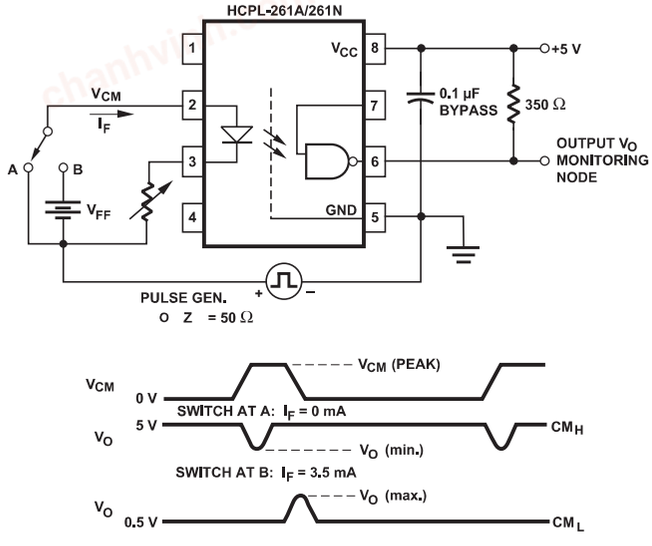

Figure 19: Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-5

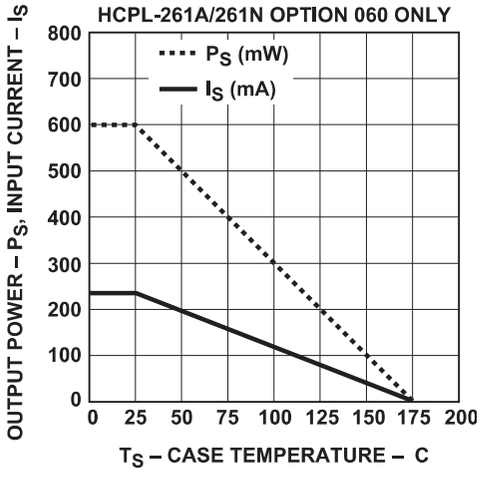

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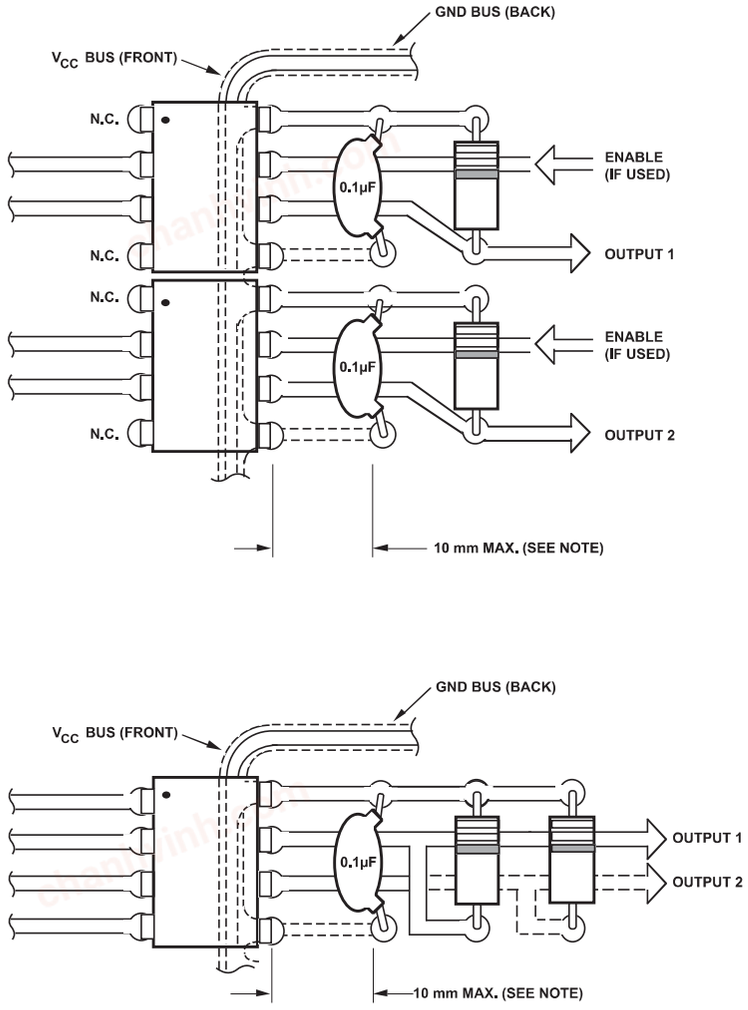
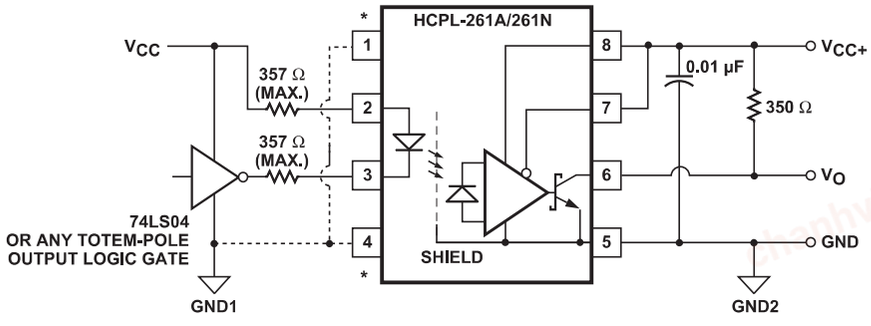
Figure 20: Recommended Printed Circuit Board Layout



Note: Bypassing of the power supply line is required with a 0.1-μF ceramic disc capacitor adjacent to each optocoupler as shown in Figure 20. The total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.

Figure 21: Recommended Drive Circuit for HCPL-261A/-261N Families for High-CMR (Similar for HCPL-263A/-263N)



* HIGHER CMR MAY BE OBTAINABLE BY CONNECTING PINS 1, 4 TO INPUT GROUND (GND1).

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Application Information

Common-Mode Rejection for HCPL-261A/HCPL-261N Families

Figure 21 shows the recommended drive circuit for the HCPL-261N/-261A for optimal common-mode rejection performance. Note the following two points:

- The enable pin is tied to V_{CC} rather than floating (this applies to single-channel parts only).
- Two LED-current setting resistors are used instead of one. This is to balance I_{LED} variation during common-mode transients.

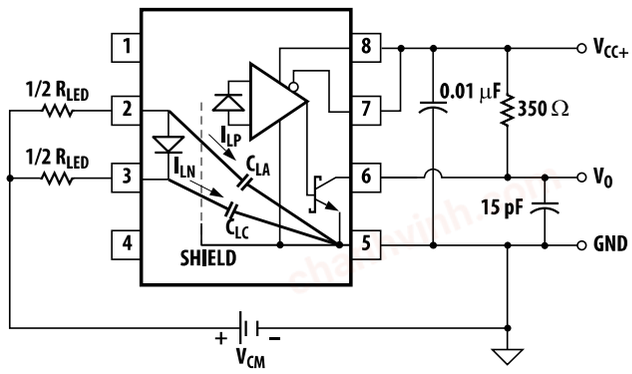
If the enable pin is left floating, it is possible for common-mode transients to couple to the enable pin, resulting in common-mode failure. This failure mechanism only occurs when the LED is on and the output is in the Low state. It is identified as occurring when the transient output voltage rises above 0.8V. Therefore, the enable pin should be connected to either V_{CC} or logic-level high for best common-mode performance with the output low (CMR_L). This failure mechanism is only present in single-channel parts (HCPL-261N, -261A, -061N, -061A) that have the enable function.

Also, common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which can be bad if the LED is on) or conversely cause current to be injected into the LED (bad if the LED is meant to be off). Figure 22 shows the parasitic capacitances that exist between LED anode/cathode and output ground (C_{LA} and C_{LC}). Also shown in Figure 22 on the input side is an AC-equivalent circuit.

Table 1 indicates the directions of I_{LP} and I_{LN} flow depending on the direction of the common-mode transient.

For transients occurring when the LED is on, common-mode rejection (CMR_L, since the output is in the *low* state) depends on the amount of LED current drive (I_F). For conditions where I_F is close to the switching threshold (I_{TH}), CMR_L also depends on the extent that I_{LP} and I_{LN} balance each other. In other words, any condition where common-mode transients cause a momentary decrease in I_F (that is, when $dV_{CM}/dt > 0$ and $|I_{FP}| > |I_{FN}|$, referring to Table 1) will cause common-mode failure for transients that are fast enough.

Figure 22: AC Equivalent Circuit



Likewise, for common-mode transients that occur when the LED is off (that is, CMR_H, since the output is *high*), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient *signal* may cause the output to drop below 2V (which constitutes a CMR_H failure).

By using the recommended circuit in Figure 21, good CMR can be achieved. (In the case of the -261N families, a minimum CMR of 15 kV/µs is achieved using this circuit.) The balanced I_{LED}-setting resistors help equalize I_{LP} and I_{LN} to reduce the amount by which I_{LED} is modulated from transient coupling through C_{LA} and C_{LC}.

Table 1: Effects of Common Mode Pulse Direction on Transient I_{LED}

If dV_{CM}/dt Is:	Then I_{LP} Flows:	And I_{LN} Flows:	If $\|I_{LP}\| < \|I_{LN}\|$, LED I_F Current Is Momentarily:	If $\|I_{LP}\| > \|I_{LN}\|$, LED I_F Current Is Momentarily:
Positive (>0)	Away from LED anode through C_{LA}	Away from LED cathode through C_{LC}	Increased	Decreased
Negative (<0)	Toward LED anode through C_{LA}	Toward LED cathode through C_{LC}	Decreased	Increased

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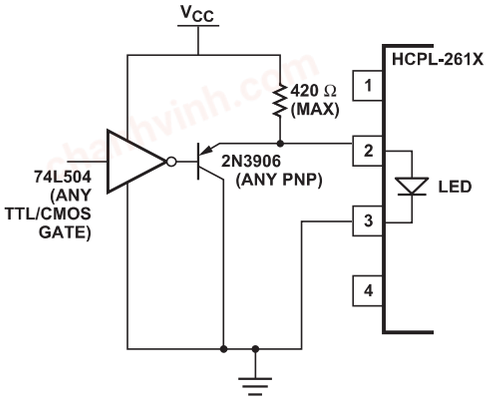
CMR with Other Drive Circuits

CMR performance with drive circuits other than that shown in Figure 21 may be enhanced by following these guidelines:

- Use of drive circuits where current is shunted from the LED in the LED *off* state (as shown in Figure 23 and Figure 24). This beneficial for good CMR_H.
- Use of I_{FH} > 3.5 mA. This is good for high CMR_L.

Using any one of the drive circuits in Figure 23 to Figure 25 with I_F = 10 mA will result in a typical CMR of 8 kV/µs for the HCPL-261N family, as long as the PC board layout practices are followed. Figure 23 shows a circuit that can be used with any totem-pole-output TTL/LSTTL/HCMOS logic gate. The buffer PNP transistor allows the circuit to be used with logic devices that have low current-sinking capability. It also helps maintain the driving-gate power-supply current at a constant level to minimize ground shifting for other devices connected to the input-supply ground.

Figure 23: TTL Interface Circuit for the HCPL-261A/-261N Families



When using an open-collector TTL or open-drain CMOS logic gate, the circuit in Figure 24 may be used. When using a CMOS gate to drive the optocoupler, the circuit shown in Figure 25 may be used. The diode in parallel with the R_{LED} speeds the turn-off of the optocoupler LED.

Figure 24: TTL Open-Collector/Open-Drain Gate Drive Circuit for HCPL-261A/-261N Families.

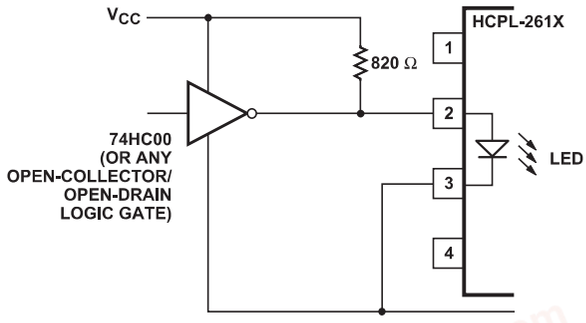
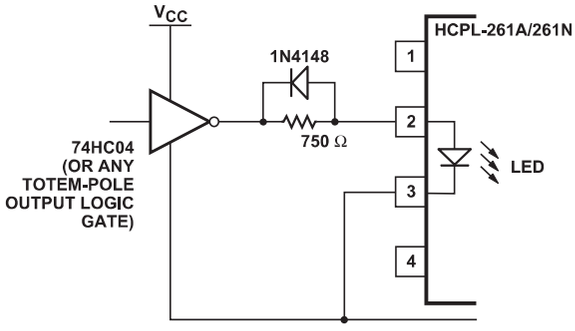


Figure 25: CMOS Gate Drive Circuit for HCPL-261A/-261N Families



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Propagation Delay, Pulse-Width Distortion, and Propagation Delay Skew

Propagation delay is a figure of merit that describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 10).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20% to 30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, and so on).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delay is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers that are operating under the same conditions (that is, the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 26, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 27 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers.

The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 27 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap; otherwise, the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature, input current, and power supply ranges.

Figure 26: Illustration of Propagation Delay Skew – t_{PSK}

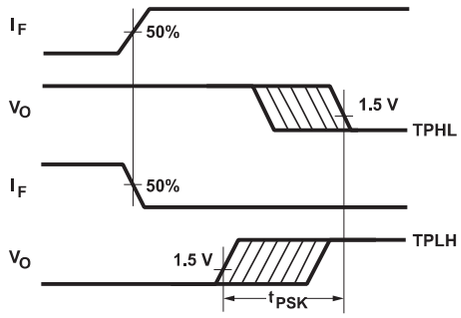
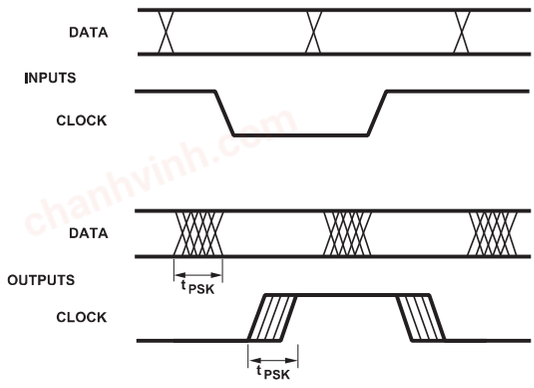


Figure 27: Parallel Data Transmission Example



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