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HCPL-260L/060L/263L/063L

High Speed LVTTL Compatible 3.3 V Optocouplers

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

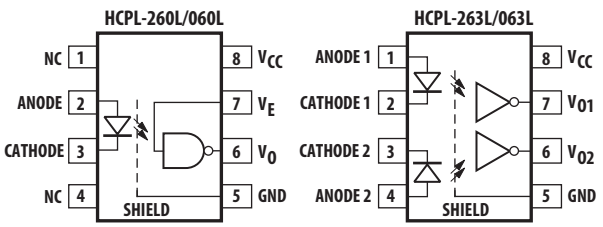
Description

The HCPL-260L/060L/263L/063L are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 15 kV/µs at 3.3V.

This unique design provides maximum AC and DC circuit isolation while achieving LVTTL/LVCMOS compati-bility. The optocoupler AC and DC operational parameters are guaranteed from –40 °C to +85 °C allowing trouble-free system performance.

These optocouplers are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Functional Diagram



Truth Table (Positive Logic)

LED	Enable	Output
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

Truth Table (Positive Logic)

LED	Output
ON	L
OFF	H

Features

- 3.3V/5V Dual Supply Voltages
- Low power consumption
- 15 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V
- High speed: 15 MBd typical
- LVTTL/LVCMOS compatible
- Low input current capability: 5 mA
- Guaranteed AC and DC performance over temperature: –40 °C to +85 °C
- Available in 8-pin DIP, SOIC-8
- Strobable output (single channel products only)
- Safety approvals: UL, CSA, IEC/EN/DIN EN 60747-5-5

Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Field buses

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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Ordering Information

HCPL-xxxx is UL Recognized with 3750 Vrms for 1 minute per UL1577

Part number	Option RoHS Compliant	Option Non RoHS Compliant	Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
HCPL-260L	-000E	No option	300mil DIP-8						50 per tube
	-300E	-300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	-020					X		50 per tube
	-320E	-320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-263L	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	-320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	-060						X	50 per tube
	-560E	-560		X	X	X		X	1000 per reel
HCPL-060L	-000E	No option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
	-060E	#060		X				X	100 per tube
	-560E	-560		X		X		X	1500 per reel
HCPL-063L	-000E	No option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
	-060E	-060		X				X	100 per tube
	-560E	-560		X		X		X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry. Combination of Option 020 and Option 060 is not available.

Example 1:

HCPL-260L-560E to order product of 300mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

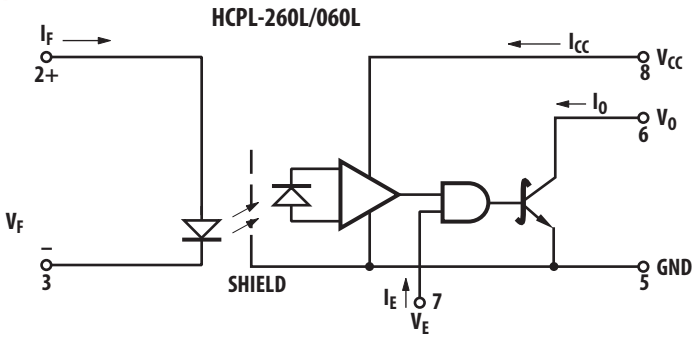
HCPL-263L to order product of 300mil DIP package in tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

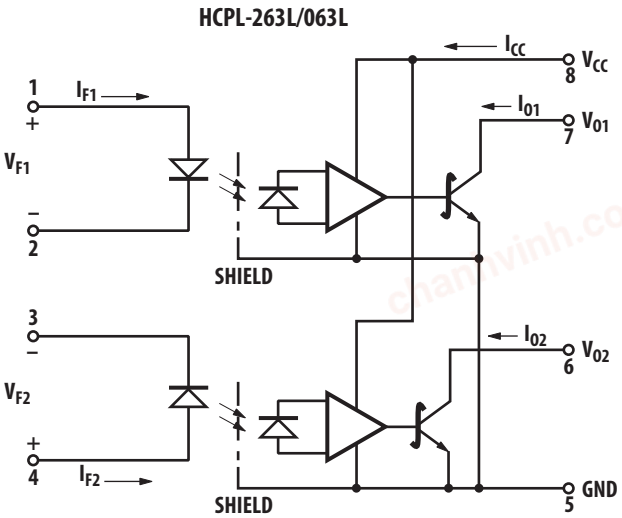
Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

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Schematic

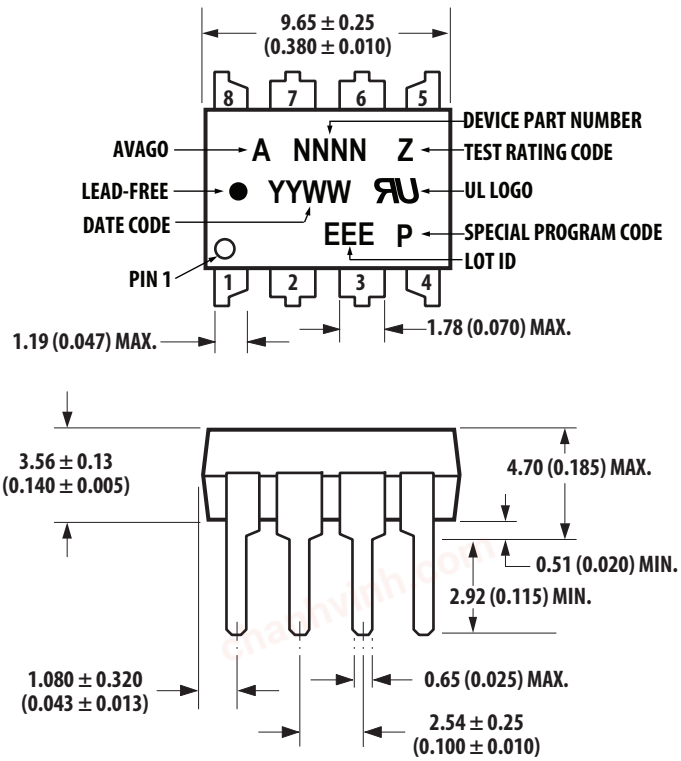


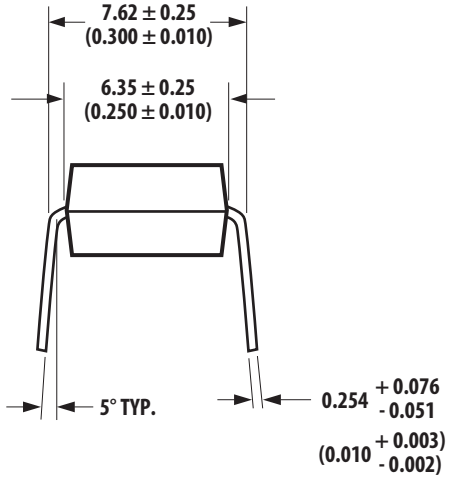
USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 5).



Package Outline Drawings

8-Pin DIP Package





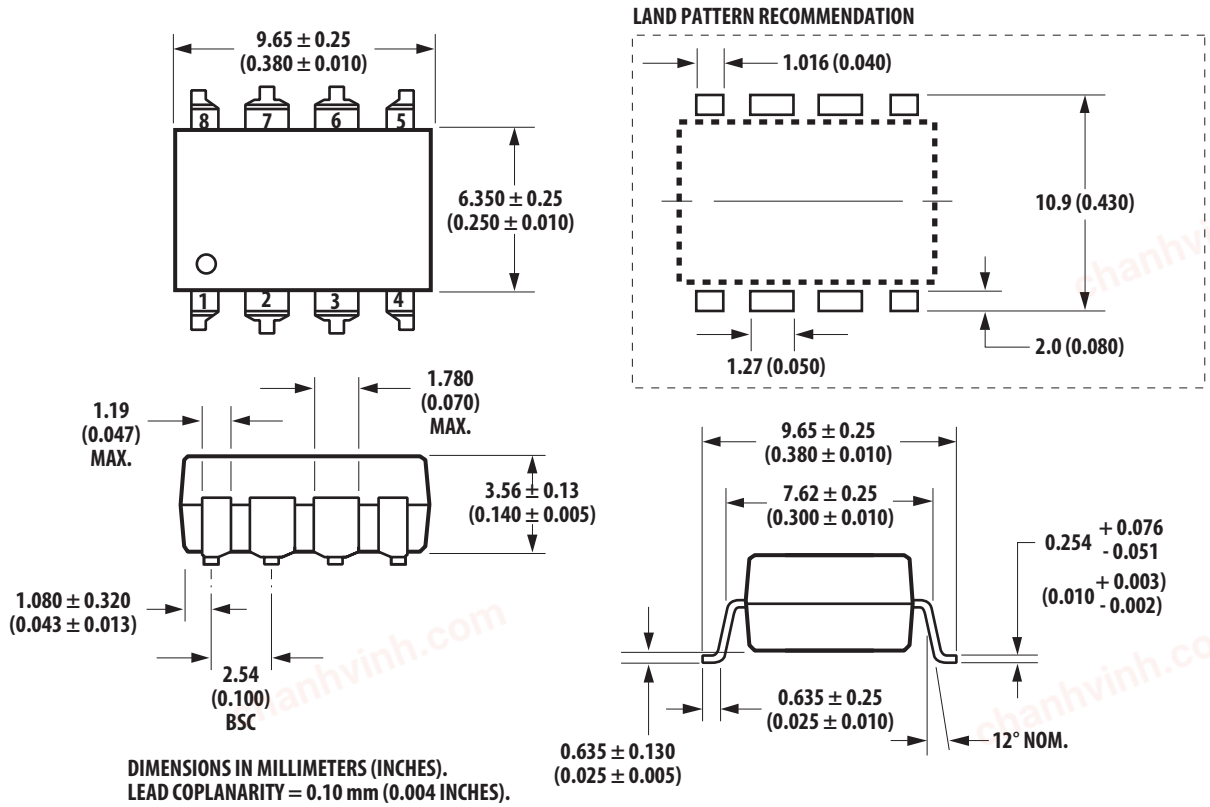
DIMENSIONS IN MILLIMETERS (INCHES).

*MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

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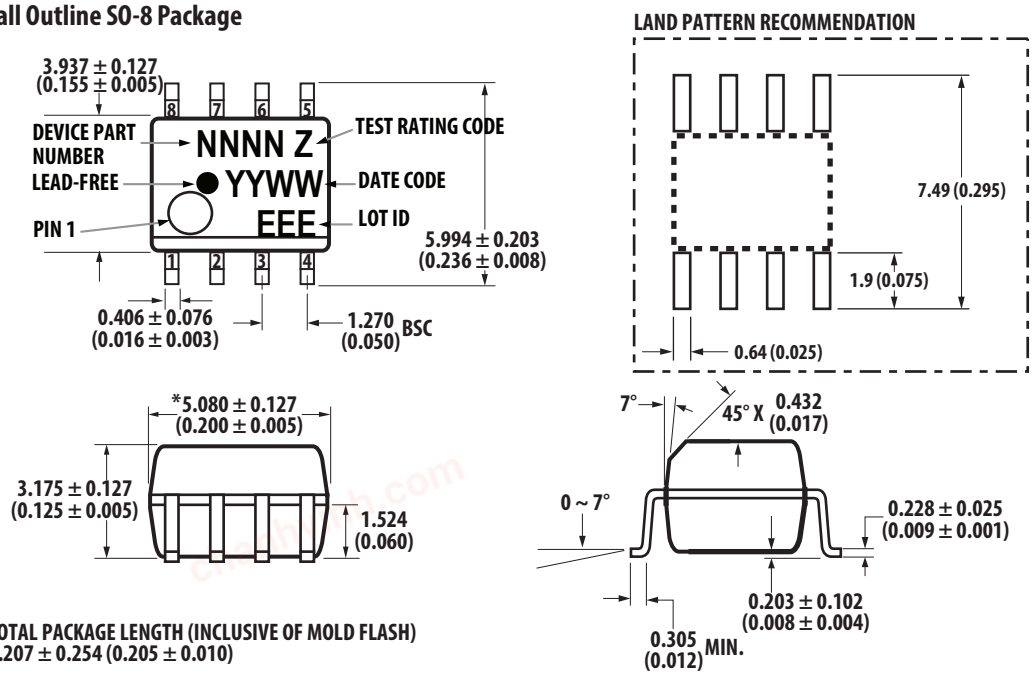
8-Pin DIP Package with Gull Wing Surface Mount in Option 500 (HCPL-260L, HCPL-263L)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Small Outline SO-8 Package



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

OPTION NUMBER 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Test Rating Code, Z	Optional Identification Code
L – Option x2x	A – Avago
V – Option x5x or x6x	– UL Logo
	P – Special Program Code

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Reflow Soldering Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The HCPL-260L/060L/263L/063L have been approved by the following organizations:

UL

Approval under UL 1577, Component Recognition Program, File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L (101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L (102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

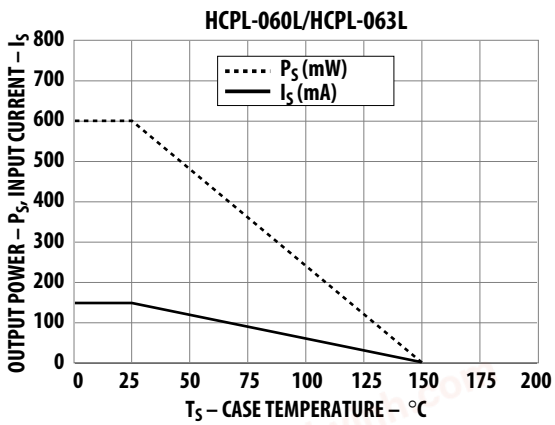
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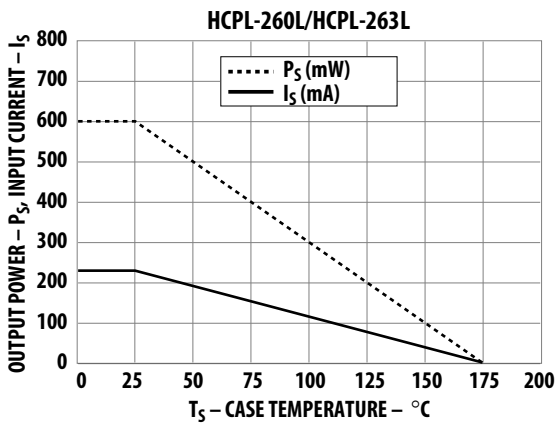
IEC/EN/DIN EN 60747-5-5 Insulation Characteristics*

Description	Symbol	PDIP Option 060	SO-8 Option 060	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 150 Vrms for rated mains voltage ≤ 300 Vrms for rated mains voltage ≤ 600 Vrms		 I – IV I – IV I – III	 I – IV I – IV I – III	
Climatic Classification		40/85/21	40/85/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	567	Vpeak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1181	1063	Vpeak
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1008	907	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	6000	Vpeak
Safety-limiting values – maximum values allowed in the event of a failure.				
Case Temperature	T_S	175	150	°C
Input Current	$I_{S, INPUT}$	230	150	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-5, for a detailed description.
Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Thermal Derating Curve Figures





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Absolute Maximum Ratings (No Derating Required up to 85 °C)

Parameter	Symbol	Package**	Min.	Max.	Units	Note
Storage Temperature	T_S		–55	125	°C	
Operating Temperature†	T_A		–40	85	°C	
Average Forward Input Current	I_F	Single 8-Pin DIP Single SO-8		20	mA	2
		Dual 8-Pin DIP Dual SO-8		15		1, 3
Reverse Input Voltage	V_R	8-Pin DIP, SO-8		5	V	1
Input Power Dissipation	P_I			40	mW	
Supply Voltage (1 Minute Maximum)	V_{CC}			7	V	
Enable Input Voltage (Not to Exceed V_{CC} by more than 500 mV)	V_E	Single 8-Pin DIP Single SO-8		V_{CC} + 0.5	V	
Enable Input Current	I_E			5	mA	
Output Collector Current	I_O			50	mA	1
Output Collector Voltage	V_O			7	V	1
Output Collector Power Dissipation	P_O	Single 8-Pin DIP Single SO-8		85	mW	
		Dual 8-Pin DIP Dual SO-8		60		1, 4

**Ratings apply to all devices except otherwise noted in the Package column.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	µA
Input Current, High Level[1]	I_{FH}**	5	15	mA
Power Supply Voltage	V_{CC}	2.7 4.5	3.6 5.5	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Operating Temperature	T_A	–40	85	°C
Fan Out (at R_L = 1 kΩ)[1]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

*The off condition can also be guaranteed by ensuring that $V_{FL} \le 0.8$ V.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.

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Electrical Specifications

Over Recommended Operating Conditions (T_A = –40 °C to +85 °C , 2.7 V ≤ V_{CC} ≤ 3.6 V), unless otherwise specified. All Typicals at V_{CC} = 3.3 V, T_A = 25 °C. All enable test conditions apply to single channel products only. See Note 5.

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*			4.5	50	µA	V_{CC} = 3.3 V, V_E = 2.0 V, V_O = 3.3 V, I_F = 250 µA	1	1, 15
Input Threshold Current	I_{TH}			3.0	5.0	mA	V_{CC} = 3.3 V, V_E = 2.0 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2	15
Low Level Output Voltage	V_{OL}*			0.35	0.6	V	V_{CC} = 3.3 V, V_E = 2.0 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	3	15
High Level Supply Current	I_{CCH}	Single		4.7	7.0	mA	V_E = 0.5 V, I_F = 0 mA		
		Dual		6.9	10.0		V_{CC} = 3.3 V		
Low Level Supply Current	I_{CCL}	Single		7.0	10.0	mA	V_E = 0.5 V, I_F = 10 mA		
		Dual		8.7	15.0		V_{CC} = 3.3 V		
High Level Enable Current	I_{EH}	Single		–0.5	–1.2	mA	V_{CC} = 3.3 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*	Single		–0.5	–1.2	mA	V_{CC} = 3.3 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	Single	2.0			V			15
Low Level Enable Voltage	V_{EL}	Single			0.8	V			
Input Forward Voltage	V_F		1.4	1.5	1.75*	V	T_A = 25 °C, I_F = 10 mA	5	1
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 µA		1
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$			–1.6		mV°C	I_F = 10 mA		1
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V		1

*The JEDEC Registration specifies 0 °C to +70 °C. Avago specifies –40 °C to +85 °C.

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Electrical Specifications (DC)

Over recommended operating conditions (T_A = -40 °C to +85 °C, 4.5 V ≤ V_{DD} ≤ 5.5 V), unless otherwise specified. All typicals at V_{CC} = 5 V, T_A = 25 °C.

Parameter	Symbol	Channel	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}			5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_{FL} = 250 µA	1	1,15
Input Threshold Current	I_{TH}	Single		2.0	5.0	mA	V_{CC} = 5.5 V, V_O = 0.6 V, I_{OL} > 13 mA	2	15
		Dual		2.5					
Low Level Output Voltage	V_{OL}			0.35	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, I_{OL}(Sinking) = 13 mA	3	15
High Level Supply Current	I_{CCH}	Single		7.0	10.0	mA	V_E =0.5V, V_{CC} = 5.5 V, I_F = 0 mA		
				6.5		mA	V_E =V_{CC}, V_{CC} = 5.5 V, I_F = 0 mA		
		Dual		10.0	15.0		V_{CC} = 5.5 V, I_F = 0 mA		
Low Level Supply Current	I_{CCL}	Single		9.0	13.0	mA	V_E =0.5 V, V_{CC} = 5.5 V, I_F = 10 mA		
				8.5		mA	V_E =V_{CC}, V_{CC} = 5.5 V, I_F = 10 mA		
		Dual		13.0	21.0	mA	V_{CC} = 5.5 V, I_F = 10 mA		
High Level Enable Current	I_{EH}	Single		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0V		
Low Level Enable Current	I_{EL}	Single		-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5V		
High Level Enable Voltage	V_{EH}	Single	2.0			V			15
Low Level Enable Voltage	V_{EL}	Single			0.8	V			
Input Forward Voltage	V_F		1.4	1.5	1.75	V	T_A = 25 °C, I_F = 10 mA		5
			1.3		1.8	V	I_F =10 mA		
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		1
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$			-1.6		mV/°C	I_F = 10 mA		1
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V		1

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Switching Specifications

Over Recommended Operating Conditions (T_A = –40 °C to +85 °C, 2.7 V ≤ V_{CC} ≤ 3.6 V), I_F = 7.5 mA, unless otherwise specified. All Typicals at T_A = 25 °C, V_{CC} = 3.3 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}			90	ns	R_L = 350 Ω C_L = 15 pF	6, 7	1, 6, 15
Propagation Delay Time to Low Output Level	t_{PHL}			75	ns	R_L = 350 Ω C_L = 15 pF		1, 7, 15
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$			25	ns	R_L = 350 Ω C_L = 15 pF	8	9, 15
Propagation Delay Skew	t_{PSK}			40	ns	R_L = 350 Ω C_L = 15 pF		8, 9, 15
Output Rise Time (10-90%)	t_r		45		ns	R_L = 350 Ω C_L = 15 pF		1, 15
Output Fall Time (90-10%)	t_f		20		ns	R_L = 350 Ω C_L = 15 pF		1, 15
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		45		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	9	10
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	9	11

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Switching Specifications (AC)

Over recommended operating conditions T_A = -40 °C to 85 °C, 4.5 V ≤ Vcc ≤ 5.5 V, I_F = 7.5 mA, unless otherwise specified. All typicals at V_{CC} = 5 V, T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	20	48	75 100	ns	T_A = 25°C, R_L = 350 Ω, C_L = 15 pF	6,7	1,6,15
Propagation Delay Time to Low Output Level	t_{PHL}	25	50	75 100	ns	T_A = 25°C, R_L = 350 Ω, C_L = 15 pF	6, 7	1,7, 15
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$		3.5	35	ns	R_L = 350 Ω, C_L = 15 pF	8	9, 15
Propagation Delay Skew	T_{PSK}			40	ns	R_L = 350 Ω, C_L = 15 pF		8,9, 15
Output Rise Time (10%-90%)	t_r		24		ns	R_L = 350 Ω, C_L = 15 pF		1,15
Output Fall Time (10%-90%)	t_f		10		ns	R_L = 350 Ω, C_L = 15 pF		1, 15
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} =0 V, V_{EH} =3 V	9	10
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		20		ns	R_L = 350Ω, C_L = 15 pF, V_{EL} =0 V, V_{EH} =3 V	9	11

Parameter	Symbol	Device	Min.	Typ.	Units	Test Conditions	Fig.	Note
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	HCPL-263L HCPL-063L HCPL-260L HCPL-060L	15	25	kV/µs	V_{CC} = 3.3 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25 °C, V_{CM} = 1000 V and V_{CM} = 10V	10	12, 14, 15
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	HCPL-263L HCPL-063L HCPL-260L HCPL-060L	15	25	kV/µs	V_{CC} = 3.3 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25 °C, V_{CM} = 1000 V and V_{CM} = 10V	10	13, 14, 15
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	HCPL-263L HCPL-063L HCPL-260L HCPL-060L	10	15	kV/µs	V_{CC} = 5 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25 °C, V_{CM} = 1000 V	10	12, 14, 15
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	HCPL-263L HCPL-063L HCPL-260L HCPL-060L	10	15	kV/µs	V_{CC} = 5 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25 °C, V_{CM} = 1000 V	10	13, 14, 15

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Package Characteristics

All Typicals at T_A = 25 °C.

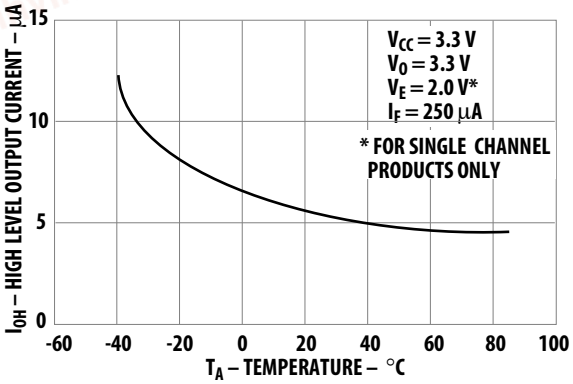
Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Insulation	I_{I-O}*	Single 8-Pin DIP Single SO-8			1	µA	45% RH, t = 5 s, V_{I-O} = 3 kV DC, T_A = 25 °C		16, 17
Input-Output Momentary Withstand Voltage**	V_{ISO}	8-Pin DIP, SO-8	3750			Vrms	RH ≤ 50%, t = 1 min, T_A = 25 °C		16, 17
Input-Output Resistance	R_{I-O}	8-Pin, SO-8		10^{12}		Ω	V_{I-O} =500 V_{dc}		1, 16, 19
Input-Output Capacitance	C_{I-O}	8-Pin DIP, SO-8		0.6		pF	f = 1 MHz, T_A = 25 °C		1, 16, 19
Input-Input Insulation Leakage Current	I_{I-I}	Dual Channel		0.005		µA	RH ≤ 45%, t = 5 s, V_{I-I} = 500 V		20
Resistance (Input-Input)	R_{I-I}	Dual Channel		10^{11}		Ω			20
Capacitance (Input-Input)	C_{I-I}	Dual 8-Pin Dip Dual SO-8		0.03 0.25		pG	f = 1 MHz		20

*The JEDEC Registration specifies 0 °C to +70 °C. Avago specifies –40 °C to +85 °C.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Each channel.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
4. Derate linearly above +80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.
5. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 11. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
6. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
8. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
9. See test circuit for measurement details.
10. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
11. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
12. CM_H is the maximum tolerable rate of rise on the common mode voltage to assure that the output will remain in a high logic state (i.e., V_o > 2.0 V).
13. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_o < 0.8 V).
14. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM}$ (p-p).
15. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance. For single channel products only. See application information provided.
16. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
17. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 Vrms for one second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
18. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for one second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
19. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together. For dual channel products only.
20. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual channel products only.

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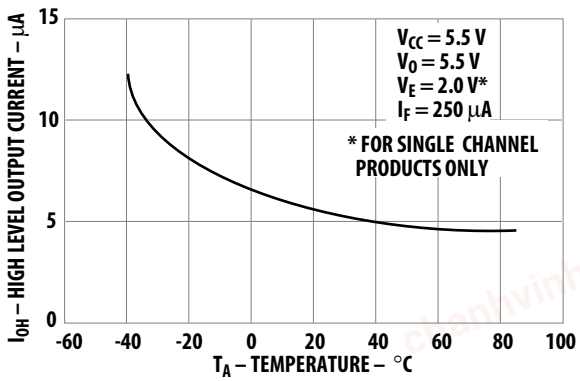
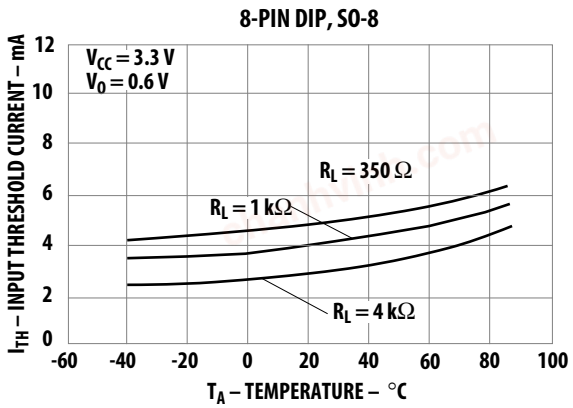


Figure 1. Typical high level output current vs. temperature



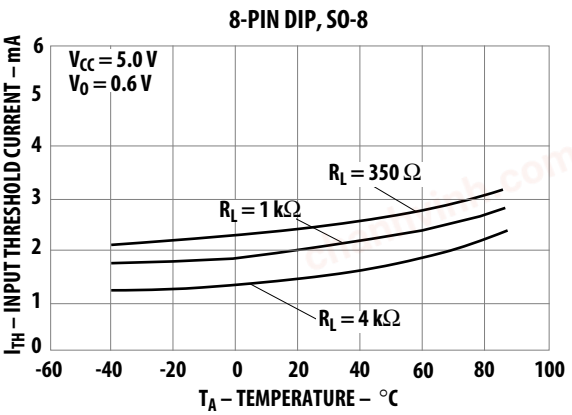
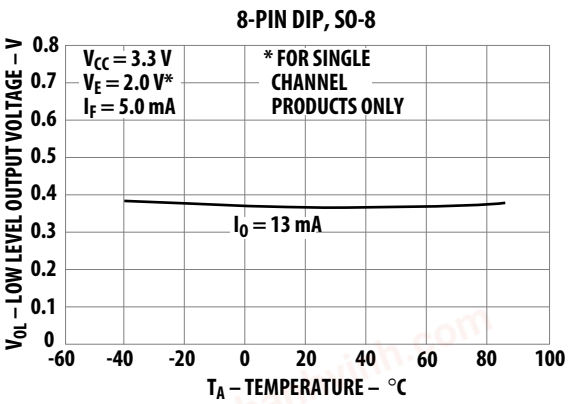


Figure 2. Typical output voltage vs. forward input current



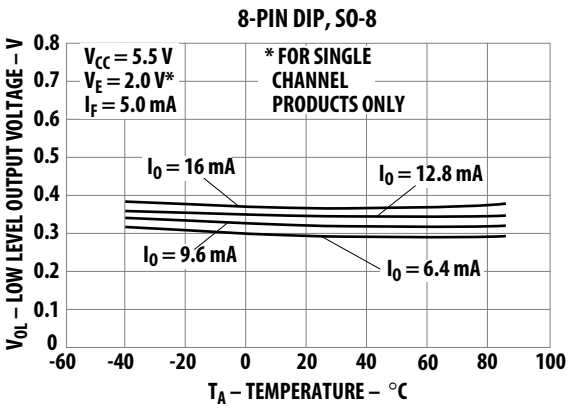


Figure 3. Typical low level output voltage vs. temperature

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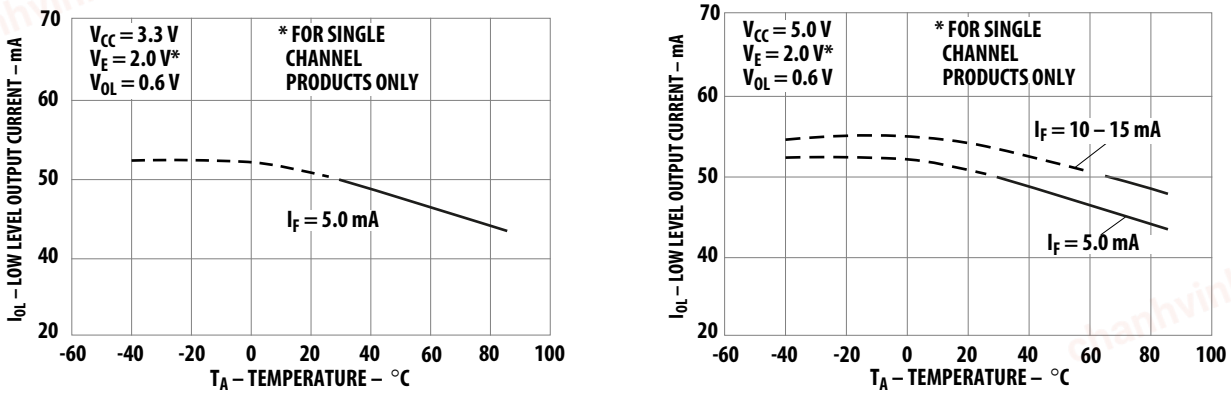


Figure 4. Typical low level output current vs. temperature

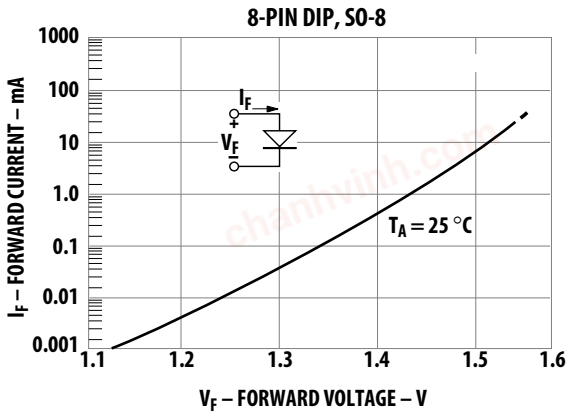


Figure 5. Typical input diode forward characteristic

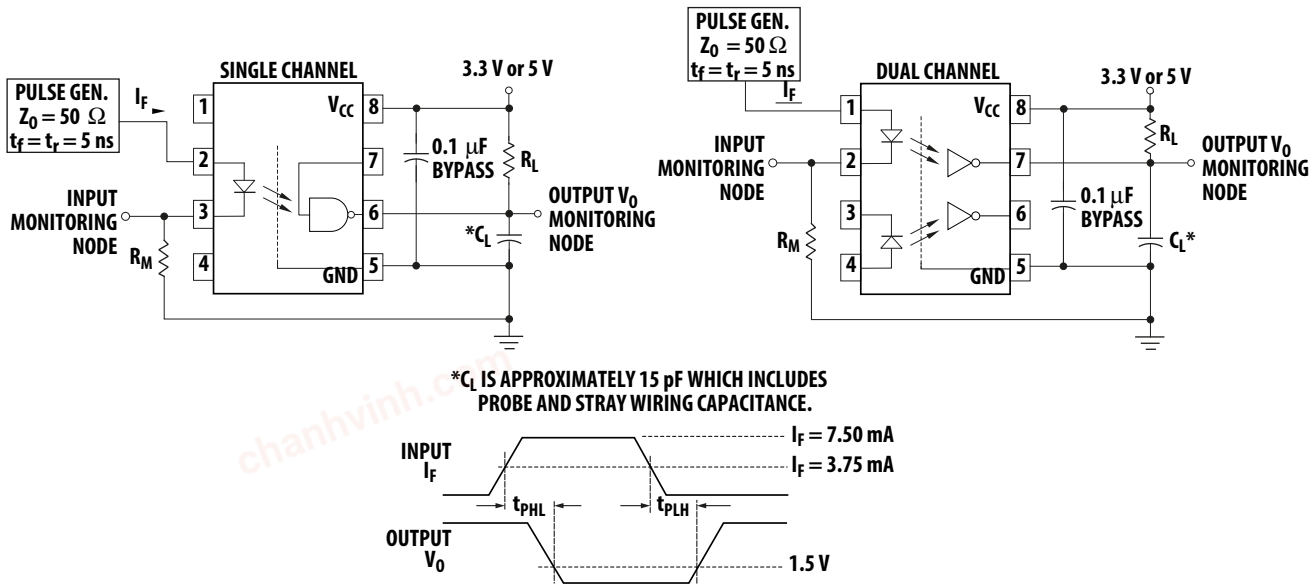
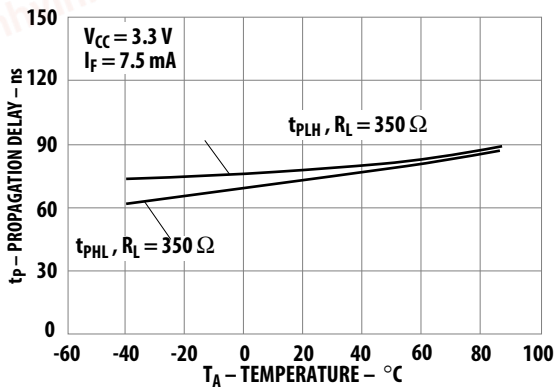


Figure 6. Test circuit for t_{PHL} and t_{PLH}

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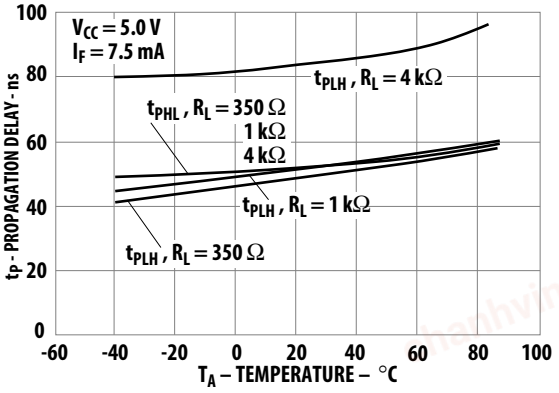
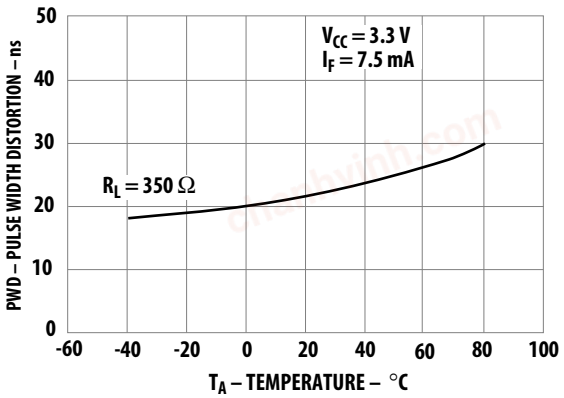


Figure 7. Typical propagation delay vs. temperature



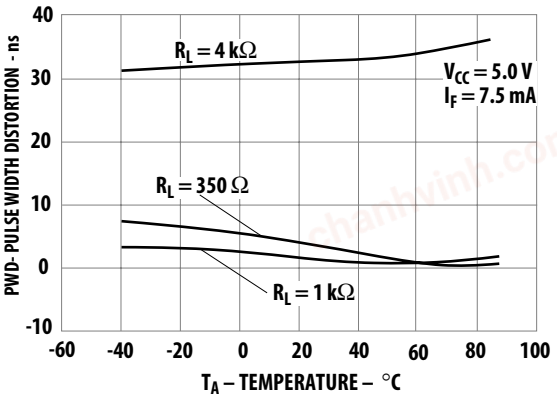


Figure 8. Typical pulse width distortion vs. temperature

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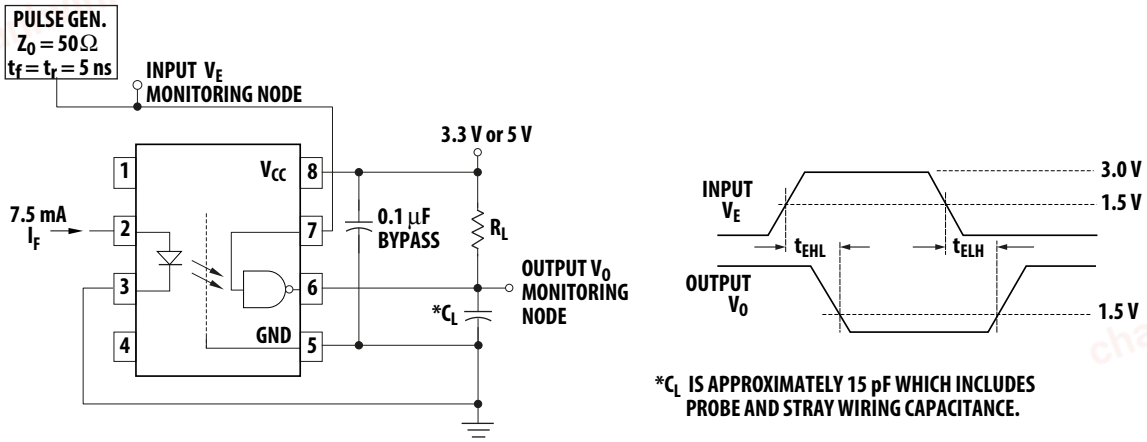


Figure 9. Test circuit for t_{EHL} and t_{ELH}

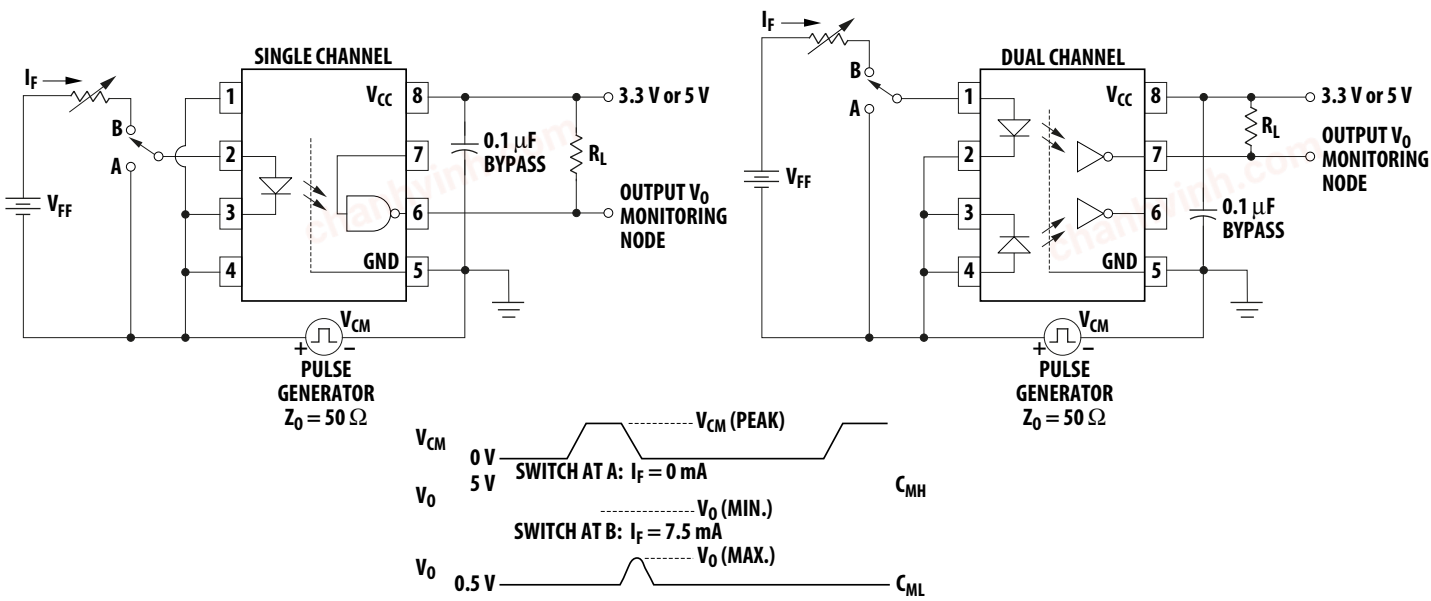


Figure 10. Test circuit for common mode transient immunity and typical waveforms

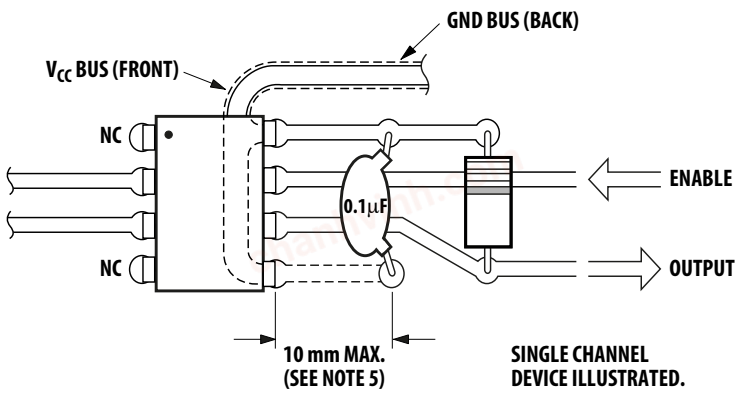
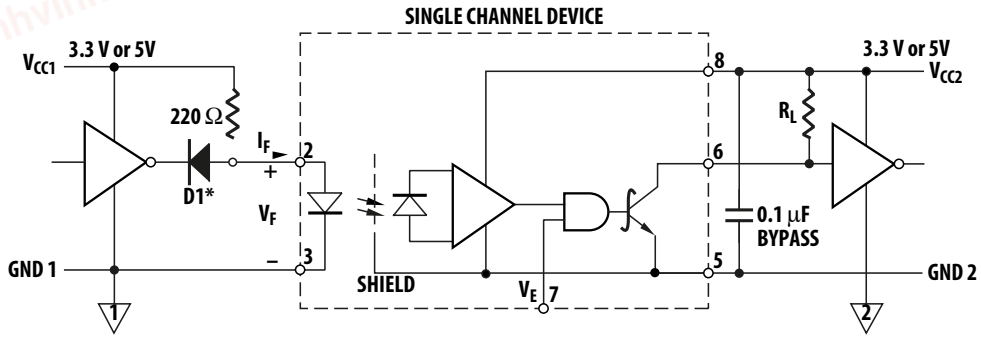


Figure 11. Recommended printed circuit board layout

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*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

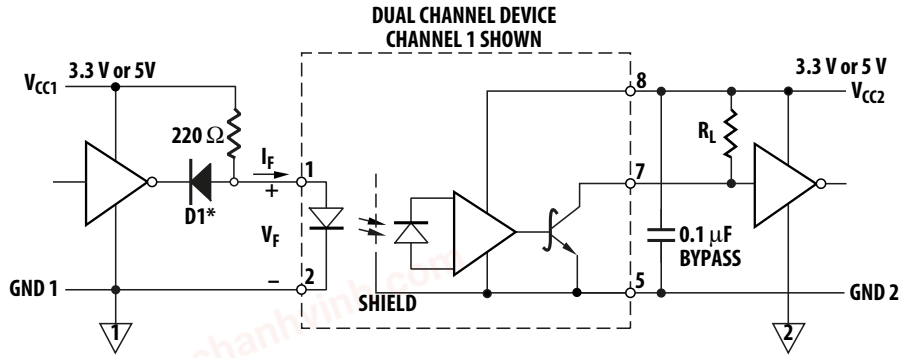


Figure 12. Recommended LVTTL interface circuit

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Application Information

Common-Mode Rejection for HCPL-260L Families:

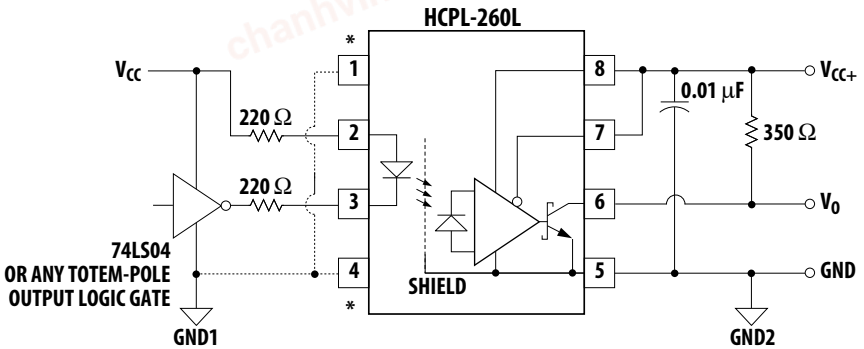
Figure 13 shows the recommended drive circuit for optimal common-mode rejection performance. Two main points to note are:

1. The enable pin is tied to V_{CC} rather than floating (this applies to single-channel parts only).
2. Two LED-current setting resistors are used instead of one. This is to balance I_{LED} variation during common-mode transients.

If the enable pin is left floating, it is possible for common-mode transients to couple to the enable pin, resulting in common-mode failure. This failure mechanism only occurs when the LED is on and the output is in the Low State. It is identified as occurring when the transient output voltage rises above 0.8 V. Therefore, the enable pin should be connected to either V_{CC} or logic-level high for best common-mode performance with the output low (CMR_L). This failure mechanism is only present in single-channel parts which have the enable function.

Also, common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which can be bad if the LED is on) or conversely cause current to be injected into the LED (bad if the LED is meant to be off). Figure 14 shows the parasitic capacitances which exists between LED anode/cathode and output ground (C_{LA} and C_{LC}). Also shown in Figure 14 on the input side is an AC-equivalent circuit.

For transients occurring when the LED is on, common-mode rejection (CMR_L, since the output is in the "low" state) depends upon the amount of LED current drive (I_F). For conditions where I_F is close to the switching threshold (I_{TH}), CMR_L also depends on the extent which I_{LP} and I_{LN} balance each other. In other words, any condition where common-mode transients cause a momentary decrease in I_F will cause common-mode failure for transients which are fast enough.



*** HIGHER CMR MAY BE OBTAINABLE BY CONNECTING PINS 1, 4 TO INPUT GROUND (GND1).**

Figure 13. Recommended drive circuit for High-CMR

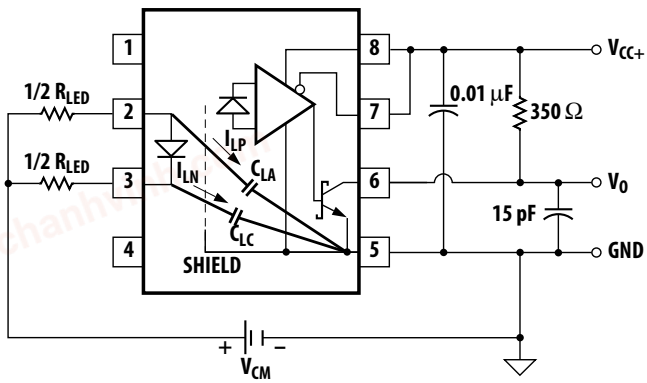


Figure 14. AC equivalent circuit

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Likewise for common-mode transients which occur when the LED is off (i.e. CMR_H, since the output is "high"), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient "signal" may cause the output to spike below 2 V (which constitutes a CMR_H failure).

By using the recommended circuit in Figure 13, good CMR can be achieved. The balanced I_{LED}-setting resistors help equalize I_{LP} and I_{LN} to reduce the amount by which I_{LED} is modulated from transient coupling through C_{LA} and C_{LC}.

CMR with Other Drive Circuits

CMR performance with drive circuits other than that shown in Figure 13 may be enhanced by following these guidelines:

1. Use of drive circuits where current is shunted from the LED in the LED "off" state (as shown in Figures 15 and 16). This is beneficial for good CMR_H.
2. Use of I_{FH} > 3.5 mA. This is good for high CMR_L.

Figure 15 shows a circuit which can be used with any totem-pole-output TTL/LSTTL/HCMOS logic gate. The buffer PNP transistor allows the circuit to be used with logic devices which have low current-sinking capability. It also helps maintain the driving-gate power-supply current at a constant level to minimize ground shifting for other devices connected to the input-supply ground.

When using an open-collector TTL or open-drain CMOS logic gate, the circuit in Figure 16 may be used. When using a CMOS gate to drive the optocoupler, the circuit shown in Figure 17 may be used. The diode in parallel with the R_{LED} speeds the turn-off of the optocoupler LED.

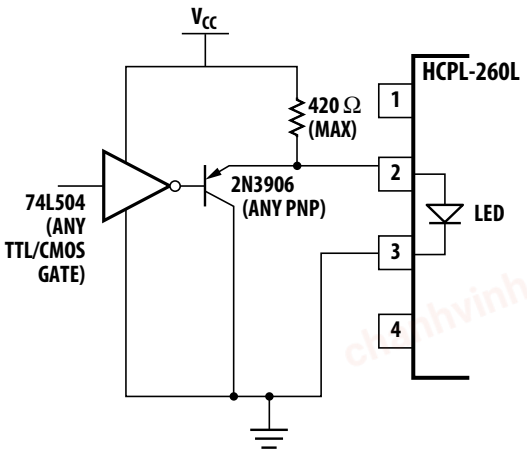


Figure 15. TTL interface circuit

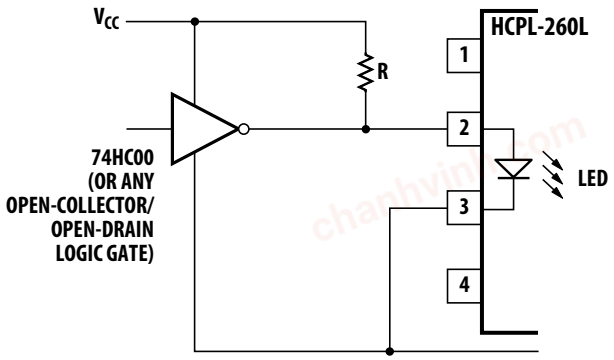


Figure 16. TTL open-collector/open-drain gate drive circuit

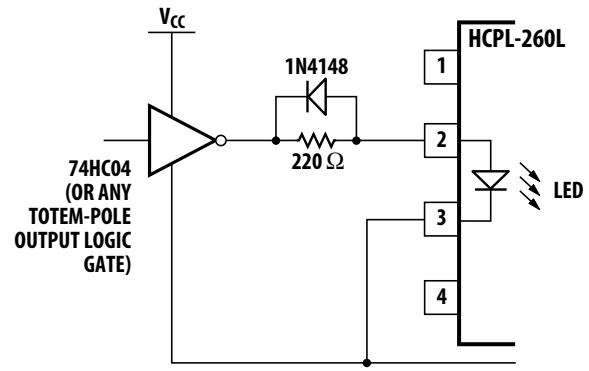


Figure 17. CMOS gate drive circuit

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