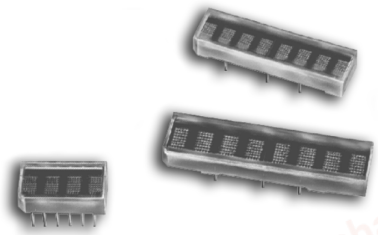
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HCMS-39x6 and HCMS-39x7

3.3 V High Performance CMOS 5x7 AlphaNumeric Displays

Data Sheet

HCMS-3906, HCMS-3966, HCMS-3916, HCMS-3976,
HCMS-3907, HCMS-3967, HCMS-3917, HCMS-3977



Description

The 3.3 V HCMS-39xx family is similar to the 5.0 V HCMS-29xx family, except it operates at a lower operating voltage. Package dimensions and pin outs are exactly the same for both families. The product has been thoroughly characterized and stringent reliability tested to ensure that the product is of high quality.

Similar to the 5.0 V platform, this family product is a high performance, easy to use dot matrix display driven by on-board CMOS IC. Each display can be directly interfaced with a microprocessor, thus eliminating the need for cumbersome interface components. The serial IC interface allows higher character count information displays with a minimum of data lines. The easy to read 5x7 pixel format allows the display of upper case, lower case, Katakana, and custom user-defined characters. These displays are stackable in the x- and y-directions, making them ideal for high character count displays.

Features

- Easy to use
- Interfaces directly with microprocessors
- 0.15" character height in 4 and 8 character package
- 0.20" character height in 4 and 8 character package
- Rugged X- and Y-stackable package
- Serial input
- Convenient brightness controls
- Wave solderable
- Low power CMOS technology
- TTL compatible
- 3.3 V operating voltage

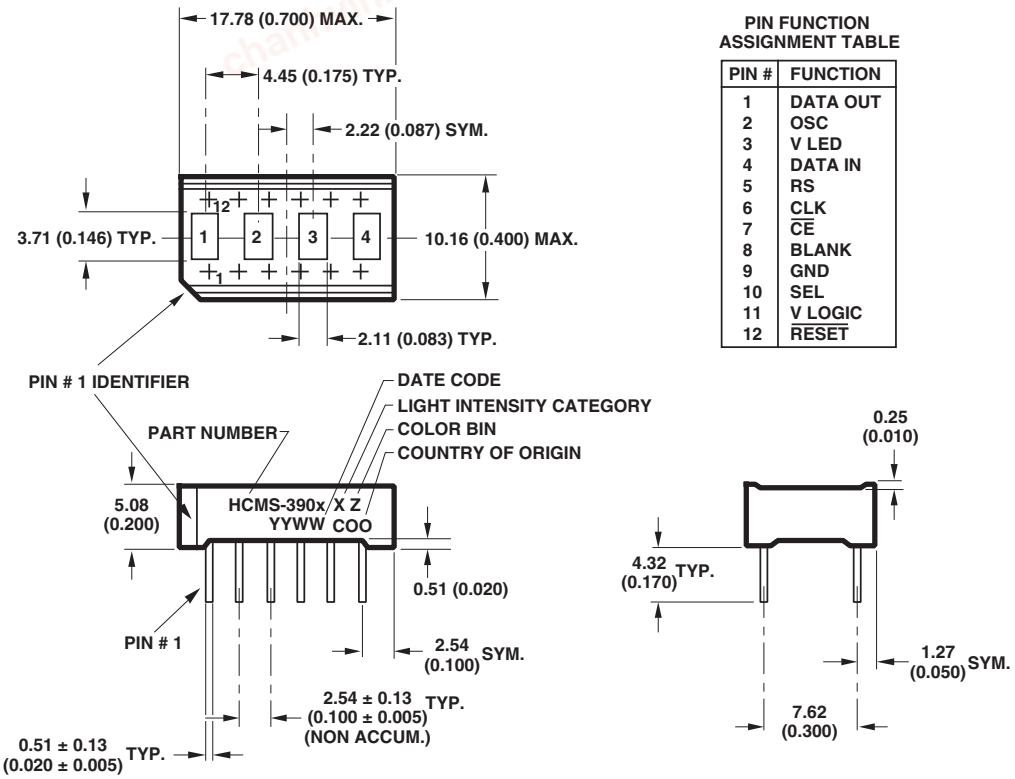
Applications

- Telecommunications equipment
- Portable data entry devices
- Computer peripherals
- Medical equipment
- Test equipment
- Business machines
- Avionics
- Industrial controls

ESD WARNING: *Standard CMOS handling precautions should be observed to avoid static discharge.*

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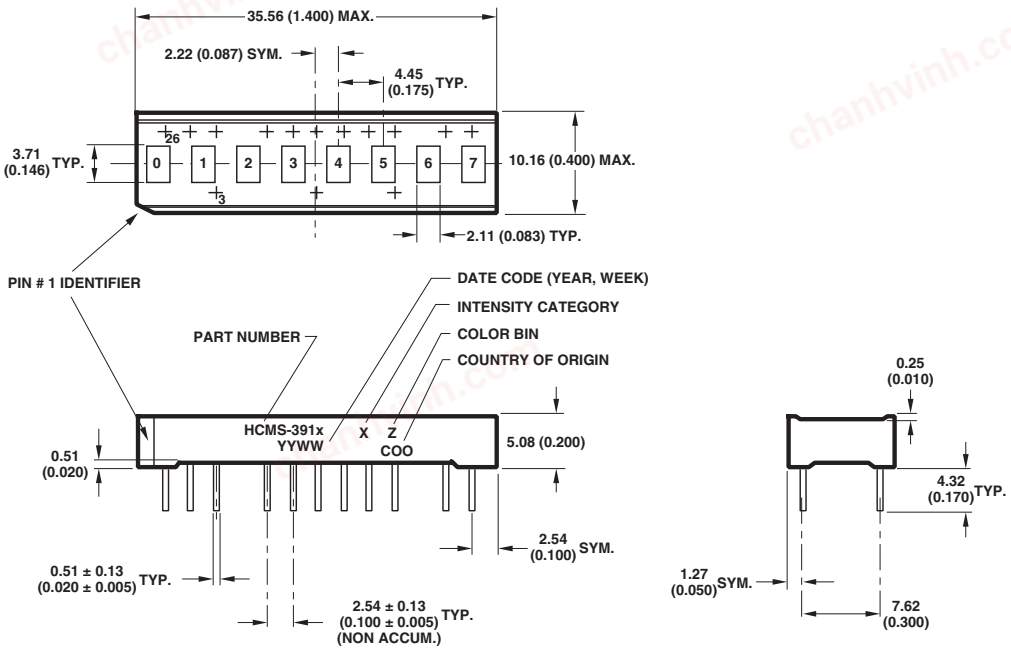
Package Dimensions



PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION
1	DATA OUT
2	OSC
3	V LED
4	DATA IN
5	RS
6	CLK
7	$\overline{CE}$
8	BLANK
9	GND
10	SEL
11	V LOGIC
12	$\overline{RESET}$

Figure 1. HCMS-390X package dimensions



PIN FUNCTION ASSIGNMENT TABLE

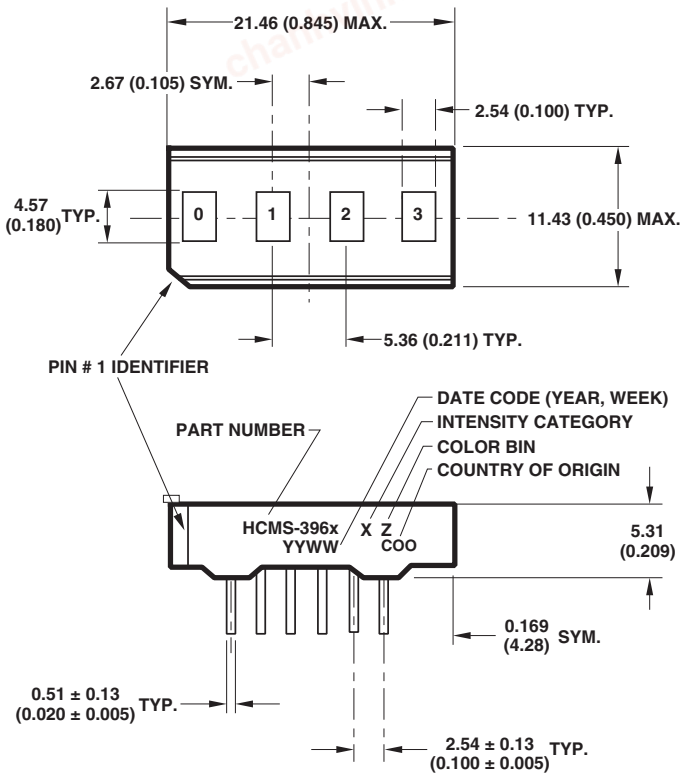
PIN #	FUNCTION
1	NO PIN
2	NO PIN
3	V LED
4	NO PIN
5	NO PIN
6	NO PIN
7	GND LED
8	NO PIN
9	NO PIN
10	V LED
11	NO PIN
12	NO PIN
13	NO PIN
14	DATA IN
15	RS
16	NO PIN
17	CLOCK
18	$\overline{CE}$
19	BLANK
20	GND LOGIC
21	SEL
22	V LOGIC
23	NO PIN
24	$\overline{RESET}$
25	OSC
26	DATA OUT

Figure 2. HCMS-391X Package dimensions

Notes:
1. Dimensions are in mm (inches).
2. Unless otherwise specified, tolerance on dimensions is ± 0.38 mm (0.015 Inch).
3. Lead material: solder plated copper alloy.

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Package Dimensions, continued



PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION
1	DATA OUT
2	OSC
3	V LED
4	DATA IN
5	RS
6	CLK
7	$\overline{CE}$
8	BLANK
9	GND
10	SEL
11	V LOGIC
12	$\overline{RESET}$

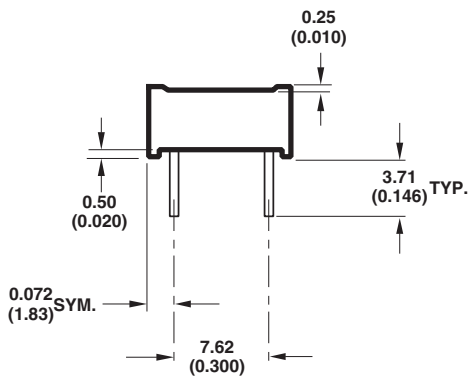
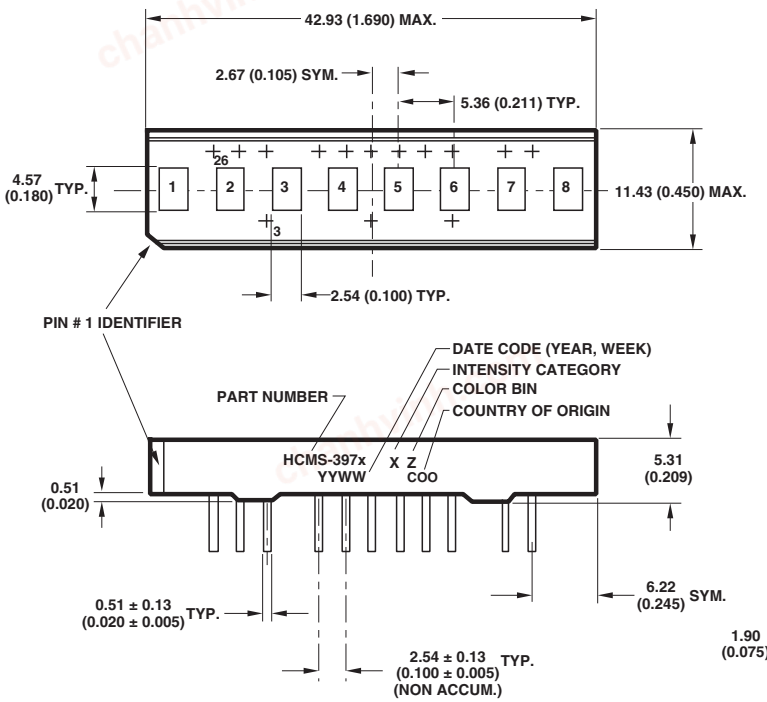


Figure 3. HCMS-396X Package dimensions



PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION
1	NO PIN
2	NO PIN
3	V LED
4	NO PIN
5	NO PIN
6	NO PIN
7	GND LED
8	NO PIN
9	NO PIN
10	V LED
11	NO PIN
12	NO PIN
13	NO PIN
14	DATA IN
15	RS
16	NO PIN
17	CLOCK
18	$\overline{CE}$
19	BLANK
20	GND LOGIC
21	SEL
22	V LOGIC
23	NO PIN
24	$\overline{RESET}$
25	OSC
26	DATA OUT

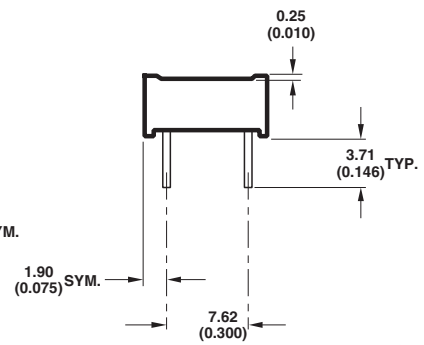


Figure 4. HCMS-397X Package dimensions

Notes:
1. Dimensions are in mm (inches).
2. Unless otherwise specified, tolerance on dimensions is ± 0.38 mm (0.015 Inch).
3. Lead material: solder plated copper alloy.

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Device Selection Guide

Description	Red	Green
1 x 4 0.15" Character	HCMS-3906	HCMS-3907
1 x 8 0.15" Character	HCMS-3916	HCMS-3917
1 x 4 0.20" Character	HCMS-3966	HCMS-3967
1 x 8 0.20" Character	HCMS-3976	HCMS-3977

Absolute Maximum Ratings

Logic Supply Voltage, V_{LOGIC} to GND_{LOGIC} ..... -0.3 V to 7.0 V
LED Supply Voltage, V_{LED} to GND_{LED} ..... -0.3 V to 5.5 V
Input Voltage, Any Pin to GND ..... -0.3 V to V_{LOGIC} +0.3 V
Free Air Operating Temperature Range T_A[1] ..... -40° C to +85° C
Relative Humidity (non-condensing)..... 85%
Storage Temperature, T_S ..... -55° C to 100° C
Soldering Temperature (1.59 mm (0.063 in.) below body)
  Solder Dipping..... 260° C for 5 secs
  Wave Soldering..... 250° C for 3 secs
ESD Protection @ 1.5 kΩ, 100 pF (each pin) ..... Class 1, 0-1999 V
TOTAL Package Power Dissipation at T_A = 25° C[1]
  4 character ..... 0.766 W
  8 character..... 1.532 W
  16 character . ..... 3.064 W

Note:
1. For operation in high ambient temperatures, see Appendix A, Thermal Considerations.

Recommended Operating Conditions over Temperature Range (-40° C to +85° C)

Parameter	Symbol	Min.	Max.	Units
Logic Supply Voltage[1]	V_{LOGIC}	3.1	5.5	V
LED Supply Voltage[1]	V_{LED}	3.1	5.5	V
GND_{LED} to GND_{LOGIC}[1]	–	-0.3	+0.3	V

Note:
1. For further description, see Appendix B, Electrical Considerations, "V_{LOGIC} and V_{LED} Considerations".

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Electrical Characteristics over Operating Temperature Range (-40° C to +85° C)

		$T_A = 25°C$ $V_{LOGIC} = 3.3\ V$		$-40°C < T_A < 85°C$ $3.0\ V < V_{LOGIC} < 5.5\ V$			
Parameter	**Symbol**	**Typ.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
Input Leakage Current	I_I					µA	$V_{IN} = 0\ V$ to V_{LOGIC}
HCMS-390X/396X (4 char)			+7.5	-2.5	+50		
HCMS-391X/397X (8 char)			+15	-5.0	+100		
I_{LOGIC} OPERATING	I_{LOGIC} (OPT)					mA	$V_{IN} = V_{LOGIC}$
HCMS-390X/396X (4 char)		0.4	2.5		5		
HCMS-391X/397X (8 char)		0.8	5		10		
I_{LOGIC} SLEEP[1]	I_{LOGIC} (SLP)					µA	$V_{IN} = V_{LOGIC}$
HCMS-390X/396X (4 char)		5	15		25		
HCMS-391X/397X (8 char)		10	30		50		
I_{LED} BLANK	I_{LED} (BL)					mA	BL = 0 V
HCMS-390X/396X (4 char)		2.0	4.0		8.4		
HCMS-391X/397X (8 char)		4.0	8.0		8.0		
I_{LED} SLEEP[1]	I_{LED} (SLP)					µA	
HCMS-390X/396X (4 char)		7.5	20		50		
HCMS-391X/397X (8 char)		15	40		100		
Peak Pixel Current[2]	I_{PIXEL}	14.0	15.9		17.1	mA	$V_{LED} = 5.5\ V$. All pixels ON, average value per pixel
HIGH level input voltage	V_{IH}			2.4		V	$3.0\ V < V_{LOGIC} < 5.5\ V$
LOW level input voltage	V_{IL}				0.4	V	$3.0\ V < V_{LOGIC} < 5.5\ V$
HIGH level output voltage	V_{OH}			2.4		V	$3.0\ V < V_{LOGIC} < 5.5\ V$
LOW level output voltage	V_{OL}				0.4	V	$3.0\ V < V_{LOGIC} < 5.5\ V$
Thermal Resistance	$R\theta_{J-P}$	70					°C/W

Notes:
1. In SLEEP mode, the internal oscillator and reference current for LED drivers are off.
2. Average peak pixel current is measured at the maximum drive current set by Control Register 0. Individual pixels may exceed this value.

Optical Characteristics at 25° C ±1° C [1]

V_{LED} = 3.3 V, 100% Peak Current, 100% Pulse Width

	Luminous Intensity per LED [2] Character Average (µcd)		**Peak Wavelength λ_{Peak} (nm)**	**Dominant Wavelength λ_d [3] (nm)**
Display Color	**Min.**	**Typ.**	**Typ.**	**Typ.**
Red	520	2300	635	624
Green	520	1000	574	572

Notes:
1. Refers to the initial case temperature of the device immediately prior to measurement.
2. Measured with all LEDs illuminated in a digit.
3. Dominant wavelength, λ_d , is derived from the CIE chromaticity diagram and represents the single wavelength which defines the perceived LED color.

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Electrical Description

Pin Function	Description
$\overline{\text{RESET}}$ ($\overline{\text{RST}}$)	Sets Control Register bits to logic low. The Dot Register contents are unaffected by the Reset pin. (logic low = reset; logic high = normal operation).
DATA IN (D_{IN})	Serial Data input for Dot or Control Register data. Data is entered on the rising edge of the Clock input.
DATA OUT (D_{OUT})	Serial Data output for Dot or Control Register data. This pin is used for cascading multiple displays.
CLOCK (CLK)	Clock input for writing Dot or Control Register data. When $\overline{\text{Chip Enable}}$ is logic low, data is entered on the rising Clock edge.
REGISTER SELECT (RS)	Selects Dot Register (RS = logic low) or Control Register (RS = logic high) as the destination for serial data entry. The logic level of RS is latched on the falling edge of the $\overline{\text{Chip Enable}}$ input.
$\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$)	This input must be a logic low to write data to the display. When $\overline{\text{CE}}$ returns to logic high and CLK is logic low, data is latched to either the LED output drivers or a Control Register.
OSCILLATOR SELECT	Selects either an internal or external display oscillator source. (SEL) (logic low = External Display Oscillator; logic high = Internal Display Oscillator).
OSCILLATOR (OSC)	Output for the Internal Display Oscillator (SEL = logic high) or input for an External Display Oscillator (SEL = logic low).
BLANK (BL)	Blanks the display when logic high. May be modulated for brightness control.
GND_{LED}	Ground for LED drivers.
GND_{LOGIC}	Ground for logic.
V_{LED}	Positive supply for LED drivers.
V_{LOGIC}	Positive supply for logic.

AC Timing Characteristics over Temperature Range (-40 to +85° C)

Timing Diagram Ref. Number	Description	Symbol	4.5 V<V_{LOGIC} < 5.5 V Min.	4.5 V<V_{LOGIC} < 5.5 V Max.	V_{LOGIC} = 3 V Min.	V_{LOGIC} = 3 V Max.	Units
1	Register Select Setup Time to $\overline{\text{Chip Enable}}$	t_{rss}	10		10		ns
2	Register Select Hold Time to $\overline{\text{Chip Enable}}$	t_{rsh}	10		10		ns
3	Rising Clock Edge to Falling $\overline{\text{Chip Enable}}$ Edge	t_{clkce}	20		20		ns
4	$\overline{\text{Chip Enable}}$ Setup Time to Rising Clock Edge	t_{ces}	35		55		ns
5	$\overline{\text{Chip Enable}}$ Hold Time to Rising Clock Edge	t_{ceh}	20		20		ns
6	Data Setup Time to Rising Clock Edge	t_{ds}	10		10		ns
7	Data Hold Time after Rising Clock Edge	t_{dh}	10		10		ns
8	Rising Clock Edge to D_{OUT} [1]	t_{dout}	10	40	10	65	ns
9	Propagation Delay D_{IN} to D_{OUT} Simultaneous Mode for one IC[1,2]	t_{doutp}		18		30	ns
10	$\overline{\text{CE}}$ Falling Edge to D_{OUT} Valid	t_{cedo}		25		45	ns
11	Clock High Time	t_{clkh}	80		100		ns
12	Clock Low Time	t_{clkl}	80		100		ns
	Reset Low Time	t_{rstl}	50		50		ns
	Clock Frequency	F_{cyc}		5		4	MHz
	Internal Display Oscillator Frequency	F_{inosc}	80	210	80	210	KHz
	Internal Refresh Frequency	F_{rf}	150	410	150	410	Hz
	External Display Oscillator Frequency	F_{exosc}					
	Prescaler = 1		51.2	1000	51.2	1000	KHz
	Prescaler = 8		410	8000	410	8000	KHz

Notes:
1. Timing specifications increase 0.3 ns per pf of capacitive loading above 15 pF.
2. This parameter is valid for Simultaneous Mode data entry of the Control Register.

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Display Overview

The HCMS-39XX series is a family of LED displays driven by on-board CMOS ICs. The LEDs are configured as 5x7 font characters and are driven in groups of 4 characters per IC. Each IC consists of a 160-bit shift register (the Dot Register), two 7-bit Control Words, and refresh circuitry. The Dot Register contents are mapped on a one-to-one basis to the display. Thus, an individual Dot Register bit uniquely controls a single LED.

Eight-character displays have two ICs that are cascaded. The Data Out line of the first IC is internally connected to the Data In line of the second IC forming a 320-bit Dot Register. The display's other control and power lines are connected directly to both ICs.

Reset

$\overline{\text{Reset}}$ initializes the Control Registers (sets all Control Register bits to logic low) and places the display in the sleep mode. The $\overline{\text{Reset}}$ pin should be connected to the system power on reset circuit. The Dot Registers are not cleared upon power-on or by Reset. After power-on, the Dot Register contents are random; however, $\overline{\text{Reset}}$ will put the display in sleep mode, thereby blanking the LEDs. The Control Register and the Control Words are cleared to all zeros by $\overline{\text{Reset}}$.

To operate the display after being $\overline{\text{Reset}}$, load the Dot Register with logic lows. Then load Control Word 0 with the desired brightness level and set the sleep mode bit to logic high.

Dot Register

The Dot Register holds the pattern to be displayed by the LEDs. Data is loaded into the Dot Register according to the procedure shown in Table 1 and Figure 5.

First RS is brought low, then $\overline{\text{CE}}$ is brought low. Next, each successive rising CLK edge will shift in the data at the DIN pin. Loading a logic high will turn the corresponding LED on; a logic low turns the LED off. When all 160 bits have been loaded (or 320 bits in an 8-digit display), $\overline{\text{CE}}$ is brought to logic high.

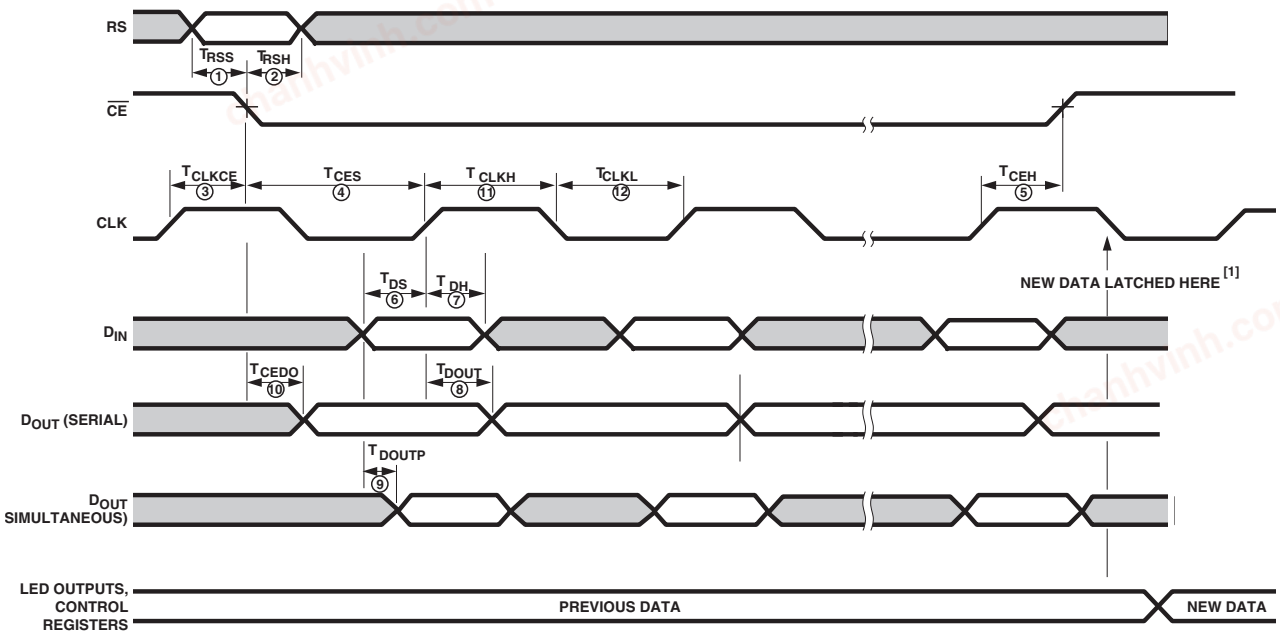
When CLK is next brought to logic low, new data is latched into the display dot drivers. Loading data into the Dot Register takes place while the previous data is displayed and eliminates the need to blank the display while loading data.

Table 1. Register Truth Table

Function	CLK	CE	RS
Select Dot Register	Not Rising	↓	L
Load Dot Register DIN = HIGH LED = "ON" DIN = LOW LED = "OFF"	↑	L	X
Copy Data from Dot Register to Dot Latch	L	H	X
Select Control Register	Not Rising	↓	H
Load Control Register [1,3]	↑	L	X
Latch Data to Control Word [2]	L	H	X

Notes:
1. BIT D_0 of Control Word 1 must have been previously set to Low for serial mode or High for simultaneous mode.
2. Selection of Control Word 1 or Control Word 0 is set by D7 of the Control Shift Register. The unselected control word retains its previous value.
3. Control Word data is loaded Most Significant Bit (D_7) first.

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NOTE:
1. DATA IS COPIED TO THE CONTROL REGISTER OR THE DOT LATCH AND LED OUTPUTS WHEN $\overline{CE}$ IS HIGH AND CLK IS LOW.

Figure 5. HCMS-39XX write cycle timing diagram.

Pixel Map

In a 4-character display, the 160- bits are arranged as 20 columns by 8 rows. This array can be conceptualized as four 5 x 8 dot matrix character locations, but only 7 of the 8 rows have LEDs (see Figures 6 & 7). The bottom row (row 0) is not used. Thus, latch location 0 is never displayed. Column 0 controls the left-most column. Data from Dot Latch locations 0-7 determine whether or not pixels in Column 0 are turned-on or turned-off. Therefore, the lower left pixel is turned-on when a logic high is stored in Dot Latch location 1. Characters are loaded in serially, with the left-most character being loaded first and the rightmost character being loaded last. By loading one character at a time and latching the data before loading the next character, the figures will appear to scroll from right to left.

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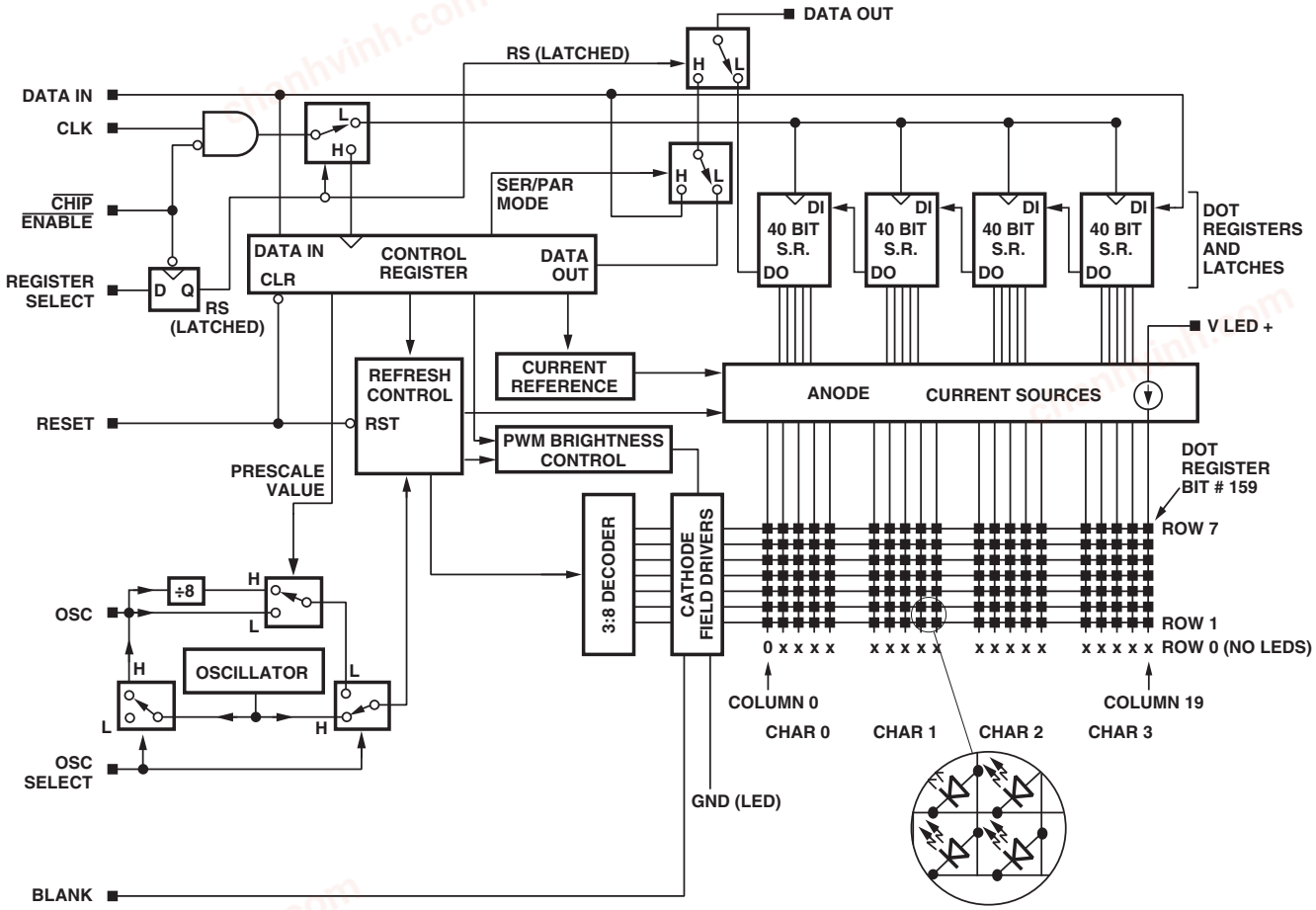


Figure 6. Block diagram for HCMS-39xx.

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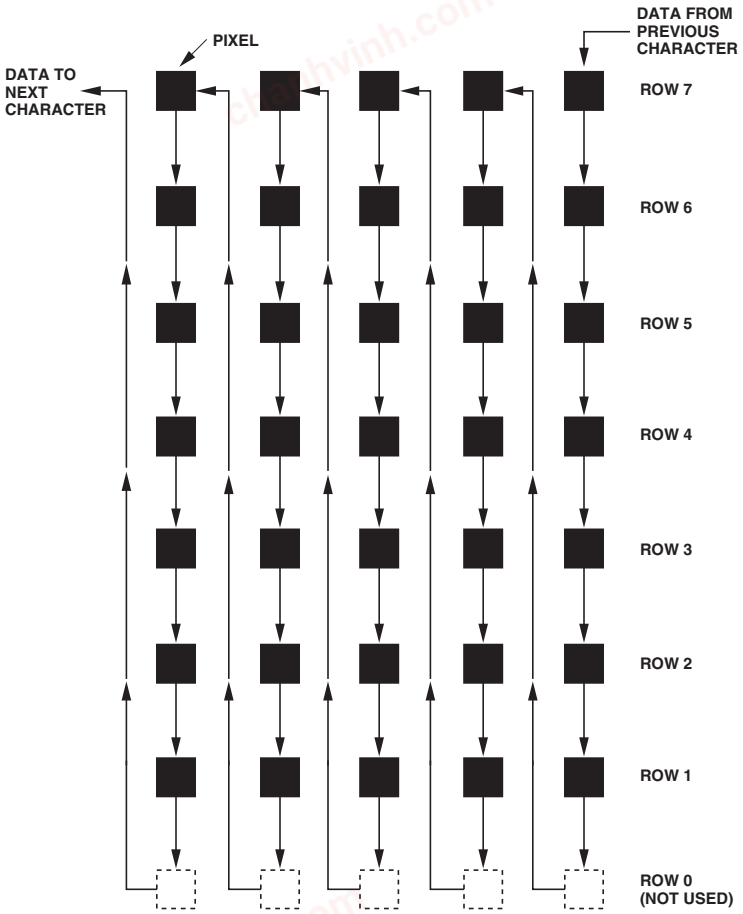


Figure 7. Pixel map

Control Register

The Control Register allows software modification of the IC's operation and consists of two independent 7-bit control words. Bit D7 in the shift register selects one of the two 7-bit control words. Control Word 0 performs pulse width modulation Figure 7. Pixel map. brightness control, peak pixel current brightness control, and sleep mode. Control Word 1 sets serial/simultaneous data out mode, and external oscillator prescaler. Each function is independent of the others.

Control Register Data Loading

Data is loaded into the Control Register, MSB first, according to the procedure shown in Table 1 and Figure 5. First, RS is brought to logic high and then $\overline{CE}$ is brought to logic low. Next, each successive rising CLK edge will shift in the data on the DIN pin. Finally, when 8 bits have been loaded, the $\overline{CE}$ line is brought to logic high. When CLK goes to logic low, new data is copied into the selected control word. Loading data into the Control Register takes place while the previous control word configures the display.

Control Word 0

Loading the Control Register with D_7 = Logic low selects Control Word 0 (see Table 2). Bits D_0-D_3 adjust the display brightness by pulse width modulating the LED on time, while Bits D_4-D_5 adjusts the display brightness by changing the peak pixel current. Bit D_6 selects normal operation or sleep mode.

Sleep mode (Control Word 0, bit D_6 = Low) turns off the Internal Display Oscillator and the LED pixel drivers. This mode is used when the IC needs to be powered up, but does not need to be active. Current draw in sleep mode is nearly zero. Data in the Dot Register and Control Words are retained during sleep mode.

Control Word 1

Loading the Control Register with D_7 = logic high selects Control Word 1. This Control Word performs two functions: serial/ simultaneous data out mode and external oscillator prescale select (see Table 2).

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Table 2. Control Shift Register.

CONTROL WORD 0

L	D_6	D_5	D_4	D_3	D_2	D_1	D_0

↑ Bit D_7 Set Low to Select Control Word 0

PWM Brightness Control

				On-Time Oscillator Cycles	Duty Factor (%)	Relative Brightness (%)
L	L	L	L	0	0	0
L	L	L	H	1	0.2	1.7
L	L	H	L	2	0.4	3.3
L	L	H	H	3	0.6	5.0
L	H	L	L	4	0.8	6.7
L	H	L	H	5	1.0	8.3
L	H	H	L	7	1.4	11.7
L	H	H	H	9	1.8	15
H	L	L	L	11	2.1	18
H	L	L	H	14	2.7	23
H	L	H	L	18	3.5	30
H	L	H	H	22	4.3	37
H	H	L	L	28	5.5	47
H	H	L	H	36	7.0	60
H	H	H	L	48	9.4	80
H	H	H	H	60	11.7	100

Peak Current Brightness Control		Typical Peak Pixel Current (mA)	Relative Full Scale Current (Relative Brightness, %)
H	L	4.0	31
L	H	6.4	50
L	L	9.3	73 (Default at Power Up)
H	H	12.8	100

SLEEP MODE

L – DISABLES INTERNAL OSCILLATOR-DISPLAY BLANK
H – NORMAL OPERATION

CONTROL WORD 1

H	L	L	L	L	L	D_1	D_0

↑ Bit D_7 Set High to Select Control Word 1

Reserved for Future Use (Bits D_2-D_6 must be set Low)

Serial/Simultaneous Data Out
L – D_{OUT} holds contents of Bit D_7
H – D_{OUT} is functionally tied to D_{in}

External Display Oscillator Prescaler
L – Oscillator Freq ÷ 1
H – Oscillator Freq ÷ 8

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Serial/Simultaneous Data Output D_0

Bit D_0 of control word 1 is used to switch the mode of D_{OUT} between serial and simultaneous data entry during Control Register writes. The default mode (logic low) is the serial D_{OUT} mode. In serial mode, D_{OUT} is connected to the last bit (D_7) of the Control Shift Register.

Storing logic high to bit D_0 changes D_{OUT} to simultaneous mode, which affects the Control Register only. In simultaneous mode, DOUT is logically connected to D_{IN}. This arrangement allows multiple ICs to have their Control Registers written to simultaneously. For example, for n ICs in the serial mode, n * 8 clock pulses are needed to load the same data in all Control Registers. In the simultaneous mode, n ICs only need 8 clock pulses to load the same data in all Control Registers. The propagation delay from the first IC to the last is n * t_{DOUTP}.

External Oscillator Prescaler Bit D_1

Bit D_1 of Control Word 1 is used to scale the frequency of an external Display Oscillator. When this bit is logic low, the external Display Oscillator directly sets the internal display clock rate. When this bit is logic high, the external oscillator is divided by 8. This scaled frequency then sets the internal display clock rate. It takes 512 cycles of the display clock (or 8 x 512 = 4096 cycles of an external clock with the divide by 8 prescaler) to completely refresh the display once. Using the prescaler bit allows the designer to use a higher external oscillator frequency without extra circuitry.

This bit has no affect on the internal Display Oscillator Frequency.

Bits D_2-D_6

These bits must always be programmed to logic low.

Cascaded ICs

Figure 8 shows how two ICs are connected within an HCMS-39XX display. The first IC controls the four left-most characters and the second IC controls the four rightmost characters. The Dot Registers are connected in series to form a 320-bit dot shift register. The location of pixel 0 has not changed. However, Dot Shift Register bit 0 of IC2 becomes bit 160 of the 320-bit dot shift register.

The Control Registers of the two ICs are independent of each other. This means that to adjust the display brightness the same control word must be entered into both ICs, unless the Control Registers are set to simultaneous mode.

Longer character string systems can be built by cascading multiple displays together. This is accomplished by creating a fiveline bus. This bus consists of $\overline{CE}$, RS, BL, $\overline{Reset}$, and CLK. The display pins are connected to the corresponding bus line. Thus, all $\overline{CE}$ pins are connected to the $\overline{CE}$ bus line. Similarly, bus lines for RS, BL, Reset, and CLK are created. Then D_{IN} is connected to the right-most display. D_{OUT} from this display is connected to the next display. The left-most display receives its D_{IN} from the D_{OUT} of the display to its right. D_{OUT} from the left-most display is not used.

Each display may be set to use its internal oscillator, or the displays may be synchronized by setting up one display as the master and the others as slaves. The slaves are set to receive their oscillator input from the master's oscillator output.

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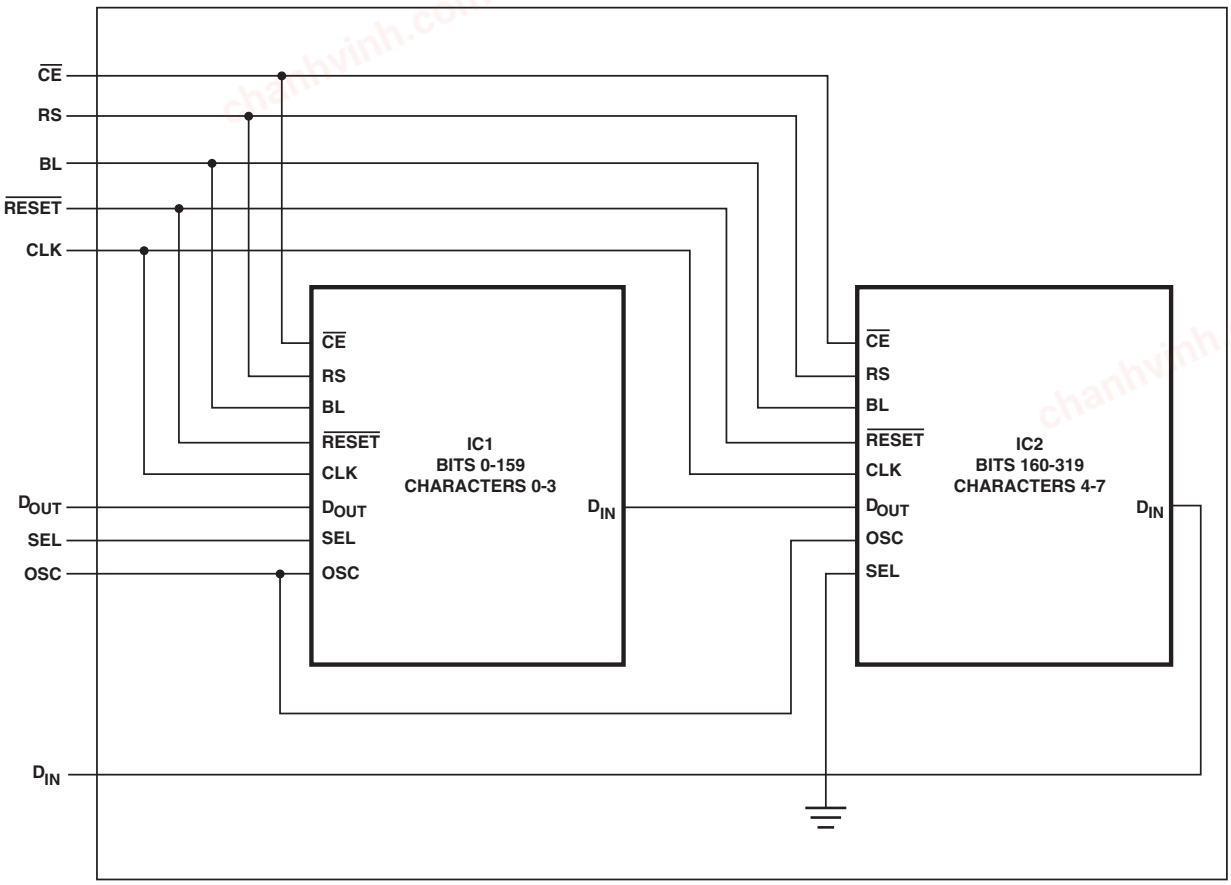


Figure 8. Cascaded ICs.

Appendix A. Thermal Considerations

The display IC has a maximum junction temperature of 150° C. The IC junction temperature can be calculated with Equation 1 in Table 3.

A typical value for $R\theta_{JA}$ is 100°C/ W. This value is typical for a display mounted in a socket and covered with a plastic filter. The socket is soldered to a 0.062 inch thick PCB with 0.020-inch wide, Figure 9. Maximum power dissipation per IC versus ambient temperature. one ounce copper traces. P_D can be calculated as Equation 2 in Table 3.

Figure 9 shows how to derate the power of one IC versus ambient temperature. Operation at high ambient temperatures may require the power per IC to be reduced. The power consumption can be reduced by changing the N, I_{PIXEL}, Osc cyc or V_{LED}. Changing V_{LOGIC} has very little impact on the power consumption.

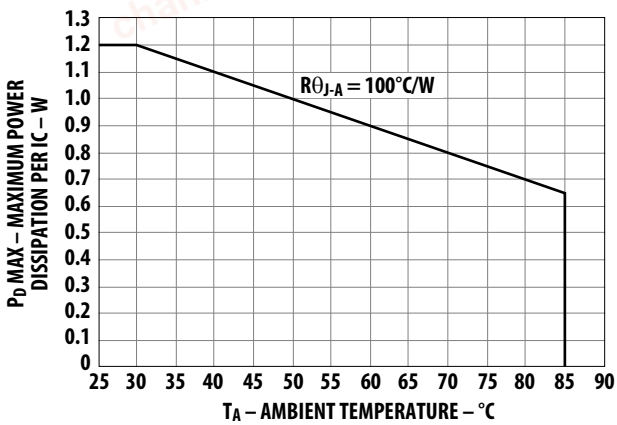


Figure 9. Maximum power dissipation per IC versus ambient temperature.

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Appendix B. Electrical Considerations

Current Calculations

The peak and average display current requirements have a significant impact on power supply selection. The maximum peak current is calculated with Equation 3 in Table 3.

The average current required by the display can be calculated with Equation 4 in Table 3.

The power supply has to be able to supply I_{PEAK} transients and supply I_{LED} (AVG) continuously. The range on V_{LED} allows noise on this supply without significantly changing the display brightness.

V_{LOGIC} and V_{LED} Considerations

The display uses two independent electrical systems. One system is used to power the display's logic and the other to power the display's LEDs. These two systems keep the logic supply clean.

Separate electrical systems allow the voltage applied to V_{LED} and V_{LOGIC} to be varied independently. Thus, V_{LED} can vary from 0 to 5.5 V without affecting either the Dot or the Control Registers. V_{LED} can be varied between 3.1 to 5.5 V without much noticeable variation in light output to the human eyes. There is also no pixel mismatch observed.

The intensity of the light output takes a plunge if operated less than 3.1 V. There is also no pixel mismatch observed at voltage as low as 2.6 V. However, operating below 3.1 V is not recommended. Dimming the display by pulse width modulating V_{LED} is also not recommended.

V_{LOGIC} can vary from 3.0 to 5.5 V without affecting either the displayed message or the display intensity. However, operating below 3 V may change the timing and logic levels and may cause Dot and Control Registers to be altered. Thus, operation of the display below 3.0 V is not recommended.

The logic ground is internally connected to the LED ground by a substrate diode. This diode becomes forward biased and conducts when the logic ground is 0.4 V greater than the LED ground. The LED ground and the logic ground should be connected to a common ground, which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the LED ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltages below -0.3 V can cause all the dots to be ON. Voltage above +0.3 V can cause dimming and dot mismatch.

Using a decoupling capacitor between the power supply and ground will help prevent any supply noise in the frequency range greater than that of the functioning display from interfering with the display's internal circuitry. The value of the capacitor depends on the series resistance from the ground back to the power supply and the range of frequencies that need to be suppressed. It is also advantageous to use the largest ground plane possible.

Electrostatic Discharge

The inputs to the ICs are protected against static discharge and input current latch up. However, for best results, standard CMOS handling precautions should be used. Before use, the HCMS-39XX should be stored in antistatic tubes or in conductive material. During assembly, a grounded conductive work area should be used and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static buildup. Input current latch up is caused when the CMOS inputs are subjected to either a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{LOGIC} ($V_{IN} > V_{LOGIC}$) and when a high current is forced into the input. To prevent input current latch up and ESD damage, unused inputs should be connected to either ground or V_{LOGIC}. Voltages should not be applied to the inputs until V_{LOGIC} has been applied to the display.

Table 3. Equations.

Equation 1:

$T_J\ MAX = T_A + P_D * R\theta_{JA}$

Where: $T_J\ MAX$ = maximum IC junction temperature
T_A = ambient temperature surrounding the display
$R\theta_{JA}$ = thermal resistance from the IC junction to ambient
P_D = total power dissipation

Equation 2:

$PD = (N * IPIXEL * Duty\ Factor * VLED) + ILOGIC * VLOGIC$

Where: P_D = total power dissipation
N = number of pixels on (maximum 4 char * 5 * 7 = 140)
I_{PIXEL} = peak pixel current.
Duty Factor = 1/8 * Osccyc/64
Osc cyc = number of ON oscillator cycles per row
I_{LOGIC} = IC logic current
V_{LOGIC} = logic supply voltage

Equation 3:

$IPEAK = M * 20 * IPIXEL$

Where: I_{PEAK} = maximum instantaneous peak current for the display
M = number of ICs in the system
20 = maximum number of LEDs on per IC
I_{PIXEL} = peak current for one LED

Equation 4:

I_{LED} (AVG) = N * IPIXEL * 1/8 * (oscillator cycles)/64
(See Variable Definitions above)

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Appendix C. Oscillator

The oscillator provides the internal refresh circuitry with a signal that is used to synchronize the columns and rows. This ensures that the right data is in the dot drivers for that row. This signal can be supplied from either an external source or the internal source.

A display refresh rate of 100 Hz or faster ensures flicker-free operation. Thus, for an external oscillator the frequency should be greater than or equal to 512 x 100 Hz = 51.2 kHz. Operation above 1 MHz without the prescaler or 8 MHz with the prescaler may cause noticeable pixel-to-pixel mismatch.

Appendix D. Refresh Circuitry

This display driver consists of 20 one-of-eight column decoders and 20 constant current sources, 1 one-of-eight row decoder and eight row sinks, a pulse width modulation control block, a peak current control block, and the circuit to refresh the LEDs. The refresh counters and oscillator are used to synchronize the columns and rows.

The 160 bits are organized as 20 columns by 8 rows. The IC illuminates the display by sequentially turning ON each of the 8 row-drivers. To refresh the display once takes 512 oscillator cycles. Because there are eight row drivers, each row driver is selected for 64 (512/8) oscillator cycles. Four cycles are used to briefly blank the display before the following row is switched on. Thus, each row is ON for 60 oscillator cycles out of a possible 64. This corresponds to the maximum LED on time.

The temperature of the display will also affect the LED brightness as shown in Figure 10.

Appendix E. Display Brightness

Two ways have been shown to control the brightness of this LED display: setting the peak current and setting the duty factor. Both values are set in Control Word 0. To compute the resulting display brightness when both PWM and peak current control are used, simply multiply the two relative brightness factors. For example, if Control Register 0 holds the word 1001101, the peak current is 73% of full scale (BIT D_5 = L, BIT D_4 = L) and the PWM is set to 60% duty factor (BIT D_3 = H, BIT D_2 = H, BIT D_1 = L, BIT D_0 = H). The resulting brightness is 44% (0.73 x 0.60 = 0.44) of full scale.

The temperature of the display will also affect the LED brightness as shown in Figure 10.

Appendix F. Reference Material

Application Note 1027: *Soldering LED Components*

Application Note 1015: *Contrast Enhancement Techniques for LED Displays*

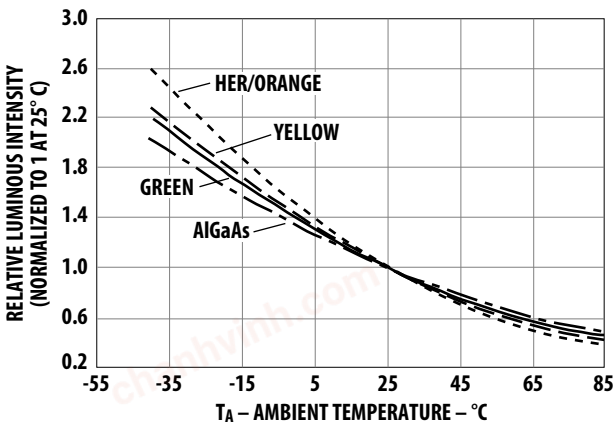


Figure 10. Relative luminous Intensity versus ambient temperature.

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