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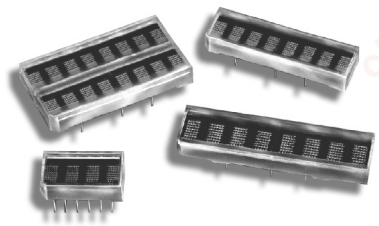
# HCMS-29xx Series

## High Performance CMOS 5×7 Alphanumeric Displays

AVAGO TECHNOLOGIES

## Data Sheet



### Description

The HCMS-29xx series are high performance, easy to use dot matrix displays driven by on-board CMOS ICs. Each display can be directly interfaced with a microprocessor, thus eliminating the need for cumbersome interface components. The serial IC interface allows higher character count information displays with a minimum of data lines. A variety of colors, font heights, and character counts gives designers a wide range of product choices for their specific applications and the easy to read 5×7 pixel format allows the display of uppercase, lower case, Katakana, and custom user-defined characters. These displays are stackable in the x- and y- directions, making them ideal for high character count displays.

### Features

- Easy to use
- Interfaces directly with microprocessors
- 0.15" character height in 4, 8, and 16 (2×8) character packages
- 0.20" character height in 4 and 8 character packages
- Rugged X- and Y-stackable package
- Serial input
- Convenient brightness controls
- Wave solderable
- Offered in five colors
- Low power CMOS technology
- TTL compatible

### Applications

- Telecommunications equipment
- Portable data entry devices
- Computer peripherals
- Medical equipment
- Test equipment
- Business machines
- Avionics
- Industrial controls

### Device Selection Guide

| Description | Deep Red HCMS- | HER HCMS- | Orange HCMS- | Yellow HCMS- | Green HCMS- | Package Drawing |
|---|---|---|---|---|---|---|
| 1 × 4 0.15" Character | 2905 | 2902 | 2904 | 2901 | 2903 | A |
| 1 × 8 0.15" Character | 2915 | 2912 | 2914 | 2911 | 2913 | B |
| 2 × 8 0.15" Character | 2925 | 2922 | 2924 | 2921 | 2923 | C |
| 1 × 4 0.20" Character | 2965 | 2962 | 2964 | 2961 | 2963 | D |
| 1 × 8 0.20" Character | 2975 | 2972 | 2974 | 2971 | 2973 | E |

*ESD WARNING: STANDARD CMOS HANDLING PRECAUTIONS SHOULD BE OBSERVED TO AVOID STATIC DISCHARGE.*

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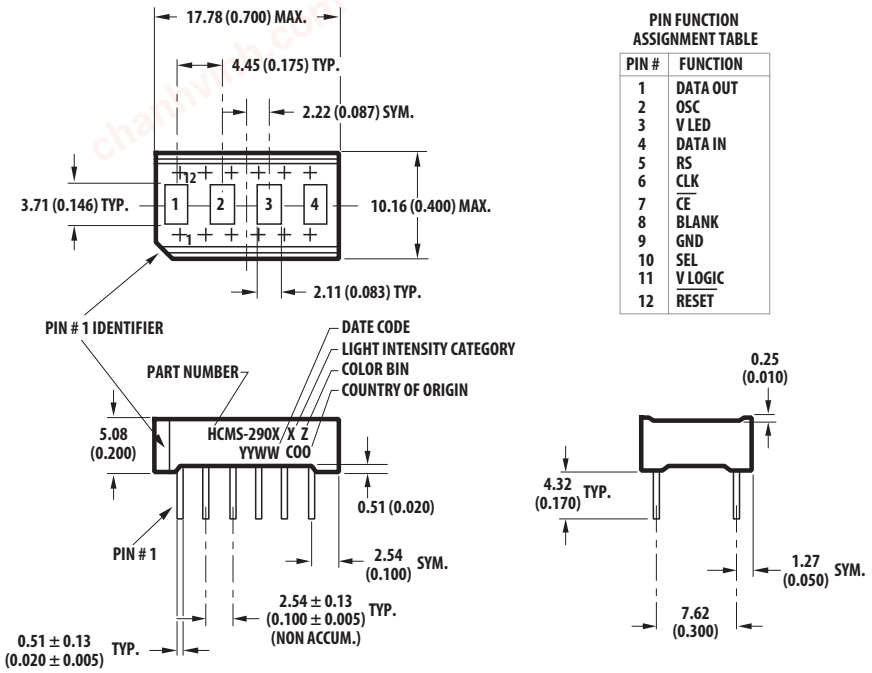
## HCMS-290x

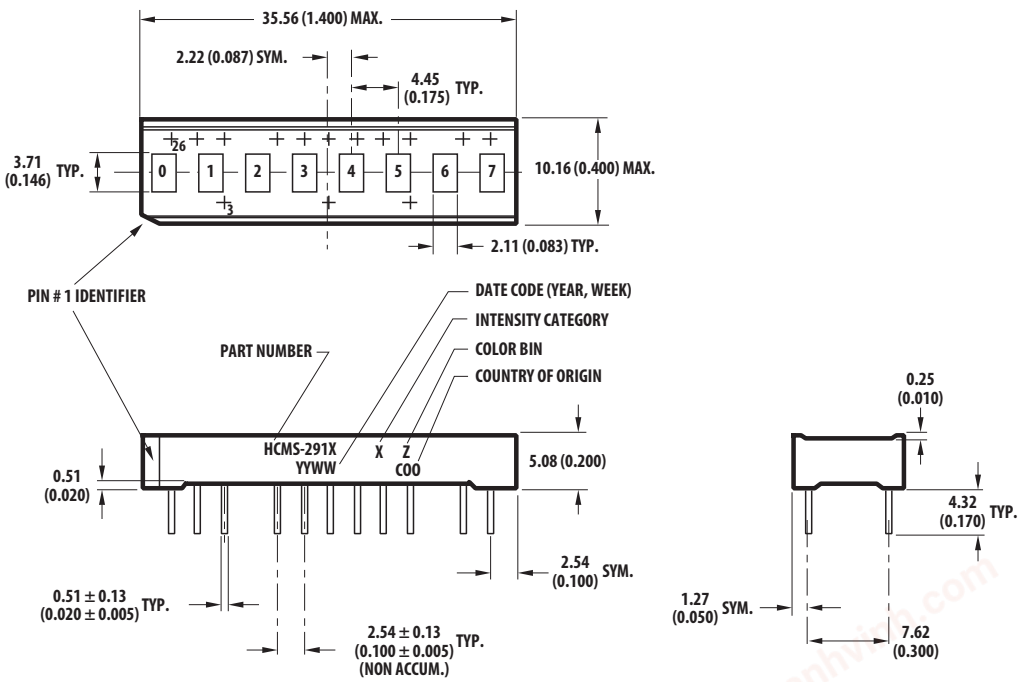



**PIN FUNCTION ASSIGNMENT TABLE**

| PIN # | FUNCTION |
|---|---|
| 1 | DATA OUT |
| 2 | OSC |
| 3 | V LED |
| 4 | DATA IN |
| 5 | RS |
| 6 | CLK |
| 7 | $\overline{CE}$ |
| 8 | BLANK |
| 9 | GND |
| 10 | SEL |
| 11 | V LOGIC |
| 12 | $\overline{RESET}$ |

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

## HCMS-291x




**PIN FUNCTION ASSIGNMENT TABLE**

| PIN # | FUNCTION |
|---|---|
| 1 | NO PIN |
| 2 | NO PIN |
| 3 | V LED |
| 4 | NO PIN |
| 5 | NO PIN |
| 6 | NO PIN |
| 7 | GND LED |
| 8 | NO PIN |
| 9 | NO PIN |
| 10 | V LED |
| 11 | NO PIN |
| 12 | NO PIN |
| 13 | NO PIN |
| 14 | DATA IN |
| 15 | RS |
| 16 | NO PIN |
| 17 | CLOCK |
| 18 | $\overline{CE}$ |
| 19 | BLANK |
| 20 | GND LOGIC |
| 21 | SEL |
| 22 | V LOGIC |
| 23 | NO PIN |
| 24 | $\overline{RESET}$ |
| 25 | OSC |
| 26 | DATA OUT |

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

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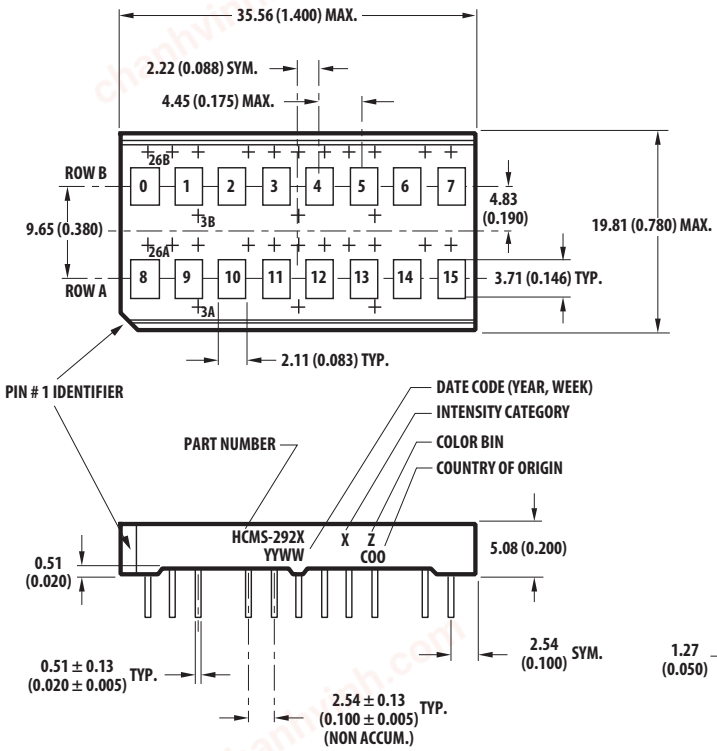
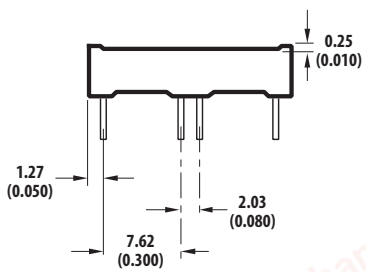
## HCMS-292x



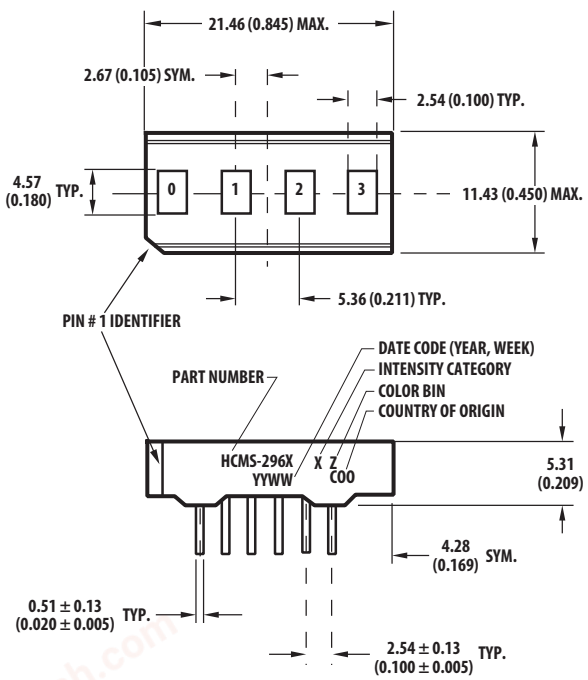




**PIN FUNCTION ASSIGNMENT TABLE**

| PIN # | FUNCTION | PIN # | FUNCTION |
|---|---|---|---|
| 1A | NO PIN | 1B | NO PIN |
| 2A | NO PIN | 2B | NO PIN |
| 3A | V LED | 3B | V LED |
| 4A | NO PIN | 4B | NO PIN |
| 5A | NO PIN | 5B | NO PIN |
| 6A | NO PIN | 6B | NO PIN |
| 7A | GND LED | 7B | GND LED |
| 8A | NO PIN | 8B | NO PIN |
| 9A | NO PIN | 9B | NO PIN |
| 10A | V LED | 10B | V LED |
| 11A | NO PIN | 11B | NO PIN |
| 12A | NO PIN | 12B | NO PIN |
| 13A | NO PIN | 13B | NO PIN |
| 14A | DATA IN | 14B | DATA IN |
| 15A | RS | 15B | RS |
| 16A | NO PIN | 16B | NO PIN |
| 17A | CLOCK | 17B | CLOCK |
| 18A | $\overline{CE}$ | 18B | $\overline{CE}$ |
| 19A | BLANK | 19B | BLANK |
| 20A | GND LOGIC | 20B | GND LOGIC |
| 21A | SEL | 21B | SEL |
| 22A | V LOGIC | 22B | V LOGIC |
| 23A | NO PIN | 23B | NO PIN |
| 24A | $\overline{RESET}$ | 24B | $\overline{RESET}$ |
| 25A | OSC | 25B | OSC |
| 26A | DATA OUT | 26B | DATA OUT |

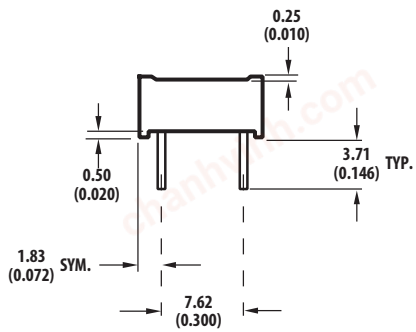
NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

## HCMS-296x




**PIN FUNCTION ASSIGNMENT TABLE**

| PIN # | FUNCTION |
|---|---|
| 1 | DATA OUT |
| 2 | OSC |
| 3 | V LED |
| 4 | DATA IN |
| 5 | RS |
| 6 | $\overline{CLK}$ |
| 7 | $\overline{CE}$ |
| 8 | BLANK |
| 9 | GND |
| 10 | SEL |
| 11 | $\overline{V\ LOGIC}$ |
| 12 | $\overline{RESET}$ |




NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

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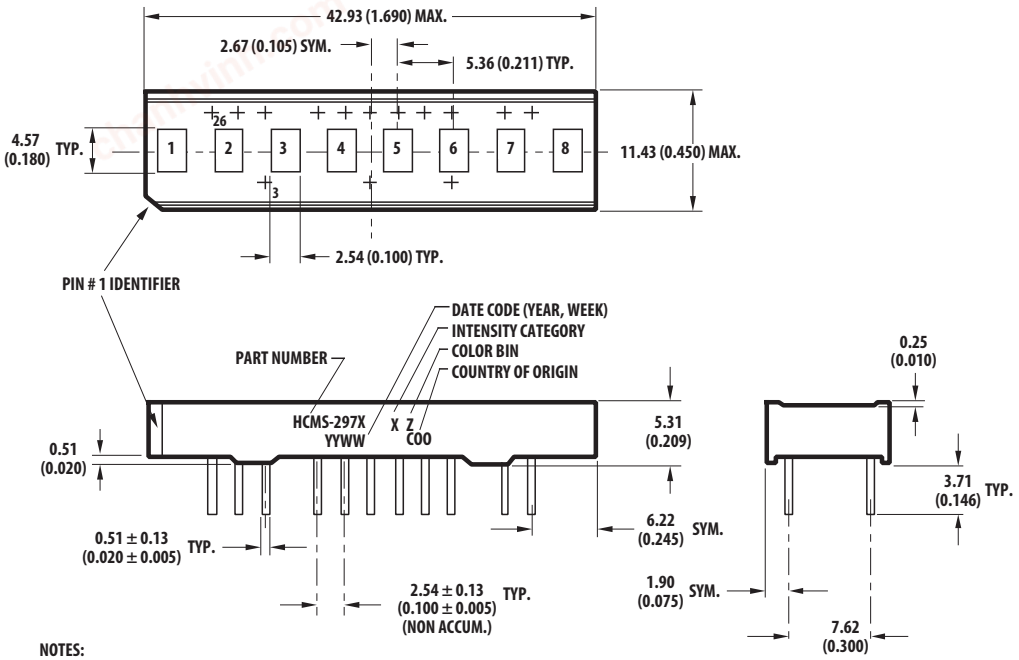
### HCMS-297x




**PIN FUNCTION ASSIGNMENT TABLE**

| PIN # | FUNCTION |
|---|---|
| 1 | NO PIN |
| 2 | NO PIN |
| 3 | V LED |
| 4 | NO PIN |
| 5 | NO PIN |
| 6 | NO PIN |
| 7 | GND LED |
| 8 | NO PIN |
| 9 | NO PIN |
| 10 | V LED |
| 11 | NO PIN |
| 12 | NO PIN |
| 13 | NO PIN |
| 14 | DATA IN |
| 15 | RS |
| 16 | NO PIN |
| 17 | CLOCK |
| 18 | $\overline{CE}$ |
| 19 | BLANK |
| 20 | GND LOGIC |
| 21 | SEL |
| 22 | V LOGIC |
| 23 | NO PIN |
| 24 | $\overline{RESET}$ |
| 25 | OSC |
| 26 | DATA OUT |

**NOTES:**
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ± 0.38 mm (0.015 INCH).
3. LEAD MATERIAL: SOLDER PLATED COPPER ALLOY.

## Absolute Maximum Ratings

| | |
|---|---|
| Logic Supply Voltage, $V_{LOGIC}$ to $GND_{LOGIC}$ | -0.3 V to 7.0 V |
| LED Supply Voltage, $V_{LED}$ to $GND_{LED}$ | -0.3 V to 5.5 V |
| Input Voltage, Any Pin to GND | -0.3 V to $V_{LOGIC}$ +0.3 V |
| Free Air Operating Temperature Range $T_A$ [1] | -40 °C to +85 °C |
| Relative Humidity (noncondensing) | 85% |
| Storage Temperature, $T_S$ | -55 °C to 100 °C |
| Soldering Temperature [1.59 mm (0.063 in.) Below Body] | |
| Solder Dipping | 260 °C for 5 secs |
| Wave Soldering | 250 °C for 3 secs |
| ESD Protection @ 1.5 kΩ, 100 pF (each pin) | Class 1, 0-1999 V |
| TOTAL Package Power Dissipation at $T_A$ = 25 °C [2] | |
| 4 Character | 1.2 W |
| 8 Character | 2.4 W |
| 16 Character | 4.8 W |

**Note:**
1. For operation in high ambient temperatures, see Appendix A, Thermal Considerations.

## Recommended Operating Conditions Over Temperature Range (-40 °C to +85 °C)

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Logic Supply Voltage | $V_{LOGIC}$ | 3.0 | 5.0 | 5.5 | V |
| LED Supply Voltage | $V_{LED}$ | 4.0 | 5.0 | 5.5 | V |
| $GND_{LED}$ to $GND_{LOGIC}$ | | -0.3 | 0 | +0.3 | V |

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## Electrical Characteristics Over Operating Temperature Range (-40 °C to +85 °C)

| Parameter | Symbol | $T_A = 25$ °C, $V_{LOGIC} = 5.0$ V Typ. | Max. | -40 °C < $T_A$ < 85 °C, 3.0 V < $V_{LOGIC}$ < 5.5 V Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_I$ | | | | | µA | $V_{IN}$ = 0 V to $V_{LOGIC}$ |
| HCMS-290x/296x (4 char) | | | +7.5 | -2.5 | +50 | | |
| HCMS-291x/297x (8 char) | | | +15 | -5.0 | +100 | | |
| HCMS-292x (16 char) | | | +15 | -5.0 | +100 | | |
| $I_{LOGIC}$ OPERATING | $I_{LOGIC}$(OPT) | | | | | mA | $V_{IN} = V_{LOGIC}$ |
| HCMS-290x/296x (4 char) | | 0.4 | 2.5 | | 5 | | |
| HCMS-291x/297x (8 char) | | 0.8 | 5 | | 10 | | |
| HCMS-292x (16 char) | | 0.8 | 5 | | 10 | | |
| $I_{LOGIC}$ SLEEP [1] | $I_{LOGIC}$(SLP) | | | | | µA | $V_{IN} = V_{LOGIC}$ |
| HCMS-290x/296x (4 char) | | 5 | 15 | | 25 | | |
| HCMS-291x/297x (8 char) | | 10 | 30 | | 50 | | |
| HCMS-292x (16 char) | | 10 | 30 | | 50 | | |
| $I_{LED}$ BLANK | $I_{LED}$(BL) | | | | | mA | BL = 0 V |
| HMCS-290x/296x (4 char) | | 2.0 | 4 | | 4.0 | | |
| HCMS-291x/297x (8 char) | | 4.0 | 8 | | 8 | | |
| HCMS-292x (16 char) | | 4.0 | 8 | | 8 | | |
| $I_{LED}$ SLEEP [1] | $I_{LED}$(SLP) | | | | | µA | |
| HCMS-290x/296x (4 char) | | 1 | 3 | | 50 | | |
| HCMS 291x/297x (8 char) | | 2 | 6 | | 100 | | |
| HCMS-292x (16 char) | | 2 | 6 | | 100 | | |
| Peak Pixel Current [2] | $I_{PIXEL}$ | | | | | | $V_{LED}$ = 5.5 V |
| HCMS-29x5 (Deep Red) | | 15.4 | 17.1 | | 18.7 | mA | All pixels ON, |
| HCMS-29xx (Other Colors) | | 14.0 | 15.9 | | 17.1 | mA | Average value per pixel |
| HIGH Level Input Voltage | $V_{ih}$ | | | 2.0 | | V | 4.5 V < $V_{LOGIC}$ < 5.5 V |
| | | | | 0.8 $V_{LOGIC}$ | | V | 3.0 V < $V_{LOGIC}$ < 4.5 V |
| LOW Level Input Voltage | $V_{il}$ | | | | 0.8 | V | 4.5 V < $V_{LOGIC}$ < 5.5 V |
| | | | | | 0.2 $V_{LOGIC}$ | V | 3.0 V < $V_{LOGIC}$ < 4.5 V |
| HIGH Level Output Voltage | $V_{oh}$ | | | 2.0 | | V | $V_{LOGIC}$ = 4.5 V, $I_{oh}$ = -40 µA |
| | | | | 0.8 $V_{LOGIC}$ | | V | 3.0 V < $V_{LOGIC}$ < 4.5 V |
| LOW Level Output Voltage | $V_{ol}$ | | | | 0.4 | V | $V_{LOGIC}$ = 5.5 V, $I_{ol}$ = 1.6 mA [3] |
| | | | | | 0.2 $V_{LOGIC}$ | V | 3.0 V < $V_{LOGIC}$ < 4.5 V |
| Thermal Resistance | $R\theta_{J-P}$ | 70 | | | | °C/W | IC junction to pin |

**Notes:**
1. In SLEEP mode, the internal oscillator and reference current for LED drivers are off.
2. Average peak pixel current is measured at the maximum drive current set by Control Register 0. Individual pixels may exceed this value.
3. For the Oscillator Output, $I_{ol}$ = 40 µA.

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**Optical Characteristics at 25 °C[1]**

$V_{LED}$ = 5.0 V, 50% Peak Current, 100% Pulse Width

| Display Color | Part Number | Luminous Intensity per LED [2] Character Average (μcd) Min. | Typ. | Peak Wavelength $\lambda_{Peak}$ (nm) Typ. | Dominant Wavelength $\lambda_d$ [3] (nm) Typ. |
|---|---|---|---|---|---|
| Deep Red | HCMS-29x5 | 95 | 2035 | 645 | 637 |
| High Efficiency Red | HCMS-29x2 | 64 | 270 | 635 | 626 |
| Orange | HCMS-29x4 | 64 | 180 | 600 | 602 |
| Yellow | HCMS-29x1 | 64 | 180 | 583 | 585 |
| Green | HCMS-29x3 | 64 | 270 | 568 | 574 |

**Notes:**
1. Refers to the initial case temperature of the device immediately before measurement.
2. Measured with all LEDs illuminated.
3. Dominant wavelength, $\lambda_d$, is derived from the CIE chromaticity diagram and represents the single wavelength, which defines the perceived LED color.

## Electrical Description

| Pin Function | Description |
|---|---|
| $\overline{\text{RESET}}$ ($\overline{\text{RST}}$) | Sets Control Register bits to logic low. The Dot Register contents are unaffected by the Reset pin. (logic low = reset; logic high = normal operation). |
| DATA IN ($D_{IN}$) | Serial Data input for Dot or Control Register data. Data is entered on the rising edge of the Clock input. |
| DATA OUT ($D_{OUT}$) | Serial Data output for Dot or Control Register data. This pin is used for cascading multiple displays. |
| CLOCK (CLK) | Clock input for writing Dot or Control Register data. When $\overline{\text{Chip}}$ $\overline{\text{Enable}}$ is logic low, data is entered on the rising Clock edge. |
| REGISTER SELECT (RS) | Selects Dot Register (RS = logic low) or Control Register (RS = logic high) as the destination for serial data entry. The logic level of RS is latched on the falling edge of the $\overline{\text{Chip}}$ $\overline{\text{Enable}}$ input. |
| $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$) | This input must be a logic low to write data to the display. When $\overline{\text{CE}}$ returns to logic high and CLK is logic low, data is latched to either the LED output drivers or a Control Register. |
| OSCILLATOR SELECT (SEL) | Selects either an internal or external display oscillator source. (logic low = External Display Oscillator; logic high = Internal Display Oscillator). |
| OSCILLATOR (OSC) | Output for the Internal Display Oscillator (SEL = logic high) or input for an External Display Oscillator (SEL = logic low). |
| BLANK (BL) | Blanks the display when logic high. May be modulated for brightness control. |
| $GND_{LED}$ | Ground for LED drivers. |
| $GND_{LOGIC}$ | Ground for logic. |
| $V_{LED}$ | Positive supply for LED drivers. |
| $V_{LOGIC}$ | Positive supply for logic. |

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**AC Timing Characteristics Over Temperature Range (-40 °C to +85 °C)**

| Timing Diagram Ref. Number | Description | Symbol | 4.5 V < $V_{LOGIC}$ <5.5 V Min. | Max. | $V_{LOGIC}$ = 3 V Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| 1 | Register Select Setup Time to $\overline{\text{Chip}}$ $\overline{\text{Enable}}$ | $t_{rss}$ | 10 | | 10 | | ns |
| 2 | Register Select Hold Time to $\overline{\text{Chip}}$ $\overline{\text{Enable}}$ | $t_{rsh}$ | 10 | | 10 | | ns |
| 3 | Rising Clock Edge to Falling $\overline{\text{Chip}}$ $\overline{\text{Enable}}$ Edge | $t_{clkce}$ | 20 | | 20 | | ns |
| 4 | $\overline{\text{Chip}}$ $\overline{\text{Enable}}$ Setup Time to Rising Clock Edge | $t_{ces}$ | 35 | | 55 | | ns |
| 5 | $\overline{\text{Chip}}$ $\overline{\text{Enable}}$ Hold Time to Rising Clock Edge | $t_{ceh}$ | 20 | | 20 | | ns |
| 6 | Data Setup Time to Rising Clock Edge | $t_{ds}$ | 10 | | 10 | | ns |
| 7 | Data Hold Time after Rising Clock Edge | $t_{dh}$ | 10 | | 10 | | ns |
| 8 | Rising Clock Edge to $D_{OUT}$ [1] | $t_{dout}$ | 10 | 40 | 10 | 65 | ns |
| 9 | Propagation Delay $D_{IN}$ to $D_{OUT}$ Simultaneous Mode for One IC [1,2] | $t_{doutp}$ | | 18 | | 30 | ns |
| 10 | $\overline{\text{CE}}$ Falling Edge to $D_{OUT}$ Valid | $t_{cedo}$ | | 25 | | 45 | ns |
| 11 | Clock High Time | $t_{clkh}$ | 80 | | 100 | | ns |
| 12 | Clock Low Time | $t_{clkl}$ | 80 | | 100 | | ns |
| | Reset Low Time | $t_{rstl}$ | 50 | | 50 | | ns |
| | Clock Frequency | $F_{cyc}$ | | 5 | | 4 | MHz |
| | Internal Display Oscillator Frequency | $F_{inosc}$ | 80 | 210 | 80 | 210 | kHz |
| | Internal Refresh Frequency | $F_{rf}$ | 150 | 410 | 150 | 400 | Hz |
| | External Display Oscillator Frequency | $F_{exosc}$ | | | | | |
| | Prescaler = 1 | | 51.2 | 1000 | 51.2 | 1000 | kHz |
| | Prescaler = 8 | | 410 | 8000 | 410 | 8000 | kHz |

**Notes:**
1. Timing specifications increase 0.3 ns per pF of capacitive loading above 15 pF.
2. This parameter is valid for Simultaneous Mode data entry of the Control Register.

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## Display Overview

The HCMS-29xx series is a family of LED displays driven by on-board CMOS ICs. The LEDs are configured as 5 x 7 font characters and are driven in groups of 4 characters per IC. Each IC consists of a 160-bit shift register (the Dot Register), two 7-bit Control Words, and refresh circuitry. The Dot Register contents are mapped on a one-to-one basis to the display. Thus, an individual Dot Register bit uniquely controls a single LED.

8-character displays have two ICs that are cascaded. The Data Out line of the first IC is internally connected to the Data In line of the second IC forming a 320-bit Dot Register. The display's other control and power lines are connected directly to both ICs. In 16-character displays, each row functions as an independent 8-character display with its own 320-bit Dot Register.

## Reset

Reset initializes the Control Registers (sets all Control Register bits to logic low) and places the display in the sleep mode. The $\overline{\text{Reset}}$ pin should be connected to the system power-on reset circuit. The Dot Registers are not cleared upon power-on or by $\overline{\text{Reset}}$. After power-on, the Dot Register contents are random; however, $\overline{\text{Reset}}$ will put the display in sleep mode, thereby blanking the LEDs. The Control Register and the Control Words are cleared to all zeros by $\overline{\text{Reset}}$.

To operate the display after being $\overline{\text{Reset}}$, load the Dot Register with logic lows. Then load Control Word 0 with the desired brightness level and set the sleep mode bit to logic high.

## Dot Register

The Dot Register holds the pattern to be displayed by the LEDs. Data is loaded into the Dot Register according to the procedure shown in Table 1 and the Write Cycle Timing Diagram.

First RS is brought low, then $\overline{\text{CE}}$ is brought low. Next, each successive rising CLK edge will shift in the data at the $D_{IN}$ pin. Loading a logic high will turn the corresponding LED on; a logic low turns the LED off. When all 160 bits have been loaded (or 320 bits in an 8-digit display), $\overline{\text{CE}}$ is brought to logic high.

When CLK is next brought to logic low, new data is latched into the display dot drivers. Loading data into the Dot Register takes place while the previous data is displayed and eliminates the need to blank the display while loading data.

## Pixel Map

In a 4-character display, the 160-bits are arranged as 20 columns by 8 rows. This array can be conceptualized as four 5 x 8 dot matrix character locations, but only 7 of the 8 rows have LEDs (see Figures 1 & 2). The bottom row (row 0) is not used. Thus, latch location 0 is never displayed. Column 0 controls the left-most column. Data from Dot Latch locations 0-7 determine whether or not pixels in Column 0 are turned-on or turned-off. Therefore, the lower left pixel is turned-on when a logic high is stored in Dot Latch location 1. Characters are loaded in serially, with the left-most character being loaded first and the right-most character being loaded last. By loading one character at a time and latching the data before loading the next character, the figures will appear to scroll from right to left.

**Table 1. Register Truth Table**

| Function | CLK | $\overline{\text{CE}}$ | RS |
|---|---|---|---|
| Select Dot Register | Not Rising | ↓ | L |
| Load Dot Register<br>$D_{IN}$ = HIGH LED = "ON"<br>$D_{IN}$ = LOW LED = "OFF" | ↑ | L | X |
| Copy Data from Dot Register to Dot Latch | L | H | X |
| Select Control Register | Not Rising | ↓ | H |
| Load Control Register [1,3] | ↑ | L | X |
| Latch Data to Control Word [2] | L | ↑ | X |

**Notes:**

1. BIT $D_0$ of Control Word 1 must have been previously set to Low for serial mode or High for simultaneous mode.
2. Selection of Control Word 1 or Control Word 0 is set by $D_7$ of the Control Shift Register. The unselected control word retains its previous value.
3. Control Word data is loaded Most Significant Bit ($D_7$) first.

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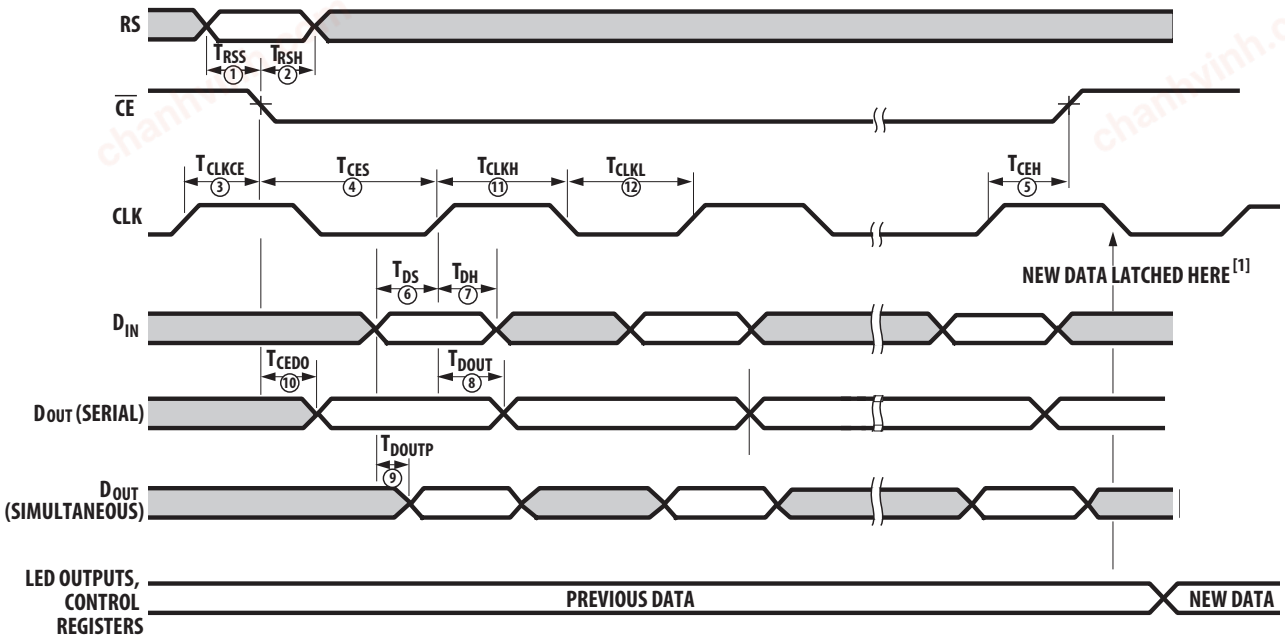
**HCMS-29xx Write Cycle Diagram**




**NOTE:**
**1. DATA IS COPIED TO THE CONTROL REGISTER OR THE DOT LATCH AND LED OUTPUTS WHEN $\overline{CE}$ IS HIGH AND CLK IS LOW.**

## Control Register

The Control Register allows software modification of the IC's operation and consists of two independent 7-bit control words. Bit $D_7$ in the shift register selects one of the two 7-bit control words. Control Word 0 performs pulse width modulation brightness control, peak pixel current brightness control, and sleep mode. Control Word 1 sets serial/simultaneous data out mode, and external oscillator prescaler. Each function is independent of the others.

## Control Register Data Loading

Data is loaded into the Control Register, MSB first, according to the procedure shown in Table 1 and the Write Cycle Timing Diagram. First, RS is brought to logic high and then $\overline{CE}$ is brought to logic low. Next, each successive rising CLK edge will shift in the data on the $D_{IN}$ pin. Finally, when 8 bits have been loaded, the $\overline{CE}$ line is brought to logic high. When CLK goes to logic low, new data is copied into the selected control word. Loading data into the Control Register takes place while the previous control word configures the display.

## Control Word 0

Loading the Control Register with $D_7$ = Logic low selects Control Word 0 (see Table 2). Bits $D_0$-$D_3$ adjust the display brightness by pulse width modulating the LED on-time, while Bits $D_4$-$D_5$ adjust the display brightness by changing the peak pixel current. Bit $D_6$ selects normal operation or sleep mode.

Sleep mode (Control Word 0, bit $D_6$ = Low) turns off the Internal Display Oscillator and the LED pixel drivers. This mode is used when the IC needs to be powered up, but does not need to be active. Current draw in sleep mode is nearly zero. Data in the Dot Register and Control Words are retained during sleep mode.

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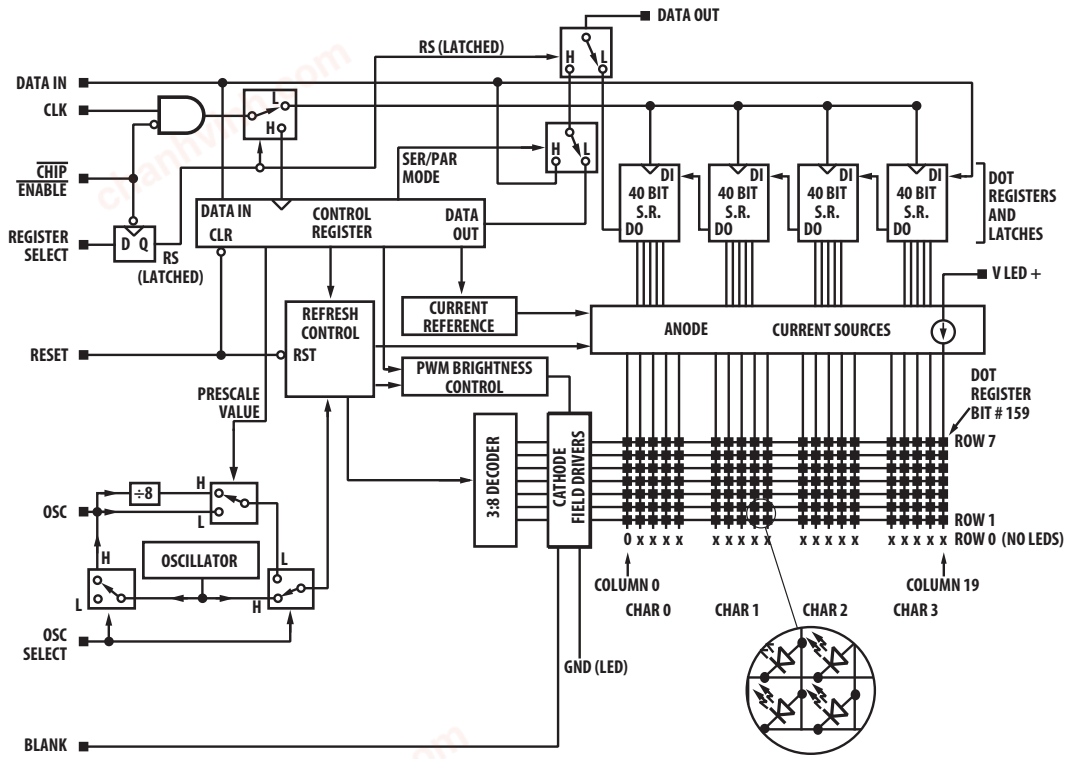


**Figure 1.**

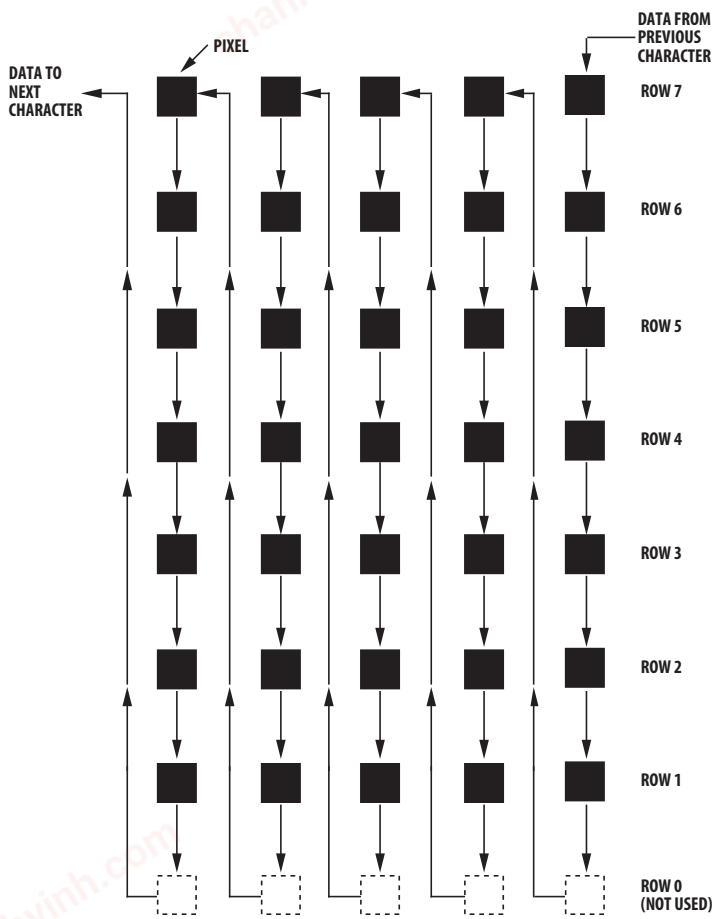


**Figure 2.**

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### Control Word 1

Loading the Control Register with $D_7$ = logic high selects Control Word 1. This Control Word performs two functions: serial/simultaneous data out mode and external oscillator prescale select (see Table 2).

### Serial/Simultaneous Data Output $D_0$

Bit $D_0$ of control word 1 is used to switch the mode of $D_{OUT}$ between serial and simultaneous data entry during Control Register writes. The default mode (logic low) is the serial $D_{OUT}$ mode. In serial mode, $D_{OUT}$ is connected to the last bit ($D_7$) of the Control Shift Register.

Storing a logic high to bit $D_0$ changes $D_{OUT}$ to simultaneous mode which affects the Control Register only. In simultaneous mode, $D_{OUT}$ is logically connected to $D_{IN}$. This arrangement allows multiple ICs to have their Control Registers written to simultaneously. For example, for N ICs in the serial mode, N*8 clock pulses are needed to load the same data in all Control Registers. In the simultaneous mode, N ICs only need 8 clock pulses to load the same data in all Control Registers. The propagation delay from the first IC to the last is $N * t_{DOUTP}$.

### External Oscillator Prescaler Bit $D_1$

Bit $D_1$ of Control Word 1 is used to scale the frequency of an external Display Oscillator. When this bit is logic low, the external Display Oscillator directly sets the internal display clock rate. When this bit is a logic high, the external oscillator is divided by 8. This scaled frequency then sets the internal display clock rate. It takes 512 cycles of the display clock (or 8 x 512 = 4096 cycles of an external clock with the divide by 8 prescaler) to completely refresh the display once. Using the prescaler bit allows the designer to use a higher external oscillator frequency without extra circuitry.

This bit has no affect on the internal Display Oscillator Frequency.

### Bits $D_2$-$D_6$

These bits must always be programmed to logic low.

### Cascaded ICs

Figure 3 shows how two ICs are connected within an HCMS-29xx display. The first IC controls the four left-most characters and the second IC controls the four right-most characters. The Dot Registers are connected in series to form a 320-bit dot shift register. The location of pixel 0 has not changed. However, Dot Shift Register bit 0 of IC2 becomes bit 160 of the 320-bit dot shift register.

The Control Registers of the two ICs are independent of each other. This means that to adjust the display brightness the same control word must be entered into both ICs, unless the Control Registers are set to simultaneous mode.

Longer character string systems can be built by cascading multiple displays together. This is accomplished by creating a five line bus. This bus consists of $\overline{CE}$, RS, BL, Reset, and CLK. The display pins are connected to the corresponding bus line. Thus, all $\overline{CE}$ pins are connected to the $\overline{CE}$ bus line. Similarly, bus lines for RS, BL, Reset, and CLK are created. Then $D_{IN}$ is connected to the right-most display. $D_{OUT}$ from this display is connected to the next display. The left-most display receives its $D_{IN}$ from the $D_{OUT}$ of the display to its right. $D_{OUT}$ from the left-most display is not used.

Each display may be set to use its internal oscillator, or the displays may be synchronized by setting up one display as the master and the others as slaves. The slaves are set to receive their oscillator input from the master's oscillator output.

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**Table 2. Control Shift Register**

CONTROL WORD 0

| L | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|

Bit $D_7$ Set Low to Select Control Word 0

**PWM Brightness Control**

| | | | | On-Time Oscillator Cycles | Duty Factor (%) | Relative Brightness (%) |
|---|---|---|---|---|---|---|
| L | L | L | L | 0 | 0 | 0 |
| L | L | L | H | 1 | 0.2 | 1.7 |
| L | L | H | L | 2 | 0.4 | 3.3 |
| L | L | H | H | 3 | 0.6 | 5.0 |
| L | H | L | L | 4 | 0.8 | 6.7 |
| L | H | L | H | 5 | 1.0 | 8.3 |
| L | H | H | L | 7 | 1.4 | 11.7 |
| L | H | H | H | 9 | 1.8 | 15 |
| H | L | L | L | 11 | 2.1 | 18 |
| H | L | L | H | 14 | 2.7 | 23 |
| H | L | H | L | 18 | 3.5 | 30 |
| H | L | H | H | 22 | 4.3 | 37 |
| H | H | L | L | 28 | 5.5 | 47 |
| H | H | L | H | 36 | 7.0 | 60 |
| H | H | H | L | 48 | 9.4 | 80 |
| H | H | H | H | 60 | 11.7 | 100 |

**Peak Current Brightness Control**

| | | Typical Peak Pixel Current (mA) | Relative Full Scale Current (Relative Brightness, %) |
|---|---|---|---|
| H | L | 4.0 | 31 |
| L | H | 6.4 | 50 |
| L | L | 9.3 | 73 (Default at Power Up) |
| H | H | 12.8 | 100 |

**SLEEP MODE**

L – DISABLES INTERNAL OSCILLATOR-DISPLAY BLANK
H – NORMAL OPERATION

CONTROL WORD 1

| H | L | L | L | L | L | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|

Bit $D_7$ Set High to Select Control Word 1

Reserved for Future Use (Bits $D_2$-$D_6$ must be set Low)

Serial/Simultaneous Data Out
L – $D_{out}$ holds contents of Bit $D_7$
H – $D_{out}$ is functionally tied to $D_{in}$

External Display Oscillator Prescaler
L – Oscillator Freq 1
H – Oscillator Freq 8

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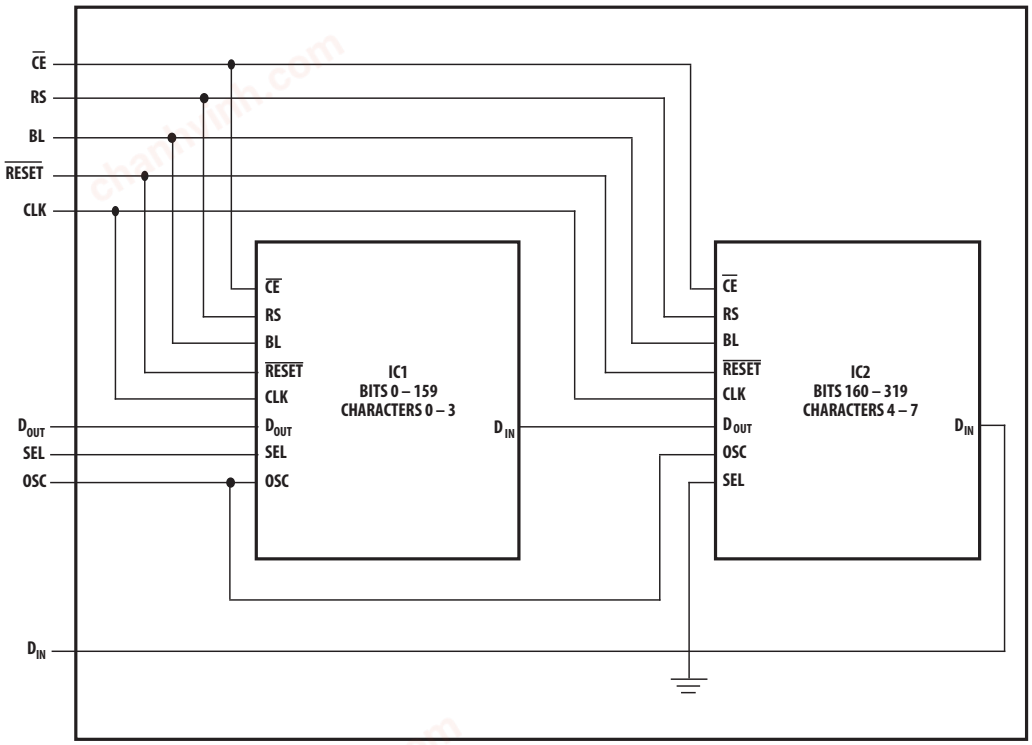


**Figure 3. Cascaded ICs**

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## Appendix A. Thermal Considerations

The display IC has a maximum junction temperature of 150°C. The IC junction temperature can be calculated with Equation 1.

A typical value for $R\theta_{J-A}$ is 100 °C/W. This value is typical for a display mounted in a socket and covered with a plastic filter. The socket is soldered to a .062 in. thick PCB with .020 inch wide, one ounce copper traces.

$P_D$ can be calculated as in Equation 2.

Figure 4 shows how to derate the power of one IC versus ambient temperature. Operation at high ambient temperatures may require the power per IC to be reduced. The power consumption can be reduced by changing either the N, $I_{PIXEL}$, Osc cyc or $V_{LED}$. Changing $V_{LOGIC}$ has very little impact on the power consumption.

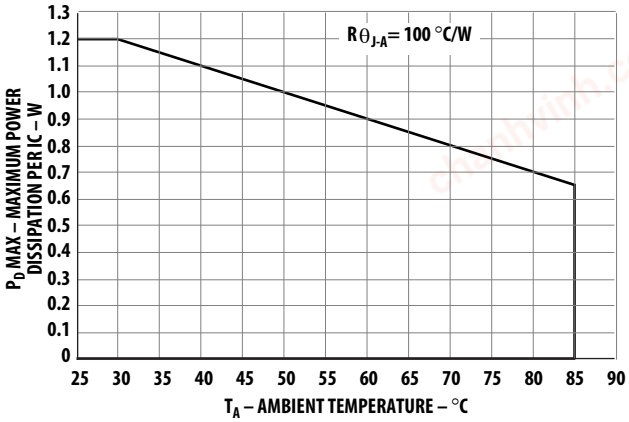


**Figure 4.**

## Appendix B. Electrical Considerations

**Equation 1:**

$T_JMAX = T_A + P_D * R\theta_{JA}$

Where:

$T_JMAX$ = maximum IC junction temperature
$T_A$ = ambient temperature surrounding the display
$R\theta_{JA}$ = thermal resistance from the IC junction to ambient
$P_D$ = power dissipated by the IC

**Equation 2:**

$P_D = (N * I_{PIXEL} * \text{Duty Factor} * V_{LED}) + I_{LOGIC} * V_{LOGIC}$

Where:

$P_D$ = total power dissipation
N = number of pixels on (maximum 4 char * 5 * 7 = 140)
$I_{PIXEL}$ = peak pixel current.
Duty Factor = 1/8 * Osc cyc/64
Osc cyc = number of ON oscillator cycles per row
$I_{LOGIC}$ = IC logic current
$V_{LOGIC}$ = logic supply voltage

**Equation 3:**

$I_{PEAK} = M * 20 * I_{PIXEL}$

Where:

$I_{PEAK}$ = maximum instantaneous peak current for the display
M = number of ICs in the system
20 = maximum number of LEDs on per IC
$I_{PIXEL}$ = peak current for one LED

**Equation 4:**

$I_{LED}(AVG) = N * I_{PIXEL} * 1/8 * (\text{oscillator cycles})/64$

(see Variable Definitions above)

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## Current Calculations

The peak and average display current requirements have a significant impact on power supply selection. The maximum peak current is calculated with Equation 3.

The average current required by the display can be calculated with Equation 4.

The power supply has to be able to supply $I_{PEAK}$ transients and supply $I_{LED}$(AVG) continuously. The range on $V_{LED}$ allows noise on this supply without significantly changing the display brightness.

## $V_{LOGIC}$ and $V_{LED}$ Considerations

The display uses two independent electrical systems. One system is used to power the display's logic and the other to power the display's LEDs. These two systems keep the logic supply clean.

Separate electrical systems allow the voltage applied to $V_{LED}$ and $V_{LOGIC}$ to be varied independently. Thus, $V_{LED}$ can vary from 0 to 5.5 V without affecting either the Dot or the Control Registers. $V_{LED}$ can be varied between 4.0 to 5.5 V without any noticeable variation in light output. However, operating $V_{LED}$ below 4.0 V may cause objectionable mismatch between the pixels and is not recommended. Dimming the display by pulse width modulating $V_{LED}$ is also not recommended.

$V_{LOGIC}$ can vary from 3.0 V to 5.5 V without affecting either the displayed message or the display intensity. However, operation below 4.5 V will change the timing and logic levels and operation below 3 V may cause the Dot and Control Registers to be altered.

The logic ground is internally connected to the LED ground by a substrate diode. This diode becomes forward biased and conducts when the logic ground is 0.4 V greater than the LED ground. The LED ground and the logic ground should be connected to a common ground which can withstand the current introduced by the switching LED drivers. When separate ground connections are used, the LED ground can vary from -0.3 V to +0.3 V with respect to the logic ground. Voltages below -0.3 V can cause all the dots to be ON. Voltage above +0.3 V can cause dimming and dot mismatch. The LED ground for the LED drivers can be routed separately from the logic ground until an appropriate ground plane is available. On long interconnections between the display and the host system, voltage drops on the analog ground can be kept from affecting the display logic levels by isolating the two grounds.

## Electrostatic Discharge

The inputs to the ICs are protected against static discharge and input current latchup. However, for best results, standard CMOS handling precautions should be used. Before use, the HCMS-29xx should be stored in antistatic tubes or in conductive material. During assembly, a grounded conductive work area should be used and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static buildup. Input current latchup is caused when the CMOS inputs are subjected to either a voltage below ground ($V_{IN}$ < ground) or to a voltage higher than $V_{LOGIC}$ ($V_{IN} > V_{LOGIC}$) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected to either ground or $V_{LOGIC}$. Voltages should not be applied to the inputs until $V_{LOGIC}$ has been applied to the display.

## Appendix C. Oscillator

The oscillator provides the internal refresh circuitry with a signal that is used to synchronize the columns and rows. This ensures that the right data is in the dot drivers for that row. This signal can be supplied from either an external source or the internal source.

A display refresh rate of 100 Hz or faster ensures flicker-free operation. Thus for an external oscillator the frequency should be greater than or equal to 512 x 100 Hz = 51.2 kHz. Operation above 1 MHz without the prescaler or 8 MHz with the prescaler may cause noticeable pixel to pixel mismatch.

## Appendix D. Refresh Circuitry

This display driver consists of 20 one-of-eight column decoders and 20 constant current sources, 1 one-of-eight row decoder and eight row sinks, a pulse width modulation control block, a peak current control block, and the circuit to refresh the LEDs. The refresh counters and oscillator are used to synchronize the columns and rows.

The 160 bits are organized as 20 columns by 8 rows. The IC illuminates the display by sequentially turning ON each of the 8 row-drivers. To refresh the display once takes 512 oscillator cycles. Because there are eight row drivers, each row driver is selected for 64 (512/8) oscillator cycles. Four cycles are used to briefly blank the display before the following row is switched on. Thus, each row is ON for 60 oscillator cycles out of a possible 64. This corresponds to the maximum LED on time.

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## Appendix E. Display Brightness

Two ways have been shown to control the brightness of this LED display: setting the peak current and setting the duty factor. Both values are set in Control Word 0. To compute the resulting display brightness when both PWM and peak current control are used, simply multiply the two relative brightness factors. For example, if Control Register 0 holds the word 1001101, the peak current is 73% of full scale (BIT $D_5$ = L, BIT $D_4$ = L) and the PWM is set to 60% duty factor (BIT $D_3$ = H, BIT $D_2$ = H, BIT $D_1$ = L, BIT $D_0$ = H). The resulting brightness is 44% (.73 x .60 = .44) of full scale.

The temperature of the display will also affect the LED brightness as shown in Figure 5.

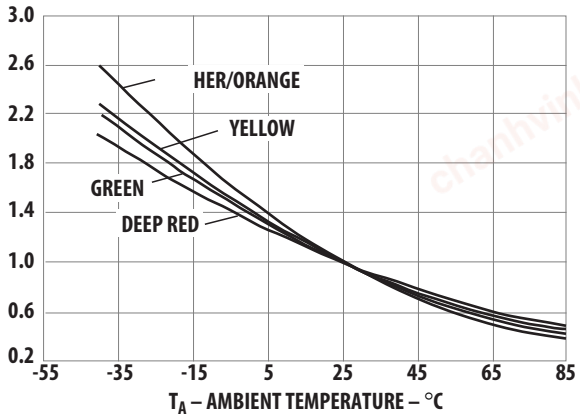


**Figure 5.**

## Appendix F. Reference Material

Application Note 1027: *Soldering LED Components*

Application Note 1015: *Contrast Enhancement Techniques for LED Displays*



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