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APDS-9306/APDS-9306-065

Miniature Surface-Mount Digital Ambient Light Sensor

AVAGO TECHNOLOGIES
A Broadcom Limited Company

Data Sheet

Description

Avago Technologies' APDS-9306/APDS-9306-065 is a low-voltage Digital Ambient Light Sensor that converts light intensity to digital signal output with I^2C interface. It consists of photodiode, ADC, oscillator and power-on reset to ensure consistent start-up. ADCs convert the photodiode currents to a digital output and the device is capable of rejecting 50Hz and 60Hz flicker caused by artificial light sources.

The APDS-9306/APDS-9306-065 approximates the response of the human-eye providing direct read out, where the output count is proportional to ambient light level. Low light functionality enables operation behind darkened glass. The APDS-9306/APDS-9306-065 supports programmable hardware interrupt with hysteresis to respond to events.

APDS-9306 ultra slim form factor with a height of only 0.34mm and APDS-9306-065 with a height of 0.65mm enables the sensor to be designed into space-sensitive applications.

Applications

- Detection of ambient light to control display backlighting
  - o Wearable devices – Smart watch, Sport Watch
  - o Mobile devices – Cell phones, PDAs, PMP
  - o Computing devices – Notebooks, Tablet PC, Key board
  - o Consumer devices – LCD Monitor, Flat-panel TVs, Video Cameras, Digital Still Camera
- Automatic Residential and Commercial Lighting Management

Features

- Ambient Light Sensing
  - Utilizes Coating Technology to Emulate Human Eye Spectral Response
  - High Sensitivity in Low Lux Condition – Ideally Suited for Operation Behind Dark Glass
  - Wide Dynamic Range 18,000,000 : 1
  - Low Lux Performance 0.01 lux
  - Up to 20-Bit Resolution
- Wide Power Supply Range 1.7V to 3.6V
  - 50Hz/60Hz light flicker immunity
  - Fluorescent light flicker immunity
- Power Management
  - Low Active Current: 85 µA typical
- I^2C-bus Interface Compatible
  - Up to 400 kHz (I^2C Fast-Mode)
  - Dedicated Interrupt Pin
- Small Package:
  - APDS-9306: L2.0 x W2.0 x H0.34mm
  - APDS-9306-065: L2.0 x W2.0 x H0.65mm

Ordering Information

Part Number	Packaging	Quantity
APDS-9306	Tape & Reel	2500 per reel
APDS-9306-065	Tape & Reel	2500 per reel

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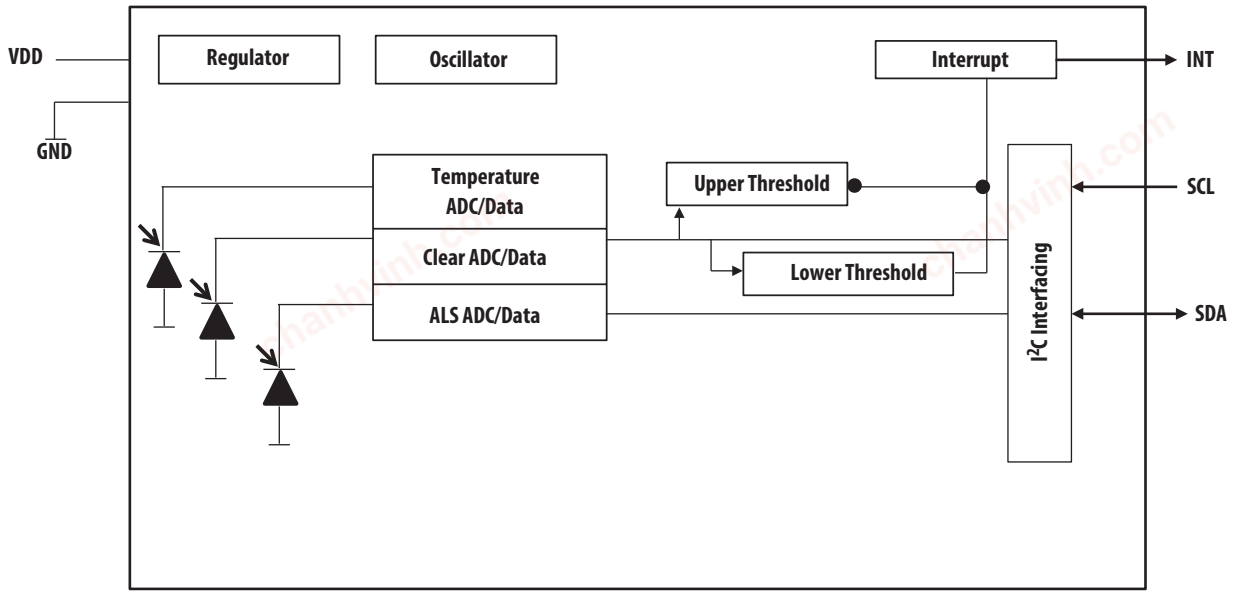
Functional Block Diagram



I/O Pins Configuration

APDS-9306 I/O Pins Configuration

Pin	Name	Type	Description
1	GND	Ground	Power supply ground. All voltages are referenced to GND
2	NC		No Connect
3	NC		No Connect
4	V_{DD}	Supply	Power supply voltage
5	SCL	I	I^2C serial clock input terminal – clock signal for I^2C serial data
6	SDA	I/O	I^2C serial data I/O terminal – serial data I/O for I^2C
7	INT	O	Interrupt – open drain
8	NC		No Connect

APDS-9306-065 I/O Pins Configuration

Pin	Name	Type	Description
1	SCL	I	I2C serial clock input terminal - clock signal for I^2C serial data
2	SDA	I/O	Serial Data I/O for I^2C
3	VDD	Supply	Power Supply Voltage
4	INT	O	Interrupt - Open Drain
5	NC		No Connect
6	GND	Ground	Power supply ground. All voltages are referenced to GND

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Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)+

Parameter	Symbol	Min	Max	Units	Conditions
Power Supply Voltage [1]	V_{DD}		3.8	V	
Max Voltage on SCL, SDA, INT pads	V_O	-0.5	3.8	V	
Storage Temperature Range	T_{stg}	–45	85	°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating Ambient Temperature	T_A	-40		85	°C
Supply Voltage	V_{DD}	1.7		3.6	V
Supply Voltage Accuracy, V_{DD} total error including transients		-3		3	%

Operating Characteristics $V_{DD} = 2.8$ V, $T_A = 25$°C (unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Current	I_{DD}		85		µA	G=18x, 50ms
	I_{STBY}			2	µA	In Standby Mode. No active I^2C communication
SCL, SDA Input High Voltage	V_{IH}	1.5		VDD	V	
SCL, SDA Input Low Voltage	V_{IL}	0		0.4	V	
VOL , INT, Output Low Voltage	V_{OL}	0		0.4	V	
Leakage Current, SDA, SCL, INT Pins	I_{LEAK}	-5		5	µA	

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ALS Characteristics, V_{DD} = 2.8 V, T_A = 25°C (unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Wavelength	λ_P		560		nm	
Output Resolution		13	18	20	bit	Programmable
Dark ALS ADC Count Value		0		3	counts	G=18x, 50ms
ALS ADC Count Value		1600	2000	2400	counts	G=3x, 100msec, λ=530nm, Ee=49.8μW/cm^2 [1] Ee=43 μW/cm^2 [2]
ALS ADC Integration Time		25		400	ms	With 50/60Hz rejection
Gain Scaling, Relative to 1x Gain Setting			3 6 9 18			AGAIN = 3x AGAIN = 6x AGAIN = 9x AGAIN = 18x

Notes
1. Applies to APDS-9306
2. Applies to APDS-9306-065

Characteristics of the SDA and SCL bus lines, V_{DD} = 2.8 V, T_A = 25°C (unless otherwise noted) †

Parameter	Symbol	Min.	Max.	Unit
SCL Clock Frequency	f_{SCL}	0	400	kHz
Hold Time (repeated) START condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$	0.6	–	μs
LOW Period of the SCL Clock	t_{LOW}	1.3	–	μs
HIGH Period of the SCL Clock	t_{HIGH}	0.6	–	μs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	0.6	–	μs
Data Hold Time	$t_{HD;DAT}$	0	0.9	μs
Data Set-Up Time	$t_{SU;DAT}$	100	–	ns
Clock/Data Fall Time	t_f	0	300	ns
Clock/Data Rise Time	t_r	0	300	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$	0.6	–	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	μs

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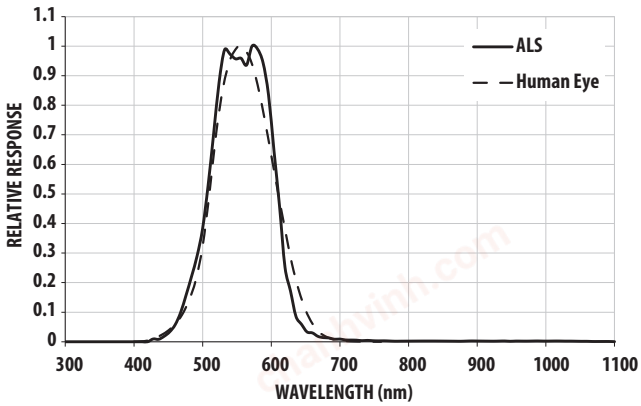

Figure 1. Spectral Response

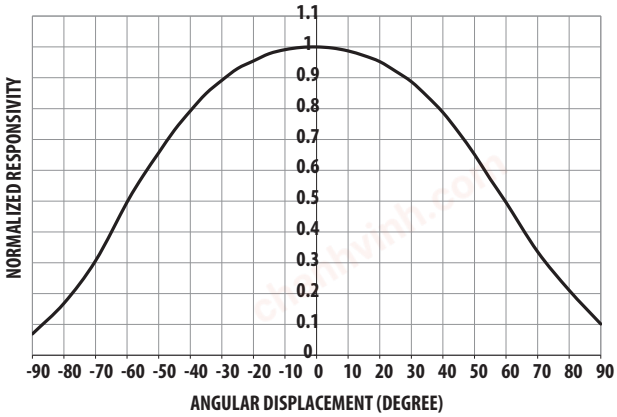

Figure 2. Normalized ALS PD Angular Response

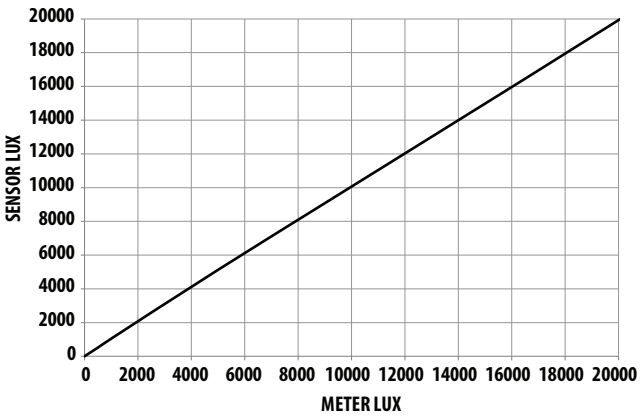

Figure 3. ALS Sensor LUX vs Meter LUX using White Light

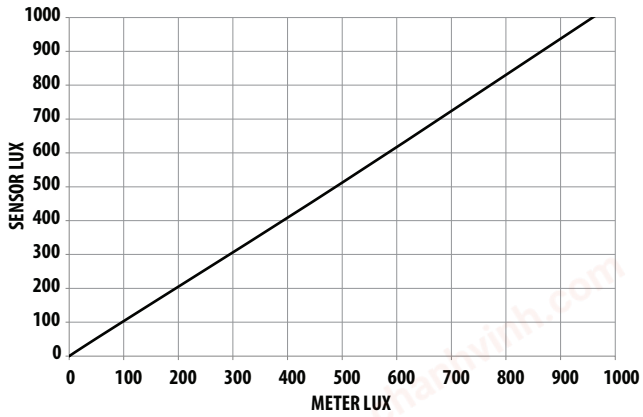

Figure 4. ALS Sensor LUX vs Meter LUX using White Light

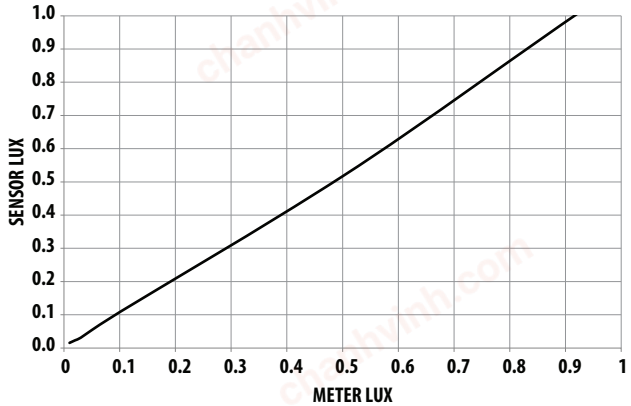

Figure 5. ALS Sensor LUX vs Meter LUX using White Light

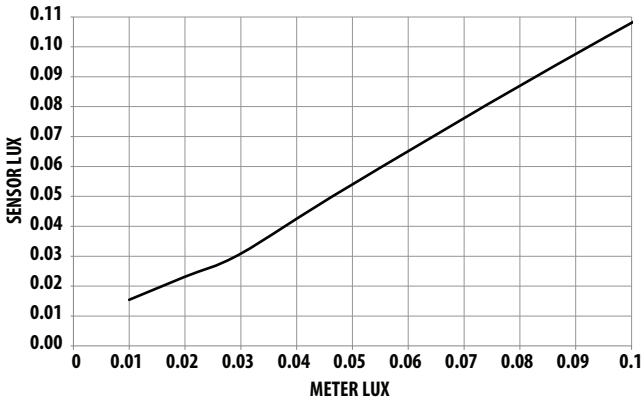

Figure 6. ALS Sensor LUX vs Meter LUX using White Light

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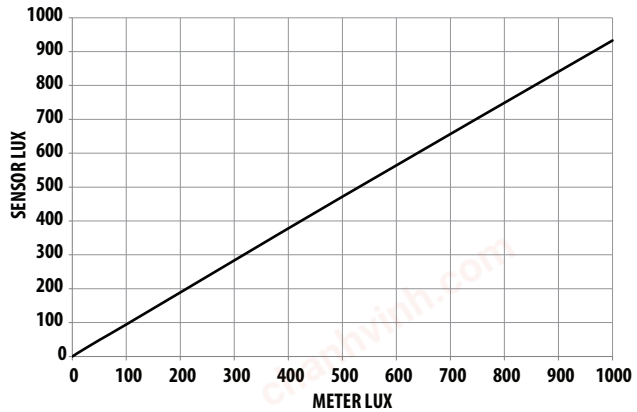

Figure 7. ALS Sensor LUX vs Meter LUX using Incandescent Light

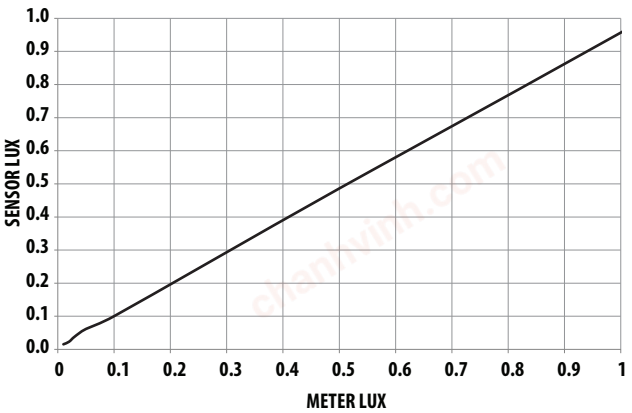

Figure 8. ALS Sensor LUX vs Meter LUX using Incandescent Light

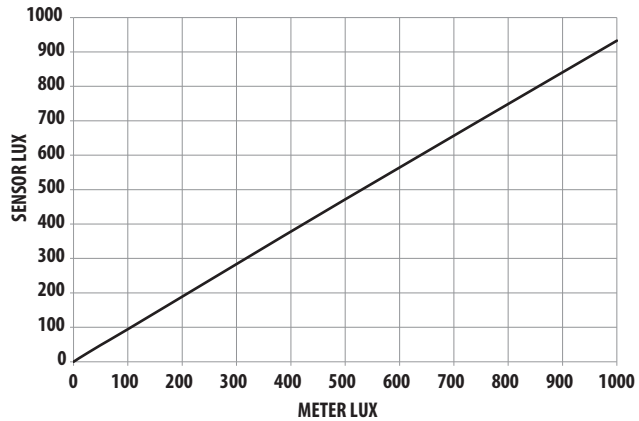

Figure 9. ALS Sensor LUX vs Meter LUX using Halogen Light

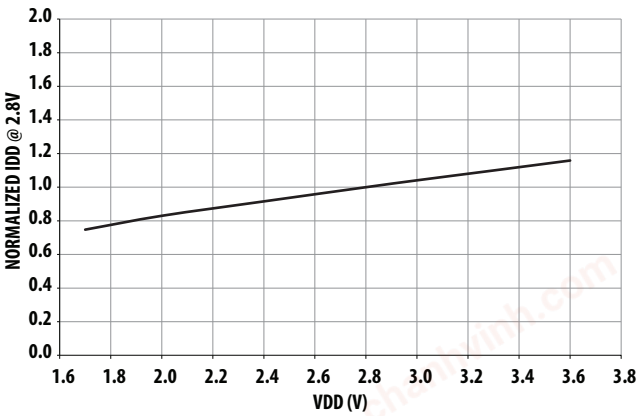

Figure 10. Normalized IDD vs VDD

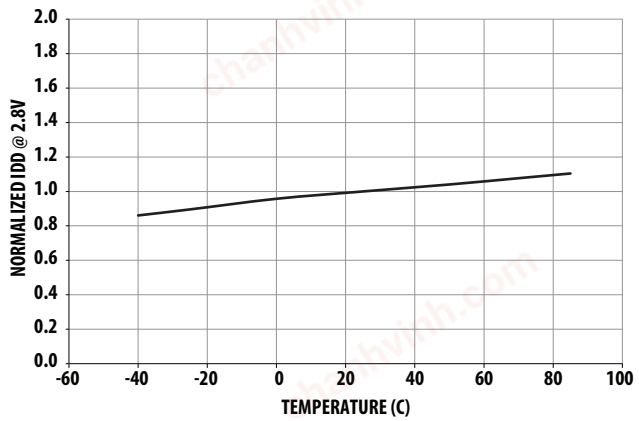

Figure 11. Normalized IDD vs Temperature

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System State Machine

Start Up after Power-On or Software Reset

The main state machine is set to "Start State" during power-on or software reset. As soon as the reset is released, the internal oscillator is started and the programmed I²C address and the trim values are read from the internal non volatile memory (NVM) trimming data block. The device enters Standby Mode as soon as the Idle State is reached.

Note: As long as the I²C address has not yet been reached, the device will respond with NACK to any I²C command and ignore any request to avoid responding to a wrong I²C address.

Standby Mode

Standby Mode is the default mode after power-up. In this state, the oscillator, all internal support blocks, and the ADCs are switched off but I²C communication is fully supported.

Ambient Light Sensor Operation

ALS measurements can be activated by setting the ALS_EN bit to 1 in the MAIN_CTRL register.

As soon as the ALS becomes activated through an I²C command, the internal support blocks are powered on. Once the voltages and currents are settled (typically after 5ms), the state machine checks for trigger events from a measurement scheduler to start the ALS conversions according to the selected measurement repeat rates.

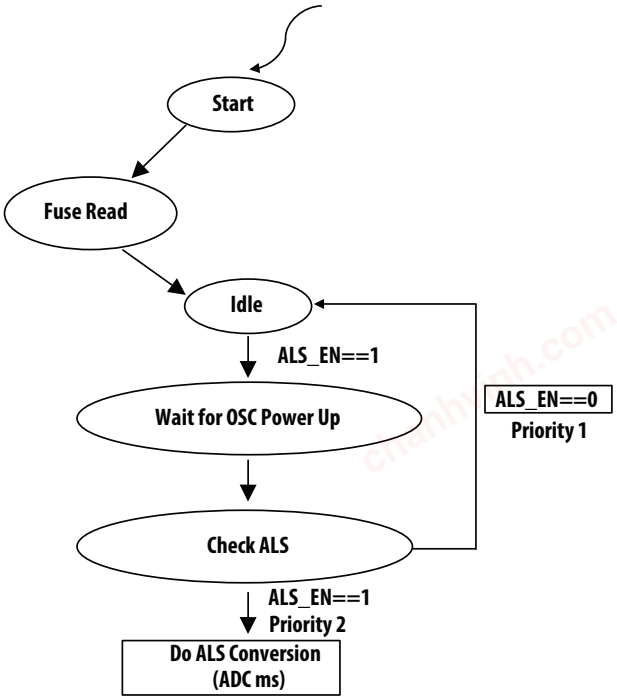
Once ALS_EN is changed back to 0, a conversation running on the respective channel will be completed and the relevant ADCs and support blocks will move to standby mode.

Ambient Light Sensor Interrupt

The ALS interrupt is enabled by ALS_INT_EN=1 and can function as either threshold triggered (ALS_VAR_MODE=0) or variance triggered (ALS_VAR_MODE =1).

The ALS threshold interrupt is enabled with ALS_INT_EN=1 and ALS_VAR_MODE=0. It is set when the ALS data is above the upper or below the lower ALS threshold for a specified number of consecutive measurements (1+ALS_PERSIST)

The ALS variance interrupt is enabled with ALS_INT_EN=1 and ALS_VAR_MODE=1. It is set when the absolute value of the difference between previous and current ALS data is above the decoded ALS variance threshold for a specified number of consecutive measurements (1+ALS_PERSIST).



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I²C Protocol

Interface and control of the APDS-9306/APDS-9306-065 is accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0X52 hex using 7-bit addressing protocol. (Contact factory for other addressing options).

I²C Register Read

The registers can be read individually or in block read mode. When two or more bytes are read in block read mode, reserved register addresses are skipped and the next valid address is referenced. If the last valid address has been reached, but the master continues with the block read, the address counter in the device will not roll over and the device returns 00HEX for every subsequent byte read.

The block read operation is the only way to ensure correct data read out of multi-byte registers and to avoid splitting of results with HIGH and LOW bytes originating from different conversions. During block read access on ALS result registers, the result update is blocked.

If a read access is started on an address belonging to a non-readable register, the APDS-9306/APDS-9306-065 will re-turn NACK until the I²C™ operation is ended.

Read operations must follow the Register Read timing diagram as below.

I²C Register Write

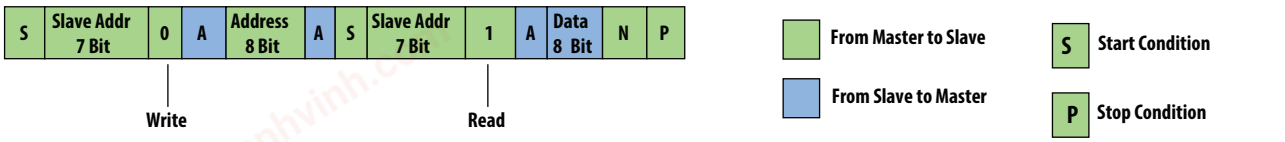
The APDS-9306/APDS-9306-065 registers can be written to individually or in block write mode. When two or more bytes are written in block write mode, reserved registers and read-only registers are skipped. The transmitted data is automatically applied to the next writable register. If a register includes read (R) and read/write (RW) bits, the register is not skipped. Data written to read-only bits are ignored.

If the last valid address of the APDS-9306/APDS-9306-065 address range is reached but the master attempts to continue the block write operation, the address counter of the APDS-9306/APDS-9306-065 will not roll over. The APDS-9306/APDS-9306-065 will return NACK for every following byte sent by the master until the I²C™ operation is ended.

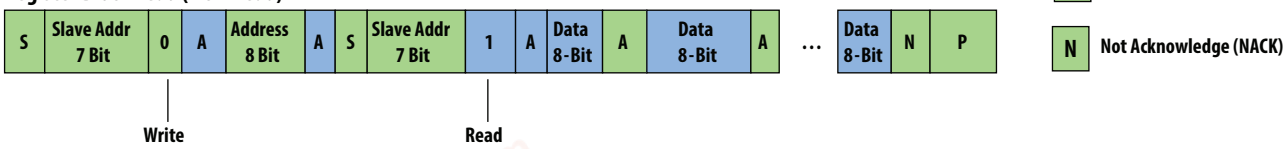
If a write access is started on an address belonging to a non-writeable register, the APDS-9306/APDS-9306-065 will return NACK until the I²C™ operation is ended.

Write operations must follow the Register Write timing diagram below.

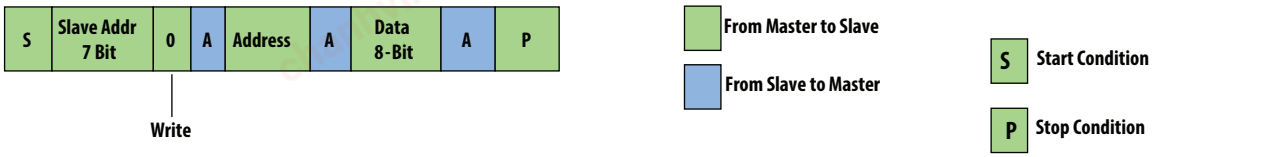
Register Read (I²C™ Read)



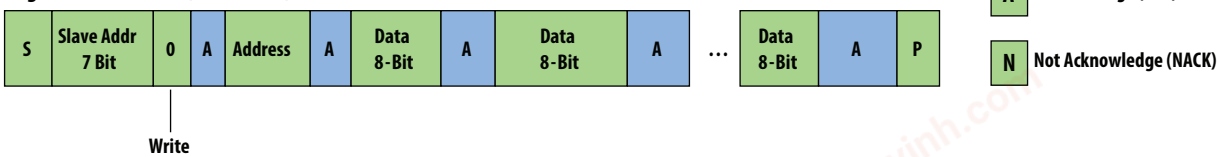
Register Block Read (I²C™ Read)



Register Write (I²C™ Write)



Register Block Write (I²C™ Write)



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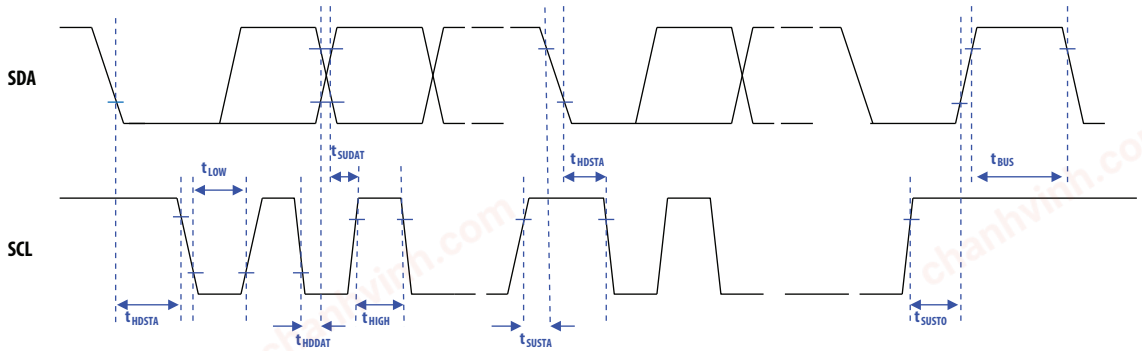
I²C Interface – Bus Timing



Bus Timing Characteristics

Parameter	Symbol	Standard Mode	Fast Mode	Units
Maximum SCL Clock Frequency	f_{SCL}	100	400	KHz
Minimum START Condition Hold Time Relative to SCL Edge	t_{DSTA}	4		µs
Minimum SCL Clock Low Width	t_{LOW}	4.7		µs
Minimum SCL Clock High Width	t_{HIGH}	4		µs
Minimum START Condition Setup Time Relative to SCL Edge	t_{SUSTA}	4.7		µs
Minimum Data Hold Time on SDA Relative to SCL Edge	t_{HDDAT}	0		µs
Minimum Data Setup Time on SDA Relative to SCL Edge	t_{SUDAT}	0.1	0.1	µs
Minimum STOP Condition Setup Time on SCL	t_{SUSTO}	4		µs
Minimum Bus Free Time Between Stop Condition and Start Condition	t_{BUS}	4.7		µs

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Register set:

The APDS-9306/APDS-9306-065 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

Address	Type	Name	Description	Reset Value
00HEX	RW	MAIN_CTRL	ALS operation mode control, SW reset	00HEX
04HEX	RW	ALS_MEAS_RATE	ALS measurement rate and resolution in Active mode	22HEX
05HEX	RW	ALS_GAIN	ALS analog gain range	01HEX
06HEX	R	Part_ID	Part number ID and revision ID	B1HEX (APDS-9306) B3HEX (APDS-9306-065)
07HEX	R	MAIN_STATUS	Power-on status, interrupt status, data status	20HEX
0AHEX	R	CLEAR_DATA_0	Clear ADC measurement data - LSB	00HEX
0BHEX	R	CLEAR_DATA_1	Clear ADC measurement data	00HEX
0CHEX	R	CLEAR_DATA_2	Clear ADC measurement data - MSB	00HEX
0DHEX	R	ALS_DATA_0	ALS ADC measurement data - LSB	00HEX
0EHEX	R	ALS_DATA_1	ALS ADC measurement data	00HEX
0FHEX	R	ALS_DATA_2	ALS ADC measurement data - MSB	00HEX
19HEX	RW	INT_CFG	Interrupt configuration	10HEX
1AHEX	RW	INT_PERSISTENCE	Interrupt persist setting	00HEX
21HEX	RW	ALS_THRES_UP_0	ALS interrupt upper threshold, LSB	FFHEX
22HEX	RW	ALS_THRES_UP_1	ALS interrupt upper threshold	FFHEX
23HEX	RW	ALS_THRES_UP_2	ALS interrupt upper threshold, MSB	0FHEX
24HEX	RW	ALS_THRES_LOW_0	ALS interrupt lower threshold, LSB	00HEX
25HEX	RW	ALS_THRES_LOW_1	ALS interrupt lower threshold	00HEX
26HEX	RW	ALS_THRES_LOW_2	ALS interrupt lower threshold, MSB	00HEX
27HEX	RW	ALS_THRES_VAR	ALS interrupt variance threshold	00HEX

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MAIN_CTRL

Default Value: 00HEX

7	6	5	4	3	2	1	0	
0	0	0	SW_Reset	0	0	ALS_EN	0	0X00

FIELD	BIT	DESCRIPTION
SW_Reset	4	1 = Reset will be triggered
ALS_EN	1	1 = ALS active 0 = ALS standby

Writing to this register stops the ongoing measurements and starts new measurements (depends on the respective enable bit).

ALS_MEAS_RATE

Default value: 22HEX

7	6	5	4	3	2	1	0	
0	ALS Resolution/Bit Width			0	ALS Measurement Rate			0X04

FIELD	BIT	DESCRIPTION
ALS Resolution/ Bit Width	6:4	000 : 20 bit – 400ms 001 : 19 bit – 200ms 010 : 18 bit – 100ms (default) 011 : 17 bit – 50ms 100 : 16 bit – 25ms 101 : 13 bit – 3.125ms 110 : Reserved 111 : Reserved
ALS Measurement Rate	2:0	000 – 25ms 001 – 50ms 010 – 100ms (default) 011 – 200ms 100 – 500ms 101 – 1000ms 110 – 2000ms 111 – 2000ms

When the measurement repeat rate is programmed to be faster than possible for the specified ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register stops the ongoing measurements and starts new measurements (depends on the respective enable bit).

ALS_GAIN

Default Value: 01HEX

7	6	5	4	3	2	1	0	
0	0	0	0	0	ALS Gain Range			0X05

FIELD	BIT	DESCRIPTION
ALS Gain Range	2:0	000 : Gain 1 001 : Gain 3 010 : Gain 6 011 : Gain 9 100 : Gain 18

Writing to this register stops the ongoing measurement and starts new measurements (depending on the respective bits).

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PART_ID

Default Value: B1HEX (APDS-9306), B3HEX (APDS-9306-065)

7	6	5	4	3	2	1	0	
Part ID				Revision ID				0X06

FIELD	BIT	DESCRIPTION
Part Number ID	7:4	Part number ID
Revision ID	3:0	Revision ID of the component

MAIN_STATUS

Default Value: 20HEX

7	6	5	4	3	2	1	0	
0	0	Power On Status	ALS Interrupt Status	ALS Data Status	0	0	0	0X07

FIELD	BIT	DESCRIPTION
Power On Status	5	1 = Part went through a power-up event, either because the part was turned on or because there was power supply disturbance. All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if necessary. The flag is cleared after the register is read.
ALS Interrupt Status	4	0 : Interrupt condition not fulfilled (default) 1 : Interrupt condition fulfilled (cleared after read)
ALS Data Status	3	0 : old data, already read (default) 1 : new data, not yet read (cleared after read)

CLEAR_DATA

Default Value: 00HEX, 00HEX, 00HEX

7	6	5	4	3	2	1	0	
CLEAR _DATA_0 [7:0]								0X0A
CLEAR_DATA_1 [15:8]								0X0B
0	0	0	0	CLEAR_DATA_2 [19:16]				0X0C

Clear channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned). The clear channel data is clipped at ($2^{Resolution} - 1$)

The clear channel output is already temperature compensated internally:

$CLEAR_DATA = (CLEAR_{int} - COMP)$

When an I²C™ read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I²C™ read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual CLEAR_DATA registers are updated as soon as there is no on-going I²C™ read operation to the address range 07HEX to 18HEX.

Reg 0AHEX Bit[7:0] Clear diode data least significant data byte
Reg 0BHEX Bit[7:0] Clear diode data intervening data byte
Reg 0CHEX Bit[3:0] Clear diode data most significant data byte

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ALS_DATA

Default value: 00HEX, 00HEX, 00HEX

7	6	5	4	3	2	1	0	
ALS_DATA_0 [7:0]								0X0D
ALS_DATA _1 [15:8]								0X0E
0	0	0	0	ALS_DATA_2 [19:16]				0X0F

ALS channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

The channel output is already temperature compensated internally:

$ALS_DATA = (ALS_{int} - COMP)$

When an I²C™ read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I²C™ read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual ALS_DATA registers are updated as soon as there is no on-going I²C™ read operation to the address range 07HEX to 18HEX.

Reg 0DHEX Bit[7:0] ALS diode data least significant data byte
Reg 0EHEX Bit[7:0] ALS diode data intervening data byte
Reg 0FHEX Bit[3:0] ALS diode data most significant data byte

INT_CFG

Default Value: 10HEX

7	6	5	4	3	2	1	0	
0	0	ALS Interrupt Source		ALS Variation Interrupt Mode	ALS Interrupt Enable	0	0	0X19
0	0	ALS_INT_SEL		ALS_VAR_MODE	ALS_INT_EN	0	0	

FIELD	BIT	DESCRIPTION
ALS_INT_SEL	5:4	00 : Clear channel 01 : ALS channel (default)
ALS_VAR_MODE	3	0 : ALS threshold interrupt mode (default) 1 : ALS variation interrupt mode
ALS_INT_EN	2	0 : ALS Interrupt disabled (default) 1 : ALS Interrupt enabled

INT_PERSISTENCE

Default value: 00HEX

7	6	5	4	3	2	1	0	
ALS_PERSIST				0	0	0	0	0X1A

This register sets the number of similar consecutive LS interrupt events that must occur before the interrupt is asserted.

FIELD	BIT	DESCRIPTION
ALS_PERSIST	7:4	0000 : Every ALS value out of threshold range (default) asserts an interrupt 0001 : 2 consecutive ALS values out of threshold range assert an interrupt … 1111 : 16 consecutive ALS values out of threshold range assert an interrupt

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ALS_THRES_UP

Default value: FFHEX, FFHEX, 0FHEX

7	6	5	4	3	2	1	0	
ALS_THRES_UP_0 [7:0]								0X21
ALS_THRES_UP_1 [15:8]								0x22
0	0	0	0	ALS_THRES_UP_2 [19:16]				0x23

ALS_THRES_UP sets the upper threshold value for the ALS interrupt. The Interrupt Controller compares the value in ALS_THRES_UP against measured data in the ALS_DATA registers. It generates an interrupt event if ALS_DATA exceeds the threshold level.

The data format for ALS_THRES_UP must match that of the ALS_DATA registers.

Reg 21HEX Bit[7:0] ALS upper interrupt threshold value, LSB
Reg 22HEX Bit[7:0] ALS upper interrupt threshold value, intervening byte
Reg 23HEX Bit[3:0] ALS upper interrupt threshold value, MSB

ALS_THRES_LOW

Default value: 00HEX, 00HEX, 00HEX

7	6	5	4	3	2	1	0	
ALS_THRES_LOW_0 [7:0]								0X24
ALS_THRES_LOW_1 [15:8]								0x25
0	0	0	0	ALS_THRES_UP_2 [19:16]				0x26

ALS_THRES_LOW sets the upper threshold value for the ALS interrupt. The Interrupt Controller compares the value in ALS_THRES_LOW against measured data in the ALS_DATA registers. It generates an interrupt event if ALS_DATA is below the threshold level.

The data format for ALS_THRES_LOW must match that of the ALS_DATA registers.

Reg 24HEX Bit[7:0] ALS lower interrupt threshold value, LSB
Reg 25HEX Bit[7:0] ALS lower interrupt threshold value, intervening byte
Reg 26HEX Bit[3:0] ALS lower interrupt threshold value, MSB

ALS_THRESH_VAR

Default Value: 00HEX

7	6	5	4	3	2	1	0	
0	0	0	0	0	ALS_THRES_VAR			0X27

FIELD	BIT	DESCRIPTION
ALS_THRES_VAR	2:0	000 : ALS result varies by 8 counts compared to previous result 001 : ALS result varies by 16 counts compared to previous result 010 : ALS result varies by 32 counts compared to previous result 011 : ALS result varies by 64 counts compared to previous result … 111 : ALS result varies by 1024 counts compared to previous result

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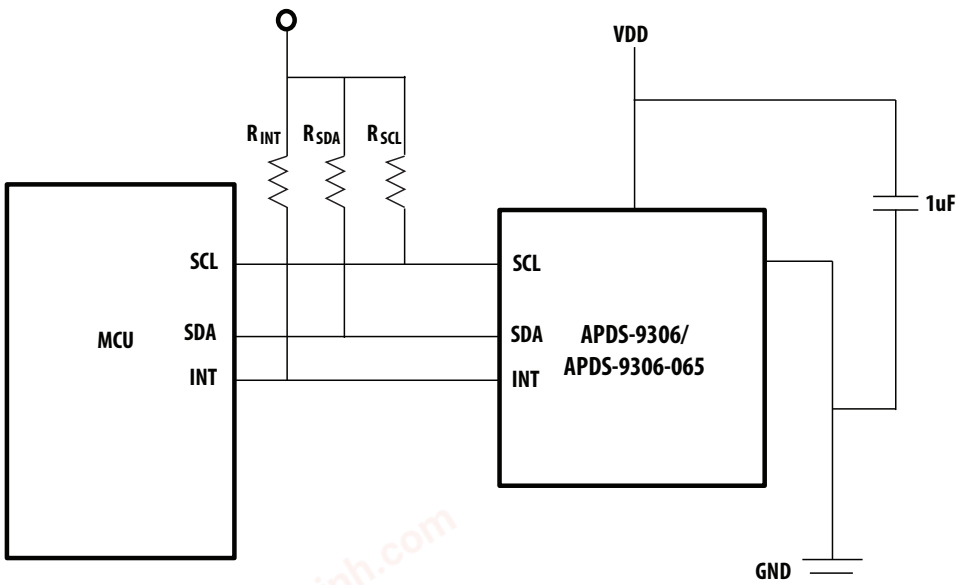
Application Information: Hardware

The application hardware circuit for implementing an ALS is simple with the APDS-9306/APDS-9306-065 and is shown in the following figure. The bypass capacitor is placed as close to the V_{DD} pin and is connected directly to the power source and to the ground, as shown in Figure below. It allows the AC component of the V_{DD} to pass through to ground. Use bypass capacitor with low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

Pull-up resistors, RSDA and RSCL, maintain the SDA and SCL lines at a high level when the bus is free and ensure the signals are pulled up from a low to a high level within the required rise time. A pull-up resistor, RINT, is also required for the interrupt (INT), which functions as a wired-AND signal in a similar fashion to the SCL and SDA lines. A typical impedance value of 10 kΩ can be used.

For a complete description of I^2C maximum and minimum R1 and R2 values, please review the I^2C Specification at http:// www.semiconductors.philips.com.



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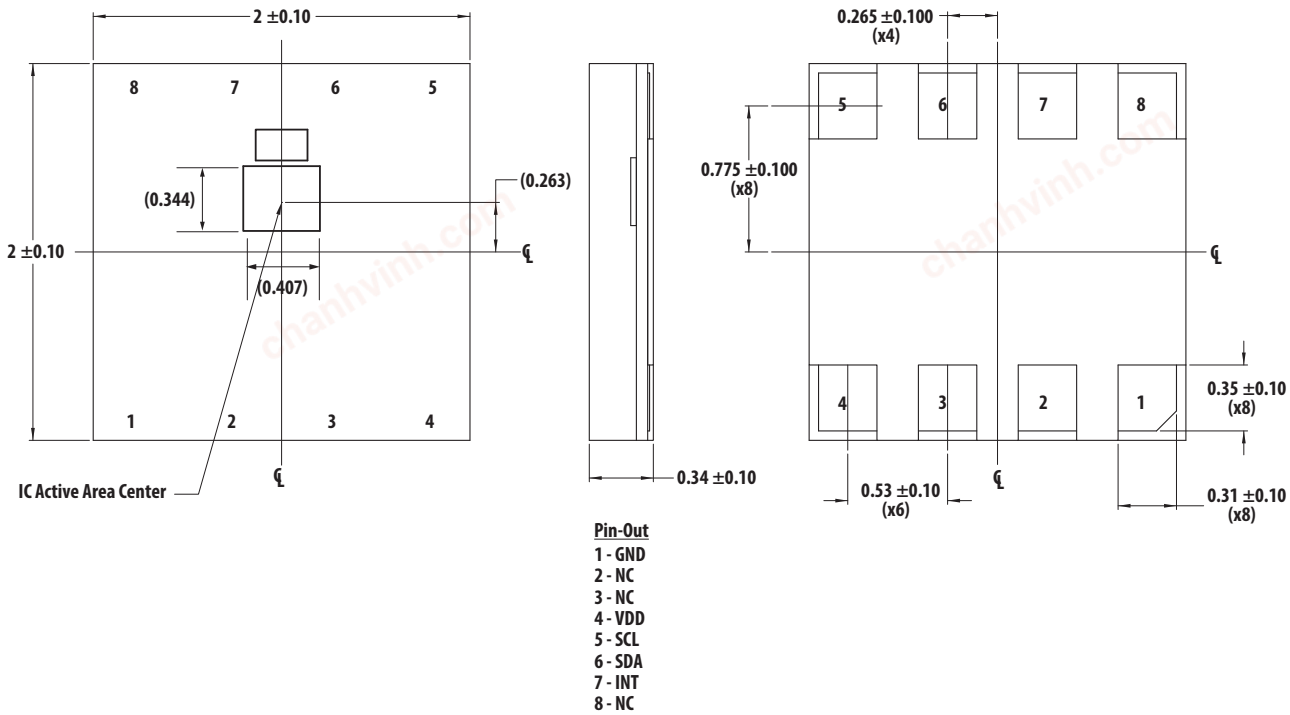
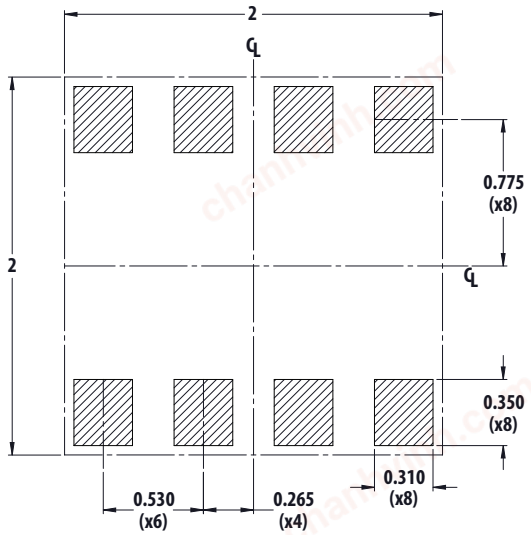
Package Outline Dimensions for APDS-9306



Pin-Out
1 - GND
2 - NC
3 - NC
4 - VDD
5 - SCL
6 - SDA
7 - INT
8 - NC

Dimensions are in mm

PCB Pad Layout for APDS-9306



Dimensions are in mm

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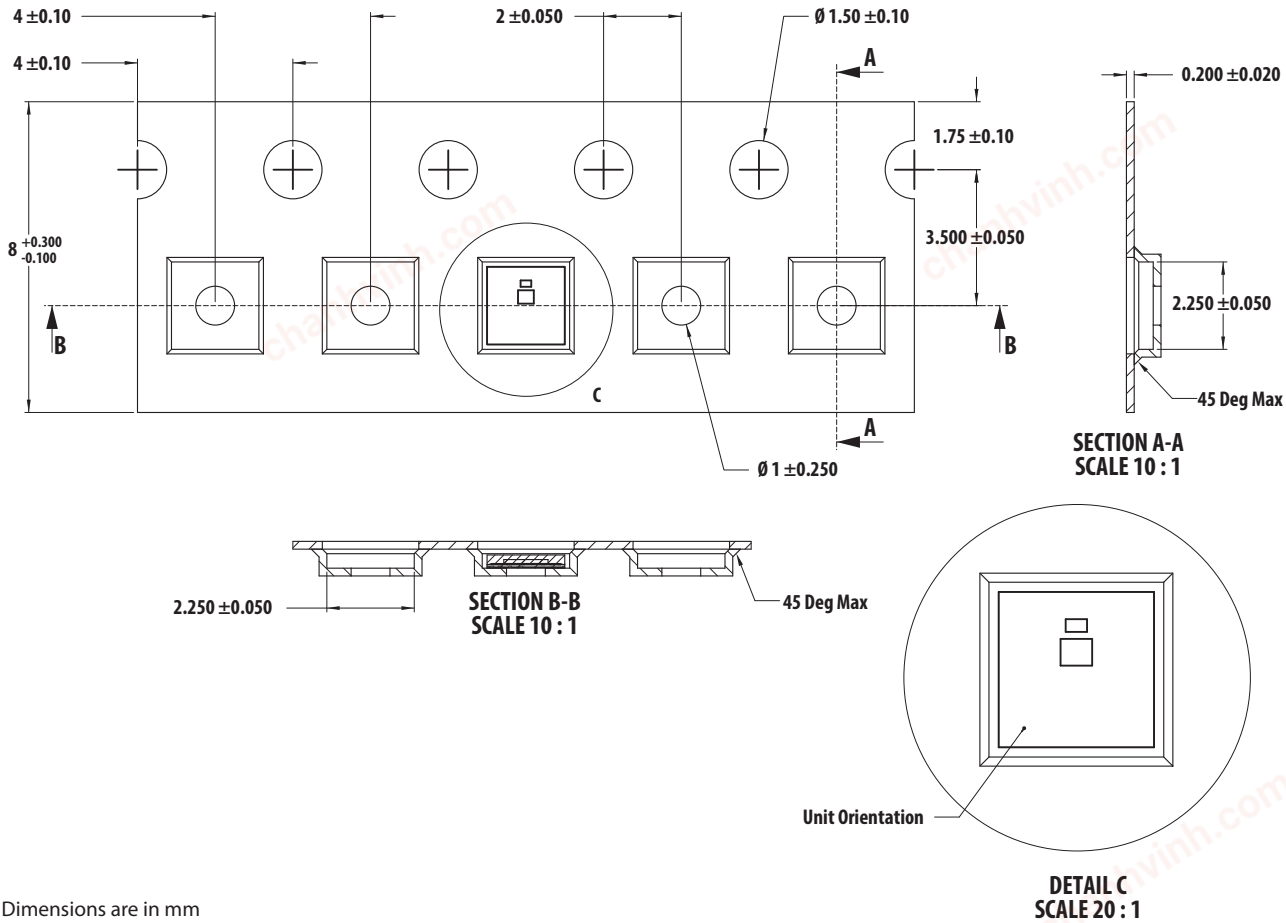
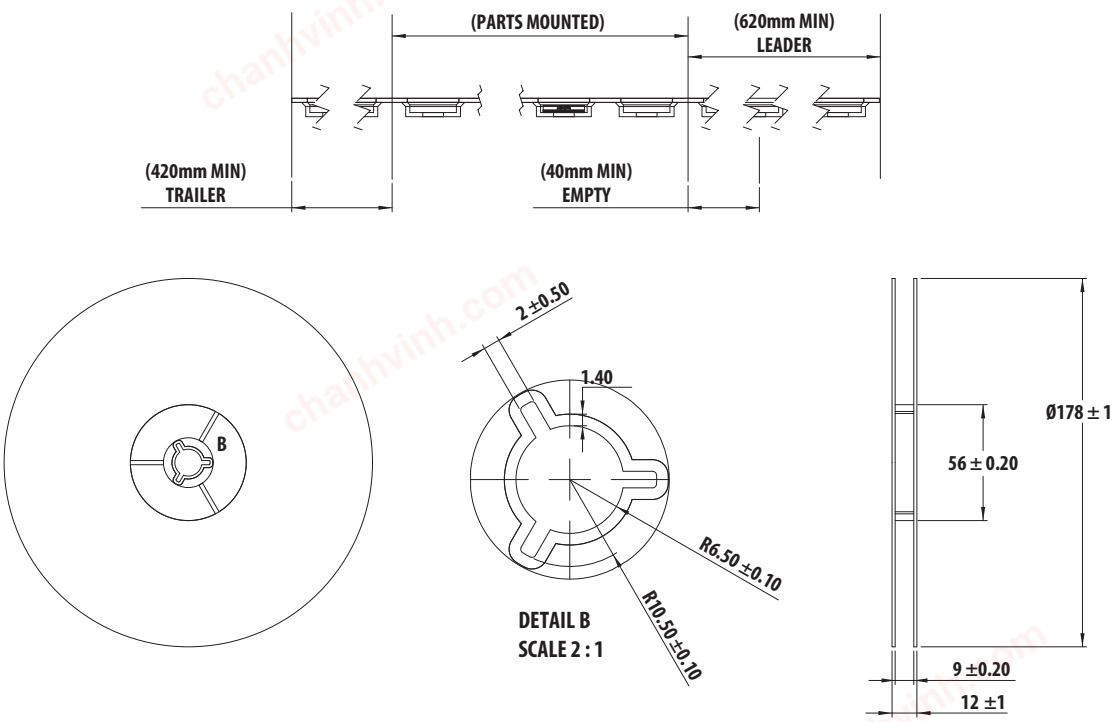
Tape Dimensions for APDS-9306



Dimensions are in mm

Reel Dimensions for APDS-9306



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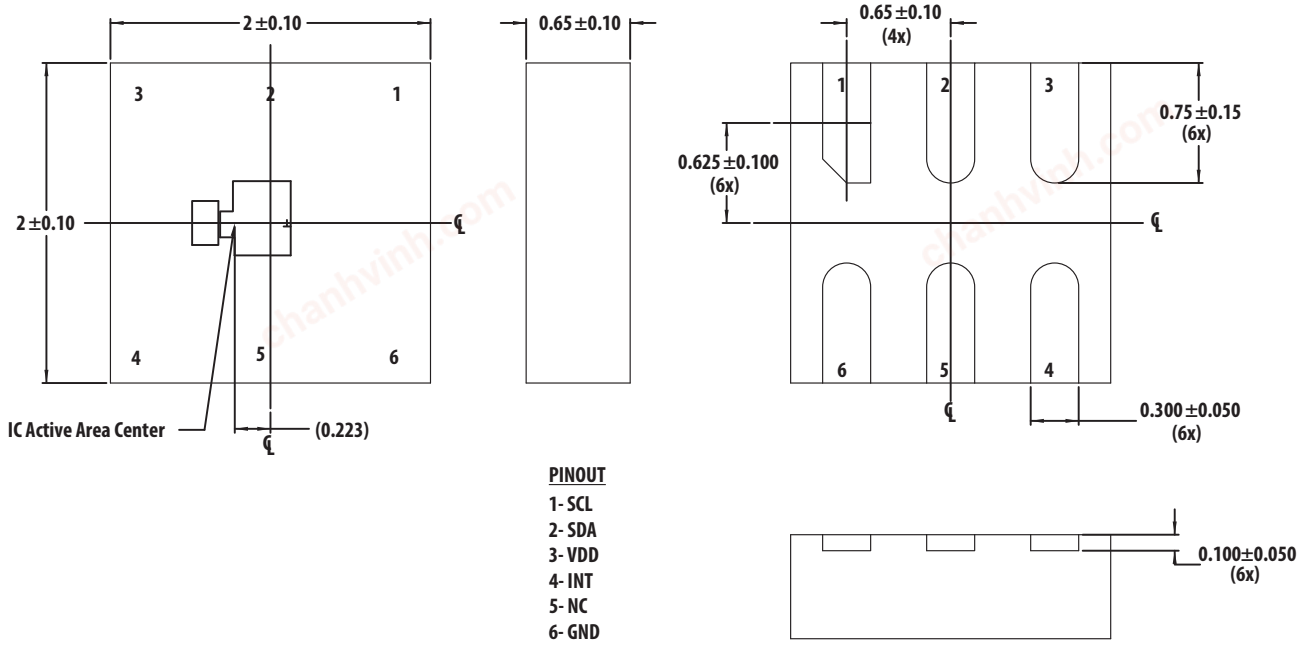
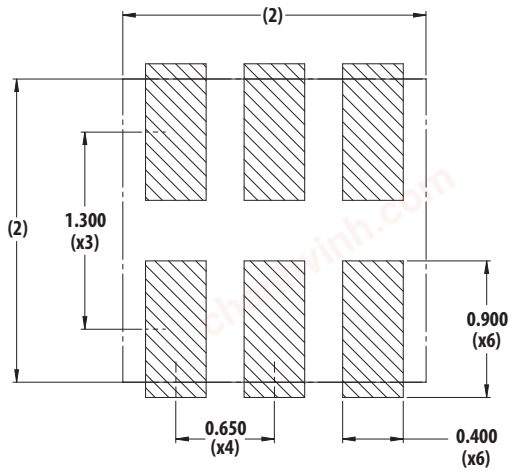
Package Outline Dimensions for APDS-9306-065



PINOUT

1- SCL
2- SDA
3- VDD
4- INT
5- NC
6- GND

PCB Pad Layout



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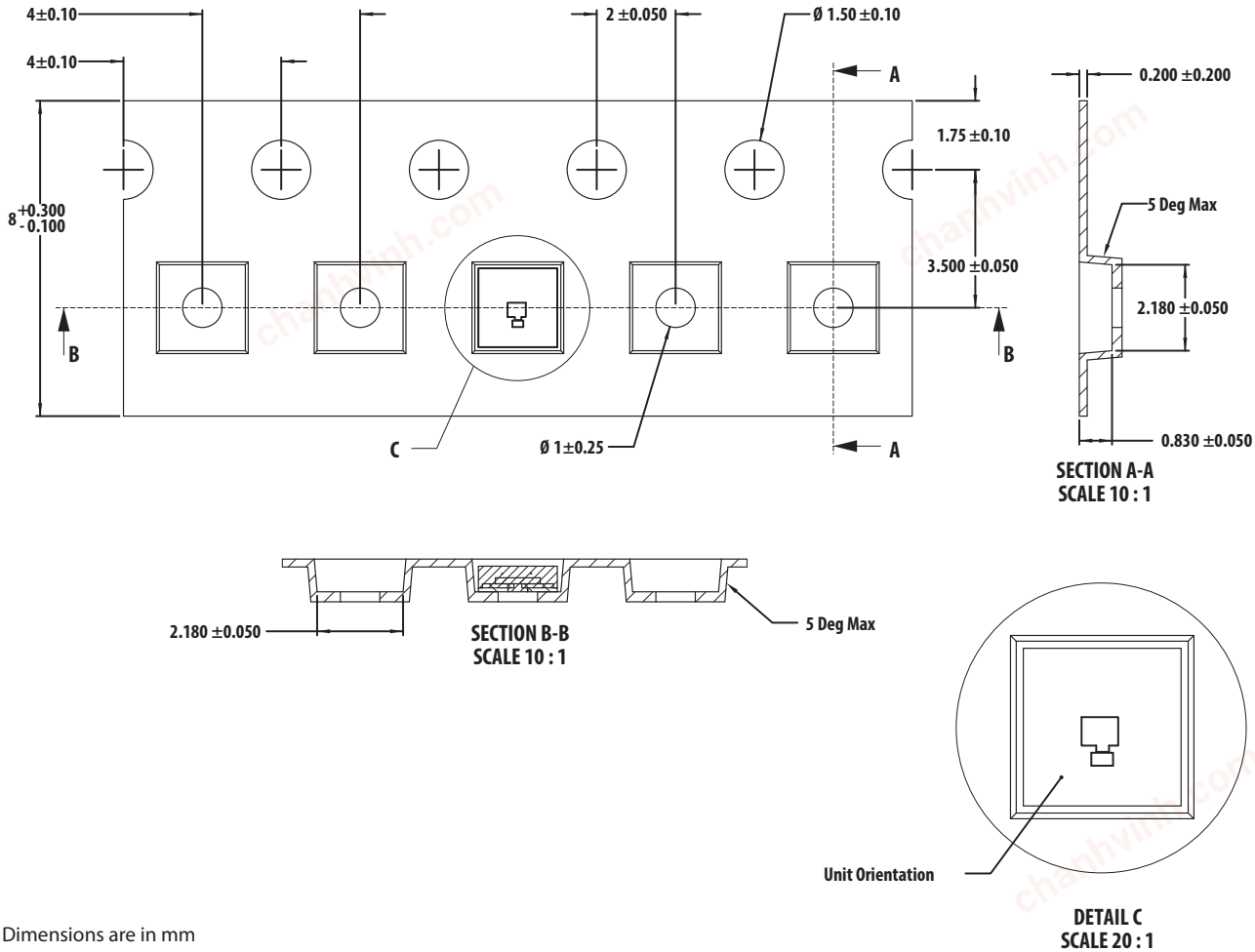
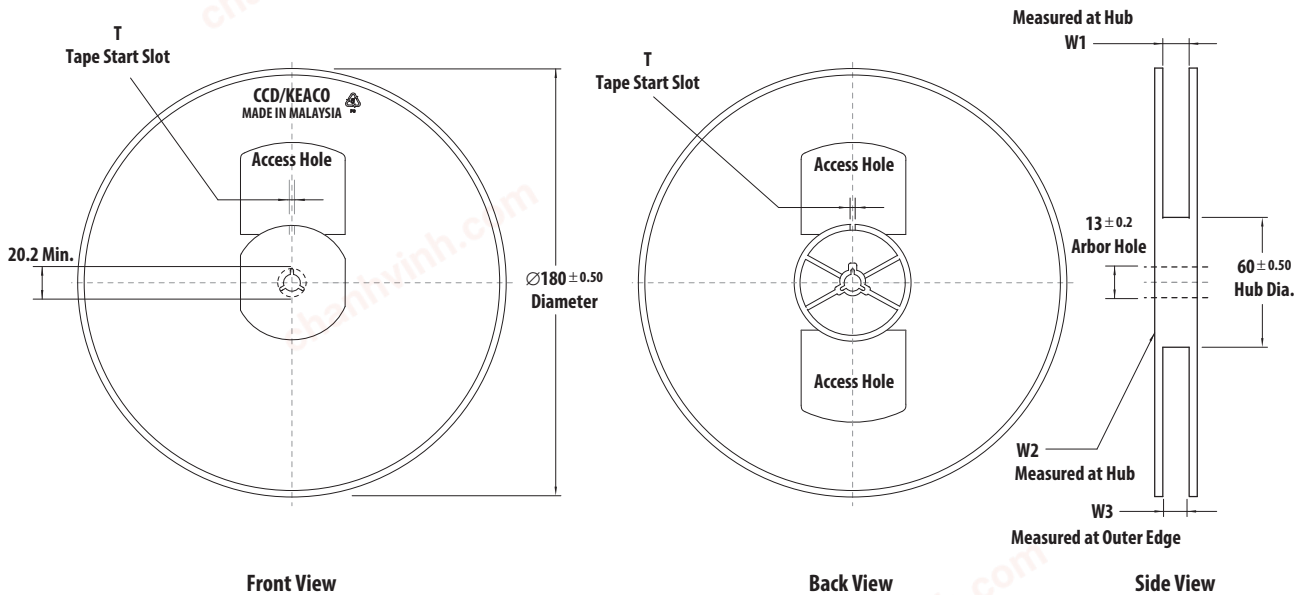
Tape Dimensions for APDS-9306-065



Dimensions are in mm

Reel Dimensions for APDS-9306-065



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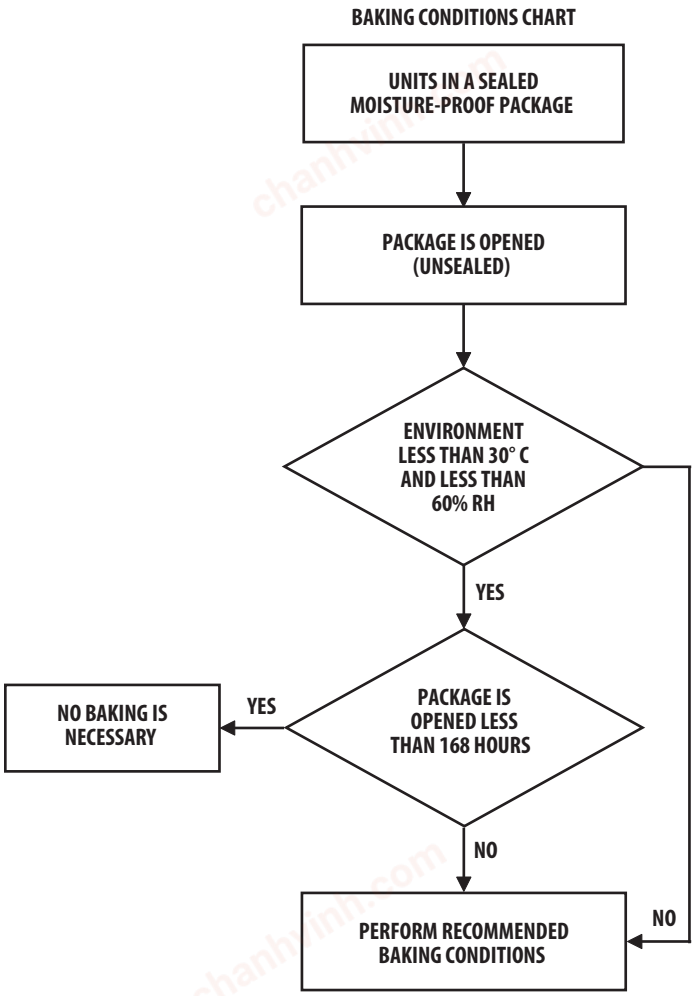
Moisture Proof Packaging Chart

All APDS-9306/APDS-9306-065 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC Level 3.



Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within seven days if stored at the recommended storage conditions. When the Moisture Barrier Bag (MBB) is opened and the parts are exposed to the recommended storage conditions more than seven days, the parts must be baked before reflow to prevent damage to the parts.

Baking conditions

If the parts are not stored per the recommended storage conditions they must be baked before reflow to prevent damage to the parts.

Package	Temp.	Time
In Reels	60°C	48 hours
In Bulk	100°C	4 hours

Note: Baking should only be done once.

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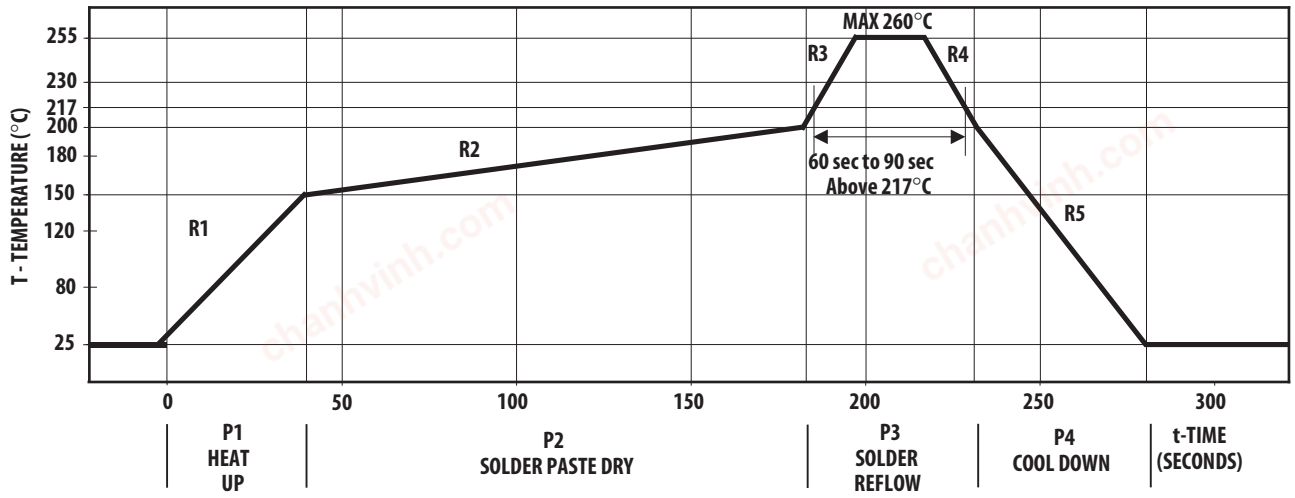
Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100 s to 180 s
Solder Reflow	P3, R3	200°C to 260°C	3°C/s
	P3, R4	260°C to 200°C	-6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s
Time maintained above liquidus point, 217° C		> 217°C	60 s to 90 s
Peak Temperature		260°C	–
Time within 5° C of actual Peak Temperature		–	20 s to 40 s
Time 25° C to Peak Temperature		25°C to 260°C	8 mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 90 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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AV02-4755EN - October 21, 2016

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