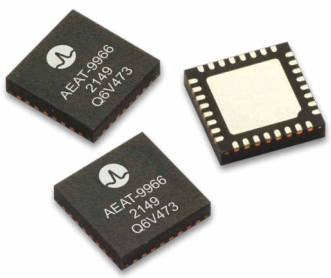
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BROADCOM®

Data Sheet

AEAT-9966

Dual/Redundancy Magnetic Encoder IC: 10-Bit to 18-Bit Programmable Angular Magnetic Encoder with Safety



Description

The Broadcom® AEAT-9966 is a stacked, dual-die, high-accuracy angular magnetic encoder for reliability operations with redundancy.

This sophisticated system uses integrated Hall sensor elements with complex analog and digital signal processing within a single device.

A simple two-pole magnet rotates to generate the magnetic field, with its poles set perpendicular to the axis of rotation. Wide magnetic field sensor configurations allow On-Axis (end of shaft) or Off-Axis (side of shaft, axial and radial) modes in application.

The AEAT-9966 is a versatile solution capable of supporting a broad range of applications with its robust architecture to measure and deliver both absolute and incremental signals.

The absolute angle measurement provides an instant indication of the magnet's angular position with a selectable and reprogrammable resolution from 10 bits to 18 bits. When selected, its positioning data is then represented in its digital form to be assessed through a standard SSI (parity) and SPI (with CRC and Parity option) communication protocol.

Where desired, users can also choose to receive its absolute angle position in PWM-encoded output signals. The incremental positions are indicated on ABI and UVW signals with a wide user-configurable resolution from 1 CPR to 20,000 CPR of ABI signals and pole pairs from 1 to 32 pole pairs (2 to 64 poles) for UVW commutation signals.

Features

- 5V and 3.3V operating voltage
- Operating temperature from –40°C to 125°C
- Two chips of magnetic encoder in one package
- 300-µA current consumption in Sleep Mode
- Programmable 10 bits up to 18 bits of absolute resolution
- The incremental positions are indicated on ABI and UVW signals with a user-configurable CPR from 1 CPR to 20,000 CPR
- Commutation angle output UVW 1 pp to 32 pp
- Absolute output over 2-wire SSI, 3-wire SSI, 4-wire SPI, and PWM
- Dedicated output pin for ABI, UVW, and serial interface
- Dedicated zero reset and error pin
- EEPROM architecture for multi-time user configuration
- Optional 56-bit memory lock function
- Automatic integral non-linearity angle correction for high accuracy
- Designed conformance to ISO26262 ASIL-D and SIL3 with secondary chip for redundancy
- Compact QFN-32 leads (5 mm × 5 mm) package
- Multi-index with one revolution
- High-impedance output for multi-device network

Applications

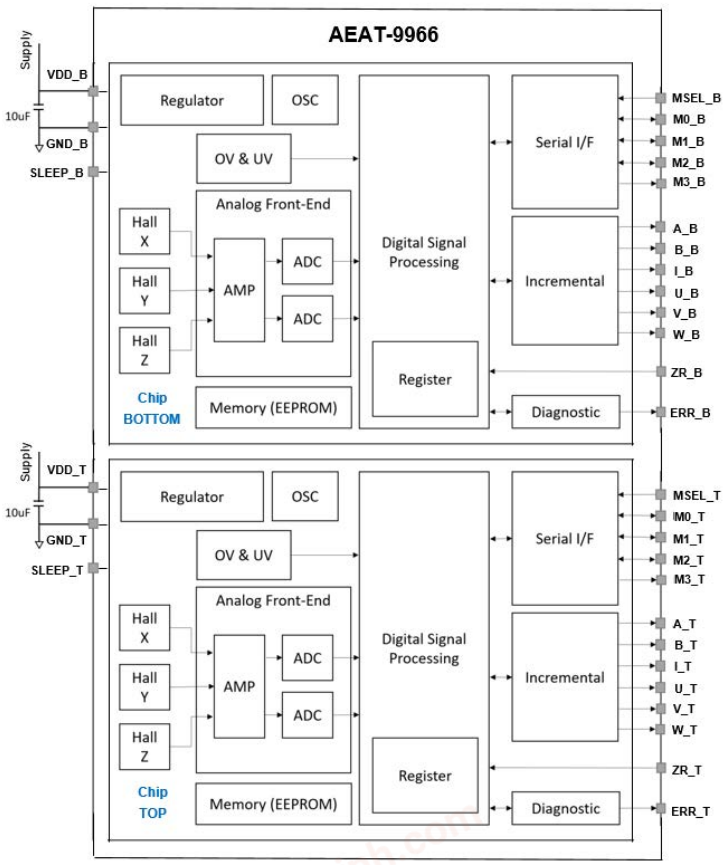
- Brushless DC motor and stepper motor
- Resolver and potentiometer replacement
- Industrial automation and robotics
- Industrial sewing machine and textile equipment
- Light Detection and Range (LiDAR)

Disclaimer: Except as expressly indicated in writing, the component is not designed or guaranteed to be suitable for use in safety-related applications where its failure or malfunction can reasonably be expected to result in injury, death, or severe equipment damage. Customers are solely responsible for determining the suitability of this product for its intended application and solely liable for all loss, damage, expense or liability in connection with such use.

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Functional Description

Figure 1: AEAT-9966 Block Diagram



The AEAT-9966 is a stacked dual-die ASIC with individual pinout in a single package.

The AEAT-9966 is manufactured with a CMOS standard process. It is capable of accurately measuring a magnet's rotational angle when it is placed in alignment and perpendicular to the device by using its integrated Hall sensors to detect its magnetic field. The detected magnetic signals are then taken as input signals to be properly conditioned to negate its non-idealities before inputting them into the analog amplifiers for strength amplification and filtering. The amplified analog signals are then fed into the internal analog-to-digital converter (ADC) to be converted into digital signals for the final stage of digital processing. The digital processing provides a digitized output of the absolute and incremental signals.

The magnet used should have sufficient magnetic field strength (mT) to generate the magnetic field for the signal generation as highlighted in Recommended Magnetic Input Specifications. The device provides digital information of magnetic field strength high (MHI) and magnetic field strength low (MLO) from output protocols to indicate whether the magnets are too close or too far away from our device's surface.

Users can assess the device's digitized absolute data using standard Synchronous Serial Interface (SSI) or Serial Peripheral Interface (SPI) protocols. In addition, an absolute angular representation can also be selected using a pulse-width modulated (PWM) signal.

The incremental outputs are available from the digital outputs of their dedicated A, B, and I pins and the commutation output U, V, and W.

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Pin Assignment

Figure 2: Pin Configurations (Bottom View)

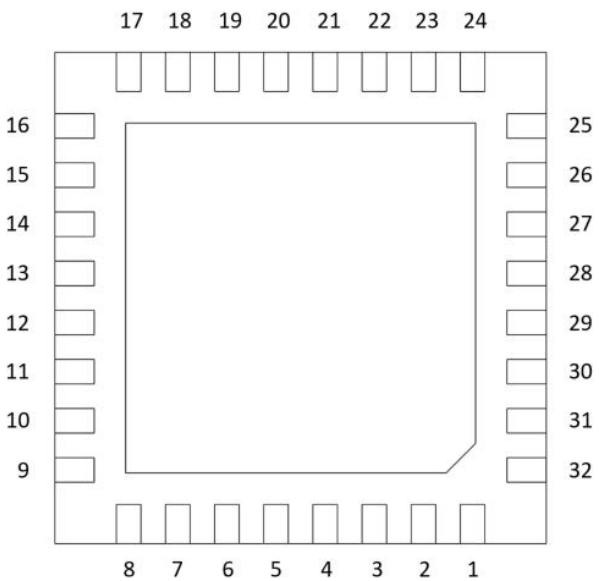


Figure 3: Label Information



AEAT-0000 = Product Part Number

YYWW = Package Assembly Date

XXXXXX= Assembly Lot Number

Pinout Description

Pin QFN32	Pin Name	Pin Type	Description	Pin QFN32	Pin Name	Pin Type	Description
1	ZR_T	I	Zero Reset, Active High (Chip Top)	17	ZR_B	I	Zero Reset, Active High (Chip Bottom)
2	M0_B	I/O	Serial Interface M0 (Chip Bottom)	18	M0_T	I/O	Serial Interface M0 (Chip Top)
3	ERR_T	O	Error, Active High (Chip Top)	19	ERR_B	O	Error, Active High (Chip Bottom)
4	M1_B	I/O	Serial Interface M1 (Chip Bottom)	20	M1_T	I/O	Serial Interface M1 (Chip Top)
5	MSEL_T	I	Interface Select (Chip Top)	21	MSEL_B	I	Interface Select (Chip Bottom)
6	M2_B	I/O	Serial Interface M2 (Chip Bottom)	22	M2_T	I/O	Serial Interface M2 (Chip Top)
7	M3_B	O	Serial Interface M3 (Chip Bottom)	23	M3_T	O	Serial Interface M3 (Chip Top)
8	A_B	O	Incremental A (Chip Bottom)	24	A_T	O	Incremental A (Chip Top)
9	B_B	O	Incremental B (Chip Bottom)	25	B_T	O	Incremental B (Chip Top)
10	I_B	O	Incremental I (Chip Bottom)	26	I_T	O	Incremental I (Chip Top)
11	U_B	O	Commutation U (Chip Bottom)	27	U_T	O	Commutation U (Chip Top)
12	VSS_T	Supply	Ground Supply (Chip Bottom)	28	VSS_B	Supply	Ground Supply (Chip Bottom)
13	V_B	O	Commutation V (Chip Bottom)	29	V_T	O	Commutation V (Chip Top)
14	VDD_T	Supply	Power Supply (Chip Top)	30	VDD_B	Supply	Power Supply (Chip Bottom)
15	W_B	O	Commutation W (Chip Bottom)	31	W_T	O	Sleep Mode (Chip Top)
16	Sleep_B	I	Sleep Mode, Active Low (Chip Bottom)	32	Sleep_T	I	Sleep Mode, Active Low (Chip Top)

NOTE: Backside pad connects to VSSA.

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Configuration Mode

The AEAT-9966 features built-in memory for multiple-time programming (MTP).

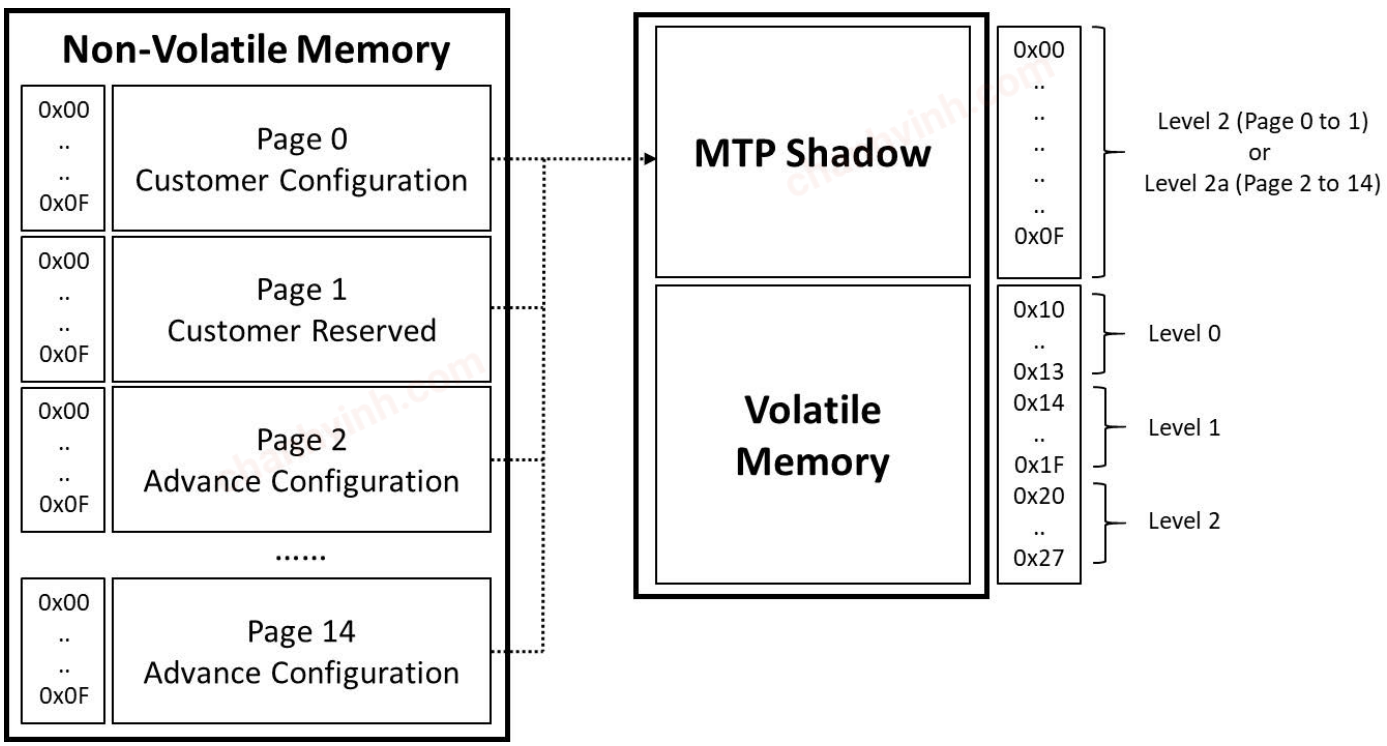
Programming the AEAT-9966 can be performed by using the HEDS-9966 programming kit or any tester/programmer device, following the provided guidelines.

For optimal performance setting and advance configuration, such as acceleration/deceleration, hysteresis, and filtering, refer to the Level 2 and Level 2a register settings detailed in the *AEAT-9966 Application Note*.

Memory Map

The AEAT-9966's memory consists of non-volatile memory and volatile memory. The following figure illustrates the concept of non-volatile memory, which is loaded into the MTP shadow. For further details on this memory setting, refer to the *AEAT-9966 Application Note*.

Figure 4: Non-volatile/Volatile Memory and MTP Shadow Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–40	125	°C
Junction Temperature	T_J	–40	150	°C
DC Supply Voltage VDDA Pin	 VDD_B, VDD_T	 –0.3	 6.06	 V
Input Voltage Range	V_{in}	–0.3	6	V
Electrostatic Discharge (HBM)	—	—	±4.0	kV
Moisture Sensitivity Level	—	—	1	—

CAUTION! Subjecting the product to stresses beyond those listed in this section may cause permanent damage to the devices. These are stress ratings only and do not imply that the devices will function beyond these ratings. Exposure to the extremes of these conditions for extended periods may affect product reliability.

Electrical Characteristics

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Operating Ambient Temperature	T_A	–40	—	125	°C	
DC Supply Voltage to VDD Pin 5V Operation 3.3V Operation	VDD_B, VDD_T	 4.5 3.0	 5.0 3.3	 5.5 3.6	 V V	
Incremental Output Frequency	f_{MAX}	—	—	1.0	MHz	Frequency = Velocity(rpm) × CPR/60
Load Capacitance	C_L	—	—	15	pF	

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Systems Parameters

Condition: Electrical characteristics over the recommended operating conditions. Typical values specified at VDD = 5.0V and 25°C, optimum placement of magnet.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Current Consumption						
Supply Current Normal Operation Mode	IDD_{NOM}	—	48	—	mA	5V
	IDD_{NOM}	—	44	—	mA	3.3V
Supply Current Sleep Mode	IDD_{IDLE}	—	600	—	µA	5V and 3.3V
Digital Outputs (DO)						
High Level Output Voltage	V_{OH}	VDD – 0.5	—	—	V	Normal operation
Low Level Output Voltage	V_{OL}	—	—	GND + 0.4	V	
Power-Up Time Absolute Output Incremental Output PWM Output	t_{PwrUp}	—	10	—	ms	
Digital Inputs (DI)						
Input High Level	V_{IH}	0.7 × VDD	—	—	V	
Input Low Level	V_{IL}	—	—	0.3 × VDD	V	
Pull-Up Low Level Input Current	I_{IL}	—	—	120	µA	
Pull-Down High Level Input Current	I_{IH}	—	—	120	µA	

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Encoding Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
System Input						
Maximum Speed	S_{MAX}	—	—	30,000	RPM	
Absolute Output						
Resolution	RES	10	—	18	Bit	Programmable 10 to 18 bits.
Integral Non-Linearity ON-Axis	INL_{nom}	—	±0.05	—	Deg	Best fit line, centered magnet. T_A = 25°C, Voltage = 5V, INL angle correction.
Integral Non-Linearity OFF-Axis		—	±0.15	—		
Integral Non-Linearity ON-Axis	INL_{dis}	—	±0.15	—	Deg	Best fit line, over displacement of magnet. T_A = 25°C, Voltage = 5V
Integral Non-Linearity OFF-Axis		—	±0.25	—		
Integral Non-Linearity ON-Axis	INL_{temp}	—	±0.10	—	Deg	Best fit line, over temperature range. T_A = –40 to +125°C, Voltage = 5V
Integral Non-Linearity OFF-Axis		—	±0.40	—		
Differential Non-Linearity	DNL_{nom}	—	±0.02	—	Deg	T_A = 25°C, Voltage = 5V
Output Sampling Rate	f_S	—	10	—	MHz	Based on the SSI protocol.
Latency	—	—	80	—	ns	At constant speed.
Incremental Output (Channel ABI)						
Resolution	R_{INC}	1	—	20,000	CPR	Programmable.
Index Pulse Width	P_O	90	—	360	°e	Programmable options: 90, 180, 270, or 360°e. See Figure 5.
Index Pulse State	P_S	90	—	360	°e	Relation between Index output to Incremental AB state. Programmable options: 0, 90, 180, or 270°e. See Figure 5.
Index State	—	90	—	360	°e	Programmable options: 90, 180, 270, or 360°e. See Figure 5.
PWM Output						
PWM Frequency	f_{PWM}	122	—	976	Hz	Adjustable based on our PWM settings.
Minimum Pulse Width	PW_{MIN}	—	1	—	µs	
Maximum Pulse Width	PW_{MAX}	—	16,384	—	µs	

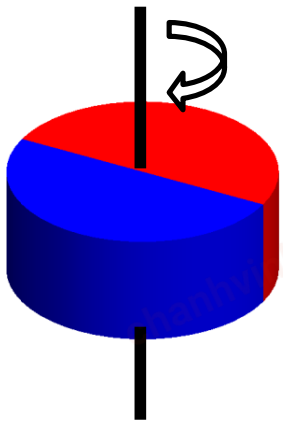
NOTE: Encoding characteristics over recommended operating range unless otherwise specified.

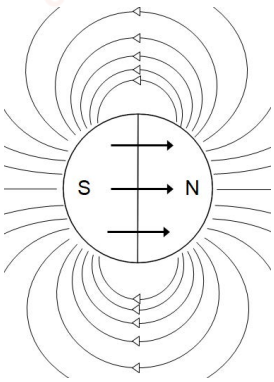
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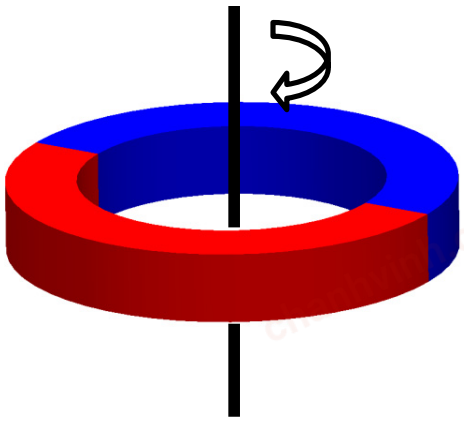
Recommended Magnetic Input Specifications

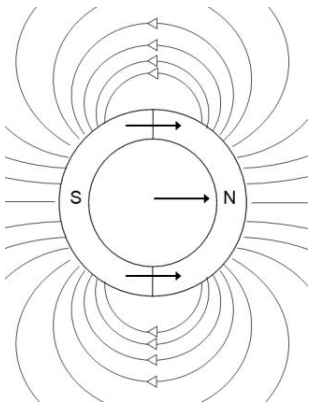
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Diameter	d				mm	Recommended magnet: cylindrical magnet or ring magnet diametrically magnetized and one pole pair.
Disc Magnet		4	6	—		
Ring Magnet Inner Diameter		—	15	—		
Ring Magnet Outer Diameter		—	25	—		
Thickness	t				mm	
Disc Magnet		—	2.5	—		
Ring Magnet		4	6	—		
Magnetic Input Field Magnitude	Bpk				mT	Required vertical/horizontal component of the magnetic field strength on the die's surface, measured along concentric circle.
On-Axis (Disc Magnet)		45	—	100		
Off-Axis (Ring Magnet)		30	—	150		
Magnet Displacement Radius	R_m	—	—	0.25	mm	Displacement between the magnet axis and the device center.
Recommended Magnet Material and Temperature Drift	—	—	–0.12	—	%/K	NdFeB (Neodymium Iron Boron), grade N35SH.

Diametrically Magnetized Magnet







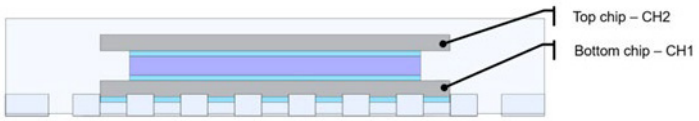


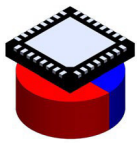
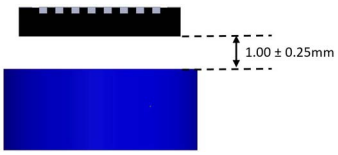
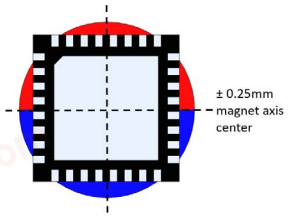
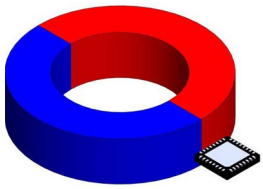
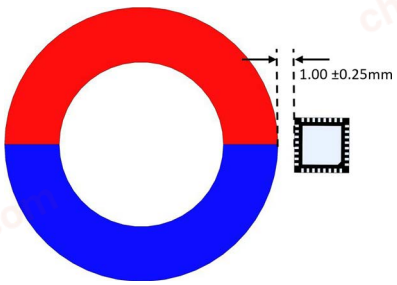
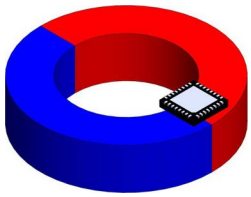
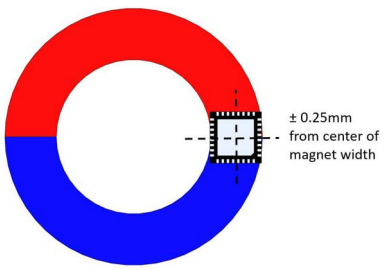
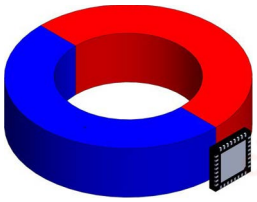
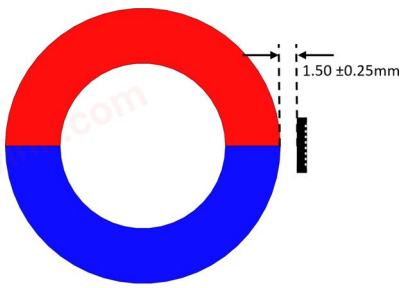
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Magnet and IC Package Placement

AEAT-9966 multi-axis capability comes from multiple integrated Hall devices that allow flexibility on the sensor mounting with respect to the magnet. Generally, the shaft-end configuration senses the vertical field (Z component perpendicular to the chip surface), and the rest of the configuration senses the horizontal field (X and Y components parallel to the chip surface).

The nominal mounting tolerance is indicated the following table.



Configuration	Gap Tolerance	X-Y Tolerance
Shaft End 		
Side Shaft 		
Axial 		
Radial 		

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NOTE: The two chips in AEAT-9966 are independent; subsequent explanations and definitions in this document are based on one chip.

Serial Interface Format

The AEAT-9966 serial interface hosts up to 10 different protocols for position output and memory access. The protocol is configurable with the combination of the physical I/O MSEL and M0 and memory settings PSEL, SPI4[0], and SPI4[1]. The default factory setting is all zeros, which is either SPI3 or SPI4-16a depending on the MSEL state. The output pin can be configured to high-impedance mode for multi-secondary connections or bus connections.

All protocol selections can be switched during operation.

MATS Table

Mode / Pin	SPI3	SSI3a	SSI3b	SSI2a	SSI2b	SPI4-16	SPI4-24a	SPI4-24b	SPI4-8	PWM
MSEL	0	0	0	0	0	1	1	1	1	1
PSEL	x	0	1	0	1	0	0	0	0	1
SPI4[1]	x	x	x	x	x	0	0	1	1	x
SPI4[0]	x	x	x	x	x	0	1	0	1	x
M0	0	1	1	1	1	NCS	NCS	NCS	NCS	-
M1	DIN	NSL	NSL	0	0	MOSI	MOSI	MOSI	MOSI	-
M2	SCK	SCL	SCL	SCL	SCL	SCK	SCK	SCK	SCK	-
M3	DO	DO	DO	DO	DO	MISO	MISO	MISO	MISO	PWM

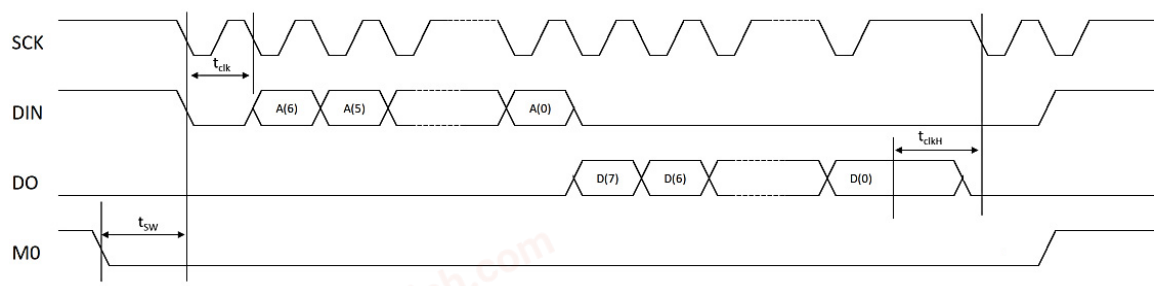
NOTE: PSEL, SPI4[1], and SPI4[0] are configured through memory. MSEL and M0 are configured through I/O pads.

Serial Peripheral Interface (SPI3)

SPI3 protocols allow access to memory read write only. Assert 0 on the MSEL and M0 pin to configure it. The SPI is implemented with CPOL=0 and CPHA=0; data is propagated on the clock falling edge.

- M1 → SPI_Data Input (DIN) signal for the SPI protocol, input to the AEAT-9966.
- M2 → SPI_Clock Input (SCK) signal for the SPI protocol, input to the AEAT-9966.
- M3 → SPI_Data Output (DO) signal for the SPI protocol, output from the AEAT-9966.

SPI3 Timing Diagram

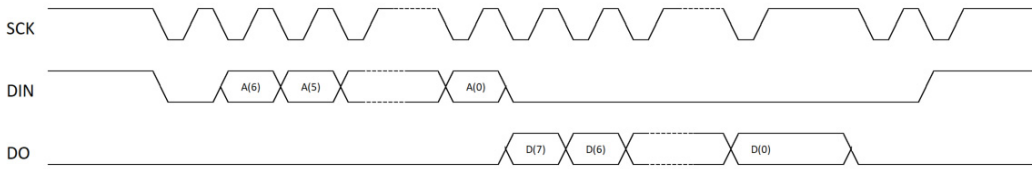


Symbol	Description	Min.	Typ.	Max.	Unit
t_{SW}	Time between the SCn falling edge and the CLK rising edge	1	—	—	µs
t_{clk}	Serial clock period	100	—	—	ns
t_{clkH}	CLK high time after the end of the last clock period	300	—	—	ns

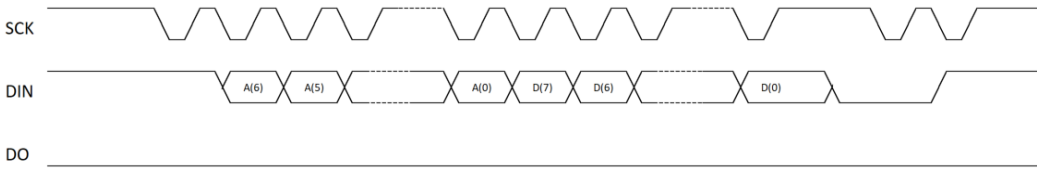
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NOTE: Read back the data to confirm that it has been written successfully.

SPI3 Read Sequence



SPI3 Write Sequence



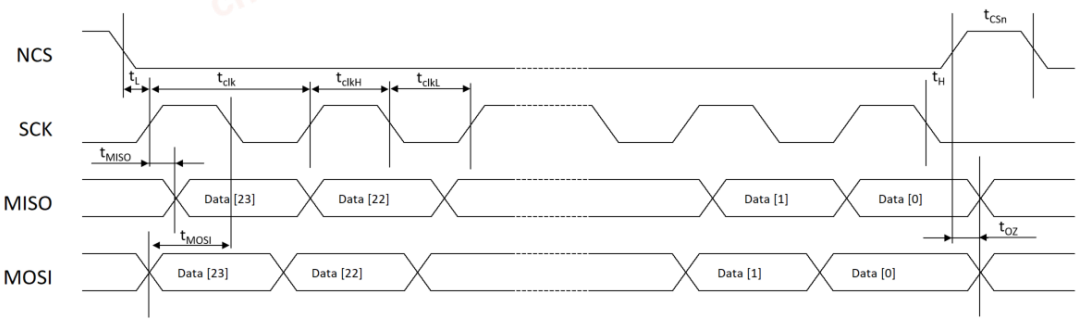
Serial Peripheral Interface (SPI4)

The SPI protocol uses four pins from the AEAT-9966. These four pins are shared between the UVW, SSI, and SPI protocols. To select the SPI4 protocol, assert 1 on the MSEL pin.

SPI4 protocols allow the user to access memory read or write and position data. It uses CPOL=0, CPHA=1 for triggering.

- M0 → SPI_Chip Select (NCS) signal for the SPI protocol, input to the AEAT-9966.
- M1 → SPI_Data Input (MOSI) signal for the SPI protocol, input to the AEAT-9966.
- M2 → SPI_Clock Input (SCK) signal for the SPI protocol, input to the AEAT-9966.
- M3 → SPI_Data Output (MISO) signal for the SPI protocol, output from the AEAT-9966.

SPI4 Timing Diagram



Symbol	Description	Min.	Typ.	Max.	Unit
t_L	Time between the SCn falling edge and the CLK rising edge	350	—	—	ns
t_{clk}	Serial clock period	100	—	—	ns
t_{clkL}	Low period of the serial clock	50	—	—	ns
t_{clkH}	High period of the serial clock	50	—	—	ns

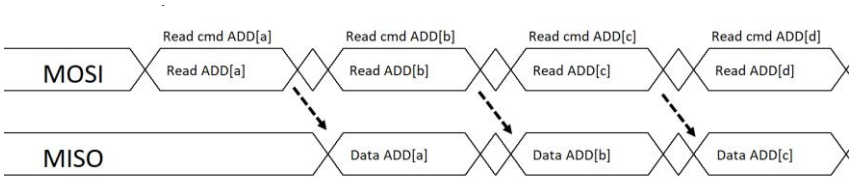
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Symbol	Description	Min.	Typ.	Max.	Unit
t_H	Time between the last falling edge of CLK and the rising edge of CSn	$t_{clk}/2$	—	—	ns
t_{CSn}	High time of CS between two transmissions	350	—	—	ns
t_{MOSI}	Data input valid to clock edge	20	—	—	ns
t_{MISO}	CLK edge to data output valid	—	—	51	ns
t_{OZ}	Time between the CSn rising edge and the MISO HiZ	—	—	10	ns

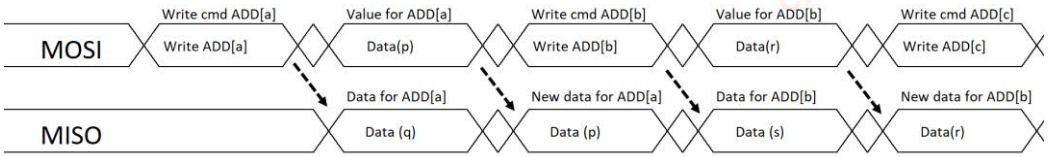
NOTE: Read back the data to confirm that it has been written successfully.

SPI4 Command and Data Frame

SPI4 Read Sequence



SPI4 Write Sequence



SPI4-16: 16-Bit (Parity)

By default, the chip is configured to SPI4 16-bit selection; PSEL = 0, SPI4[1] = 0, SPI4[0] = 0 in the register setting.

	Data Format																			
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller to Peripheral					P	RW	0	0	0	0	0	0	Addr/Data[7:0]							
Peripheral to Controller (memory)					P	EF	0	0	0	0	0	0	Data[7:0]							
Peripheral to Controller (pos 8b)					P	EF	Pos[7:0]						0	0	0	0	0	0		
Peripheral to Controller (pos 9b)					P	EF	Pos[8:0]							0	0	0	0	0		
Peripheral to Controller (pos 10b)					P	EF	Pos[9:0]								0	0	0	0		
Peripheral to Controller (pos 11b)					P	EF	Pos[10:0]									0	0	0		
Peripheral to Controller (pos 12b)					P	EF	Pos[11:0]										0	0		
Peripheral to Controller (pos 13b)					P	EF	Pos[12:0]											0		
Peripheral to Controller (pos 14b)					P	EF	Pos[13:0]													
Peripheral to Controller (pos 15b)				P	EF	Pos[14:0]														
Peripheral to Controller (pos 16b)			P	EF	Pos[15:0]															
Peripheral to Controller (pos 17b)		P	EF	Pos[16:0]																
Peripheral to Controller (pos 18b)	P	EF	Pos[17:0]																	

P: Parity
EF: Error Flag
RW: Read = 1, Write = 0

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SPI4-24a: 24-Bit (Parallel CRC)

To configure the chip to SPI4 24-bit selection (Parallel CRC), set PSEL = 0, SPI4[1] = 0, SPI4[0] = 1 in the register setting.

	Data Format																								
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller to Peripheral					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Peripheral to Controller (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Peripheral to Controller (pos 8b)					W	E	Pos[7:0]								0	0	0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 9b)					W	E	Pos[8:0]									0	0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 10b)					W	E	Pos[9:0]										0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 11b)					W	E	Pos[10:0]											0	0	0	CRC[7:0]							
Peripheral to Controller (pos 12b)					W	E	Pos[11:0]												0	0	CRC[7:0]							
Peripheral to Controller (pos 13b)					W	E	Pos[12:0]													0	CRC[7:0]							
Peripheral to Controller (pos 14b)					W	E	Pos[13:0]														CRC[7:0]							
Peripheral to Controller (pos 15b)				W	E	Pos[14:0]															CRC[7:0]							
Peripheral to Controller (pos 16b)			W	E	Pos[15:0]																CRC[7:0]							
Peripheral to Controller (pos 17b)		W	E	Pos[16:0]																	CRC[7:0]							
Peripheral to Controller (pos 18b)	W	E	Pos[17:0]																		CRC[7:0]							

	Input for CRC Calculation																								
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
									0	RW	0	0	0	0	0	0	Addr/Data[7:0]								Data+CRC =24b
									W	E	0	0	0	0	0	0	Data[7:0]								Data+CRC =24b
									W	E	Pos[7:0]							0	0	0	0	0	0		Data+CRC =24b
									W	E	Pos[8:0]								0	0	0	0	0		Data+CRC =24b
									W	E	Pos[9:0]									0	0	0	0		Data+CRC =24b
									W	E	Pos[10:0]										0	0	0		Data+CRC =24b
									W	E	Pos[11:0]											0	0		Data+CRC =24b
									W	E	Pos[12:0]												0		Data+CRC =24b
									W	E	Pos[13:0]														Data+CRC =24b
W	E	Pos[14:0]																0	0	0	0	0	0	0	Data+CRC >24b
W	E	Pos[15:0]																	0	0	0	0	0	0	Data+CRC >24b
W	E	Pos[16:0]																		0	0	0	0	0	Data+CRC >24b
W	E	Pos[17:0]																			0	0	0	0	Data+CRC >24b

When Data+CRC =24b, use Data (16b) to calculate CRC based
When Data+CRC >24b, pad 0 at behind Data until it is 24b, then calculate CRC

W: Warning
E: Error
RW: Read = 1, Write = 0

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SPI4-24b: 24-Bit (Serial CRC)

To configure the chip to SPI4 24-bit selection (Serial CRC), set PSEL = 0, SPI4[1] = 1, SPI[0] = 0 in the register setting.

Data Format

	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller to Peripheral					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Peripheral to Controller (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Peripheral to Controller (pos 8b)					W	E	Pos[7:0]						0	0	0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 9b)					W	E	Pos[8:0]							0	0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 10b)					W	E	Pos[9:0]								0	0	0	0	CRC[7:0]							
Peripheral to Controller (pos 11b)					W	E	Pos[10:0]									0	0	0	CRC[7:0]							
Peripheral to Controller (pos 12b)					W	E	Pos[11:0]										0	0	CRC[7:0]							
Peripheral to Controller (pos 13b)					W	E	Pos[12:0]											0	CRC[7:0]							
Peripheral to Controller (pos 14b)					W	E	Pos[13:0]												CRC[7:0]							
Peripheral to Controller (pos 15b)				W	E	Pos[14:0]													CRC[7:0]							
Peripheral to Controller (pos 16b)			W	E	Pos[15:0]														CRC[7:0]							
Peripheral to Controller (pos 17b)		W	E	Pos[16:0]															CRC[7:0]							
Peripheral to Controller (pos 18b)	W	E	Pos[17:0]																CRC[7:0]							

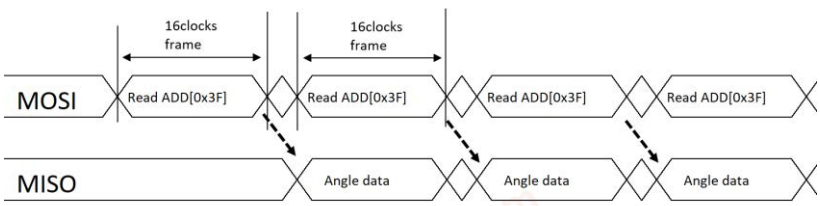
Input for CRC Calculation

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RW	0	0	0	0	0	0	Addr/Data[7:0]												
W	E	0	0	0	0	0	0	Data[7:0]												
W	E	Pos[7:0]										0	0	0	0	0	0		
W	E	Pos[8:0]											0	0	0	0	0		
W	E	Pos[9:0]												0	0	0	0		
W	E	Pos[10:0]													0	0	0		
W	E	Pos[11:0]														0	0		
W	E	Pos[12:0]															0		
W	E	Pos[13:0]																	
W	E	Pos[14:0]																	
W	E	Pos[15:0]																	
W	E	Pos[16:0]																	
W	E	Pos[17:0]																	

W: Warning
E: Error
RW: Read = 1, Write = 0

Position Read

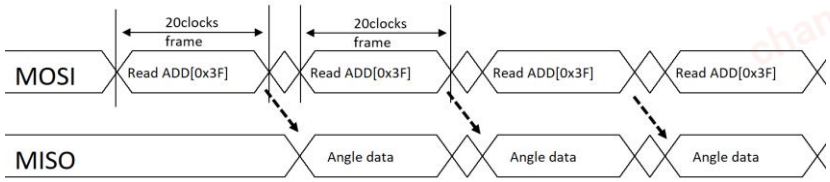
Absolute position data can be obtained by sending a read command to address 0x3F.



In the event of higher single-turn resolution (15-bit and above), the command and data frame size is adjusted accordingly.

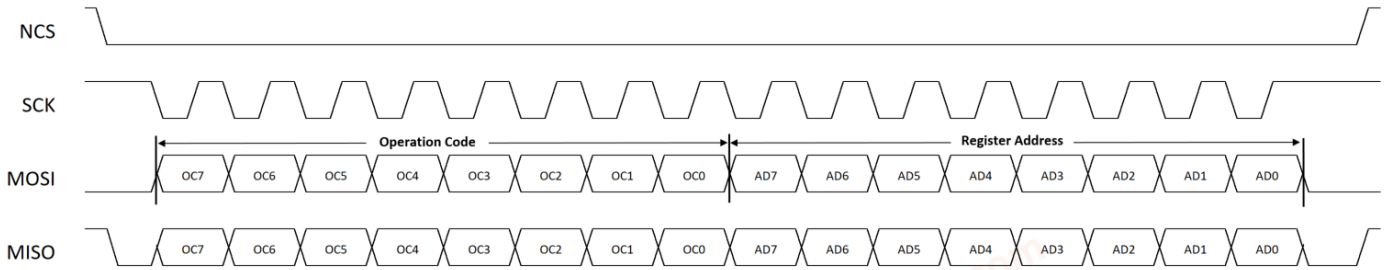
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Example: 18bit + 2bit (parity and error)



SPI4-8

To configure the chip to SPI4 8-bit selection, set PSEL = 0, SPI4[1] = 1, SPI4[0] = 1 in the register setting.

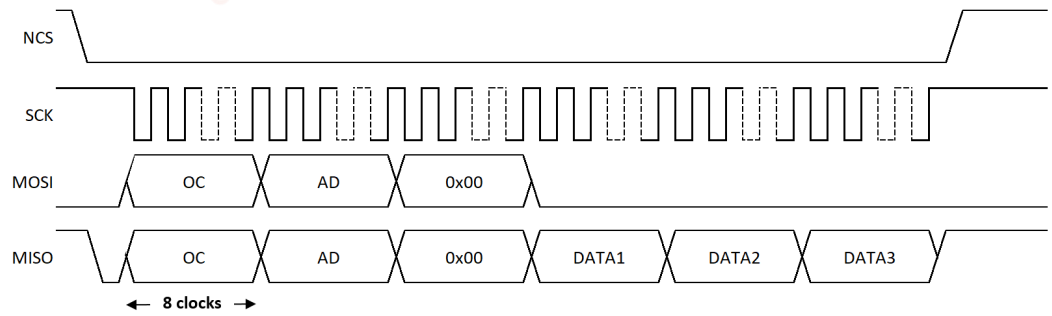


When NCS is low, the communication line is activated and the data is sampled on the rising edge of SCK.

The MISO state turns to high impedance mode (hi-Z) when NCS is high. The transmission works over specific operation code (OC).

Register Read (OC=0x81'h)

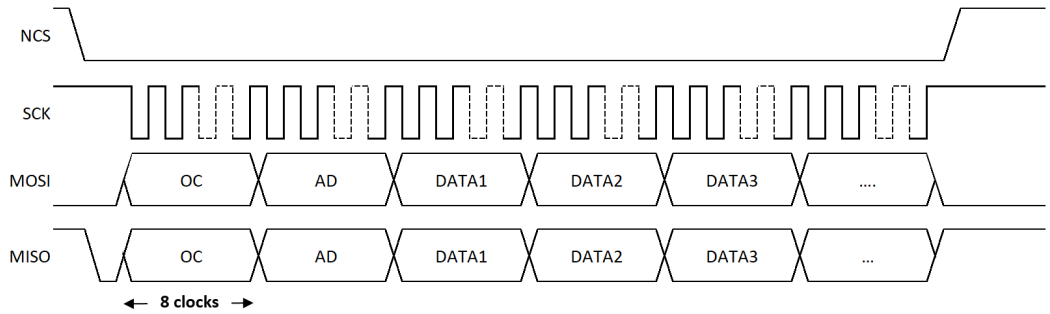
This operation is used to read data from the internal register of the chip. It can be performed consecutively starting from any register address. The data continues to be transmitted as long the clock (SCK) is sent and the chip select (NCS) remains active.



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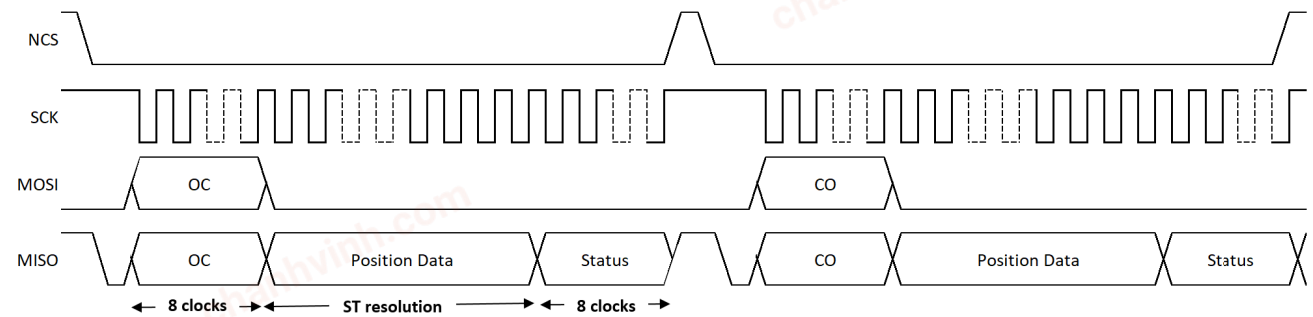
Register Write (OC=0xCF'h)

This operation is used to write data into the internal register of the chip. It can be performed consecutively starting from any register address. The subsequent data byte is written into the next register address (AD+1), while the NCS signal stays active. Complete written data is transmitted back via MISO.

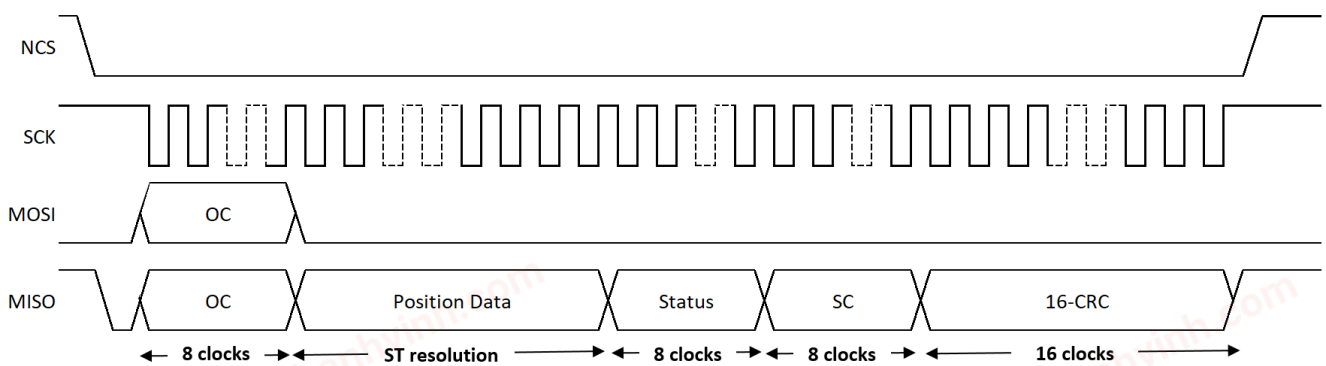


Position Read (OC=0xA6'h)

Read the absolute position by sending the operation code, and the data will be transmitted on the MISO line. The position data consists of the single-turn position data length and status byte. The position data length follows the single-turn resolution setting.



For safety format, there are additional bytes: sequence counter (SC) and CRC.



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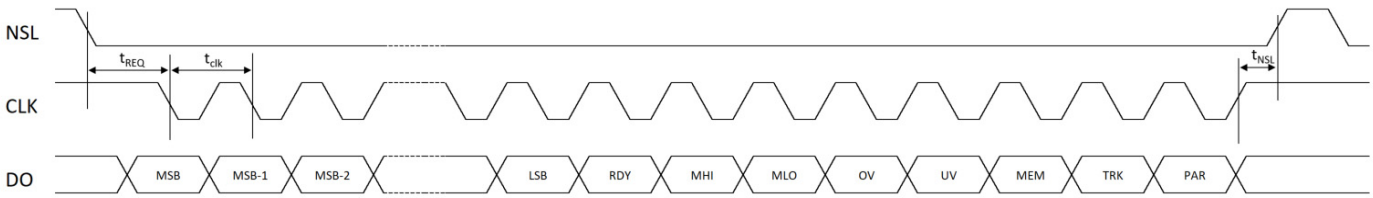
Serial Synchronous Interface 3-Wire (SSI3)

The SSI3 protocol uses three pins from the AEAT-9966. These three pins are shared between the UVW, SSI, and SPI protocols. To activate the SSI3 protocol, assert 0 on the MSEL pin and assert 1 on the M0 pin.

- M1 → SSI_NSL Input (NSL) signal for the SSI protocol, input to the AEAT-9966.
- M2 → SSI_Clock Input (CLK) signal for the SSI protocol, input to the AEAT-9966.
- M3 → SSI_Data Output (DO) signal for the SSI protocol, output from the AEAT-9966.

It is available in two options per PSEL register setting.

SSI Protocol Timing Diagram. Default: Data Output with 3-Wire SSI to 10-MHz Clock Rates

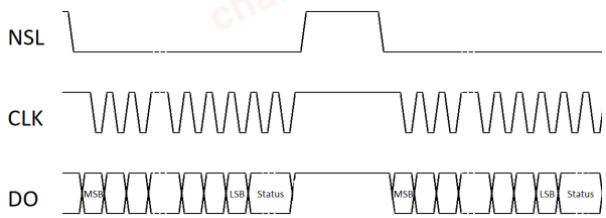


Symbol	Description	Min.	Typ.	Max.	Unit
t_{clk}	SSI_SPI_SEL switch time	1	—	—	µs
t_{REQ}	SCL high time between the NSL falling edge and the first SCL falling edge	300	—	—	ns
t_{NSL}	NSL high time between two successive SSI reads	200	—	—	ns

SSI3(A)

By default, the chip is configured to SSI3(A) selection; PSEL = 0 in the register setting.

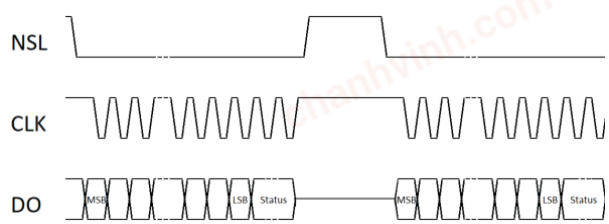
The DO pin is held at a high state once the NSL pin is high.



SSI3(B)

To configure the chip to SSI3(B) selection, set PSEL = 1 in the register setting.

The DO pin is at a tristate (high-impedance) state once the NSL pin is high.



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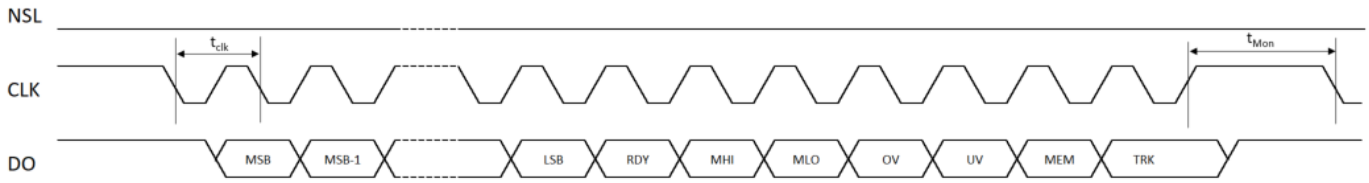
Serial Synchronous Interface 2-Wire (SSI2)

The SSI2 protocol uses two pins from the AEAT-9966. These two pins are shared between the SSI and SPI protocols. To activate the SSI2 protocol, assert 0 on the MSEL and M1 pins and assert 1 on the M0 pin upon power-up.

- M2 → SSI_Clock Input (CLK) signal for the SSI protocol, input to the AEAT-9966.
- M3 → SSI_Data Output (DO) signal for the SSI protocol, output from the AEAT-9966.

Depending on the PSEL setting, it can be configured as SSI2(A) Ring Mode or SSI2(B) No Ring Mode.

Data is latched on the first CLK falling edge and is transmitted on the next falling edge.

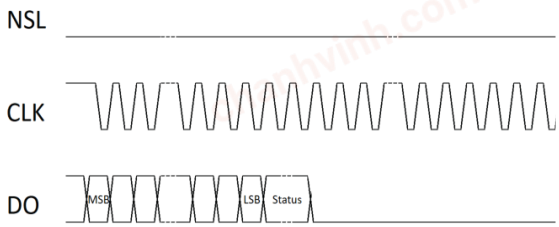


Symbol	Description	Min.	Typ.	Max.	Unit
t_{clk}	Serial clock period	250	—	$t_M/2$	ns
t_M	Time required to place the chip in standby mode	—	16.5	18.0	µs

SSI2(A)

By default, the chip is configured to SSI2(A) selection; PSEL = 0 in the register setting.

Outputs single data position and remains low after LSB until the next monoflop (t_M) expires.

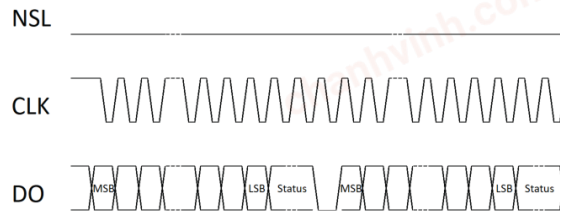


SSI2(B)

To configure the chip to SSI2(B) selection, set PSEL = 1 in the register setting.

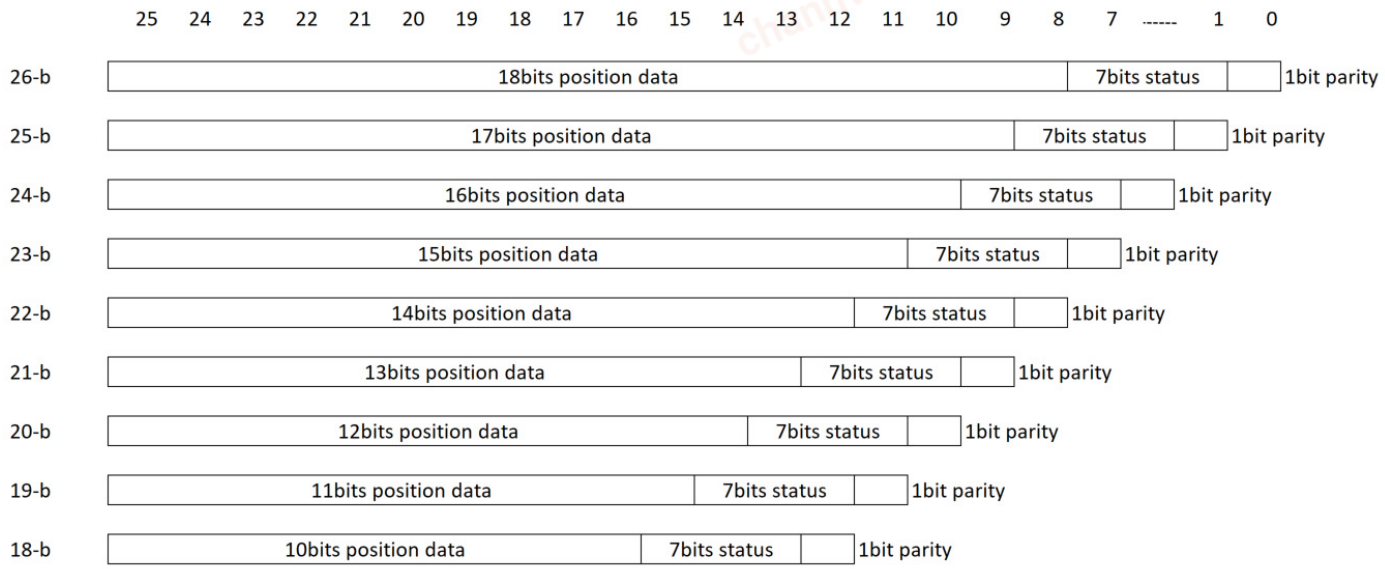
The same position data can be continuously output by sending clock train, and the data is separated by a single low pulse.

Data will be refreshed when the next monoflop (t_M) expires.



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SSI Read Data Format



NOTE:

- 7-b status: {Ready, MHI, MLO, OV, UV, Mem, Trck}
- See Alarm for more details.

Safety and Non-safety Protocol Format

The position serial interface is available in Safety and Non-safety format; applicable for SSI3, SSI2, and SPI-8.

Position (n-bit)	Status / Alarm (7-bit)							Parity (1-bit)
Position[(n-1):0]	READY	MHI	MLO	OV	UV	MEM	TRK	parity

Position (n-bit)	Status / Alarm (8-bit)							SC (8-bit)	CRC (8/16-bit)
Position[(n-1):0]	Status[1:0] (1)	MHI	MLO	OV	UV	MEM	TRK	SC [7:0] (2)	CRC [7/15:0] (3)

NOTE:

1. 2-bit status to indicate the safety status:
   - Status = 2b'00: Encoder not ready.
   - Status = 2b'01: Encoder not ready, Force test failed.
   - Status = 2b'10: Encoder ready.
   - Status = 2b'11: Encoder ready, Force test passed.
2. SC denotes as *Sequence Count* or life counter that automatically increments on every position transmission. The counting starts from 1 to 255, and the initial value upon power-up is configurable.
3. CRC polynomial 16b-CRC is 0x1021'h and 8b-CRC is 0x1D'h. The initial value is configurable (0x0000, 5555, AAAA, FFFF).

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Alarm

Details of the alarm bit are available in the following register.

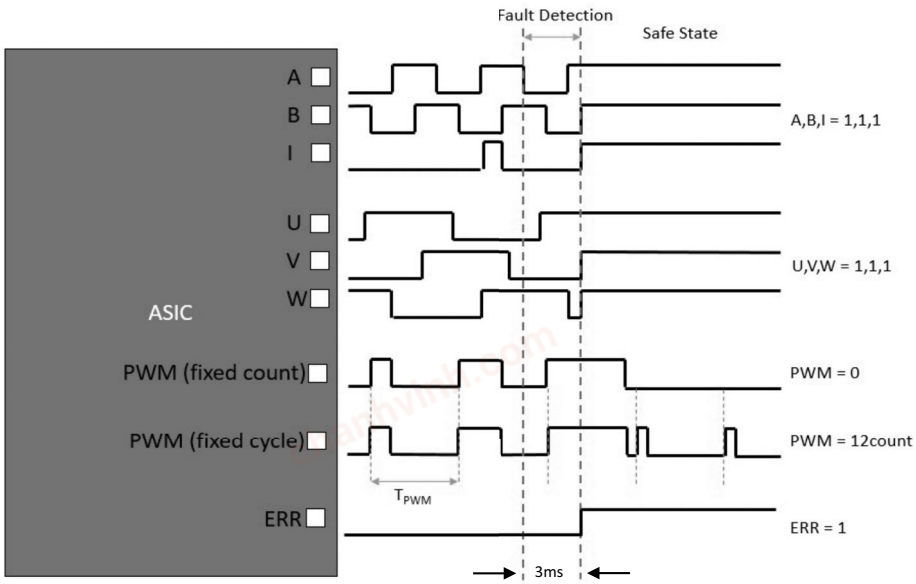
Address	Bit							
	7	6	5	4	3	2	1	0
0x29	RDY[1]	RDY[0]	MHI	MLO	OV	UV	MEM	TRACK

- **Ready:** The chip is ready, and the ready value is 1.
- **Parity:** 1-b parity is even parity.
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is set high consistently, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is set low consistently, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Overvoltage (OV) Error:** This indicates that the input supply has exceeded the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Undervoltage (UV) Error:** This indicates that the input supply has dropped below the limit. When this is set high consistently, check the supply line. The value for this alarm is represented as 1.
- **Memory Error (MEM) Error:** This indicates that memory corruption has occurred. When this is set high, perform a power-cycle to reload the memory. The value for this alarm is represented as 1.
- **Tracker (TRK) Error:** This indicates that the angular error has exceeded 5° within 5 ms. When this is set high consistently, perform a power-cycle to re-initialize the sensor. The value for this alarm is represented as 1.

The ERR pin is a dedicated hardware pin for error indication and will automatically be cleared once all error bits in the register are cleared. It is a push-pull output configuration; float if unused. The output of the ERR pin uses OR logic, meaning that if any of the alarm bits (MHI, MLO, OV, UV, MEM, TRACK) is high, the ERR pin output will also become high.

Clear the alarm register by sending 0x3F'h to address 0x12'h.

Under Safety Mode, once a fault is detected, the error pin flags to high after 3 ms. The incremental ABI, the commutation UVW, and PWM enter Safe State. Alternatively, users may turn OFF ABI/UVW safe state behavior by setting 1 on address 0x01'h bit [3] (Inc. Safety Off).

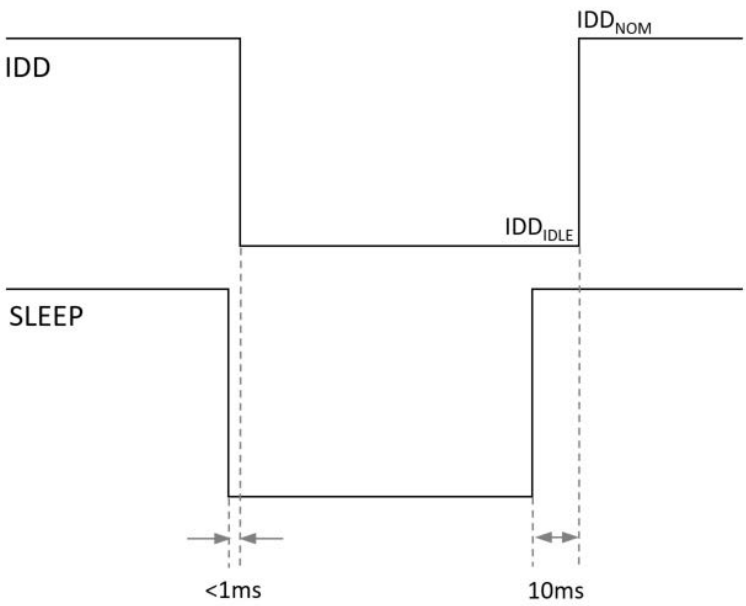


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Power Modes

The AEAT-9966 is designed with two power modes:

- **Active Mode** where the chip operates under full functions with normal current consumption, IDD_{NOM}.
- **Sleep Mode** powers down the chip front-end and digital processing blocks, leaving only the detection block to track on user input with low current consumption, IDD_{IDLE}. The SLEEP pin is an active low, tied to VDD is unused.



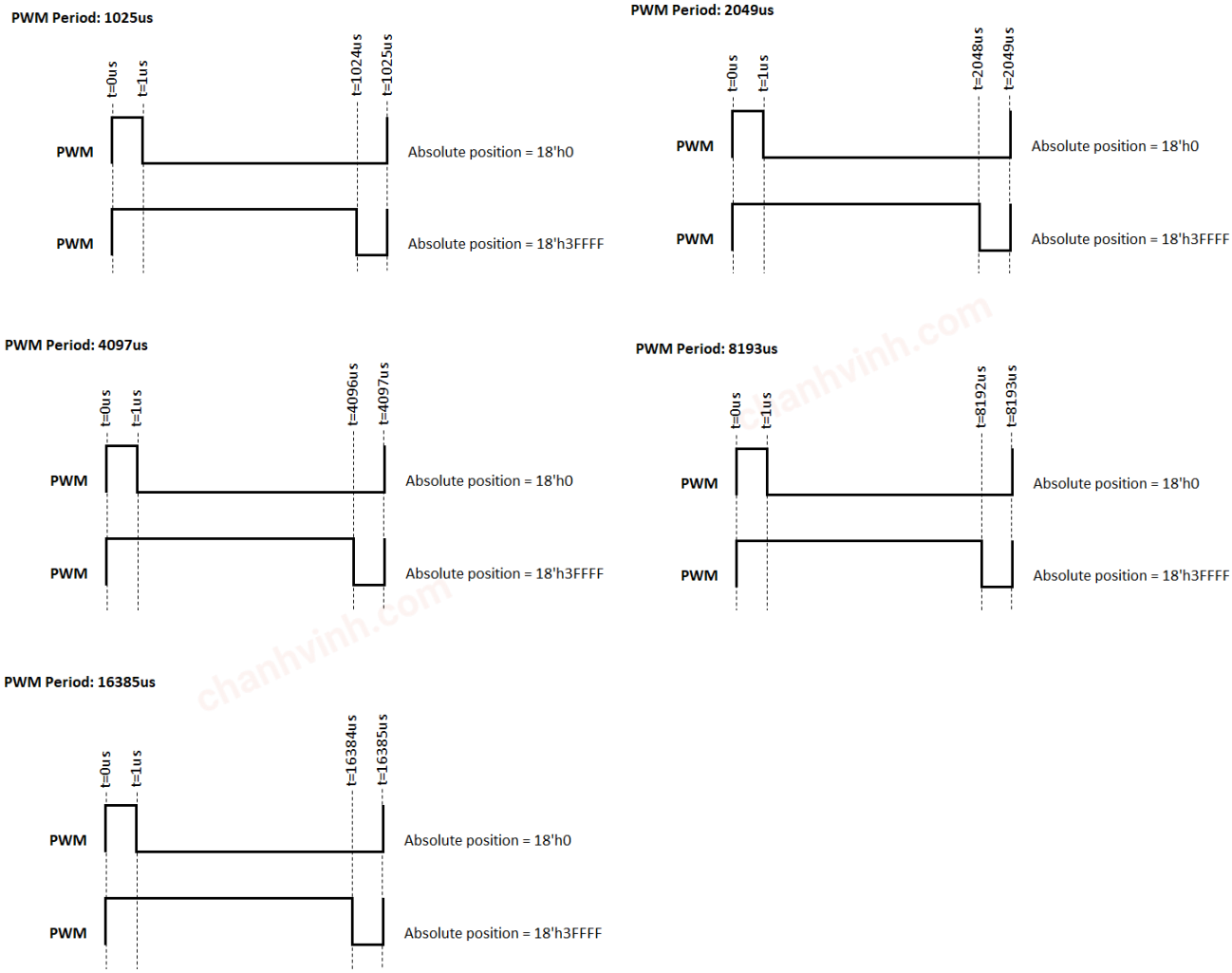
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PWM

The PWM protocol uses one output pin (W_PWM) from the AEAT-9966. Note that the W_PWM pin is shared between the UVW and PWM protocols. The PWM signals are configurable to have a period of 1025, 2049, 4097, 8193, or 16,385 µs. During power-up, the PWM signal is 0 before chip ready.

PWM Signals (Period = 1025/2049/4097/8193/16385 µs)

PWM Period: 1025, 2049, 4097, 8193, 16385 µs

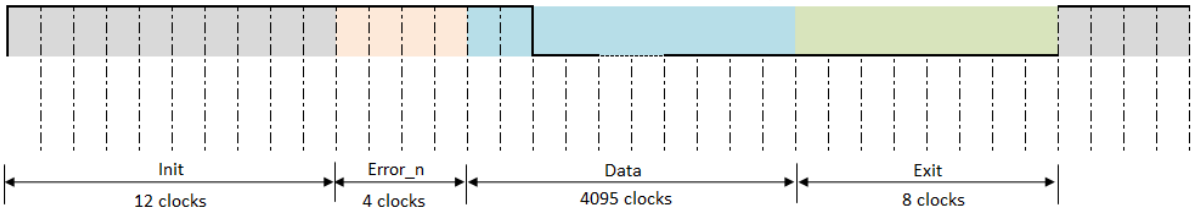


The PWM protocol is also available with Init, Error_n, and Exit along with data information.

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PWM Signals (Period = 1047/2071/4119/8215/16407 µs)

PMW Period: 4119 µs



Incremental Output Format

The AEAT-9966 provides ABI and UVW signals to indicate the incremental position of the motor.

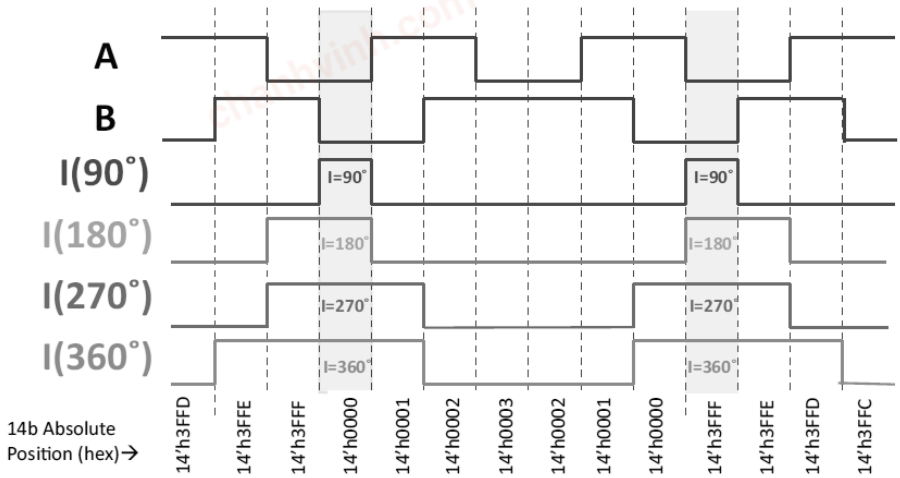
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

The index signal marks the absolute angular position and typically occurs once per revolution. The ABI signal is configurable using the memory map registers. It supports the following configuration:

- Programmable CPR: 1 to 20,000 CPR
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (°e)
- Programmable I-state: 90, 180, 270, or 360 electrical degrees (°e)

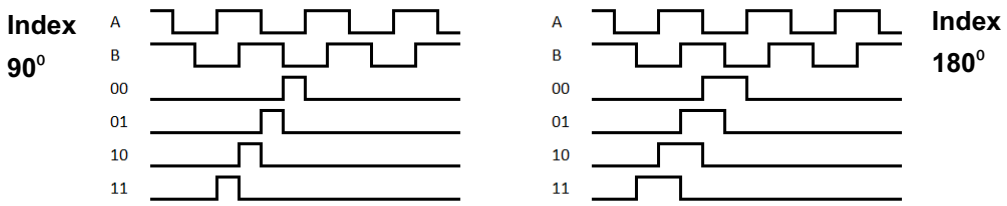
Figure 5: ABI Signal (4096 CPR, with Different I-Width Settings), Assuming the User Sets Hysteresis at 0.02 Mechanical Degrees

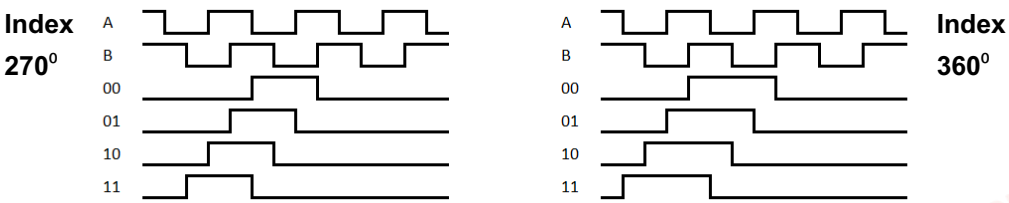


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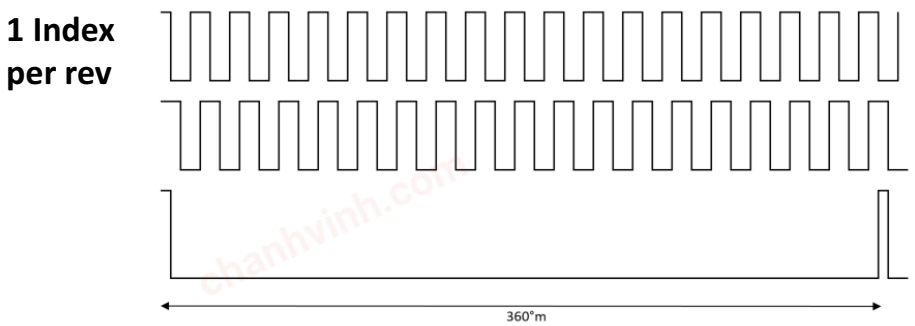
The index position is configurable among the incremental states.

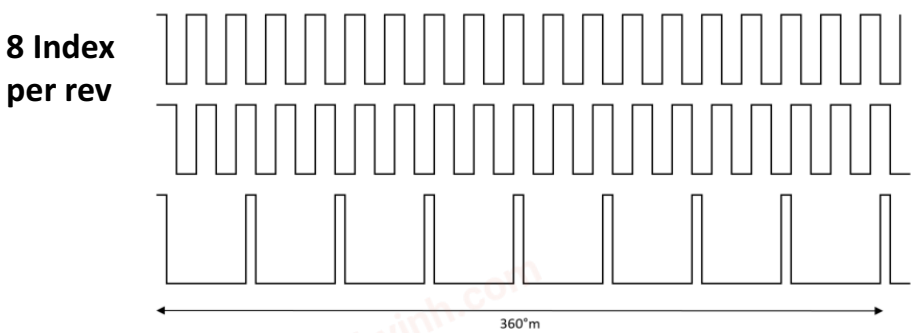
The index signal rises high once per turn at the absolute zero position.





The number of indexes per revolutions is configurable from 1 pulse up to 128 pulses.



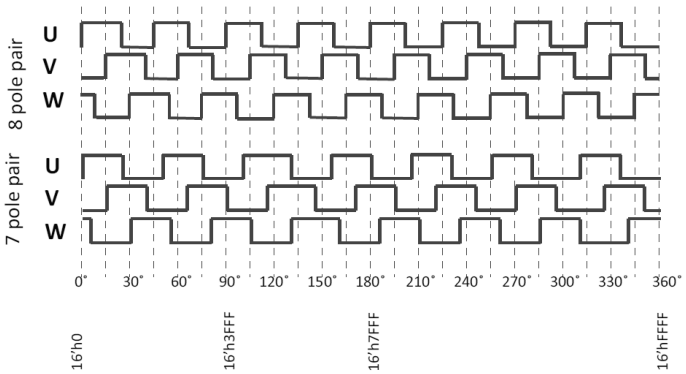


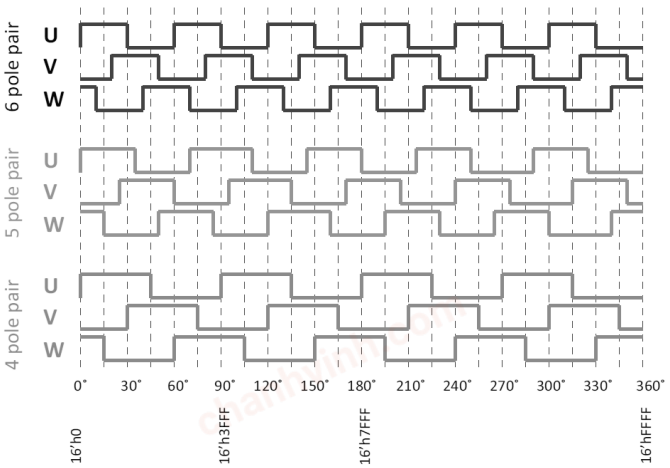
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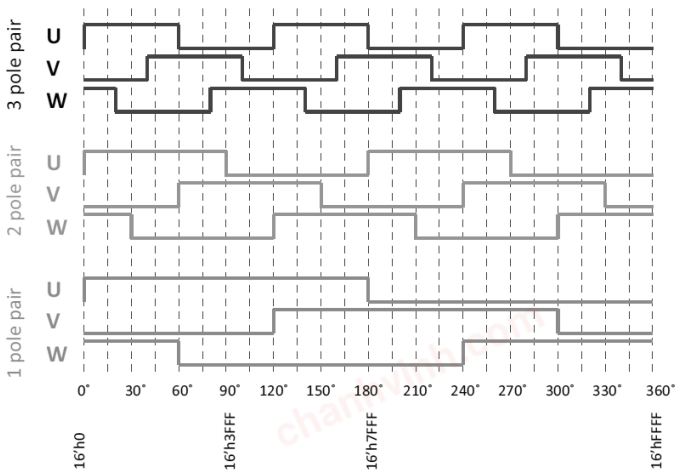
UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. Note that the W_PWM pin is shared between the UVW and PWM protocols.

The AEAT-9966 can configure pole pairs from 1 to 32 (equivalent to 2 to 64 poles).



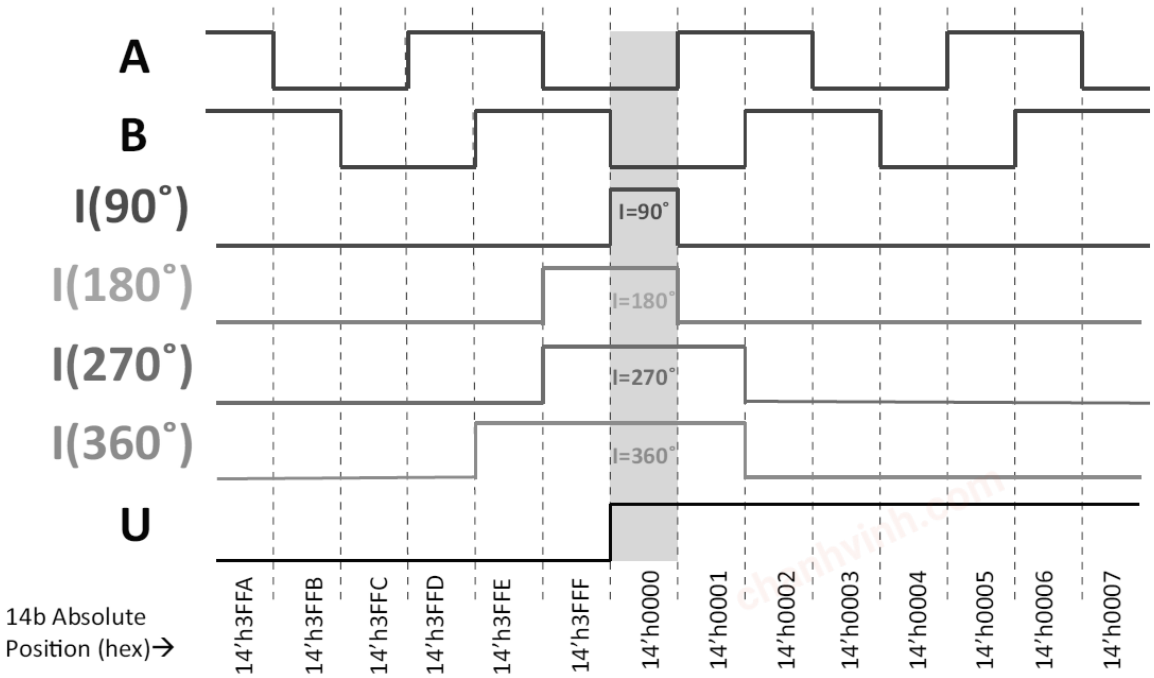




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Note that signal U from the UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 6: U-to-I Tagging



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Package Drawings (in mm)

Figure 7: AEAT-9966, 32 QFN Dimensions

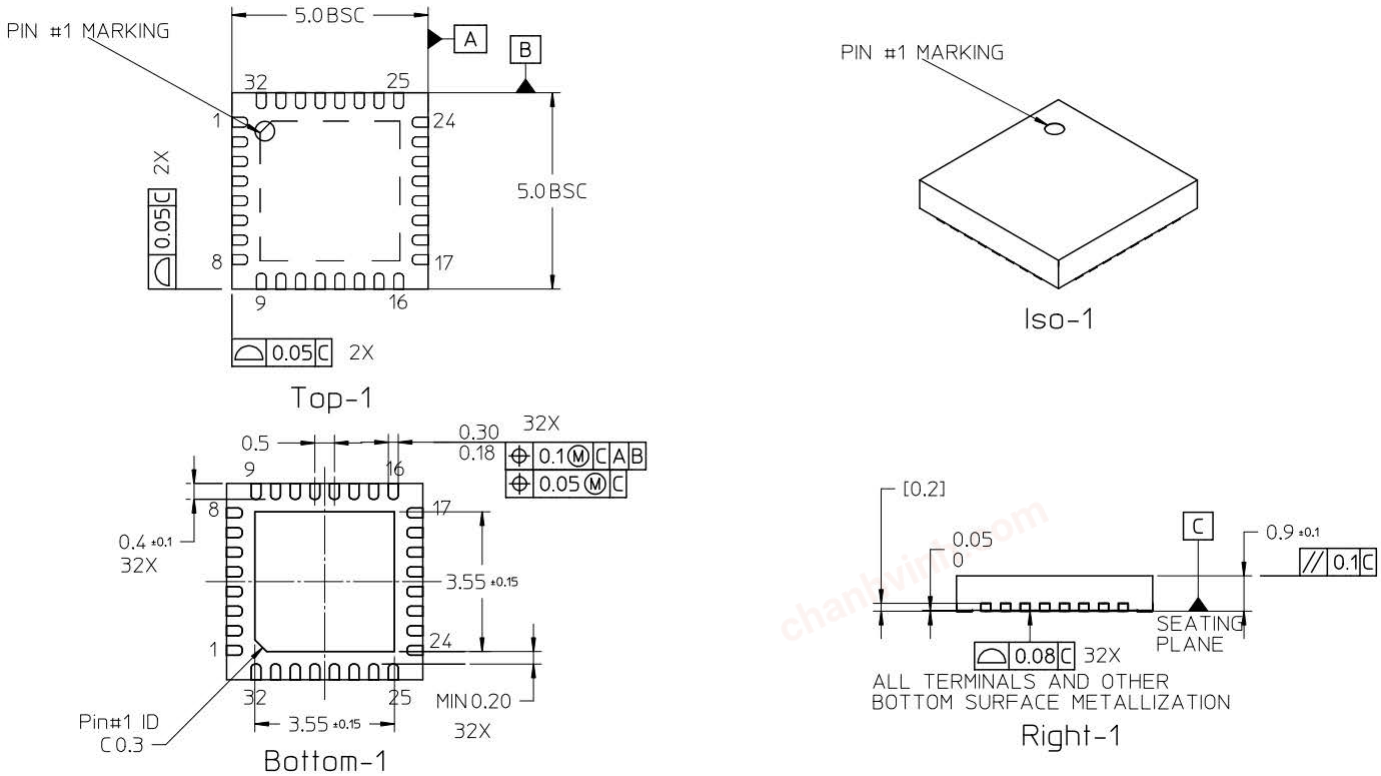
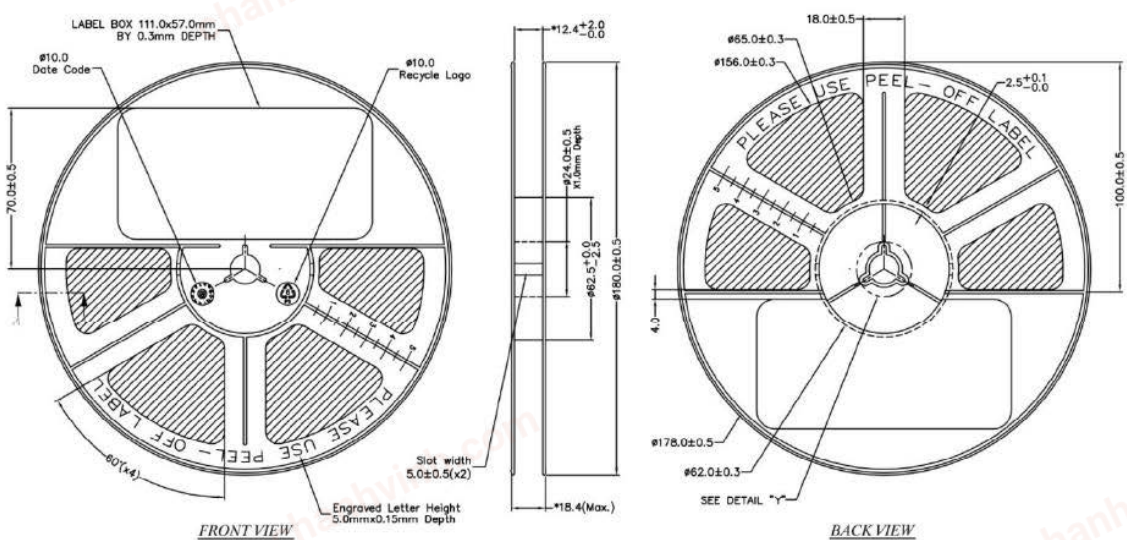


Figure 8: Reel Dimensions



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Product Ordering Information

Ordering Part Number	Product Description	Package	Delivery Form
AEAT-9966-100	18-Bits Magnetic Encoder On-Off Axis Tape Reel 1000	QFN 32 leads, 5 mm × 5 mm	Tape and Reel
AEAT-9966-102	18-Bits Magnetic Encoder On-Off Axis Tape Reel 100	QFN 32 leads, 5 mm × 5 mm	Tape and Reel
AEAT-9966-Q32	18-Bits Magnetic Encoder On-Off Axis	QFN 32 leads, 5 mm × 5 mm	Tube
HEDS-9966EVB	AEAT-9966 Evaluation Board	—	—
HEDS-9966PRGEVB	AEAT-9966 Programming Kit with Evaluation Board and Magnet	—	—

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