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BROADCOM®

Data Sheet

ACSL-6xx0

Multi-Channel and Bi-Directional, 15 MBd Digital Logic Gate Optocoupler

Description

The Broadcom® ACSL-6xx0 are truly isolated, multi-channel and bi-directional, high-speed optocouplers. Integration of multiple optocouplers in monolithic form is achieved through patented process technology. These devices provide full duplex and bidirectional isolated data transfer and communication capability in compact surface mount packages. Available in the 15-Mbd speed option and wide supply voltage range.

These high channel density make them ideally suited to isolating data conversion devices, parallel buses and peripheral interfaces.

They are available in 8-pin and 16–pin narrow-body SOIC package and are specified over the temperature range of –40°C to +100°C.

Features

- Available in dual, triple and quad channel configurations
- Bi-directional
- Wide supply voltage range: 3.0V to 5.5V
- High-speed: 15 MBd typical, 10 MBd minimum
- 10kV/µs minimum Common Mode Rejection (CMR) at Vcm = 1000V
- LSTTL/TTL compatible
- Safety and regulatory approvals
  - 2500 V_{rms} for 1 min. per UL1577
  - cUL (CSA Component Acceptance Notice 5A)
  - IEC/EN/DIN EN 60747-5-5
- 16-pin narrow-body SOIC package for triple and quad channels
- –40°C to 100°C temperature range

Applications

- Serial Peripheral Interface (SPI)
- Inter-Integrated Interface (I^2C)
- Full duplex communication
- Isolated line receiver
- Microprocessor system interfaces
- Digital isolation for A/D and D/A conversion
- Instrument input/output isolation
- Ground loop elimination

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

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Device Selection Guide

Device Number	Channel Configuration	Package
ACSL-6210	Dual, Bi-Directional	`8-pin Small Outline
ACSL-6300	Triple, All-in-One	16-pin Small Outline
ACSL-6310	Triple, Bi-Directional, 2/1	16-pin Small Outline
ACSL-6400	Quad, All-in-One	16-pin Small Outline
ACSL-6410	Quad, Bi-Directional, 3/1	16-pin Small Outline
ACSL-6420	Quad, Bi-Directional, 2/2	16-pin Small Outline

Ordering Information

ACSL-6xx0 is UL Recognized with 2500 V_{rms} for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	RoHS Compliant[a]	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACSL-6210	-00RE	SO-8	X			100 per tube
	-06RE	SO-8	X		X	100 per tube
	-50RE	SO-8	X	X		1500 per reel
	-56RE	SO-8	X	X	X	1500 per reel
ACSL-6300	-00TE	SO-16	X			50 per tube
ACSL-6310	-06TE	SO-16	X		X	50 per tube
ACSL-6400	-50TE	SO-16	X	X		1000 per reel
ACSL-6410	-56TE	SO-16	X	X	X	1000 per reel
ACSL-6420						

a. The ACSL-6xx0 product family is only offered in RoHS compliant option.

To order, choose a part number from the Part Number column and combine it with the desired option from the RoHS Compliant column to form an order entry.

Example 1:

ACSL-6210-56RE refers to ordering a surface mount SO-8 package in tape and reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

ACSL-6400-00TE refers to ordering a surface mount SO-16 package product in tube packaging and in RoHS compliant.

Pin Description

Symbol	Description	Symbol	Description
V_{DD1}	Power Supply 1	GND1	Power Supply Ground 1
V_{DD2}	Power Supply 2	GND2	Power Supply Ground 2
$ANODE_x$	LED Anode	NC	Not Connected
$CATHODE_x$	LED Cathode	VOX	Output Signal

Truth Table

LED	Output
ON	L
OFF	H

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Functional Diagrams

Figure 1: ACSL-6210 – Dual-Ch, Bi-Dir

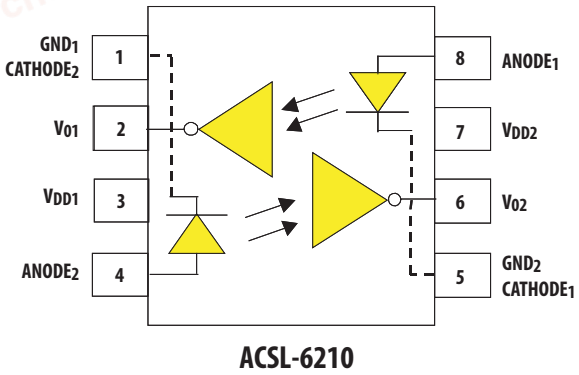


Figure 2: ACSL-6300 – Triple-Ch, All-in-One

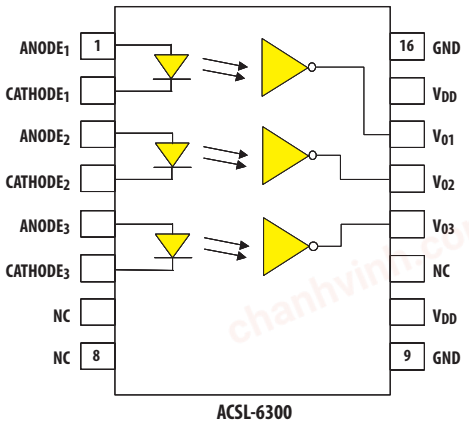


Figure 3: ACSL-6310 – Triple-Ch, Bi-Dir (2/1)

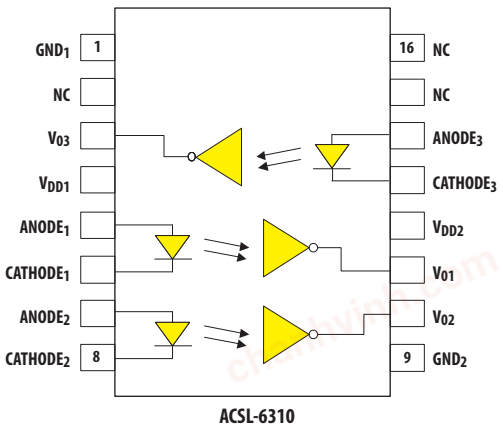


Figure 4: ACSL-6400 – Quad-Ch, All-in-One

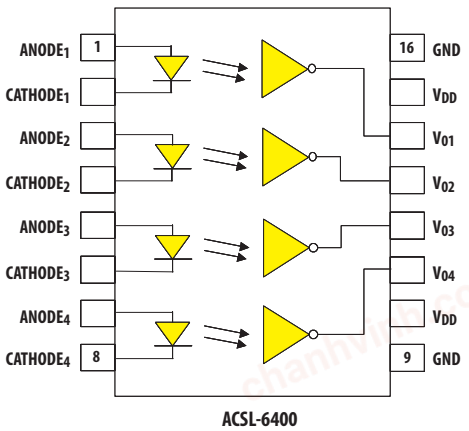


Figure 5: ACSL-6410 – Quad-Ch, Bi-Dir (3/1)

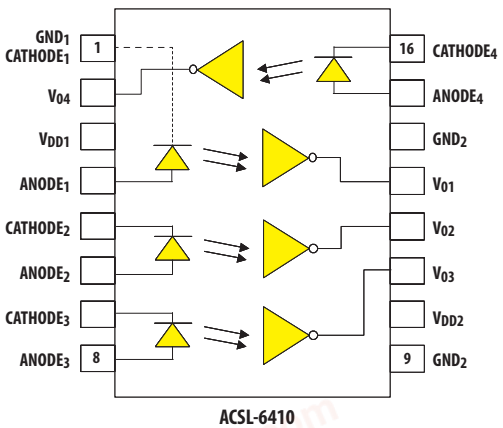
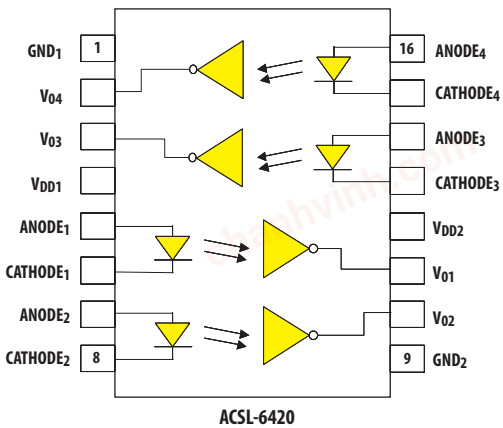


Figure 6: ACSL-6420 – Quad-Ch, Bi-Dir (2/2)



A 0.1-µF bypass capacitor must be connected as close as possible between the power supply pins, VDD and GND, VDD1 and GND1, VDD2 and GND2.

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Schematic Diagrams

The ACSL-6xx0 series optocouplers feature the GaAsP LEDs with proprietary back emission design. They offer the designer a broad range of input drive current, from 7 mA to 15 mA, thus providing greater flexibility in designing the drive circuit.

The output detector integrated circuit (IC) in the optocoupler consists of a photodiode at the input of a two-stage amplifier that provides both high gain and high bandwidth. The secondary amplifier stage of the detector IC feeds into an open collector Schottky-clamped transistor.

The entire output circuit is electrically shielded so that any common-mode transient capacitively coupled from the LED side of the optocoupler is diverted from the photodiode to ground. With this electric shield, the optocoupler can withstand transients that slopes up to 10,000V/µs, and amplitudes up to 1000V.

Figure 7: ACSL-6210 – Dual-Ch, Bi-Dir

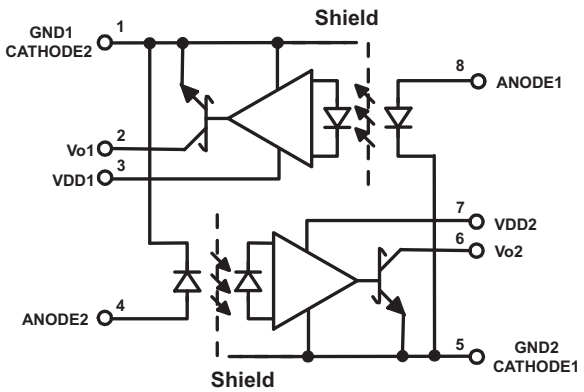


Figure 8: ACSL-6300 – Triple-Ch, All-in-One

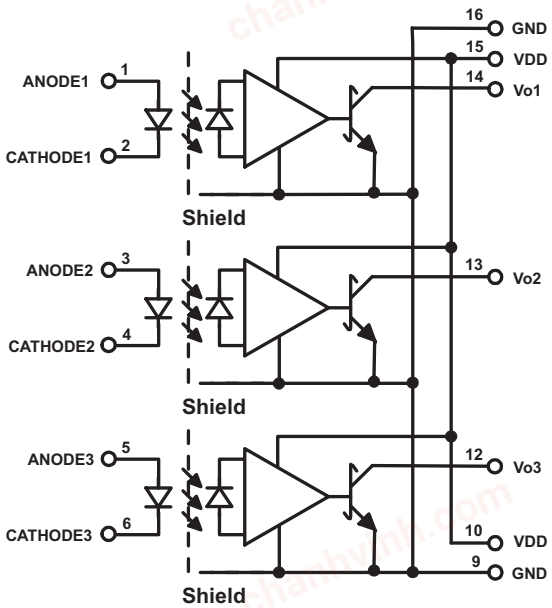
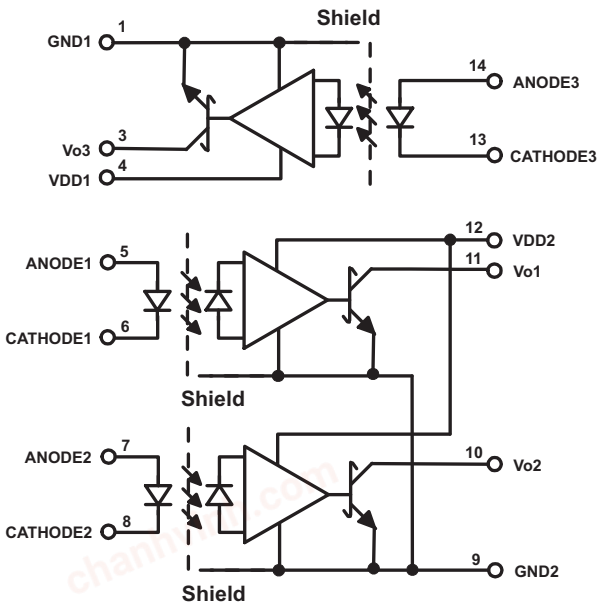


Figure 9: ACSL-6310 – Triple-Ch, Bi-Dir (2/1)



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Schematic Diagrams, continued

Figure 10: ACSL-6400 - Quad-Ch, All-in-One

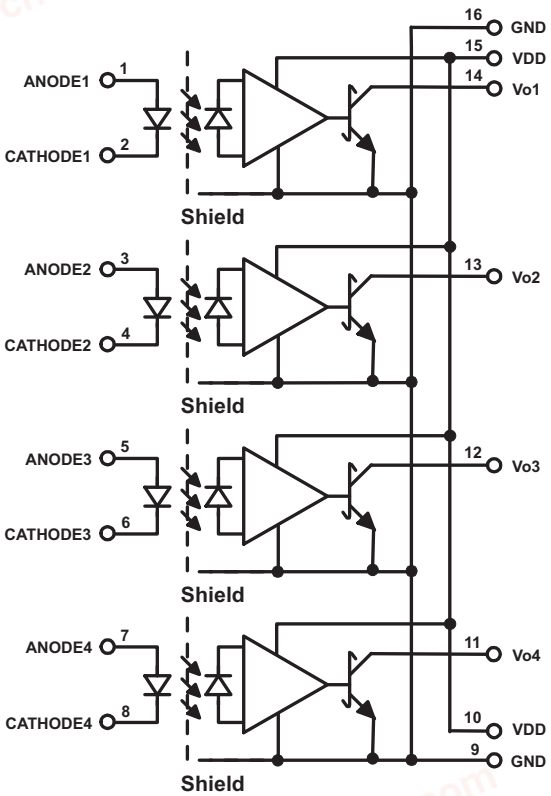
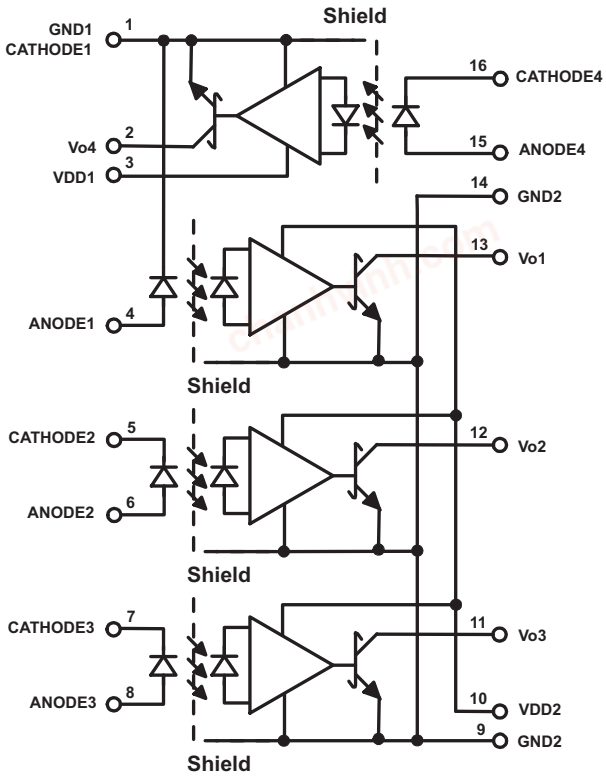


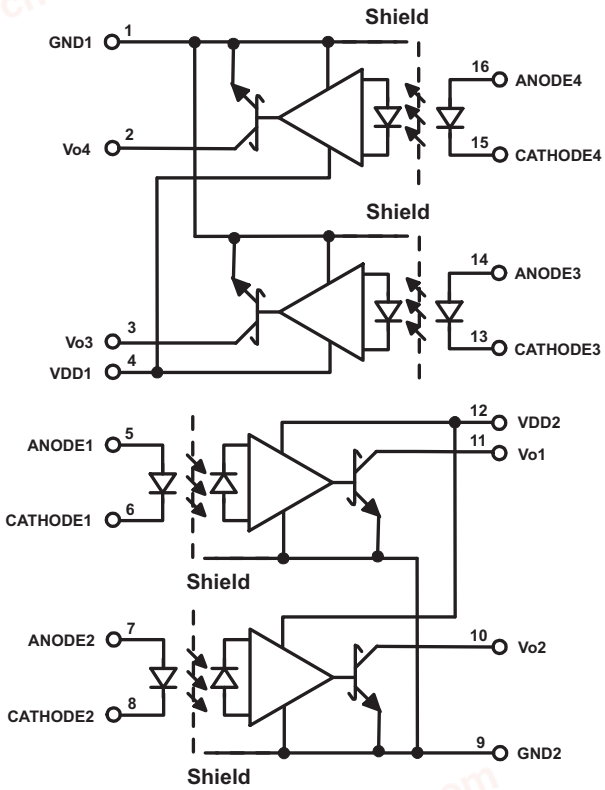
Figure 11: ACSL-6410 - Quad-Ch, Bi-Dir (3/1)



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Schematic Diagrams, continued

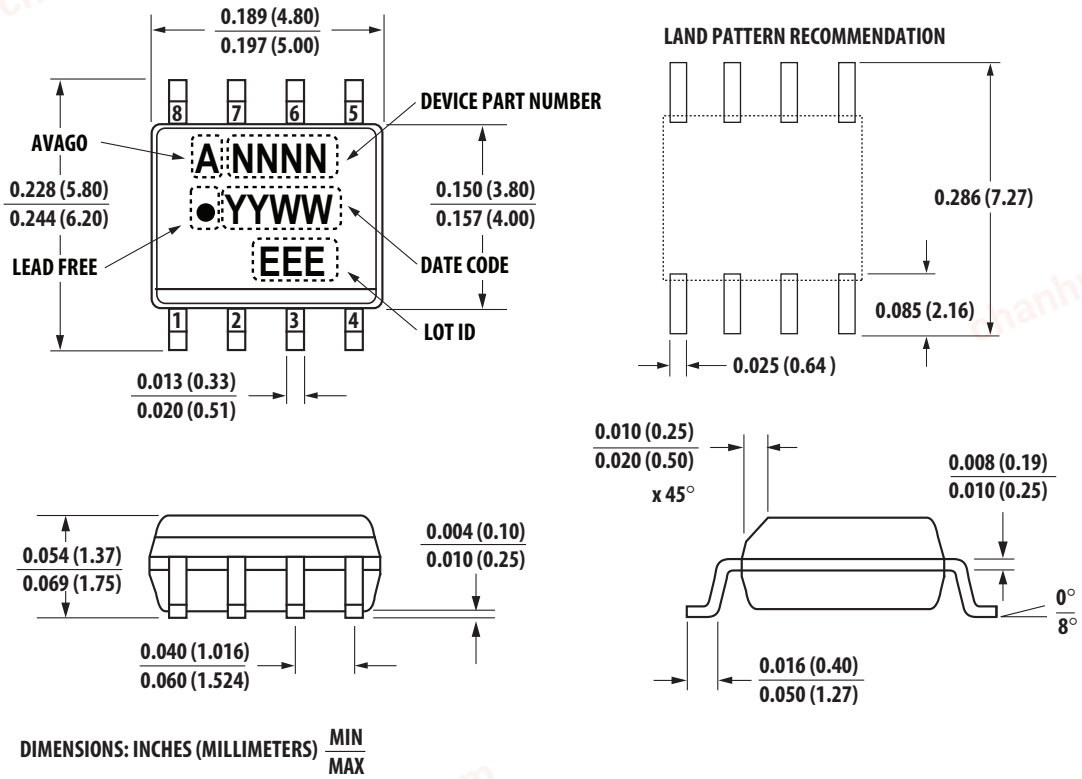
Figure 12: ACSL-6420 - Quad-Ch, Bi-Dir (2/2)



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Package Outline Drawings

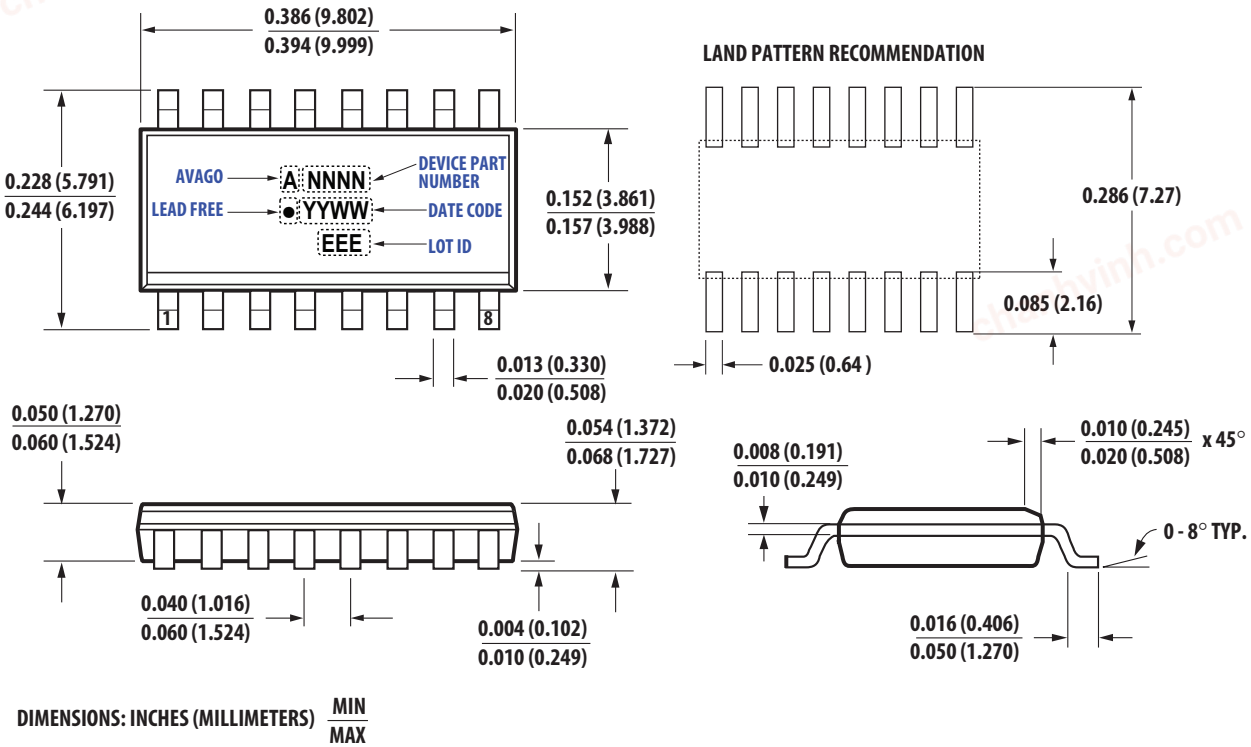
Figure 13: ACSL-6210 Small Outline SO-8 Package



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Package Outline Drawings, continued

Figure 14: ACSL-6300, ACSL-6310, ACSL-6400, ACSL-6410 and ACSL-6420 Small Outline SO-16 Package



Reflow Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Use non-halide flux.

Regulatory Information

Table 1: Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	4.9	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.5	mm	Measured from input terminals to output terminals, shortest distance path through body
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	175	Volts	DIN IEC 112/VDE0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

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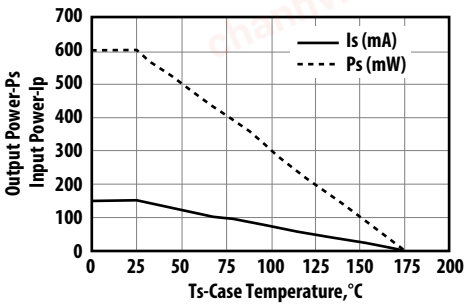
Table 2: IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[a] (Option x6xx)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – III	
Climatic Classification		40/100/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec,ond Partial discharge < 5 pC	V_{PR}	1063	V_{peak}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial discharge < 5 pC	V_{PR}	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 seconds)	V_{IOTM}	4000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current[b]	$I_{S, INPUT}$	150	mA
Output Power[b]	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

b. See Figure 15 for dependence of P_S and I_S on ambient temperature.

Figure 15: P_S and I_S on Ambient Temperature



NOTE: This optocoupler is suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_s	–55	125	°C
Operating Temperature	T_A	–40	100	°C
Supply Voltage (1 Minute Maximum)	V_{DD1}, V_{DD2}	—	7	V
Reverse Input Voltage (Per Channel)	V_R	—	5	V
Output Voltage (Per Channel)	V_O	—	7	V
Average Forward Input Current[a] (Per Channel)	I_F	—	15	mA
Output Current (Per Channel)	I_O	—	50	mA
Input Power Dissipation[b] (Per Channel)	P_I	—	27	mW
Output Power Dissipation[b] (Per Channel)	P_O	—	65	mW

a. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed its maximum values.

b. Derate total package power dissipation, P_T linearly above +95°C free-air temperature at a rate of 1.57 mW/°C for the SO8 package mounted on low conductivity board per JESD 51-3. Derate total package power dissipation, P_T linearly above +80°C free-air temperature at a rate of 1.59 mW/°C for the SO16 package mounted on low conductivity board per JESD 51-3. P_T = number of channels multiplied by (P_I + P_O).

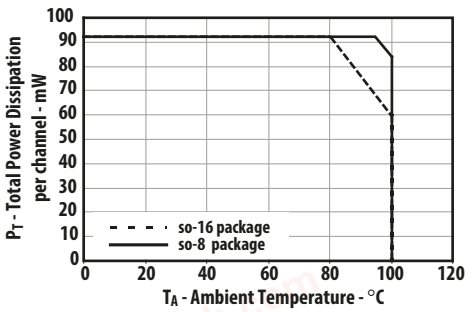
Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating Temperature	T_A	–40	100	°C
Input Current, Low Level[a]	I_{FL}	0	250	µA
Input Current, High Level[b]	I_{FH}	7	15	mA
Supply Voltage	V_{DD1}, V_{DD2}	3.0	5.5	V
Fan Out (at R_L = 1 kΩ)	N	—	5	TTL Loads
Output Pull-up Resistor	R_L	330	4k	Ω

a. The off condition can be guaranteed by ensuring that VFL ≤ 0.8V.

b. The initial switching threshold is 7 mA or less. It is recommended that minimum 8 mA be used for best performance and to permit guardband for LED degradation.

Figure 16: P_I vs. Ambient Temperature



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Electrical Specifications

Over recommended operating range (3.0V ≤ V_{DD1} ≤ 3.6V, 3.0V ≤ V_{DD2} ≤ 3.6V, T_A =–40°C to +100°C) unless otherwise specified. All typical specifications are at T_A = +25°C, V_{DD1} = V_{DD2} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Threshold Current	I_{TH}	—	2.7	7.0	mA	$I_{OL(Sinking)}$ = 13 mA, V_O = 0.6V
High Level Output Current	I_{OH}	—	4.7	100.0	µA	I_F = 250 µA, V_O = 3.3V
Low Level Output Voltage	V_{OL}	—	0.36	0.68	V	$I_{OL(Sinking)}$ = 13 mA, I_F = 7mA
High Level Supply Current (per channel)	I_{DDH}	—	3.2	5.0	mA	I_F = 0 mA
Low Level Supply Current (per channel)	I_{DDL}	—	4.6	7.5	mA	I_F = 10 mA
Input Forward Voltage	V_F	1.25	1.52	1.80	V	I_F = 10 mA, T_A = 25°C
Input Reverse Breakdown Voltage	BV_R	5.0	—	—	V	I_R = 10 µA
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	–1.8	—	mV/°C	I_F = 10 mA
Input Capacitance	C_{IN}	—	80	—	pF	f = 1 MHz, V_F = 0V

Switching Specifications

Over recommended operating range (3.0V ≤ V_{DD1} ≤ 3.6V, 3.0V ≤ V_{DD2} ≤ 3.6V, I_F = 8.0mA, T_A = –40°C to +100°C) unless otherwise specified. All typical specifications are at T_A = +25°C, V_{DD1} = V_{DD2} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Maximum Data Rate		10	15	—	MBd	R_L = 350Ω, C_L = 15 pF
Pulse Width	t_{PW}	100	—		ns	R_L = 350Ω, C_L = 15 pF
Propagation Delay Time to Logic High Output Level[a]	t_{PLH}	—	52	100	ns	R_L = 350Ω, C_L = 15 pF
Propagation Delay Time to Logic Low Output Level[b]	t_{PHL}	—	44	100	ns	R_L = 350Ω, C_L = 15 pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	|PWD|	—	8	35	ns	R_L = 350Ω, C_L = 15 pF
Propagation Delay Skew[c]	t_{PSK}	—	—	40	ns	R_L = 350Ω, C_L = 15 pF
Output Rise Time (10–90%)	t_R	—	35	—	ns	R_L = 350Ω, C_L = 15 pF
Output Fall Time (10–90%)	t_F	—	12	—	ns	R_L = 350Ω, C_L = 15 pF
Logic High Common Mode Transient Immunity[d]	$\lvert CM_H \rvert$	10	—	—	kV/µs	V_{cm} = 1000V, I_F = 0 mA, V_O = 2.0V, R_L = 350Ω, T_A = 25°C
Logic Low Common Mode Transient Immunity[d]	$\lvert CM_L \rvert$	10	—	—	kV/µs	V_{cm} = 1000V, I_F = 8 mA, V_O = 0.8V, R_L = 350Ω, T_A = 25°C

a. t_{PLH} is measured from the 4.0 mA level on the falling edge of the input pulse to the 1.5V level on the rising edge of the output pulse.

b. t_{PHL} is measured from the 4.0 mA level on the rising edge of the input pulse to the 1.5V level on the falling edge of the output pulse.

c. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.

d. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining V_O > 2.0V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining V_O < 0.8V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges

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Electrical Specifications

Over recommended operating range (4.5V ≤ V_{DD1} ≤ 5.5V, 4.5V ≤ V_{DD2} ≤ 5.5V, T_A = –40°C to +100°C) unless otherwise specified. All typical specifications are at T_A = +25°C, V_{DD1} = V_{DD2} = +5.0V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Threshold Current	I_{TH}	—	2.7	7.0	mA	$I_{OL(Sinking)}$ = 13 mA, VO = 0.6V
High Level Output Current	I_{OH}	—	3.8	100.0	µA	I_F = 250 µA, V_O= 5.5V
Low Level Output Voltage	V_{OL}	—	0.36	0.6	V	$I_{OL(Sinking)}$ = 13 mA, I_F = 7 mA
High Level Supply Current (per channel)	I_{DDH}	—	4.3	7.5	mA	I_F = 0 mA
Low Level Supply Current (per channel)	I_{DDL}	—	5.8	10.5	mA	I_F = 10 mA
Input Forward Voltage	V_F	1.25	1.52	1.8	V	I_F = 10 mA, T_A = 25°C
Input Reverse Breakdown Voltage	BV_R	5.0	—	—	V	I_R = 10 µA
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	–1.8	—	mV/°C	I_F = 10 mA
Input Capacitance	C_{IN}	—	80	—	pF	f = 1 MHz, V_F = 0V

Switching Specifications

Over recommended operating range (4.5V ≤ V_{DD1} ≤ 5.5V, 4.5V ≤ V_{DD2} ≤ 5.5V, IF = 8.0 mA, TA = –40°C to +100°C) unless otherwise specified. All typical specifications are at T_A = +25°C, V_{DD1} = V_{DD2} = +5.0V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Maximum Data Rate		10	15	—	MBd	R_L = 350Ω, C_L =15 pF
Pulse Width	t_{PW}	100	—	—	ns	R_L = 350Ω, C_L =15 pF
Propagation Delay Time to Logic High Output Level[a]	t_{PLH}	—	46	100	ns	R_L = 350Ω, C_L =15 pF
Propagation Delay Time to Logic Low Output Level[b]	t_{PHL}	—	43	100	ns	R_L = 350Ω, C_L =15 pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH}\rvert$	|PWD|	—	5	35	ns	R_L = 350Ω, C_L =15 pF
Propagation Delay Skew[c]	t_{PSK}	—	—	40	ns	R_L = 350Ω, C_L =15 pF
Output Rise Time (10–90%)	t_R	—	30	—	ns	R_L = 350Ω, C_L =15 pF
Output Fall Time (10–90%)	t_F	—	12	—	ns	R_L = 350Ω, C_L =15 pF
Logic High Common Mode Transient Immunity[d]	$\lvert CM_H\rvert$	10	—	—	kV/µs	V_{cm} = 1000V, I_F = 0 mA, V_O = 2.0V, R_L = 350Ω, T_A = 25°C
Logic Low Common Mode Transient Immunity[d]	$\lvert CM_L\rvert$	10	—	—	kV/µs	V_{cm} = 1000V, I_F = 8 mA, V_O = 0.8V, R_L = 350Ω, T_A = 25°C

a. t_{PLH} is measured from the 4.0 mA level on the falling edge of the input pulse to the 1.5V level on the rising edge of the output pulse.

b. t_{PHL} is measured from the 4.0 mA level on the rising edge of the input pulse to the 1.5V level on the falling edge of the output pulse.

c. t_{PSK} is equal to the worst case difference in tPHL and/or tPLH that will be seen between units at any given temperature and specified test conditions.

d. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining V_O > 2.0V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining V_O < 0.8V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

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Package Characteristics

All specifications are at T_A = +25°C.

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage[a]	SO8	V_{ISO}	2500	—	—	V_{RMS}	RH 50%, t = 1 min.
	SO16	V_{ISO}	2500	—	—		RH 50%, t = 1 min.
Input-Output Resistance[b]	SO8	R_{I-O}	10^9	10^{11}	—	Ω	V_{I-O} = 500V DC
	SO16	R_{I-O}	10^9	10^{11}	—		V_{I-O} = 500V DC
Input-Output Capacitance[b]	SO8	C_{I-O}	—	0.7	—	pF	f = 1 MHz
	SO16	C_{I-O}	—	0.7	—		f = 1 MHz
Input-Input Insulation Leakage Current[c]	SO8	I_{I-I}	—	0.005	—	µA	RH 45%, t = 5s, V_{I-I} = 500V
	SO16	I_{I-I}	—	0.005	—		RH 45%, t = 5s, V_{I-I} = 500V
Input-Input Resistance[c]	SO8	R_{I-I}	—	10^{11}	—	Ω	RH 45%, t = 5s, V_{I-I} = 500V
	SO16	R_{I-I}	—	10^{11}	—		RH 45%, t = 5s, V_{I-I} = 500V
Input-Input Capacitance[[c]	SO8	C_{I-I}	—	0.1	—	pF	f = 1 MHz
	SO16	C_{I-I}	—	0.12	—		f = 1 MHz

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

b. Measured between each input pair shorted together and all output connections for that channel shorted together.

c. Measured between inputs with the LED anode and cathode shorted together.

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Typical Performance

Figure 17: Typical Input Threshold Current vs. Temperature for 3.3V Operation

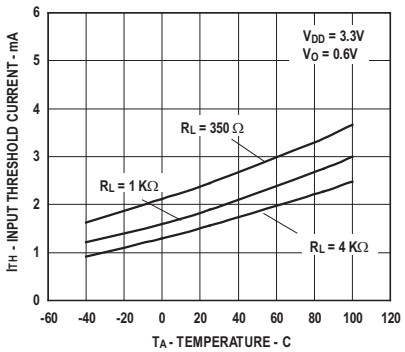


Figure 18: Typical Input threshold Current vs. Temperature for 5V Operation

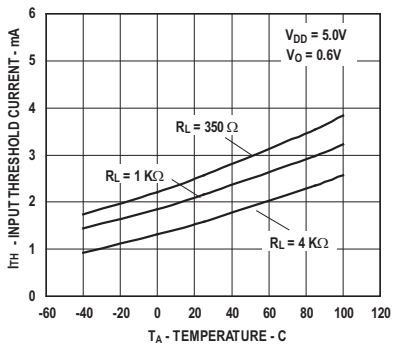


Figure 19: Typical Low Level Output Current vs. Temperature for 3.3V Operation

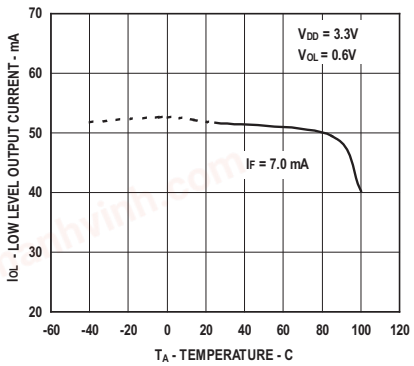


Figure 20: Typical Low Level Output Current vs. Temperature for 5V Operation

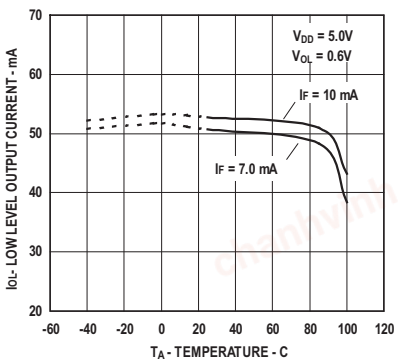


Figure 21: Typical High Level Output Current vs. Temperature for 3.3V Operation

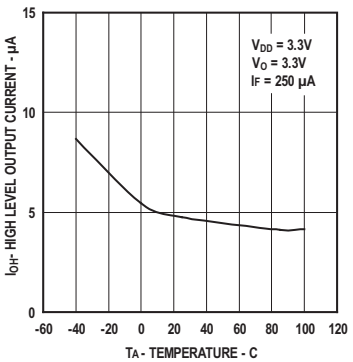


Figure 22: Typical High Level Output Current vs. Temperature for 5V Operation

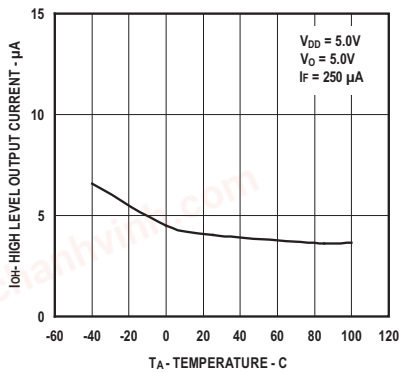


Figure 23: Typical Low Level Output Voltage vs. Temperature for 3.3V Operation

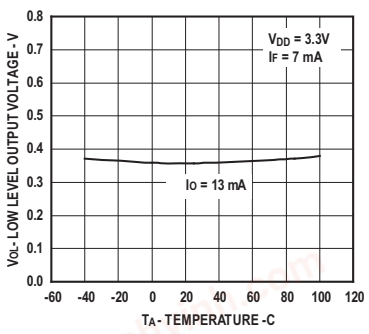


Figure 24: Typical Low Level Output Voltage vs. Temperature for 5V Operation

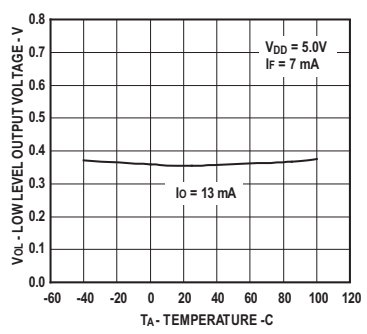
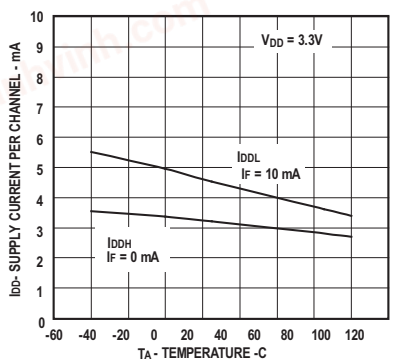


Figure 25: Typical Supply Current per Channel vs. Temperature for 3.3V Operation



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Typical Performance, continued

Figure 26: Typical Supply Current per Channel vs. Temperature for 5V Operation

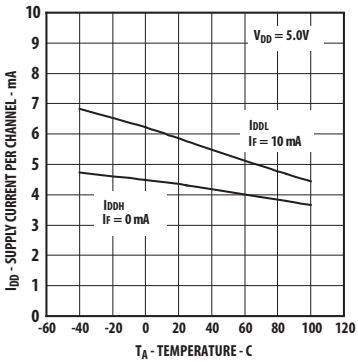


Figure 27: Typical Input Diode Forward Characteristics

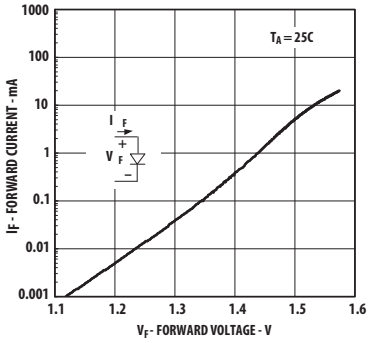


Figure 28: Typical Propagation Delay vs. Temperature for 3.3V Operation

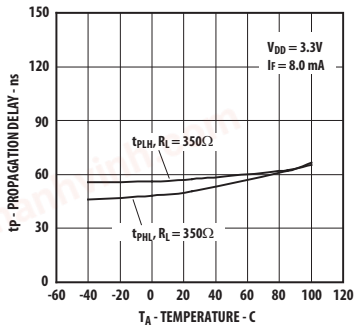


Figure 29: Typical Propagation Delay vs. Temperature for 5V Operation

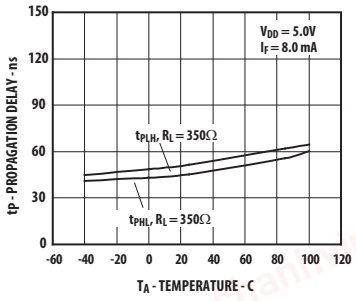


Figure 30: Typical Pulse Width Distortion vs. Temperature for 3.3V Operation

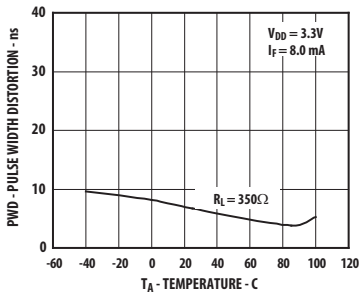
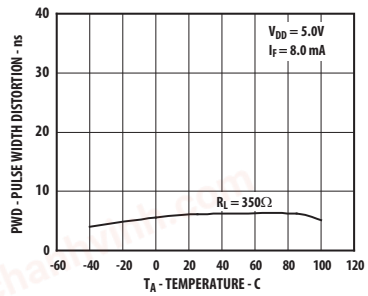


Figure 31: Typical Pulse Width Distortion vs. Temperature for 5V Operation



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Test Circuits

Figure 32: Test Circuit for t_{PHL}. t_{PLH}, t_F, and t_R

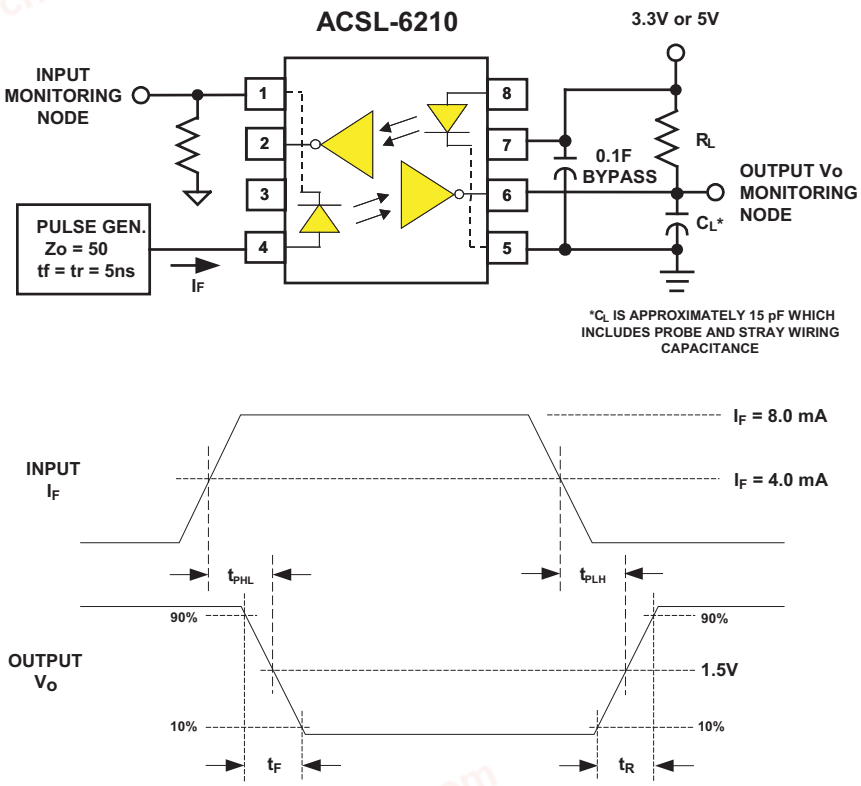
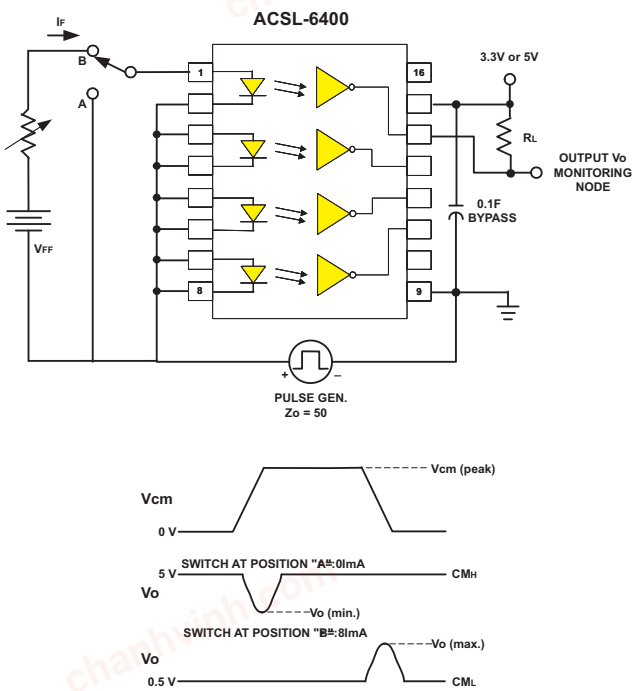


Figure 33: Test Circuit for Common Mode Transient Immunity and Typical Waveforms



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Application Information

ON and OFF Conditions

The ACSL-6xx0 series has the ON condition defined by current, and the OFF condition defined by voltage. To guarantee that the optocoupler is OFF, the forward voltage across the LED must be less than or equal to 0.8V for the entire operating temperature range. This has direct implications for the input drive circuit. If the design uses a TTL gate to drive the input LED, then one has to ensure that the gate output voltage is sufficient to cause the forward voltage to be less than 0.8V. The typical threshold current for the ACSL6xx0 series optocouplers is 2.7 mA; however, this threshold could increase over time due to the aging effects of the LED. Drive circuit arrangements must provide for the ON state LED forward current of at least 7 mA, or more if faster operation is desired.

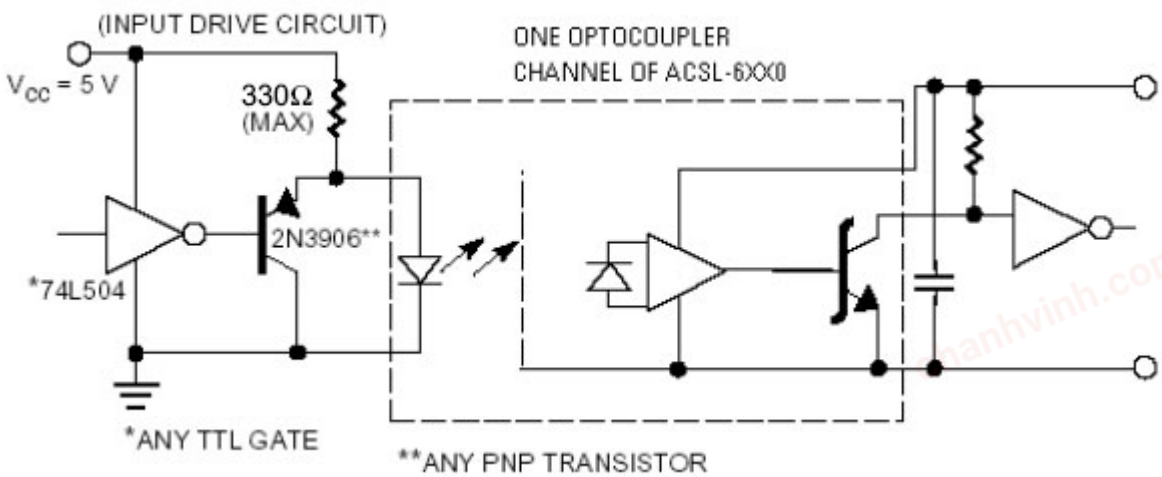
Maximum Input Current and Reverse Voltage

The average forward input current should not exceed the 15-mA Absolute Maximum Rating as stated; however, peaking circuits with transient input currents up to 50 mA are allowed provided the average current does not exceed 15 mA. If the input current maximum rating is exceeded, the local temperature of the LED can rise, which in turn may affect the long-term reliability of the device. When designing the input circuit, one must also ensure that the input reverse voltage does not exceed 5V. If the optocoupler is subjected to reverse voltage transients or accidental situations that may cause a reverse voltage to be applied, thus an anti-parallel diode across the LED is recommended.

Suggested Input Circuits for Driving the LED

Figure 34, Figure 35, and Figure 36 show some of the several techniques for driving the ACSL-6xx0 LED. Figure 34 shows the recommended circuit when using any type of TTL gate. The buffer PNP transistor allows the circuit to be used with TTL or CMOS gates that have low sinking current capability. One advantage of this circuit is that there is very little variation in power supply current due to the switching of the optocoupler LED. This can be important in high-resolution analog-to-digital (A/D) systems where ground loop currents due to the switching of the LEDs can cause distortion in the A/D output.

Figure 34: TTL Interface Circuit for the ACSL-6xx0



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With a CMOS gate to drive the optocoupler, the circuit shown in Figure 35 can be used. The diode in parallel to the current limiting resistor speeds the turn-off of the optocoupler LED. Any HC or HCT series CMOS gate can be used in this circuit.

For high common-mode rejection applications, the drive circuit shown in Figure 36 is recommended. In this circuit, only an open-collector TTL, or an open drain CMOS gate can be used. This circuit drives the optocoupler LED with a 220Ω current-limiting resistor to ensure that an I_F of 7 mA is applied under worst case conditions and thus guarantee the 10,000 V/µs optocoupler common mode rejection rating. The designer can obtain even higher common-mode rejection performance than 10,000 V/µs by driving the LED harder than 7mA.

Phase Relationship to Input

The output of the optocoupler is inverted when compared to the input. The input is defined to be logic HIGH when the LED is ON. If there is a design that requires the optocoupler to behave as a non-inverting gate, then the series input drive circuit shown in Figure 35 can be used. This input drive circuit has an inverting function, and because the optocoupler also behaves as an inverter, the total circuit is non-inverting. The shunt drive circuits shown in Figure 34 and Figure 36 will cause the optocoupler to function as an inverter.

Figure 35: CMOS Drive Circuit for the ACSL-6xx0

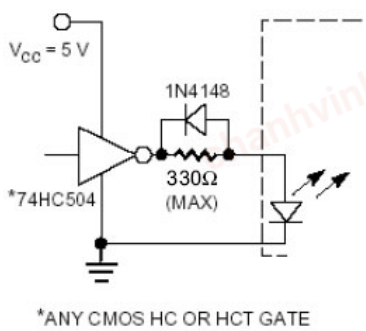
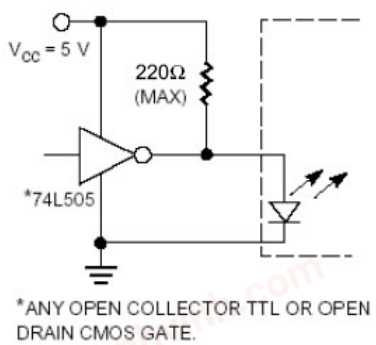


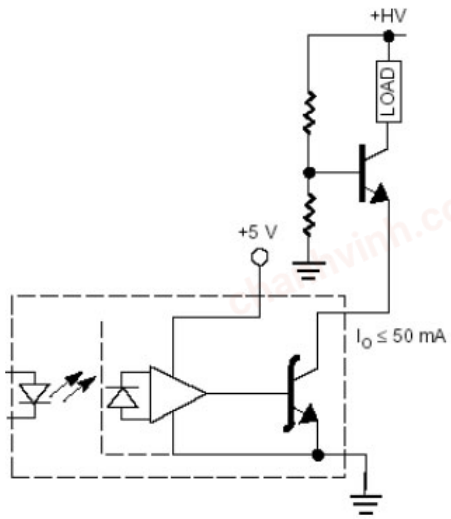
Figure 36: High CMR Drive Circuit for the ACSL-6xx0



Current and Voltage Limitations

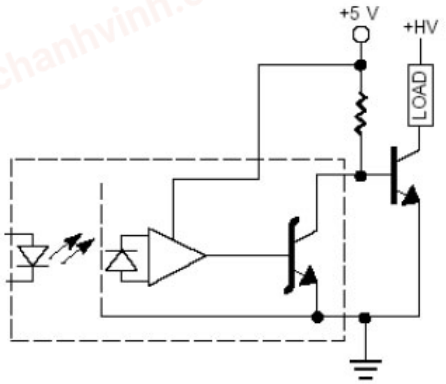
The absolute maximum voltage allowable at the output supply voltage pin and the output voltage pin of the optocoupler is 7V. However, the recommended maximum voltage at these two pins is 5.5V. The output sinking current should not exceed 13 mA to make the Low Level Output Voltage be less than 0.6V. If the output voltage is not a consideration, the absolute maximum current allowed through the ACSL-6xx0 is 50 mA. If the output requires switching either higher currents or voltages, output buffer stages as shown in Figure 37 and Figure 38 are suggested.

Figure 37: High Voltage Switching with ACSL-6xx0



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Figure 38: High Voltage and High Current Switching with ACSL-6xx0



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