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ACPL-W60L/K63L

High Speed LVTTL Compatible 3.3 Volt/5 Volt Optocouplers

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

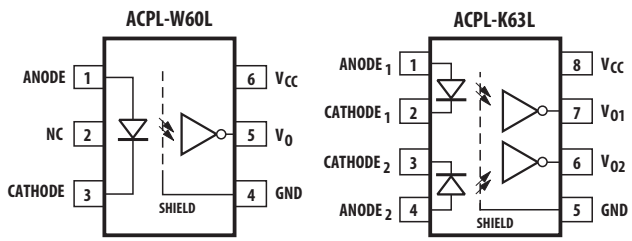
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The ACPL-W60L/K63L are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 15 kV/µs at 3.3V.

This unique design provides maximum AC and DC circuit isolation while achieving LVTTL/LVCMOS compatibility. The optocoupler AC and DC operational parameters are guaranteed from –40˚C to +85˚C allowing trouble-free system performance.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

A 0.1 µF bypass capacitor must be connected between pins 4 and 6 for ACPL-W60L and pins 5 and 8 for ACPL-K63L.

Features

- Dual Voltage Operation (3.3V/5V)
- Package clearance/creepage at 8 mm
- Low power consumption
- 15 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1000V
- High speed: 15 MBd typical
- LVTTL/LVCMOS compatible
- Low input current capability: 5 mA
- Guaranteed AC and DC performance over temperature: –40˚C to +85˚C
- Available in 6-pin stretched SO-6 and 8 pin stretched SO-8
- Safety approvals: UL, CSA, IEC/EN/DIN EN 60747-5-2 – in process

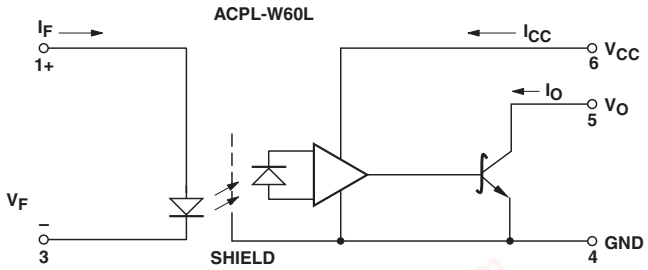
Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Fieldbus

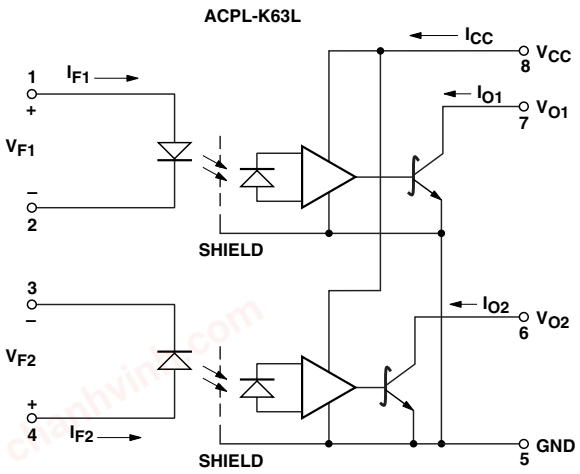
CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

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Schematic Diagrams



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 5).



These optocouplers are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

These optocouplers are available in stretched SO-6 and SO-8 package. The part numbers are as follows:

Part number	Package
ACPL-W60L	Stretched SO-6
ACPL-K63L	Stretched SO-8

Ordering Information

ACPL-xxxx is UL Recognized with 3750 V_{rms} for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option RoHS Compliant	Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 V_{rms}/ 1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-W60L	-000E	Stretched SO-6	X					100 per tube
	-500E		X		X			1000 per reel
	-520E		X		X	X		1000 per reel
	-560E		X		X		X	1000 per reel
ACPL-K63L	-000E	Stretched SO-8	X					80 per tube
	-500E		X		X			1000 per reel
	-520E		X		X	X		1000 per reel
	-560E		X		X		X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry. Combination of Option 020 and Option 060 is not available.

Example 1:

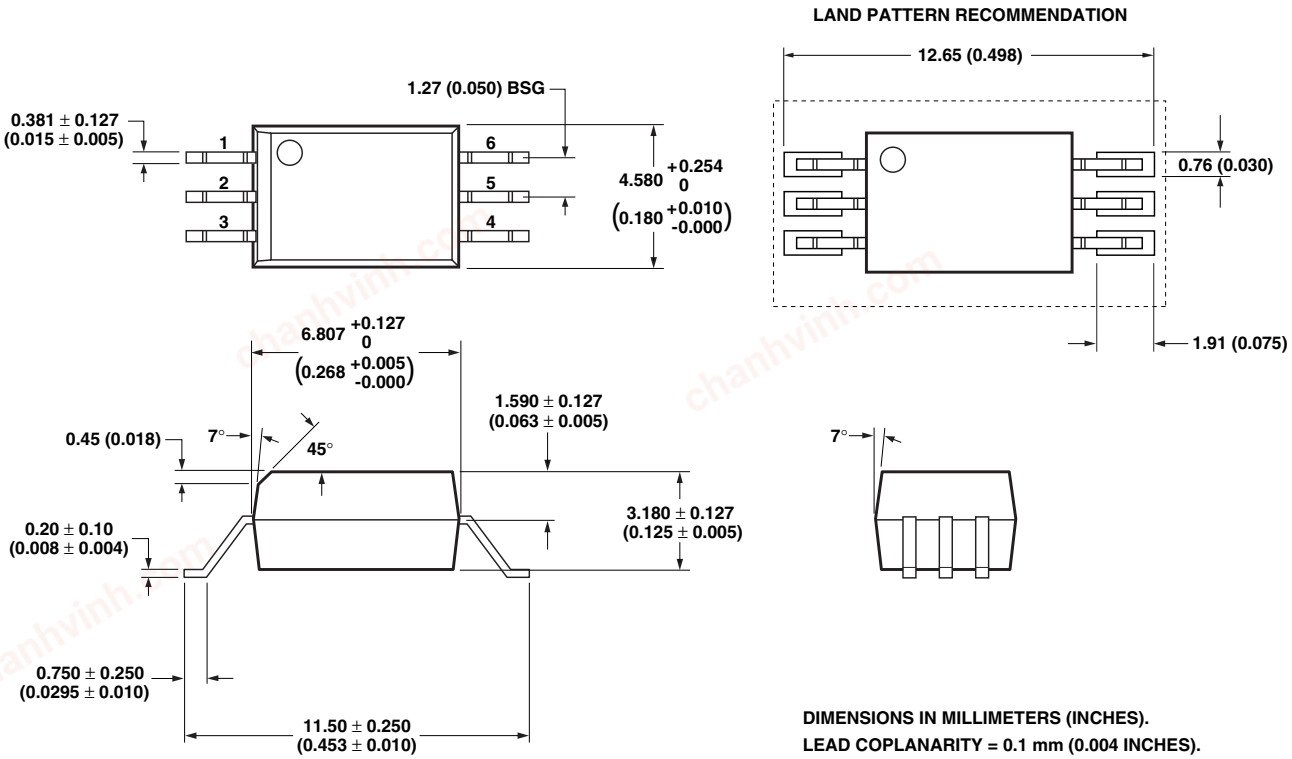
ACPL-W60L-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

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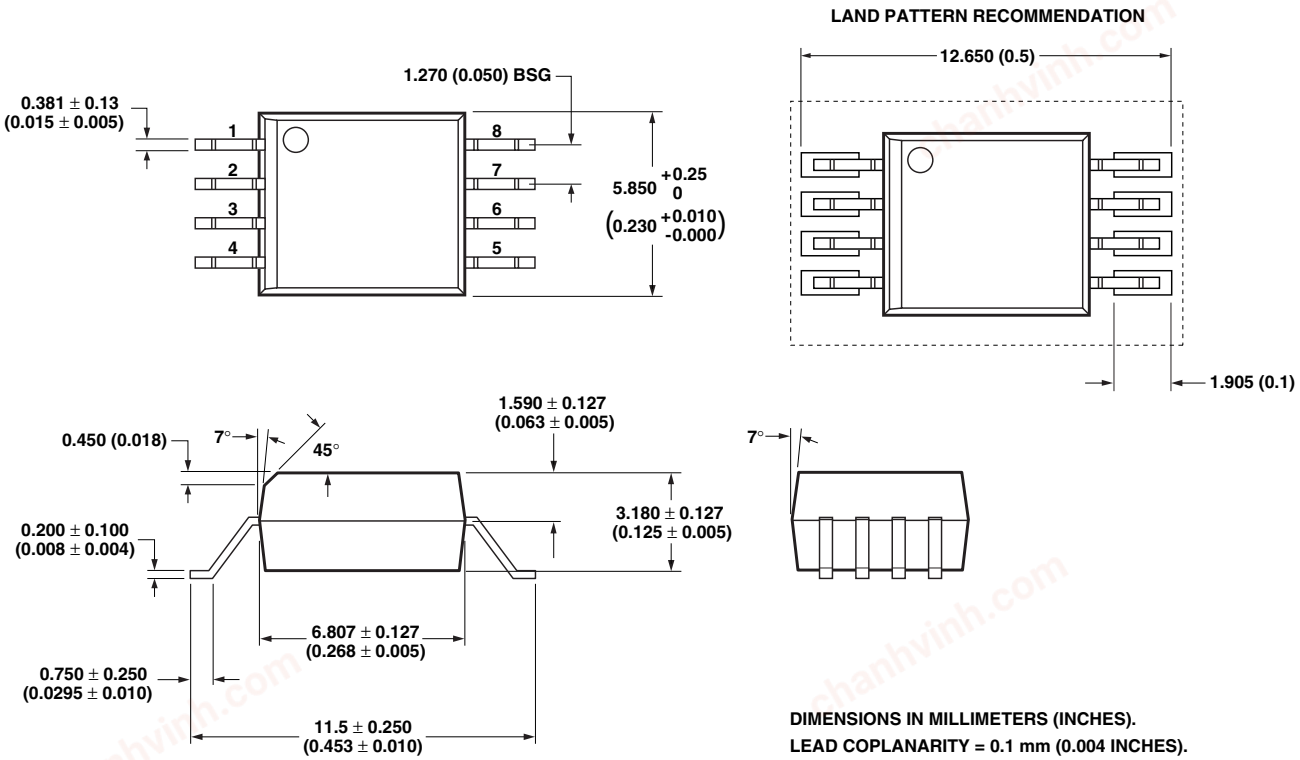
Package Outline Drawings

ACPL-W60L Stretched SO-6 Package



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.1 mm (0.004 INCHES).

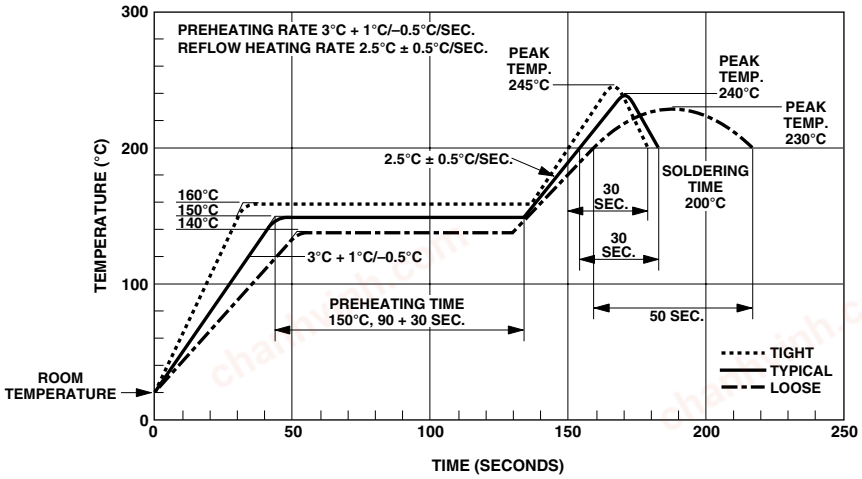
ACPL-K63L Stretched SO-8 Package



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.1 mm (0.004 INCHES).

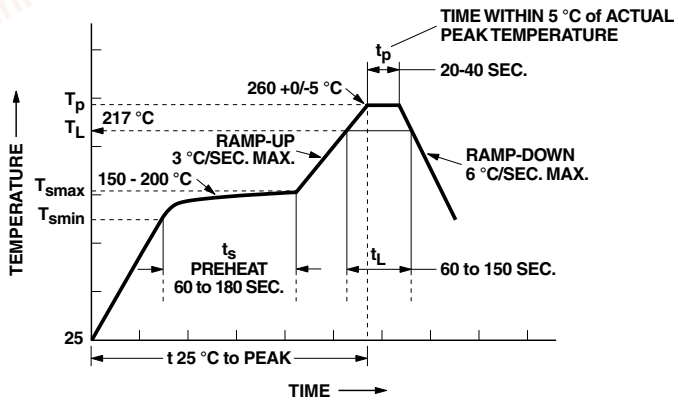
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Recommended Solder Reflow Thermal Profile



Note: Non-halide flux should be used.

Recommended PB-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Regulatory Information

The ACPL-W60L/K63L have been approved by the following organizations:

UL

Approval under UL 1577, Component Recognition Program, File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2

Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884Teil 2):2003-01 Option 060 only)

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Insulation and Safety Related Specifications

Parameter	Symbol	Stretched S0-6 and S0-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L (101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L (102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics

Description	Symbol	Stretched S0-6 & S0-8 Value	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V rms		I-IV	
for rated mains voltage ≤ 300 V rms		I-III	
for rated mains voltage ≤ 450 V rms		I-III	
for rated mains voltage ≤ 600 V rms		I-III	
for rated mains voltage ≤ 1000 V rms		I-II	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	1710	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

Notes:
* Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2, for a detailed description.
1. Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

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Absolute Maximum Ratings (No Derating Required up to 85°C)

Parameter	Symbol	Package**	Min.	Max.	Units	Note
Storage Temperature	T_S		–55	125	°C	
Operating Temperature†	T_A		–40	85	°C	
Average Forward Input Current	I_F	Single Stretched SO-6		20	mA	2
		Dual Stretched SO-8		15		1, 3
Reverse Input Voltage	V_R			5	V	1
Input Power Dissipation	P_I			40	mW	
Supply Voltage (1 Minute Maximum)	V_{CC}			7	V	
Output Collector Current	I_O			50	mA	1
Output Collector Voltage	V_O			7	V	1
Output Power Dissipation	P_O	Single Stretched SO-6		85	mW	
		Dual Stretched SO-8		60		1, 4
Solder Reflow Temperature Profile			See Package Outline Drawings section			

**Ratings apply to all devices except otherwise noted in the Package column.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	µA
Input Current, High Level[1]	I_{FH}**	5	15	mA
Power Supply Voltage	V_{CC}	2.7	3.6	V
		4.5	5.5	V
Operating Temperature	T_A	–40	85	°C
Fan Out (at R_L = 1 kΩ)[1]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.

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Electrical Specifications

Over Recommended Operating Conditions (T_A = –40°C to +85°C , 2.7V ≤ Vcc ≤ 3.6V) unless otherwise specified.
All Typicals at V_{CC} = 3.3 V, T_A = 25˚C.

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*			4.5	50	µA	V_{CC} = 3.3 V, V_O = 3.3 V, I_F = 250 µA	1	1
Input Threshold Current	I_{TH}			3.0	5.0	mA	V_{CC} = 3.3 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2	
Low Level Output Voltage	V_{OL}*			0.35	0.6	V	V_{CC} = 3.3 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	3	
High Level Supply Current	I_{CCH}	Single		4.7	7.0	mA	I_F = 0 mA		
		Dual		6.9	10.0		V_{CC} = 3.3 V		
Low Level Supply Current	I_{CCL}	Single		7.0	10.0	mA	I_F = 10 mA		
		Dual		8.7	15.0		V_{CC} = 3.3 V		
Input Forward Voltage	V_F		1.4	1.5	1.75*	V	T_A = 25˚C, I_F = 10 mA	5	1
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 µA		1
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$			–1.6		mV/˚C	I_F = 10 mA		1
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V		1

Electrical Specifications (DC)

Over recommended operating conditions (T_A=-40°C to +85°C, 4.5V ≤ V_{DD} ≤ 5.5V) unless otherwise specified.
All typicals at V_{CC} = 5 V, TA = 25 °C.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}			5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_{FL} = 250 µA	1	1
Input Threshold Current	I_{TH}			2.0	5.0	mA	V_{CC} = 5.5 V, V_O = 0.6 V, I_{OL} > 13 mA	2	
Low Level Output Voltage	V_{OL}			0.35	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, $I_{OL(Sinking)}$ = 13 mA	3	
High Level Supply Current	I_{CCH}	Single		7.0	10.0	mA	V_{CC} = 5.5 V, I_F = 0 mA		
		Dual		10.0	15.0	mA	V_{CC} = 5.5 V, I_F = 0 mA		
Low Level Supply Current	I_{CCL}	Single		9.0	13.0	mA	V_{CC} = 5.5 V, I_F = 10 mA		
		Dual		13.0	21.0	mA	V_{CC} = 5.5 V, I_F = 10 mA		
Input Forward Voltage	V_F		1.4	1.5	1.75	V	T_A = 25 °C, I_F = 10 mA	5	1
			1.3		1.8				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		1
Input Diode Temperature Coefficient	ΔVF/ΔTA			-1.6		mV/°C	I_F = 10 mA		1
Input Capacitance	CIN			60		pF	f = 1 MHz, V_F = 0 V		1

*All Typical at TA=25C, Vcc=5V

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Switching Specifications

Over Recommended Temperature (T_A = –40°C to +85°C), V_{CC} = 3.3 V, I_F = 7.5 mA unless otherwise specified.
All Typicals at T_A = 25°C, V_{CC} = 3.3 V.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}			90	ns	R_L = 350 Ω C_L = 15 pF	6, 7, 8	1, 6
Propagation Delay Time to Low Output Level	t_{PHL}			75	ns			1, 7
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$			25	ns		8	9
Propagation Delay Skew	t_{PSK}			40	ns			8, 9
Output Rise Time (10-90%)	t_r		45		ns			1
Output Fall Time (90-10%)	t_f		20		ns			1

Switching Specifications (AC)

Over recommended operating conditions T_A = -40°C to 85°C, V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified.
All typicals at V_{CC} = 5 V, T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	20	48	75	ns	T_A = 25°C, R_L = 350Ω, C_L = 15 pF	6,7,8	1,6
				100	ns	R_L = 350Ω, C_L = 15 pF		
Propagation Delay Time to Low Output Level	t_{PHL}	25	50	75	ns	T_A = 25°C R_L = 350Ω, C_L = 15 pF		1,7
				100	ns	R_L = 350Ω, C_L = 15 pF		
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$		3.5	35	ns	R_L = 350 Ω, C_L = 15 pF	8	9
Propagation Delay Skew	t_{psk}			40	ns	R_L = 350Ω, C_L = 15 pF		8,9
Output Rise Time (10%-90%)	t_r		24		ns	R_L = 350Ω, C_L = 15 pF		1
Output Fall Time (10%-90%)	t_f		10		ns	R_L = 350Ω, C_L = 15 pF		1

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Parameter	Sym.	Device	Min.	Typ.	Units	Test Conditions	Fig.	Note
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	ACPL-W60L ACPL-K63L	15	25	kV/µs	V_{CC} = 3.3 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C, V_{CM} = 1000 V and V_{CM} = 10 V	9	10, 12
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	ACPL-W60L ACPL-K63L	15	25	kV/µs	V_{CC} = 3.3 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C, V_{CM} = 1000 V and V_{CM} = 10 V	9	10, 12
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	ACPL-W60L ACPL-K63L	10	15	kV/µs	V_{CC} = 5 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C, V_{CM} = 1000 V	9	10, 12
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	ACPL-W60L ACPL-K63L	10	15	kV/µs	V_{CC} = 5 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C, V_{CM} = 1000 V	9	11, 12

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Package Characteristics

All Typicals at T_A = 25°C.

Parameter	Sym.	Package	Min.	Typ.	Max	Units	Test Conditions	Fig.	Note
Input-Output Insulation	I_{I-O}*	Single			1	μA	45% RH, t = 5 s, V_{I-O} = 3 kV DC, T_A = 25°C		13, 14
Input-Output Momentary Withstand Voltage*	V_{ISO}	Single, Dual Channel	3750			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		13, 14
Input-Output Resistance	R_{I-O}	Single, Dual Channel		10^{12}		Ω	V_{I-O} =500 V dc		1, 13, 15
Input-Output Capacitance	C_{I-O}	Single, Dual Channel		0.5		pF	f = 1 MHz, T_A = 25°C		1, 13, 15
Input-Input Insulation Leakage Current	I_{I-I}	Dual Channel		0.005		μA	RH ≤ 45%, t = 5 s, V_{I-I} = 500 V		16
Resistance (Input-Input)	R_{I-I}	Dual Channel		10^{11}		Ω			16
Capacitance (Input-Input)	C_{I-I}	Dual Channel		0.25		pG	f = 1 MHz		16

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Each channel.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
4. Derate linearly above +80°C free-air temperature at a rate of 2.7 mW/°C.
5. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 11. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
6. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
8. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
9. See test circuit for measurement details.
10. CM_H is the maximum tolerable rate of rise on the common mode voltage to assure that the output will remain in a high logic state (i.e., V_o > 2.0 V).
11. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_o < 0.8 V).
12. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM}$ (p-p).
13. Single channel device is considered a two-terminal part when pins 1, 2, 3 are shorted together, and pins 4, 5, 6 shorted together separately. Dual channel device is considered a two-terminal part when pins 1, 2, 3, 4 are shorted together, and pins 5, 6, 7, 8 are shorted together separately.
14. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V rms for one second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
15. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together. For dual channel products only.
16. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual channel products only.

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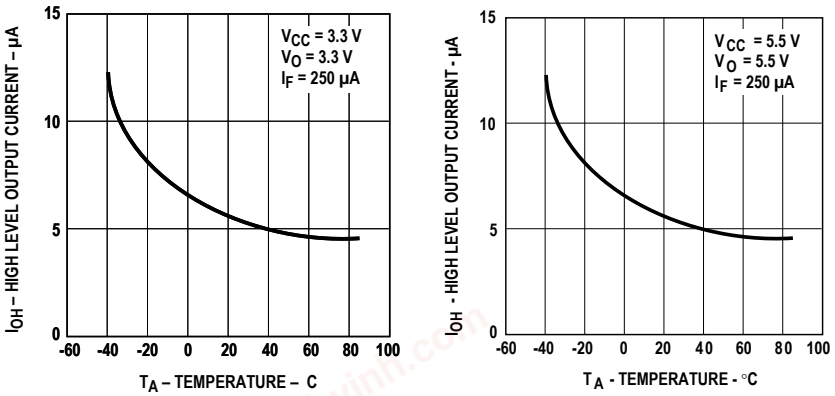


Figure 1. Typical high level output current vs. temperature.

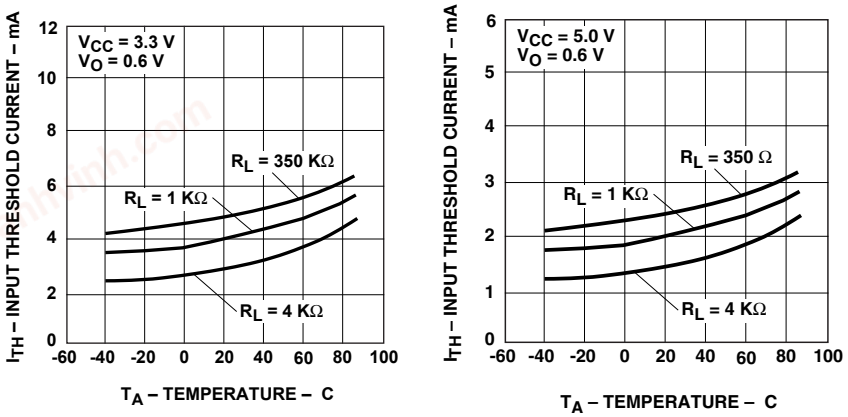


Figure 2. Typical input threshold current vs. temperature.

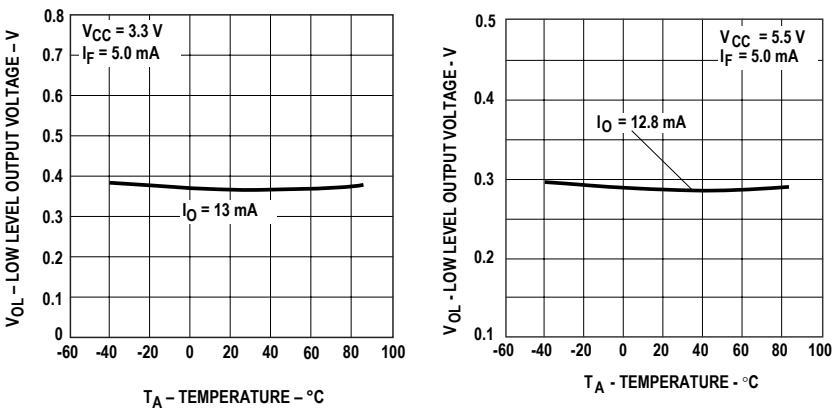
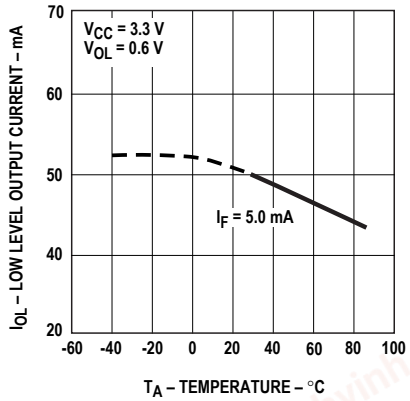


Figure 3. Typical low level output voltage vs. temperature.

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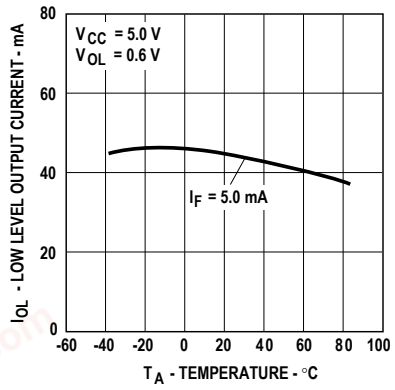


Figure 4. Typical low level output current vs. temperature.

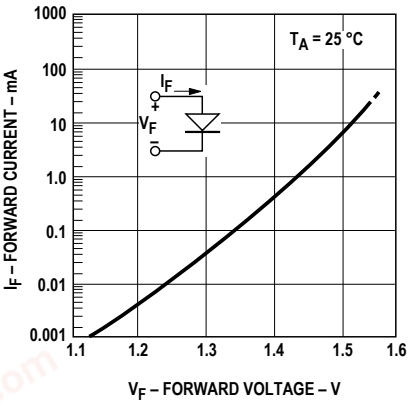


Figure 5. Typical input diode forward characteristic.

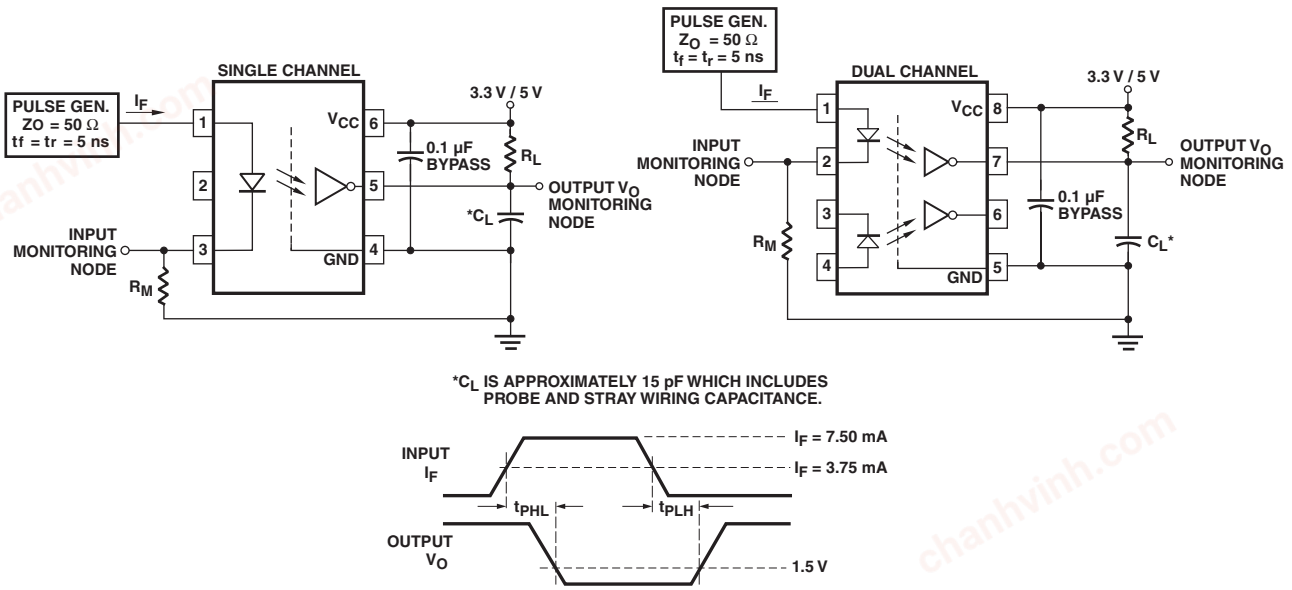


Figure 6. Test circuit for t_{PHL} and t_{PLH}.

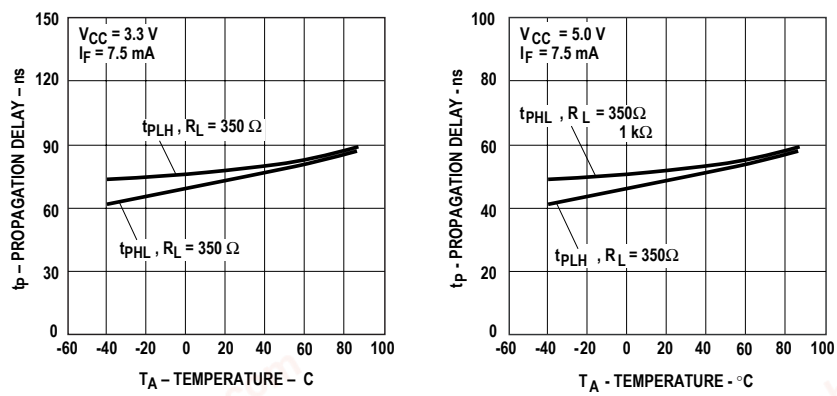


Figure7. Typical propagation delay vs. temperature.

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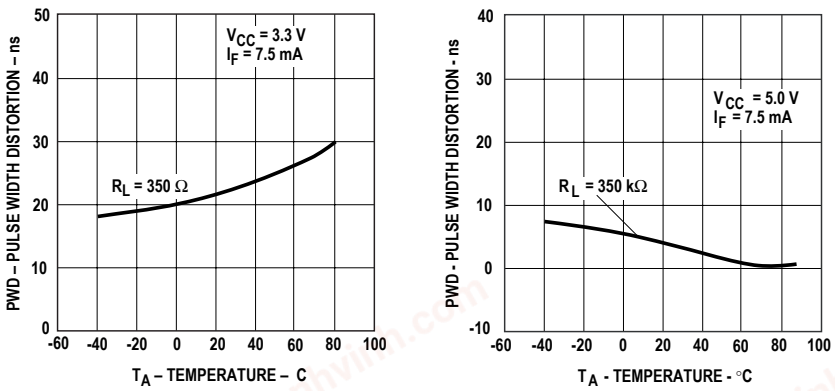


Figure 8. Typical pulse width distortion vs. temperature.

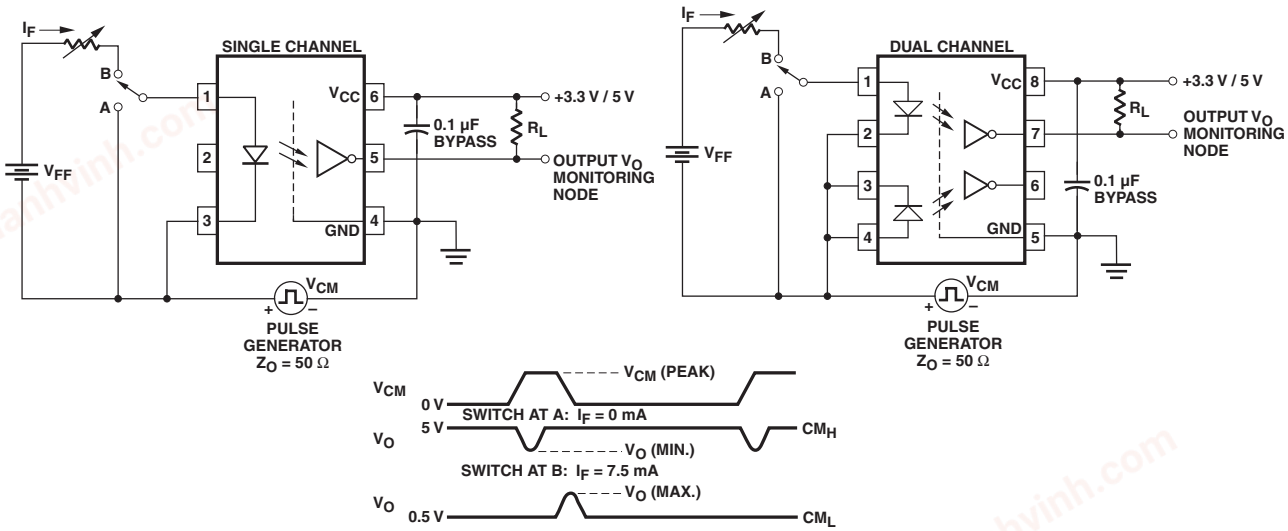


Figure 9. Test circuit for common mode transient immunity and typical waveforms.

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