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ACPL-P454 and ACPL-W454
High CMR High Speed Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

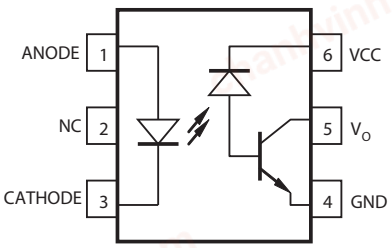
Description

The ACPL-W454/P454 is similar to Avago Technologies other high speed transistor output optocouplers, but with shorter propagation delays and higher CTR. The ACPL-W454/P454 also has a guaranteed propagation delay difference (t_{PLH} - t_{PHL}). These features make the ACPL-W454/P454 an excellent solution to IPM inverter dead time and other switching problems.

The ACPL-W454/P454 CTR, propagation delays, and CMR are specified both for TTL load and drive conditions and for IPM (Intelligent Power Module) load and drive conditions. Specifications and typical performance plots for both TTL and IPM conditions are provided for ease of application.

This diode-transistor optocoupler uses an insulating layer between the light emitting diode and an integrated photo detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional phototransistor coupler by reducing the base-collector capacitance.

Functional Diagram

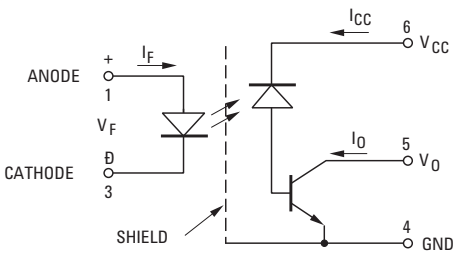


TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

A 0.1 µF bypass capacitor between pins 4 and 6 is recommended.

Schematic



Features

- Package Clearance/Creepage at 8mm (ACPL-W454)
- Function Compatible with HCPL-4504
- Surface Mountable in 6-pin stretched SO6
- Short Propagation Delays for TTL and IPM Applications
- Very High Common Mode Transient Immunity: Guaranteed 15 kV/µs at V_{CM} = 1500 V
- High CTR: >25% at 25°C
- Guaranteed Specifications for Common IPM Applications
- TTL Compatible
- Guaranteed AC and DC Performance Over Temperature: 0°C to 70°C
- Open Collector Output
- Safety approval
  UL Recognized 3750 Vrms for 1 minute (5000 Vrms for 1 minute under ACPL-W454 devices) per UL1577
  CSA Approved
  IEC/EN/DIN EN 60747-5-2 Approved with V_{IORM} = 1140 Vpeak (ACPL-W454) and V_{IORM} = 891 Vpeak (ACPL-P454) for Option 060.

Applications

- Inverter Circuits and Intelligent Power Module (IPM) Interfacing – Shorter propagation delays and guaranteed (t_{PLH} - t_{PHL}) specifications.
- High Speed Logic Ground Isolation
  - TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL
- Line Receivers
  - High common mode transient immunity (>15 kV/µs for a TTL load/drive) and low input-output capacitance (0.6 pF).
- Replace Pulse Transformers
  - Save board space and weight
- Analog Signal Ground Isolation
  - Integrated photo detector provides improved linearity over phototransistors

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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Ordering Information

ACPL-P454 and ACPL-W454 are UL Recognized with 3750 Vrms (5000 Vrms under ACPL-W454) for 1 minute per UL1577 and are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-P454 ACPL-W454	-000E	Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P454-560E to order product of Stretched SO-6 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

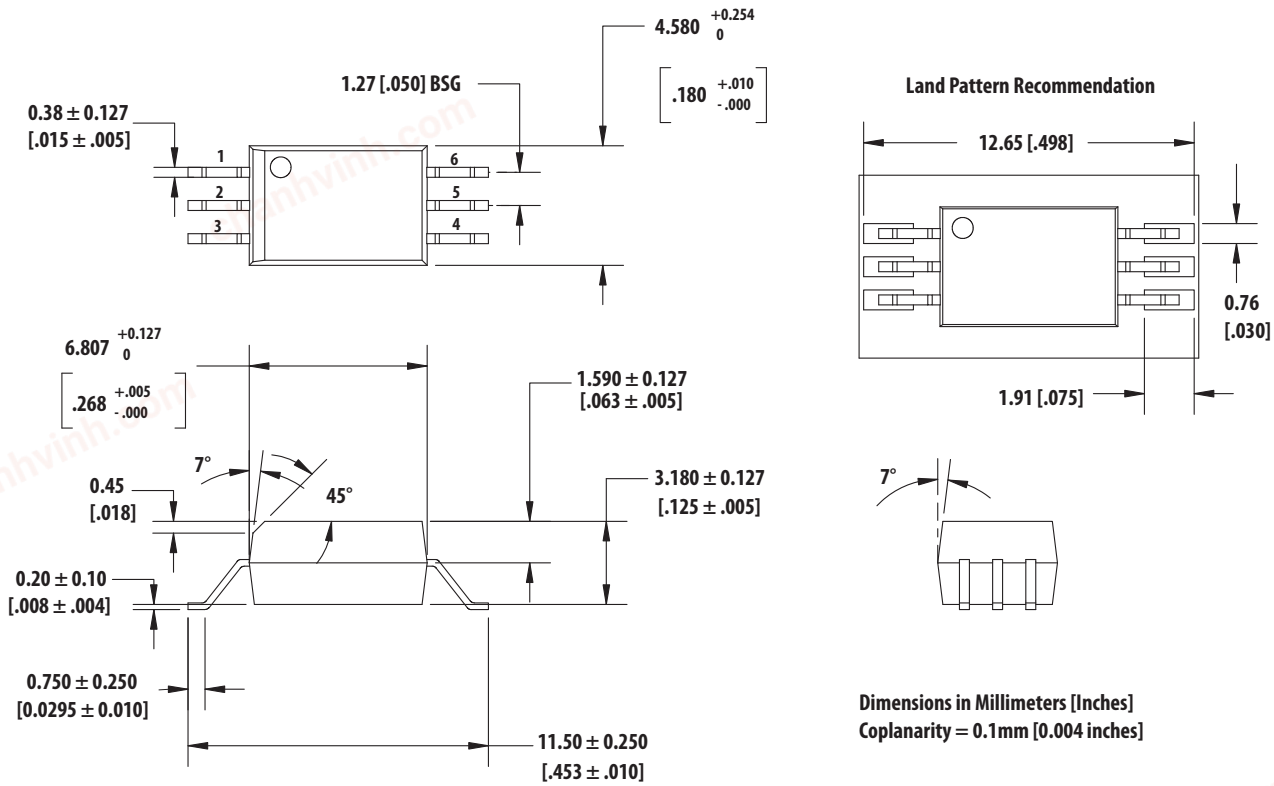
Example 2:

ACPL-P454-000E to order product of Stretched SO-6 package in tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-W454 (Stretched SO6, 8mm Clearance)



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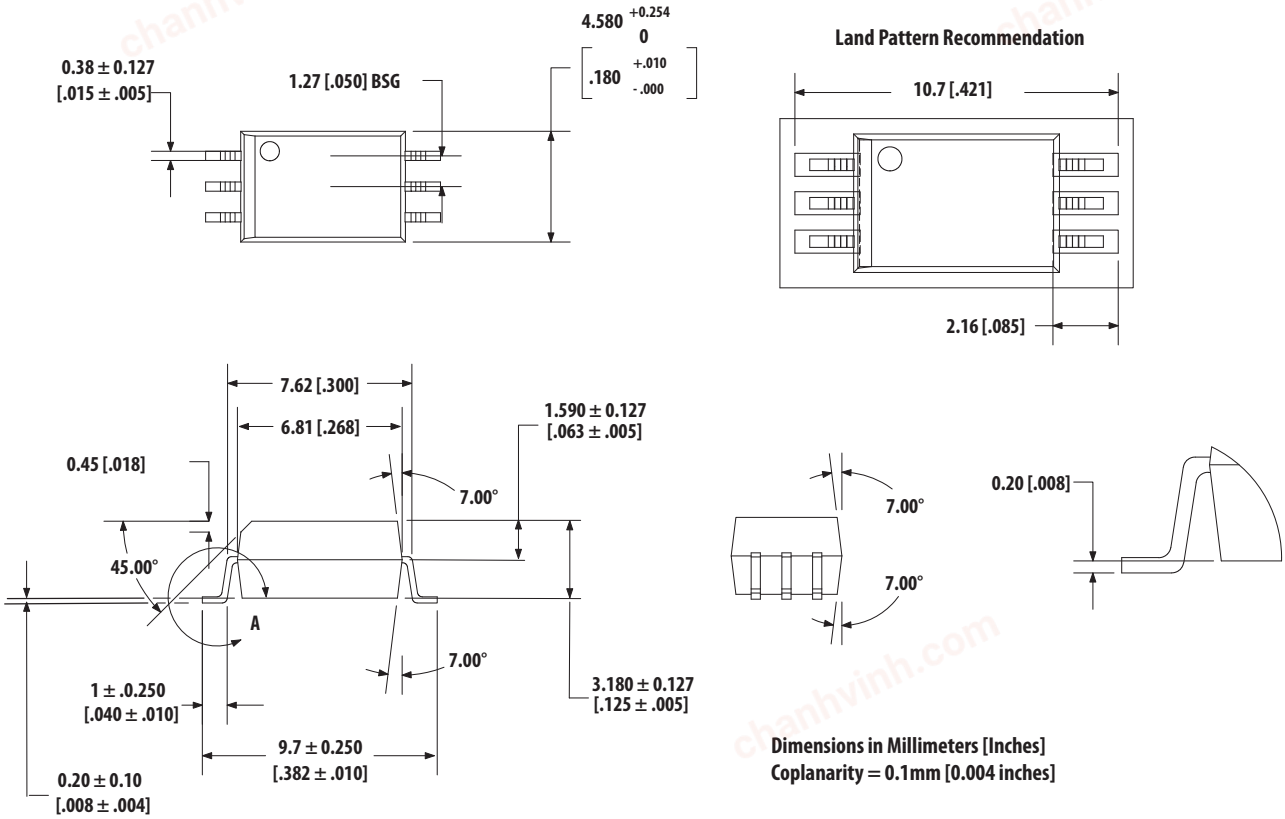
ACPL-P454 (Stretched SO6, 7mm Clearance)



Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-W454/P454 are approved by the following organizations:

IEC/EN/DIN EN 60747-5-2 (Option 060 only)
Approval under:
IEC 60747-5-2 :1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01

UL - Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} (5000VRMS for ACPL-W454). File E55361.

CSA - Approval under CSA Component Acceptance Notice #5, File CA 88324.

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Insulation Related Specifications

Parameter	Symbol	W454 Value	P454 Value	Units	Conditions
Min External Air Gap (Clearance)	L(IO1)	8	7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	8	8	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa			Material Group DIN VDE 0109

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics (Option 060 only)

Description	Symbol	ACPL-W454	ACPL-P454	Units
Installation classification per DIN VDE 0110/1.89, Table 1				
for rated mains voltage ≤ 150 Vrms		I-IV	I-IV	
for rated mains voltage ≤ 300 Vrms		I-IV	I-IV	
for rated mains voltage ≤ 450 Vrms		I-III	I-III	
for rated mains voltage ≤ 600 Vrms		I-III	I-III	
for rated mains voltage ≤ 1000 Vrms		I-II		
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	1140	891	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec Partial Discharge < 5 pC,	V_{PR}	2137	1670	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	1710	1336	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	8000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure)				
Case Temperature	T_S	175	175	°C
Input Current	$I_{S,INPUT}$	230	230	mA
Output Power	$P_{S,OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\leq 10^9$	$\leq 10^9$	Ω

* Refer to the optocoupler section of the Designer's Catalog, under regulatory information (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

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Absolute Maximum Ratings

Storage Temperature	-55°C to +125°C
Operating Temperature	-55°C to +100°C
Average Input Current - I_F	25 mA[1]
Peak Input Current - I_F	50 mA[2] (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current - I_F	1.0 A (≤1 ms pulse width, 300 pps)
Reverse Input Voltage - V_R (Pin3-1)	5 V
Input Power Dissipation	45 mW[3]
Average Output Current - I_O (Pin 5)	8 mA
Peak Output Current	16 mA
Output Voltage - V_O (Pin 5-4)	-0.5 V to 20 V
Supply Voltage - V_{CC} (Pin 6-4)	-0.5 V to 30 V
Output Power Dissipation	100 mW[4]
Solder Reflow Temperature Profile	see Package Outline Drawings section

DC Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	25	32	60	%	T_A = 25°C	V_O = 0.4 V	I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 4	5
		21	34				V_O = 0.5 V			
Current Transfer Ratio	CTR	26	35	65	%	T_A = 25°C	V_O = 0.4 V	I_F = 12 mA, V_{CC} = 4.5 V		5
		22	37				V_O = 0.5 V			
Logic Low Output Voltage	V_{OL}		0.2	0.4	V	T_A = 25°C	I_O = 3.0 mA	I_F = 16 mA, V_{CC} = 4.5 V	1	
			0.2	0.5			I_O = 2.4 mA			
Logic High Output Current	I_{OH}		0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	5	
			0.01	1		T_A = 25°C	V_O = V_{CC} = 15.0 V			
				50						
Logic Low Supply Current	I_{CCL}		50	200	µA	I_F = 16 mA, V_{CC} = 15 V		V_O = open,		11
Logic High Supply Current	I_{CCH}		0.02	1	µA	T_A = 25°C	I_F = 16 mA, V_O = Open,	V_{CC} = 15 V		11
			0.02	2						
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
			1.5	1.8						
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA				
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0				

*All typicals at T_A = 25°C.

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Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.2	0.3	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10% I_F = 16 mA, V_{CC} = 5.0 V R_L = 1.9 kΩ, C_L = 15 pF V_{THHL} = 1.5 V	6,8,9	9
			0.2	0.5					
		0.2	0.5	0.7		T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50% I_F = 12 mA, V_{CC} = 15.0 V R_L = 20 kΩ, C_L = 100 pF V_{THHL} = 1.5 V	6, 10-14	10
		0.1	0.5	1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}		0.3	0.5	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10% I_F = 16 mA, V_{CC} = 5.0 V R_L = 1.9 kΩ, C_L = 15 pF V_{THHL} = 1.5 V	6,8,9	9
			0.3	0.7					
		0.3	0.8	1.1		T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50% I_F = 12 mA, V_{CC} = 15.0 V R_L = 20 kΩ, C_L = 100 pF V_{THHL} = 2.0 V	6, 10-14	10
		0.2	0.8	1.4					
Propagation Delay Difference Between Any 2 Parts	t_{PLH} - t_{PHL}	-0.4	0.3	0.9	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50% I_F = 12 mA, V_{CC} = 15.0 V R_L = 20 kΩ, C_L = 100 pF V_{THHL} = 1.5 V V_{THLH} = 2.0V	6, 10-14	13
		-0.7	0.3	1.3	µs				
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C	V_{CC} = 5.0 V, R_L = 1.9 kΩ C_L = 15 pF, I_F = 0 mA V_{CM} = 1500 V_{P-P}	7	7,9
		15	30			T_A = 25°C	V_{CC} = 15.0 V, R_L = 20 kΩ C_L = 100 pF, I_F = 0 mA V_{CM} = 1500 V_{P-P}	7	8,10
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C	V_{CC} = 5.0 V, R_L = 1.9 kΩ C_L = 15 pF, I_F = 16 mA V_{CM} = 1500 V_{P-P}	7	7,9
		15	30			T_A = 25°C	V_{CC} = 15.0 V, R_L = 20 kΩ C_L = 100 pF, I_F = 12 mA V_{CM} = 1500 V_{P-P}	7	8,10
		15	30			T_A = 25°C	V_{CC} = 15.0 V, R_L = 20 kΩ C_L = 100 pF, I_F = 16 mA V_{CM} = 1500 V_{P-P}	7	8,10

*All typicals at T_A = 25°C.

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Package Characteristics

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			Vrms	RH ≤ 50%, t = 1 min, T_A = 25°C		6,12
		5000 (For "ACPL-W454)						
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		6
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz; V_{I-O} = 0 Vdc		6

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable).

Notes:
1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O), to the forward LED input current (I_F), times 100.
6. Device considered a two-terminal device: Pins 1 and 3 shorted together and Pins 4, 5 and 6 shorted together.
7. Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., VO < 0.8 V).
8. Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, VCM, to assure that the output will remain in a Logic High state (i.e., V_O > 3.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal,V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 1.0 V).
9. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
10. The R_L = 20 kΩ, C_L = 100 pF load represents an IPM (Intelligent Power Mode) load.
11. Use of a 0.1 µF bypass capacitor connected between pins 4 and 6 is recommended.
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA); each optocoupler under ACPL-W454 is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).
13. The difference between t_{PLH} and t_{PHL}, between any two ACPL-W454/P454 parts under the same test condition. (See Power Inverter Dead Time and Propagation Delay Specifications section).

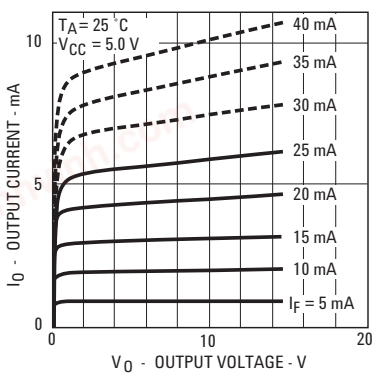

Figure 1. DC and Pulsed Transfer Characteristics.

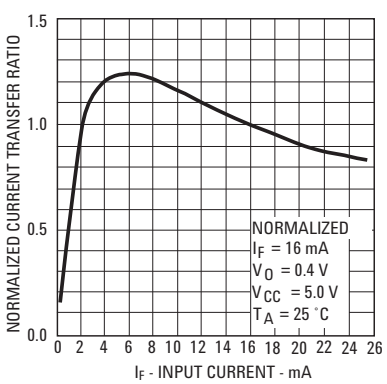

Figure 2. Current Transfer Ratio vs. Input Current.

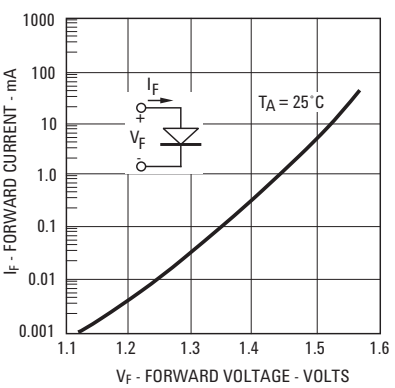

Figure 3. Input Current vs. Forward Voltage.

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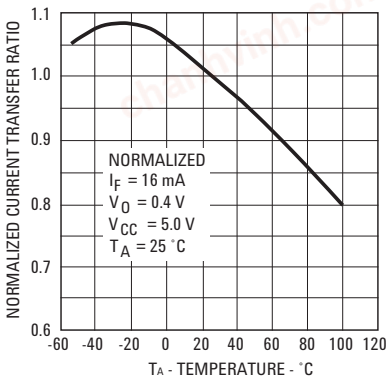

Figure 4. Current Transfer Ratio vs. Temperature.

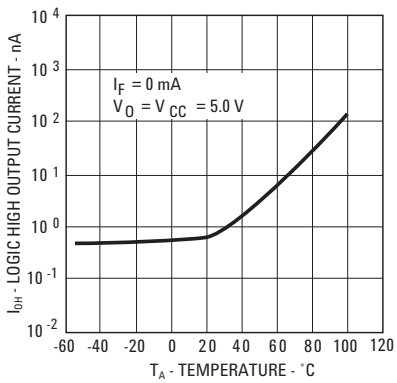

Figure 5. Logic High Output Current vs. Temperature.

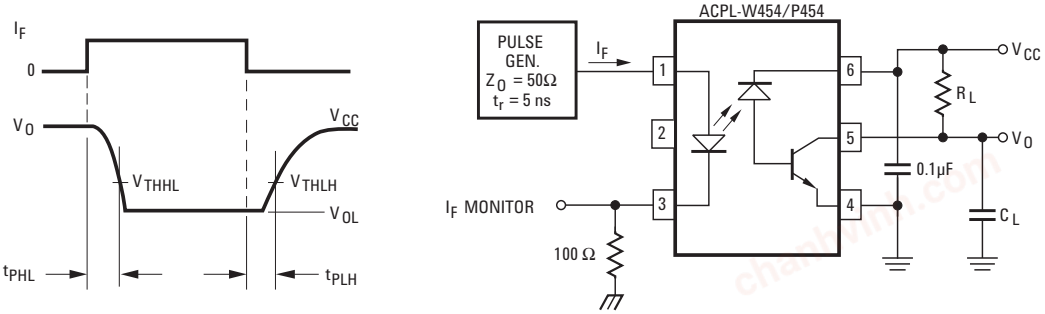

Figure 6. Switching Test Circuit.

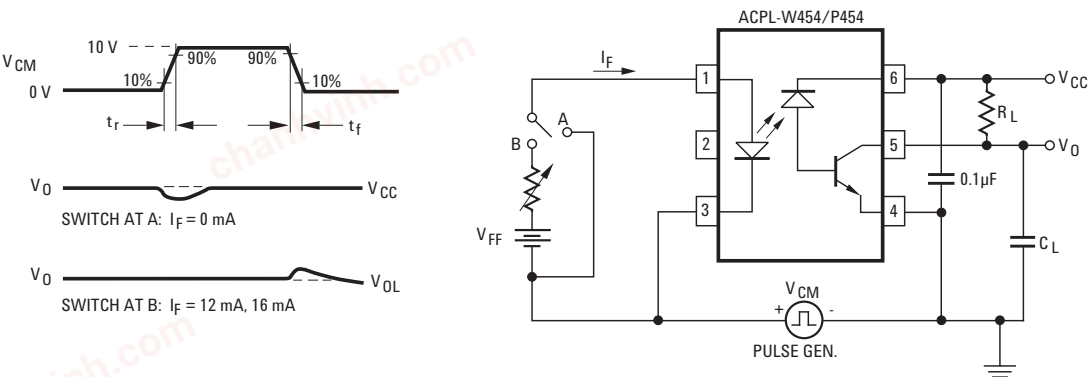

Figure 7. Test Circuit for Transient Immunity and Typical Waveforms.

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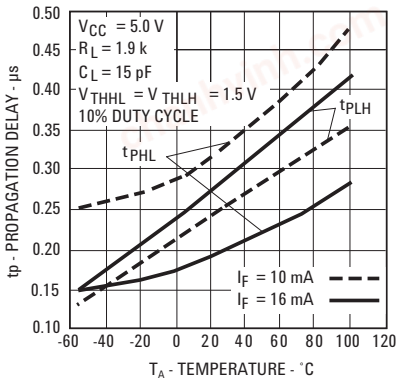

Figure 8. Propagation Delay Time vs. Temperature.

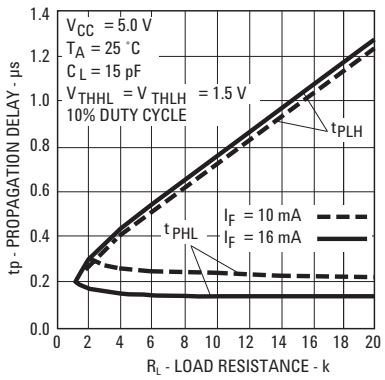

Figure 9. Propagation Delay Time vs. Load Resistance.

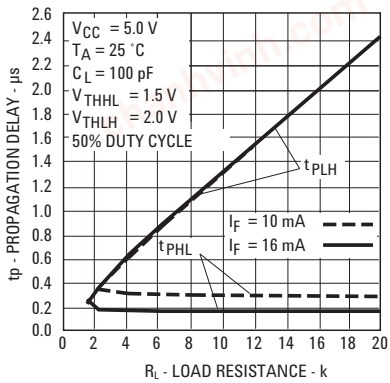

Figure 10. Propagation Delay Time vs. Load Resistance.

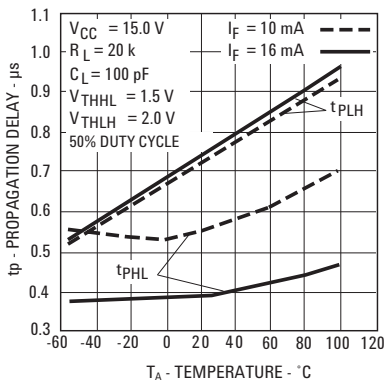

Figure 11. Propagation Delay Time vs. Temperature.

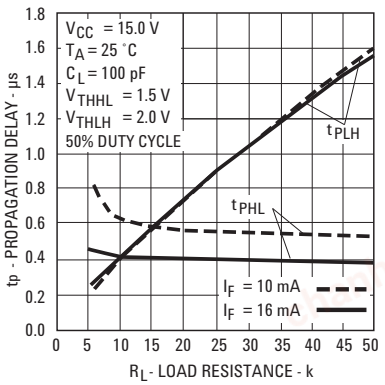

Figure 12. Propagation Delay Time vs. Load Resistance.

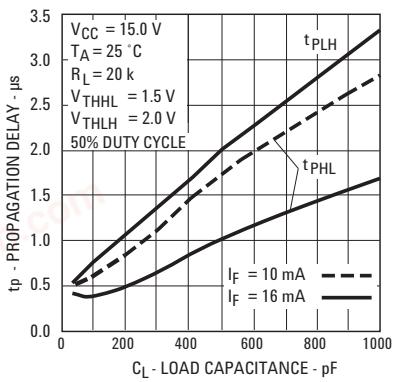

Figure 13. Propagation Delay Time vs. Load Capacitance.

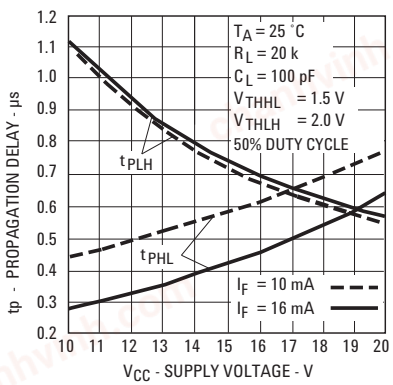

Figure 14. Propagation Delay Time vs. Supply Voltage.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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AV02-1307EN - August 4, 2010