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# ACPL-M43T

## Wide Operating Temperature Automotive Digital Optocoupler with R²Coupler® Isolation and 5-Pin SMT Package

AVAGO TECHNOLOGIES
A Broadcom Limited Company

## Data Sheet

**Lead (Pb) Free**
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

### Description

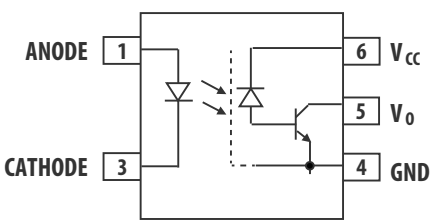
The ACPL-M43T is a single channel, high temperature, high CMR, high speed digital optocoupler in a five lead miniature footprint specifically used in the automotive applications. The SO-5 JEDEC registered (MO-155) package outline does not require "through holes" in a PCB. This package occupies approximately one-fourth the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

This digital optocoupler uses an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The ACPL-M43T has an increased common mode transient immunity of 30kV/μs minimum at $V_{CM}$ = 1500V over extended temperature range.

Avago R²Coupler® isolation products provide the reinforced insulation and reliability needed for critical in automotive and high temperature industrial applications.

### Functional Diagram




**Truth Table**

| LED | Vo |
|---|---|
| ON | LOW |
| OFF | HIGH |

Note: The connection of a 0.1 F bypass capacitor between pins 4 and 6 is recommended.

### Features

- Qualified to AEC-Q100 Test Guidelines
- Wide Temperature Range: -40°C ~ 125°C
- High Temperature and Reliability IPM Driver for Automotive Application
- 30 kV/μs High Common-Mode Rejection at $V_{CM}$ = 1500 V (typ)
- Compact, Auto-Insertable SO5 Packages
- High Speed: 1 MBd (Typ)
- Low LED Drive Current: 10 mA (typ)
- Low Propagation Delay: 300 ns (typ)
- Worldwide Safety Approval:
  - UL1577 recognized, 4000 Vrms/1 min
  - CSA Approved
  - IEC/EN/DIN EN 60747-5-5

### Applications

- Automotive IPM Driver for DC-DC converters and motor inverters
- CANBus Communications Interface
- High Temperature Digital/Analog Signal Isolation
- Power Transistor Isolation

***CAUTION:*** *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.*

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## Ordering Information

| Part number | Option RoHS Compliant | Package | Surface Mount | Tape & Reel | IEC/EN/DIN EN 60747-5-5 | Quantity |
|---|---|---|---|---|---|---|
| ACPL-M43T | -000E | SO-5 | X | | | 100 per tube |
| | -060E | | X | | X | 100 per tube |
| | -500E | | X | X | | 1500 per reel |
| | -560E | | X | X | X | 1500 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-M43T-500E to order product of Mini-flat Surface Mount 5-pin package in Tape and Reel packaging with RoHS compliant.

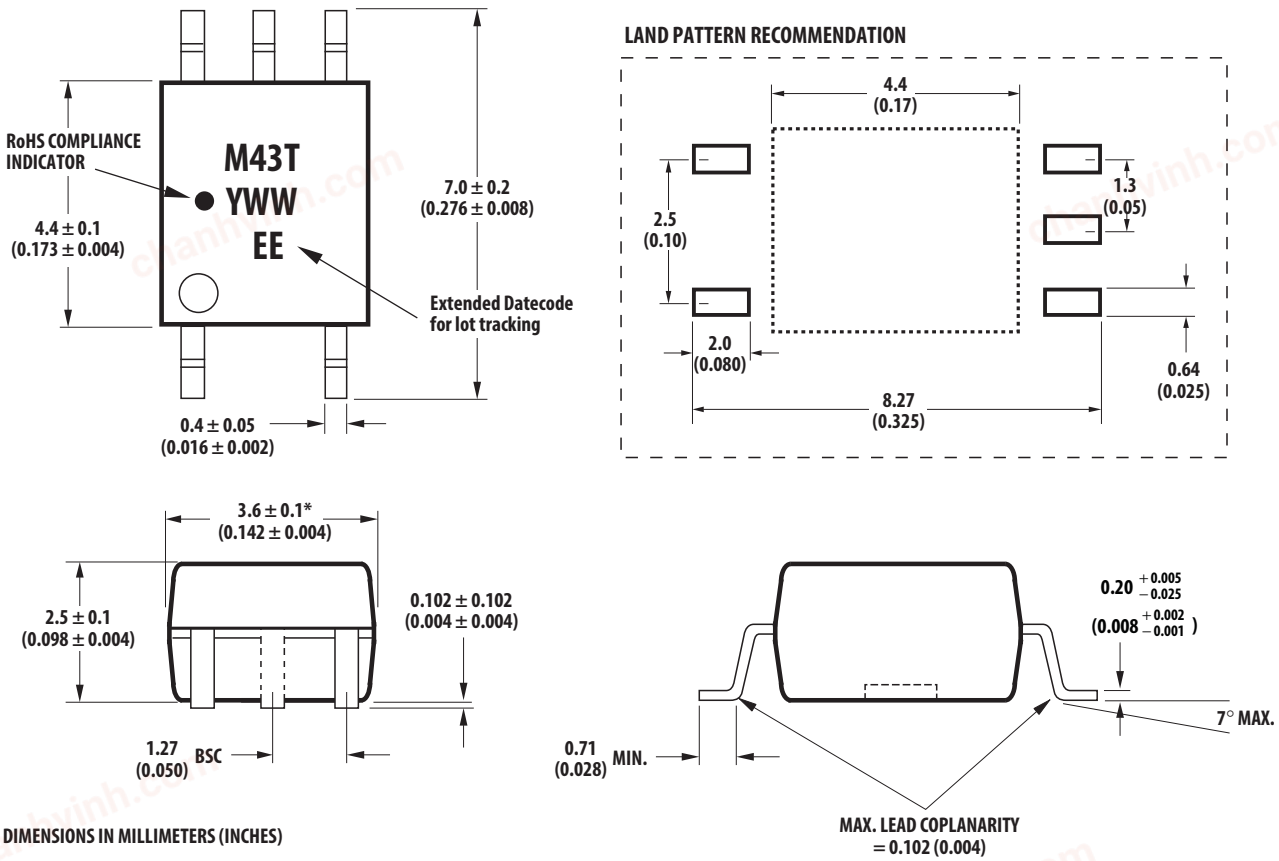
Example 2:

ACPL-M43T to order product of Mini-flat Surface Mount 5-pin package in tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings

### ACPL-M43T Small Outline SO-5 Package (JEDEC MO-155)




DIMENSIONS IN MILLIMETERS (INCHES)

* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

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## Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used.

## Regulatory Information

The ACPL-M43T is approved by the following organizations:

| | |
|---|---|
| **UL** | Approved under UL 1577, component recognition program up to $V_{ISO}$ = 4000 $V_{RMS}$ |
| **CSA** | Approved under CSA Component Acceptance Notice #5. |
| **IEC/EN/DIN EN 60747-5-5** | Approved under: IEC 60747-5-5, EN 60747-5-5 & DIN EN 60747-5-5 |

### IEC/EN/DIN EN 60747-5-5 Insulation Characteristics*

| Description | Symbol | Characteristic | Unit |
|---|---|---|---|
| Installation classification per DIN VDE 0110/1.89, Table 1 | | | |
| for rated mains voltage ≤ 150 $V_{rms}$ | | I – IV | |
| for rated mains voltage ≤ 300 Vrms | | I – III | |
| for rated mains voltage ≤ 600 $V_{rms}$ | | I – II | |
| Climatic Classification | | 40/125/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 567 | $V_{peak}$ |
| Input to Output Test Voltage, Method b* $V_{IORM}$ x 1.875=$V_{PR}$, 100% Production Test with $t_m$=1 sec, Partial discharge < 5 pC | $V_{PR}$ | 1063 | $V_{peak}$ |
| Input to Output Test Voltage, Method a* $V_{IORM}$ x 1.6=$V_{PR}$, Type and Sample Test, $t_m$=10 sec, Partial discharge < 5 pC | $V_{PR}$ | 907 | $V_{peak}$ |
| Highest Allowable Overvoltage (Transient Overvoltage $t_{ini}$ = 60 sec) | $V_{IOTM}$ | 6000 | $V_{peak}$ |
| Safety-limiting values – maximum values allowed in the event of a failure. | | | |
| Case Temperature | $T_S$ | 175 | °C |
| Input Current | $I_{S, INPUT}$ | 230 | mA |
| Output Power | $P_{S, OUTPUT}$ | 600 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | $>10^9$ | Ω |

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

### Insulation and Safety Related Specifications

| Parameter | Symbol | ACPL-M43T | Units | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (Clearance) | L(101) | 5 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (Creepage) | L(102) | 5 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | mm | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index) | CTI | 175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group (DIN VDE0109) | | IIIa | | Material Group (DIN VDE 0109) |

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## Absolute Maximum Ratings

| Parameter | | Symbol | Min. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Storage Temperature | | $T_S$ | –55 | 150 | °C | |
| Operating Temperature | | $T_A$ | –40 | 125 | °C | |
| Junction Temperature | | $T_J$ | | 139 | °C | |
| Lead Soldering Cycle | - Temperature | | | 260 | °C | |
| | - Time | | | 10 | s | |
| Average Forward Input Current | | $I_{F(avg)}$ | | 20 | mA | |
| Peak Forward Input Current (50% duty cycle, 1ms pulse width) | | $I_{F(peak)}$ | | 40 | mA | |
| Peak Transient Input Current (<= 1us pulse width, 300ps) | | $I_{F(trans)}$ | | 100 | mA | |
| Reversed Input Voltage | | $V_R$ | | 5 | V | Pin 3 - 1 |
| Input Power Dissipation | | $P_{IN}$ | | 30 | mW | |
| Output Power Dissipation | | $P_O$ | | 100 | mW | |
| Average Output Current | | $I_O$ | | 8 | mA | |
| Peak Output Current | | Io(pk) | | 16 | mA | |
| Supply Voltage (Pins 6-4) | | $V_{CC}$ | –0.5 | 30 | V | |
| Output Voltage (Pins 5-4) | | $V_O$ | –0.5 | 20 | V | |
| Solder Reflow Temperature Profile | | See Reflow Temperature Profile | | | | |

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units | Note |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3.0 | 20.0 | V | |
| Operating Temperature | $T_A$ | –40 | 125 | °C | |

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## Electrical Specifications (DC)

Over recommended operating $T_A$ = –40°C to 125°C, unless otherwise specified

| Parameter | Sym. | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Current Transfer Ratio | CTR | 32 | 65 | 100 | % | $T_A$ = 25°C, $V_{CC}$ = 4.5 V, $V_O$ = 0.4 V, $I_F$ = 10 mA | 1, 2, 4 | 1 |
| | | 24 | 65 | | | | | |
| | | 33 | 160 | | | $V_{CC}$ = 4.5 V, $V_O$ = 0.4 V, $I_F$ = 1.5 mA | | |
| | | 25 | 165 | | | $V_{CC}$ = 4.5 V, $V_O$ = 0.4 V, $I_F$ = 0.8 mA | | |
| Logic Low Output Voltage | $V_{OL}$ | | 0.1 | 0.5 | V | $V_{CC}$ = 4.5 V, $I_O$ = 2.4 mA, $I_F$ = 10 mA | | |
| | | | 0.1 | | | $V_{CC}$ = 4.5 V, $I_O$ = 0.5 mA, $I_F$ = 1.5 mA | | |
| | | | 0.1 | | | $V_{CC}$ = 4.5 V, $I_O$ = 0.2 mA, $I_F$ = 0.8 mA | | |
| Logic High Output Current | $I_{OH}$ | | $3x10^{-5}$ | 0.5 | µA | $T_A$ = 25°C, $V_O$ = $V_{CC}$ = 5.5 V, $I_F$ = 0 mA | 11, 12 | |
| | | | $8x10^{-5}$ | 5 | | $V_O$ = $V_{CC}$ = 20 V | | |
| Logic Low Supply Current | $I_{CCL}$ | | 85 | 200 | µA | $I_F$ = 10 mA, $V_O$ = open, $V_{CC}$ = 20 V | | |
| | | | 15 | | | $I_F$ = 1.5 mA, $V_O$ = open, $V_{CC}$ = 20 V | | |
| Logic High Supply Current | $I_{CCH}$ | | 0.02 | 1 | µA | $T_A$ = 25°C, $I_F$ = 0 mA, $V_O$ = open, $V_{CC}$ = 20 V | | |
| | | | | 2.5 | | | | |
| Input Forward Voltage | $V_F$ | 1.45 | 1.55 | 1.75 | V | $T_A$ = 25°C, $I_F$ = 10 mA | 3 | |
| | | 1.25 | 1.55 | 1.85 | | | | |
| Input Reversed Breakdown Voltage | $BV_R$ | 5 | | | V | $I_R$ = 10 µA | | |
| Temperature Coefficient of Forward Voltage | $\Delta V_F / \Delta T_A$ | | –1.5 | | mV/°C | $I_F$ =10 mA | | |
| | | | –1.8 | | | $I_F$ =1.5 mA | | |
| Input Capacitance | $C_{IN}$ | | 90 | | pF | F = 1 MHz, $V_F$ = 0 | | |

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### Switching Specifications (AC)

Over recommended operating ($T_A$ = -40°C to 125°C), $V_{CC}$ = 5.0 V unless otherwise specified.

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions | | | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low at Output | $t_{PHL}$ | 0.07 | 0.15 | 0.8 | µs | $T_A$ = 25°C | $I_F$ = 10 mA, $R_L$ = 1.9 kΩ | Pulse: f = 10 kHz, Duty cycle = 50%, $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $V_{THHL}$ = 1.5 V | 5, 6, 7, 8, 9, 10, 13 | 2, 3 |
| | | 0.06 | | 1.0 | | | | | | |
| | | | 0.7 | 5 | | | $I_F$ = 1.5 mA, $R_L$ = 10 kΩ | | | |
| | | | 1 | 10 | | | $I_F$ = 0.8 mA, $R_L$ = 27 kΩ | | | |
| Propagation Delay Time to Logic High at Output | $t_{PLH}$ | 0.15 | 0.5 | 0.8 | µs | $T_A$ = 25°C | $I_F$ = 10 mA, $R_L$ = 1.9 kΩ | Pulse: f = 10 kHz, Duty cycle = 50%, $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $V_{THHL}$ = 2.0 V | 5, 6, 7, 8, 9, 10, 13 | 2, 3 |
| | | 0.03 | | 1.0 | | | | | | |
| | | | 0.9 | 5 | | | $I_F$ = 1.5 mA, $R_L$ = 10 kΩ | | | |
| | | | 2 | 10 | | | $I_F$ = 0.8 mA, $R_L$ = 27 kΩ | | | |
| Pulse Width \Distortion | PWD | | 0.35 | 0.45 | µs | $T_A$ = 25°C | Pulse: f = 10 kHz, Duty cycle = 50%, $I_F$ = 10 mA, $V_{CC}$ = 5.0 V, $R_L$ = 1.9 kΩ, $C_L$ = 15 pF, $V_{THHL}$ = 1.5 V, $V_{THLH}$ = 2.0 V | | | 2, 3, 4 |
| | | | | 0.85 | | | | | | |
| Propagation Delay Difference Between Any 2 Parts | PDD | | 0.35 | 0.5 | µs | $T_A$ = 25°C | Pulse: f = 10 kHz, Duty cycle = 50%, $I_F$ = 10 mA, $V_{CC}$ = 5.0 V, $R_L$ = 1.9 kΩ, $C_L$ = 15 pF, $V_{THHL}$ = 1.5 V, $V_{THLH}$ = 2.0 V | | | 2, 3, 5 |
| | | | | 0.9 | | | | | | |
| Common Mode Transient Immunity at Logic High Output | $\|CM_H\|$ | 15 | 30 | | kV/µs | $I_F$ = 0 mA | $V_{CM}$ = 1500 $V_{p-p}$, $R_L$ = 1.9 kΩ, $V_{CC}$ = 5 V, $T_A$ = 25° C | | 14 | 6 |
| Common Mode Transient Immunity at Logic Low Output | $\|CM_L\|$ | 15 | 30 | | kV/µs | $I_F$ = 10 mA | | | | |
| Common Mode Transient Immunity at Logic High Output | $\|CM_H\|$ | | 5 | | kV/µs | $I_F$ = 0 mA | $V_{CM}$ = 1500 $V_{p-p}$, $R_L$ = 10 kΩ, $V_{CC}$ = 5 V, $T_A$ = 25° C | | 14 | 6 |
| Common Mode Transient Immunity at Logic Low Output | $\|CM_L\|$ | | 5 | | kV/µs | $I_F$ = 1.5 mA | | | | |

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## Package Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage* | $V_{ISO}$ | 4000 | | | $V_{RMS}$ | RH ≤ 50%, t = 1 min; $T_A$ = 25°C | | 7, 8 |
| Input-Output Resistance | $R_{I-O}$ | | $10^{14}$ | | Ω | $V_{I-O}$ = 500 Vdc | | 7 |
| Input-Output Capacitance | $C_{I-O}$ | | 0.6 | | pF | f = 1 MHz; $V_{I-O}$ = 0 Vdc | | 7 |

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.

Notes:
1. Current Transfer Ratio in percent is defined as the ratio of output collector current, $I_O$, to the forward LED input current, $I_F$, times 100.
2. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
3. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
4. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
5. The difference between $t_{PLH}$ and $t_{PHL}$ between any two parts under the same test condition.
6. Common transient immunity in a Logic High level is the maximum tolerable (positive) $dV_{CM}/dt$ on the rising edge of the common mode pulse, $V_{CM}$, to assure that the ouput will remain in a Logic High state (i.e., $V_O$ > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) $dV_{CM}/dt$ on the falling edge of the common mode pulse signal, $V_{CM}$ to assure that the output will remain in a Logic Low state (i.e., $V_O$ < 0.8 V).
7. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 $V_{RMS}$ for 1 second.

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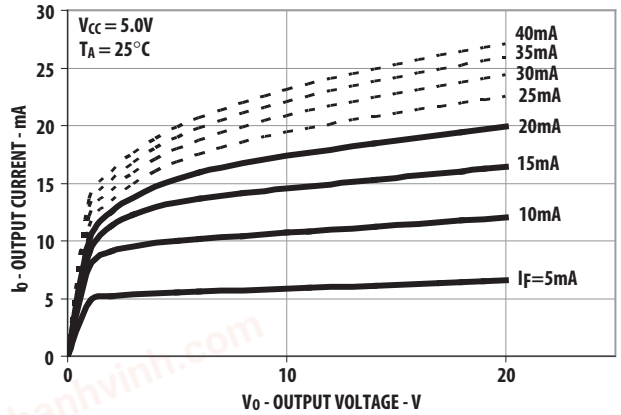


Figure 1. DC and Pulsed Transfer Characteristics

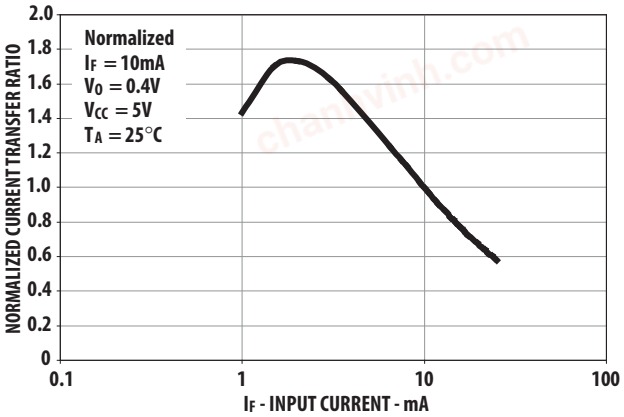


Figure 2. Current Transfer Ratio vs. Input Current

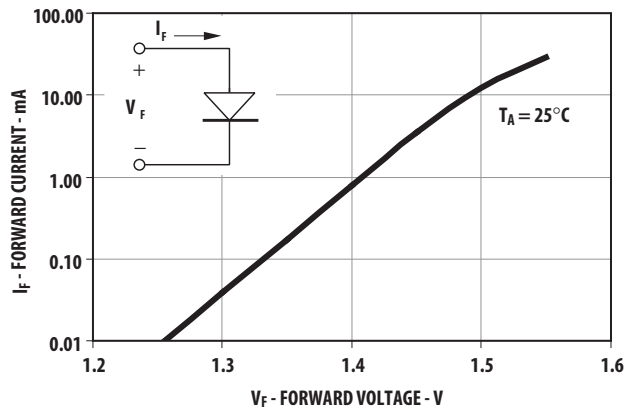


Figure 3. Input Current vs. Forward Voltage

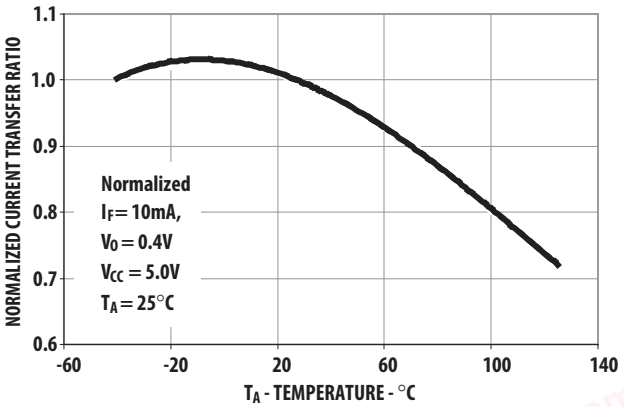


Figure 4. Current Transfer Ratio vs. Temperature

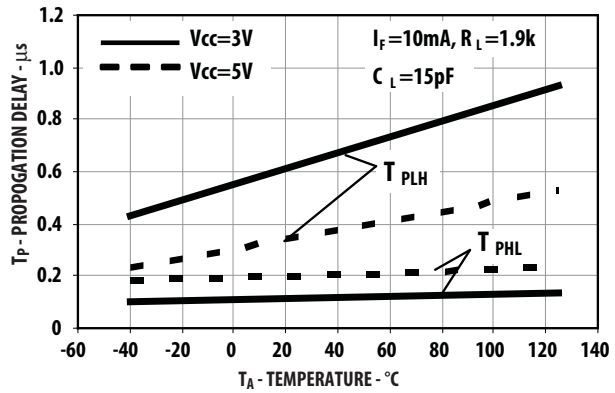


Figure 5. Propagation Delay vs. Temperature

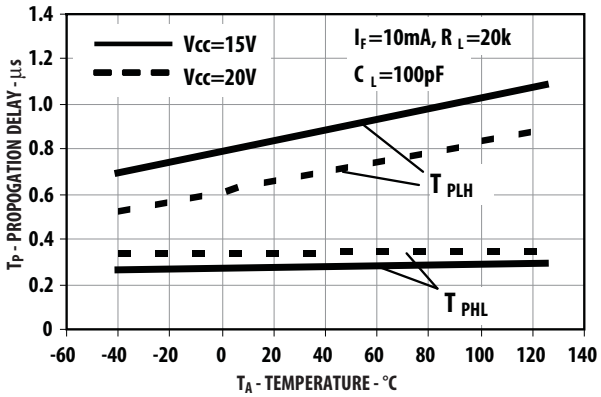


Figure 6. Propagation Delay vs. Temperature

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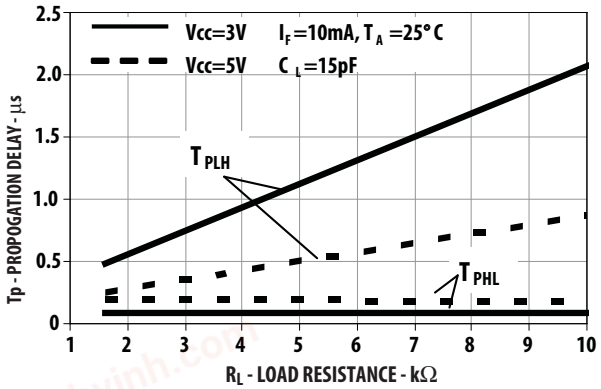


Figure 7. Propagation Delay Time vs. Load Resistance

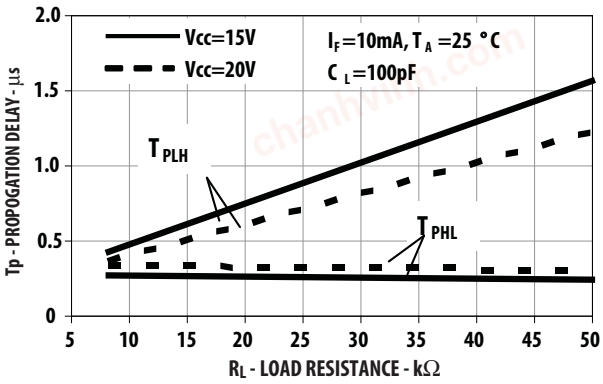


Figure 8. Propagation Delay Time vs. Load Resistance

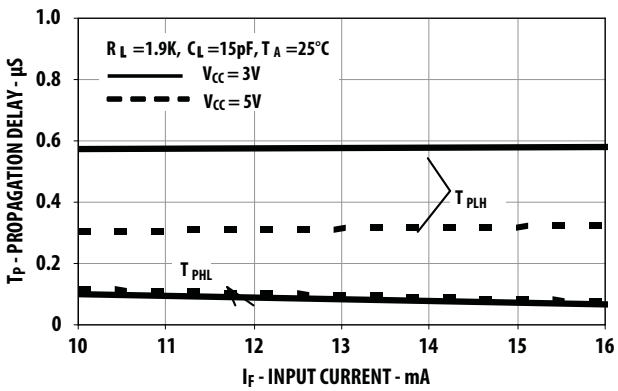


Figure 9. Propagation Delay Time vs. Input Current

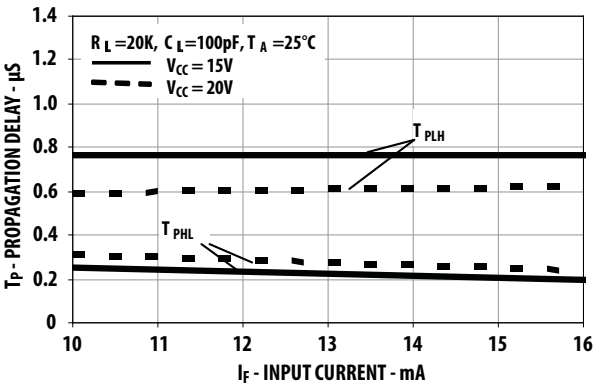


Figure 10. Propagation Delay Time vs. Input Current

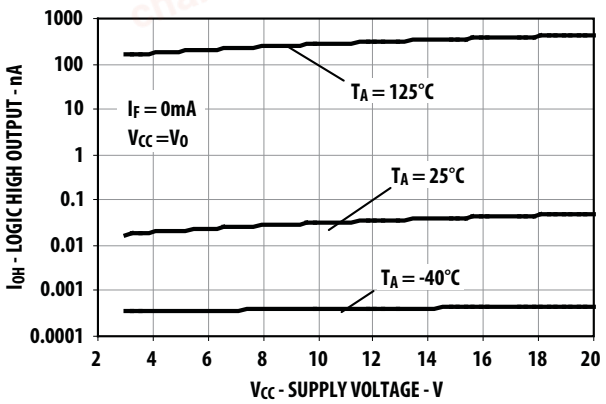


Figure 11. Logic High Output Current vs. Supply Voltage

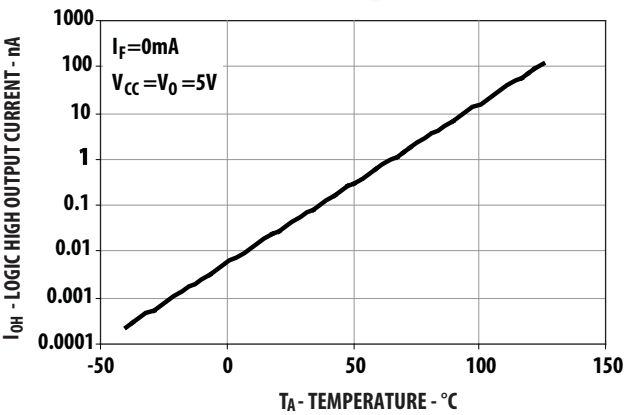


Figure 12. Logic High Output Current vs. Temperature

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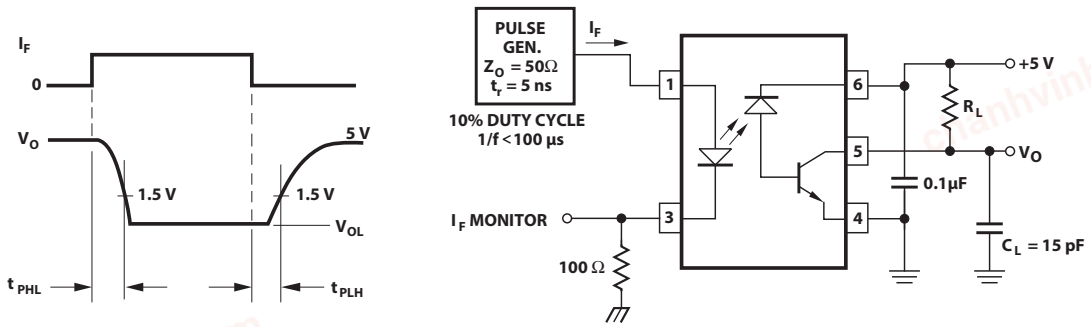


**Figure 13. Switching Test Circuit**

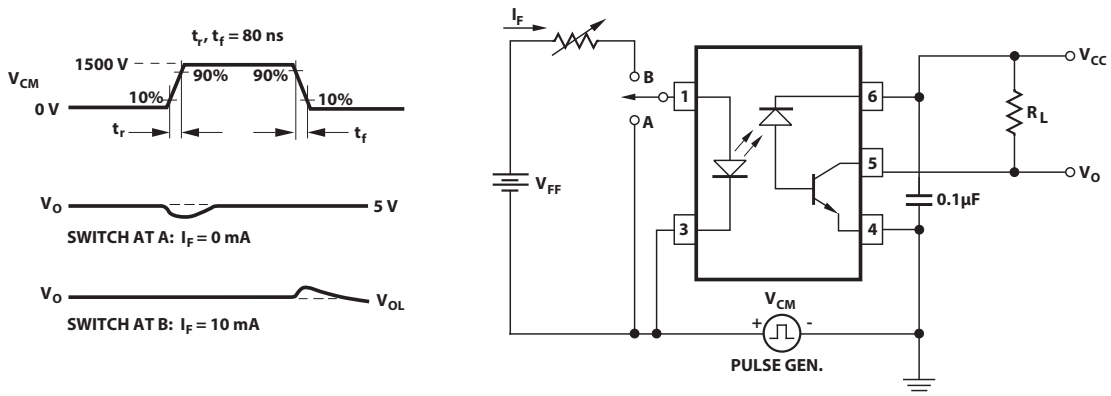


**Figure 14. Test Circuit for Transient Immunity and Typical Waveforms**

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