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Data Sheet

ACPL-K70A/K73A

Low Input Current, High Current Gain, LVTTL, LVCMOS Optocoupler

Description

These high gain series couplers use a light-emitting diode (LED) and an integrated high gain photodetector to provide an extremely high current transfer ratio between input and output. Separate pins for photodiode and output stage result in LVTTL-compatible saturation voltages and high-speed operation. Where desired, the V_{CC} and V_O terminals may be tied together to achieve conventional photo-darlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

These optocouplers are for use in LVTTL/LVCMOS or other low-power applications.

The ACPL-K70A and ACPL-K73A are surface-mount devices that are packaged in an industry-standard stretched SOIC-8 footprint.

The stretched SOIC-8 does not require through holes in a PCB.

Figure 1: Functional Diagram

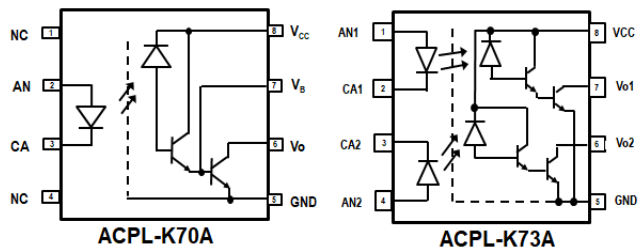


Table 1: Truth Table

LED	Output
ON	L
OFF	H

A 0.1-µF bypass capacitor must be connected between pins V_{CC} and GND.

Features

- 3.3V/5V dual supply voltages
- Low power consumption
- High current transfer ratio
- Low input current requirements: 0.04 mA
- Stretched SO8 package
- LVTTL/LVCMOS compatible output
- Guaranteed performance within the temperature range –40°C to +105°C
- Base access allows gain bandwidth adjustment
- High output current: 60 mA
- Worldwide Safety Approval:
  - UL1577 recognized: 5000 V_{rms}/1 min
  - CSA approval
  - IEC 60747-5-5 approval for reinforced insulation

Applications

- EIA RS-232C/low input current line receiver
- Low power systems: ground isolation
- Line voltage status indicator; low input power dissipation

CAUTION! Take normal static precautions in handling and assembling this component to prevent damage and/or degradation that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

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Ordering Information

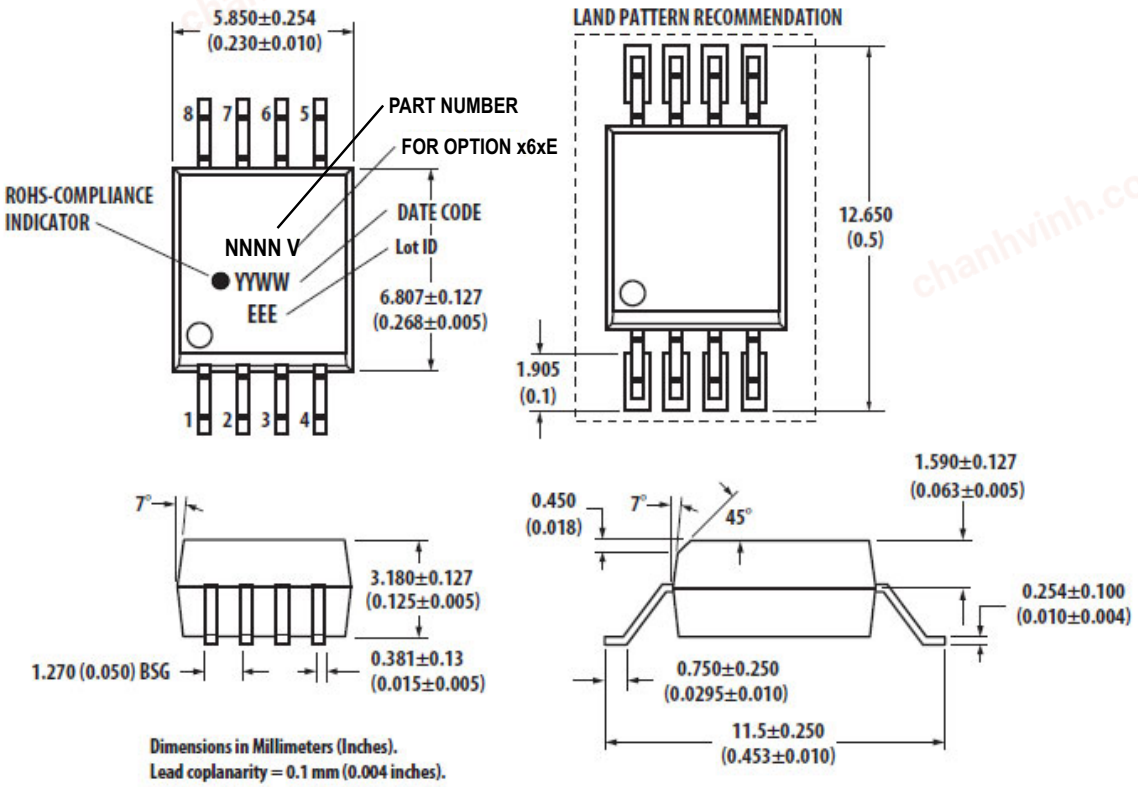
ACPL-K70A/K73A is UL recognized with 5000 V_{rms} for 1 minute per UL 1577.

Part Number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	UL 1577	IEC 60747-5-5	Quantity
ACPL-K70A/K73A	-000E	Stretched SO8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To form an order entry, choose a part number from the Part Number column and combine with the desired option from the Option column.

Package Outline Drawing

Figure 2: ACPL-K70A/K73A Stretched SO8 Package



Solder Reflow Profile

Recommended reflow condition as per JEDEC standard J-STD-020 (latest revision). Non-halide flux should be used.

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Regulatory Information

The ACPL-K70A/K73A is pending approval by the following organizations:

- **UL** – Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS} File E55361.
- **CSA** – Approval under CSA Component Acceptance Notice #5, File CA 88324.
- **IEC 60747-5-5**

Table 2: Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-K70A/K73A	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group	—	IIIa	—	Material Group (DIN VDE 0110, 1/89, Table 1).

Table 3: IEC 60747-5-5 Insulation Characteristics[1]

Description	Symbol	Characteristic ACPL-K70A/K73A	Unit
Installation classification per DIN VDE 0110/39, Table 1	—		—
For rated mains voltage ≤ 150 V_{rms}		I - IV	
For rated mains voltage ≤ 300 V_{rms}		I - IV	
For rated mains voltage ≤ 600 V_{rms}		I - IV	
For rated mains voltage ≤ 1000 V_{rms}		I - III	
Climatic Classification	—	40/105/21	—
Pollution Degree (DIN VDE 0110/39)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b[1] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a[1] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}

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Table 3: IEC 60747-5-5 Insulation Characteristics[1] (Continued)

Description	Symbol	Characteristic ACPL-K70A/K73A	Unit
Safety-limiting values: maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

1. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog*, under the "Product Safety Regulations" section, (IEC 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

Table 4: Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units
Storage Temperature		T_S	–55	125	°C
Operating Temperature		T_A	–40	105	°C
Lead Soldering Cycle	Temperature			260	°C
	Time			10	s
Average Forward Input Current		$I_{F(avg)}$	—	20	mA
Peak Forward Input Current (50% duty cycle, 1-ms pulse width)		$I_{F(peak)}$	—	40	mA
Peak Transient Input Current (≤ 1 µs pulse width, 300 pps)		$I_{F(trans)}$	—	1.0	A
Reversed Input Voltage		V_R	—	5	V
Input Power Dissipation		P_{IN}	—	35	mW
Output Power Dissipation		P_O	—	100	mW
Output Current		$I_{O(AVG)}$	—	60	mA
Emitter Base Reverse Voltage (Pin 5–7)		V_{EB}	—	0.5	V
Output Transistor Base Current		I_B	—	5	mA
Supply Voltage and Output Voltage		V_{CC}	–0.5	18	V
Solder Reflow Temperature Profile		See Package Outline Drawing.			

Table 5: Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	3.3	18.0	V
Forward Input Current (ON)	$I_{F(ON)}$	0.04	12	mA
Operating Temperature	T_A	–40	105	°C
Forward Input Voltage (OFF)	$V_{F(OFF)}$	—	0.8	V
Output Current	$I_{O(AVG)}$	—	25	mA

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Table 6: Electrical Specifications (DC)

Over-recommended operating (T_A = –40°C to 105°C) unless otherwise specified. All typical specifications are at T_A = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions		Fig.
Current Transfer Ratio	CTR[1]	800	8000	25,000	%	I_F = 0.04 mA	V_{CC} = 3.3V or 5V V_O = 0.4V	4, 5
		400	3500	8000	%	I_F = 0.5 mA		
		300	1980	5000	%	I_F = 1.6 mA		
Logic Low Output Voltage	V_{OL}	—	0.02	0.4	V	I_F = 0.04 mA I_O = 280 µA	V_{CC} = 3.3V or 5V	—
		—	0.04	0.4	V	I_F = 0.5 mA or 1.6 mA, I_O = 3.0 mA		—
Logic High Output Current	I_{OH}	—	0.003	5	µA	–40°C ≤ T_A ≤ 70°C	V_O = V_{CC} = 3.3V or 5V I_F = 0 mA	—
		—	18	100	µA	70°C < T_A ≤ 105°C		
		—	0.01	80	µA	–40°C ≤ T_A ≤ 70°C	V_O = V_{CC} = 18V I_F = 0 mA	—
		—	50	250	µA	70°C < T_A ≤ 105°C		
Logic Low Supply Current[2]	I_{CCL}	—	0.03	0.2	mA	I_F = 0.04 mA	V_O = open V_{CC} = 18V	—
		—	0.53	1	mA	I_F = 0.5 mA		
		—	1.75	2.5	mA	I_F = 1.6 mA		
Logic High Supply Current[2]	I_{CCH}	—	0.08	10	µA	I_F = 0 mA V_O = open V_{CC} = 18V	—	—
Input Forward Voltage	V_F	—	1.3	1.7	V	I_F = 0.04 mA to 1.6 mA	—	3
		—	1.4	1.8	V	I_F = 12 mA		
Input Reversed Breakdown Voltage	BV_R	2.5	5	—	V	I_R = 100 µA	—	—
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	I_F = 1.6 mA	—	—
Input Capacitance	C_{IN}	—	18	—	pF	f = 1 MHz V_F = 0	—	—

1. Current transfer ratio in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, multiplied by 100%.
2. Each channel.

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Table 7: Switching Specifications

Over-recommended operating (T_A = –40°C to 105°C) unless otherwise specified. All typical specifications are at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.
Propagation Delay Time to Logic Low at Output	t_{PHL}	—	36	500	µs	I_F = 0.04 mA V_{CC} = 3.3/5.0V R_L = 11 kΩ		8, 9, 14
		—	3.5	30	µs	I_F = 0.5 mA V_{CC} = 3.3/5.0V R_L = 4.7 kΩ		10, 11, 14
		—	1.2	25	µs	I_F = 1.6 mA V_{CC} = 3.3/5.0V R_L = 2.2 kΩ		14
		—	0.2	2	µs	I_F = 12 mA V_{CC} = 3.3/5.0V R_L = 270Ω		12, 13, 14
Propagation Delay Time to Logic High at Output	t_{PLH}	—	170	1500	µs	I_F = 0.04 mA R_L = 11 kΩ	V_{CC} = 3.3V	8, 9, 14
		—	100	800	µs		V_{CC} = 5.0V	
		—	85	700	µs	I_F = 0.5 mA R_L = 4.7 kΩ	V_{CC} = 3.3V	10, 11, 14
		—	50	500	µs		V_{CC} = 5.0V	
		—	43	400	µs	I_F = 1.6 mA R_L = 2.2 kΩ	V_{CC} = 3.3V	14
		—	26	300	µs		V_{CC} = 5.0V	
		—	7	80	µs	I_F = 12 mA R_L = 270Ω	V_{CC} = 3.3V	12, 13, 14
		—	4.2	40	µs		V_{CC} = 5.0V	
Common Mode Transient Immunity at Logic High Output[1]	$\|CM_H\|$	10	—	—	kV/µs	T_A = 25°C	V_{CM} = 1000V I_F = 0 mA R_L = 270Ω V_{CC} = 3.3V/5V	15
Common Mode Transient Immunity at Logic Low Output[2]	$\|CM_L\|$	10	—	—	kV/µs	T_A = 25°C	V_{CM} = 1000V I_F = 12 mA R_L = 270Ω V_{CC} = 3.3V/5V	15

1. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to ensure that the output will remain in a Logic High state (that is, V_O > 2.0V).
2. Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to ensure that the output will remain in a Logic Low state (that is, V_O < 0.8V).

Table 8: Package Characteristics

All typical specifications are at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage[1]	V_{ISO}	5000	—	—	V_{rms}	RH ≤ 50%, t = 1 min., T_A = 25°C
Input-Output Resistance[1]	R_{I-O}	—	10^{12}	—	Ω	V_{I-O} = 500 Vdc
Input-Output Capacitance[1]	C_{I-O}	—	0.6	—	pF	f = 1 MHz, T_A = 25°C

1. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.

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Figure 3: Input Current vs. Forward Voltage

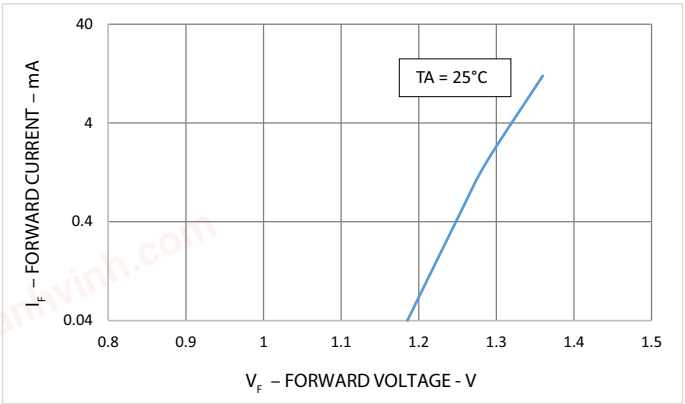


Figure 4: Current Transfer Ratio vs Forward Current

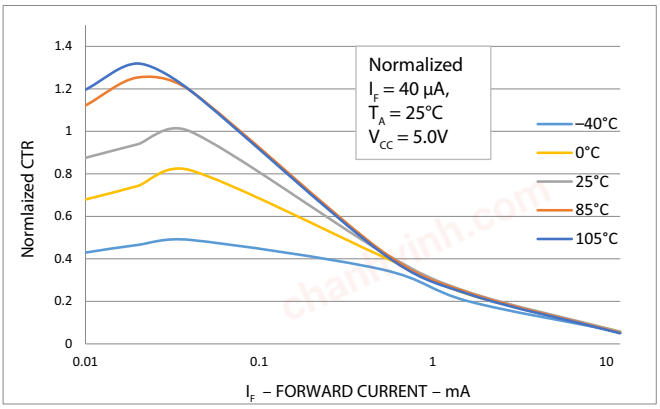


Figure 5: Current Transfer Ratio vs Forward Current

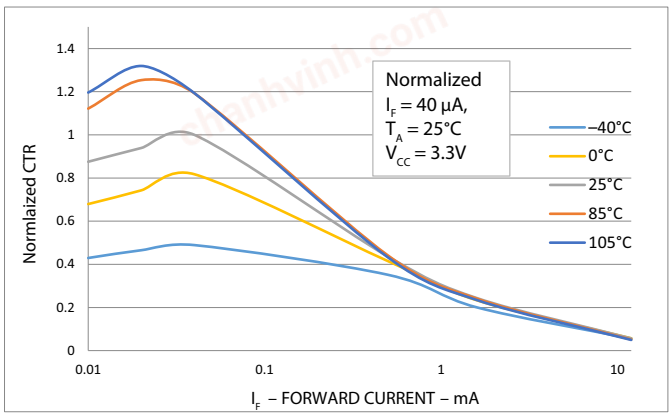


Figure 6: Logic Low Output Current vs. Temperature

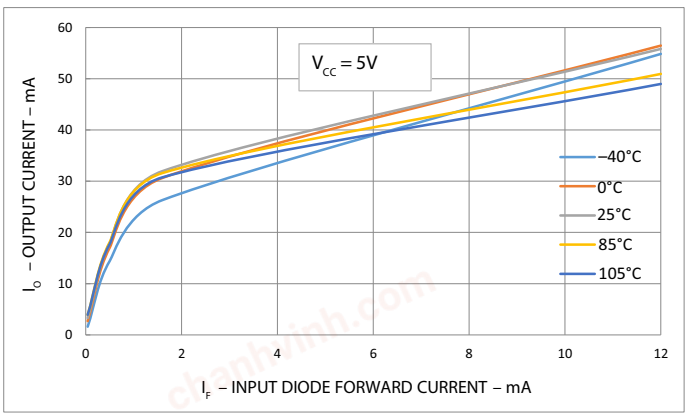


Figure 7: Logic Low Output Current vs. Temperature

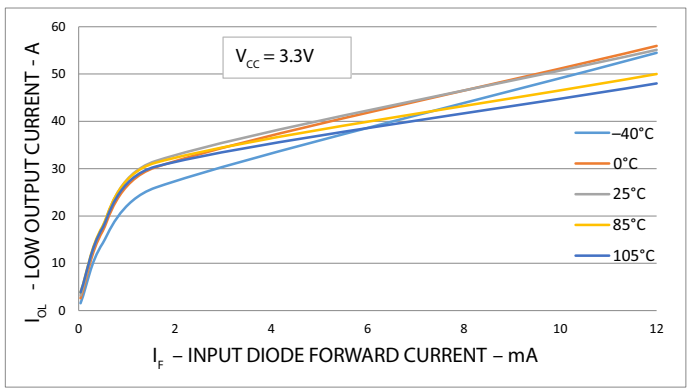
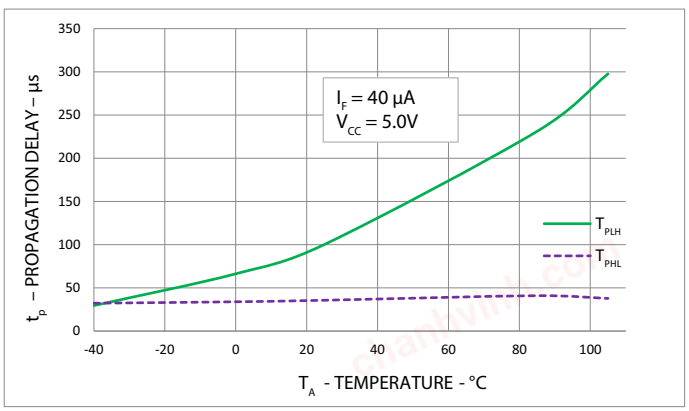


Figure 8: Typical Propagation Delay vs. Temperature



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Figure 9: Typical Propagation Delay vs. Temperature

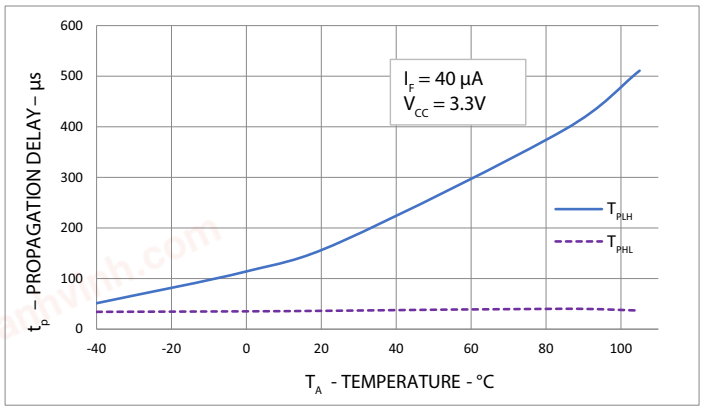


Figure 10: Typical Propagation Delay vs. Temperature

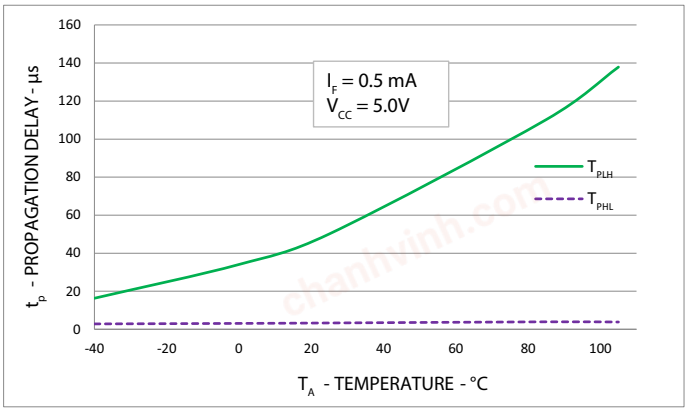


Figure 11: Typical Propagation Delay vs. Temperature

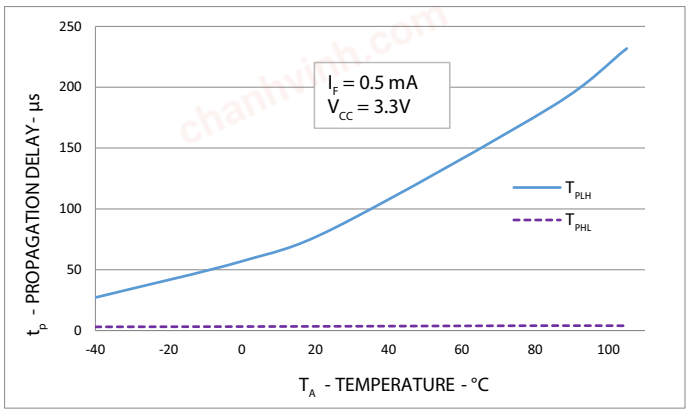


Figure 12: Typical Propagation Delay vs. Temperature

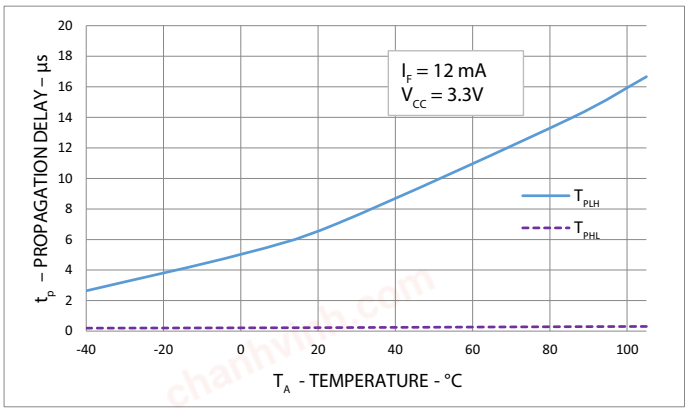
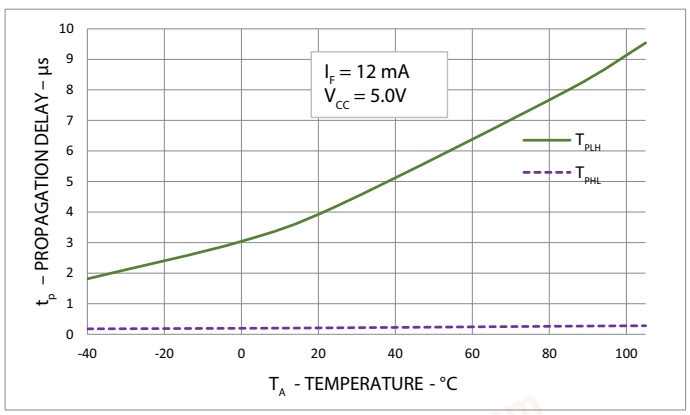


Figure 13: Typical Propagation Delay vs. Temperature



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Figure 14: Switching Test Circuits

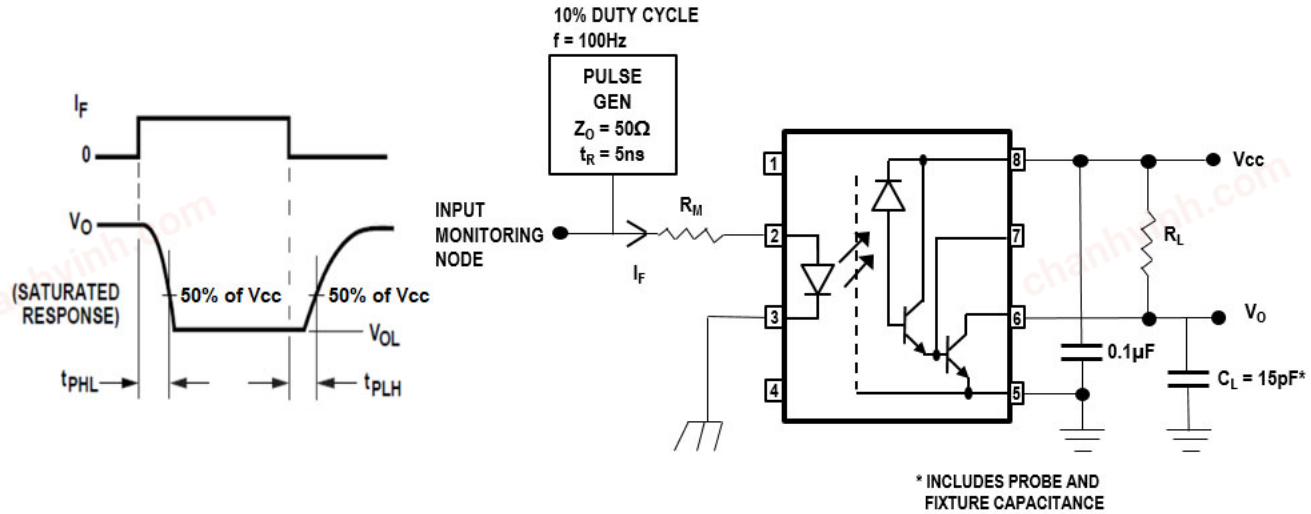
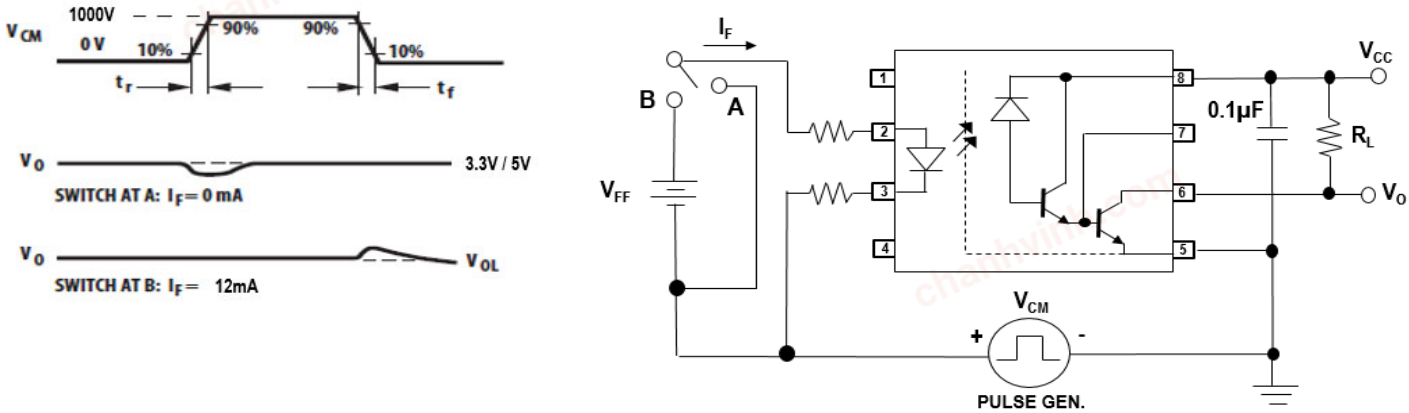


Figure 15: Test Circuit for Transient Immunity and Typical Waveforms



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