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Data Sheet

# ACPL-C877

## Precision Optically Isolated Digital Voltage Sensor

## Description

The Broadcom® ACPL-C877 digital voltage sensor is a 1-bit, second-order sigma-delta (Σ-Δ) modulator, designed specifically for voltage sensing. The sigma-delta (Σ-Δ) modulator converts an analog input signal from 0V to 2V into high-speed data stream with galvanic isolation based on optical coupling technology. The 2V wide differential input linear voltage range and high 1-GΩ input impedance make it well suited for isolated voltage sensing requirements in electronic power converters applications, including motor drives and renewable energy systems. In a typical voltage sensing implementation, a resistive voltage divider is used to scale the DC-link voltage to suit the input linear range of the digital voltage sensor. The ACPL-C877 operates from a 5V power supply with dynamic range of 76 dB with an appropriate digital filter.

The analog input is continuously sampled by a means of sigma-delta over-sampling using an in-built clock. The signal information is contained in the modulator data, as a density of ones with data rate of 10 MHz, and the data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter. The serial interface for data and clock has a wide supply range of 3V to 5.5V.

Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With 0.5 mm minimum distance through insulation (DTI), the ACPL-C877 provides reliable reinforced insulation and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive- or magnetic-coupling with DTI in micro-meter range. Offered in a Stretched SO-8 (SSO-8) package, the isolated ADC delivers the reliability, small size, superior isolation and over-temperature performance motor drive designers need to accurately measure voltage.

## Features

- Superior optical isolation and insulation
- 10-MHz internal clock
- 1-bit, second-order sigma-delta modulator
- 16 bits resolution no missing codes (10 bits ENOB)
- 76 dB typical SNR, 66 dB typical SNDR
- ±10 mV maximum offset error at room temperature
- 8 µV/°C typical offset drift
- ±1% maximum gain error
- Internal reference voltage
- 0V to 2V linear range with single 5V supply (3.2V full scale)
- 3V to 5.5V wide supply range for digital interface
- –40°C to +110°C operating temperature range
- Output slew rate control
- SSO-8 package
- 25-kV/µs common-mode transient immunity
- Safety and regulatory approval:
  - IEC/EN 60747-5-5: 1414 Vpeak working insulation voltage
  - UL 1577: 5000 $V_{rms}$/1 min isolation voltage
  - CAN/CSA-C22.2 No. 62368-1

## Applications

- Isolated voltage sensing in AC and servo motor drives
- Isolated DC-bus voltage sensing in solar inverters and wind turbine inverters
- Isolated sensor interfaces
- Signal isolation in data acquisition systems
- General-purpose voltage sensing
- Voltage sensing in insulation resistance measurements

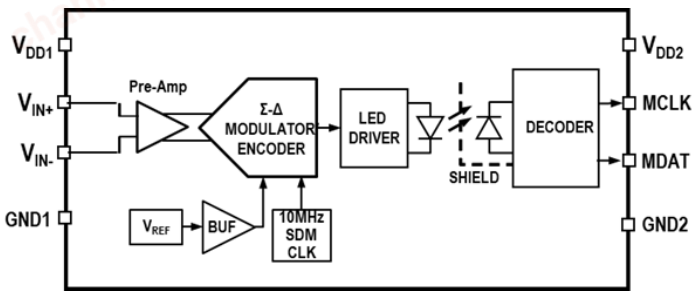
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**CAUTION!** Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments. The component is also not AEC-Q100 and not recommended for automotive applications.

# Functional Block Diagram

**Figure 1: Functional Block Diagram**




# Pin Configurations and Descriptions

**Figure 2: Pin Configuration**

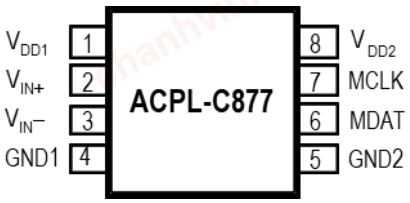



**Table 1: Pin Descriptions**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply voltage for signal input side (analog side), relative to GND1. |
| 2 | $V_{IN+}$ | Positive analog input, recommended input range 0V to 2V. |
| 3 | $V_{IN-}$ | Negative analog input, recommended input range 0V to 2V (normally connected to GND1). |
| 4 | GND1 | Supply ground for signal input side. |
| 5 | GND2 | Supply ground for data/clock output side (digital side). |
| 6 | MDAT | Modulator data output. |
| 7 | MCLK | Modulator clock output. |
| 8 | $V_{DD2}$ | Supply voltage for data output side, relative to GND2. |

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# Ordering Information

The ACPL-C877 is UL recognized with 5000 $V_{rms}$/1 minute rating per UL 1577.

| Part Number | Option (RoHS Compliant) | Package | Tape and Reel | IEC/EN 60747-5-5 | Quantity |
|---|---|---|---|---|---|
| ACPL-C877 | -000E | Stretched SO-8 | — | X | 80 per tube |
| | -500E | | X | X | 1000 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

**Example:**

ACPL-C877-500E to order product of Surface Mount package in Tape and Reel packaging with IEC/EN 60747-5-5 Safety Approval and RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

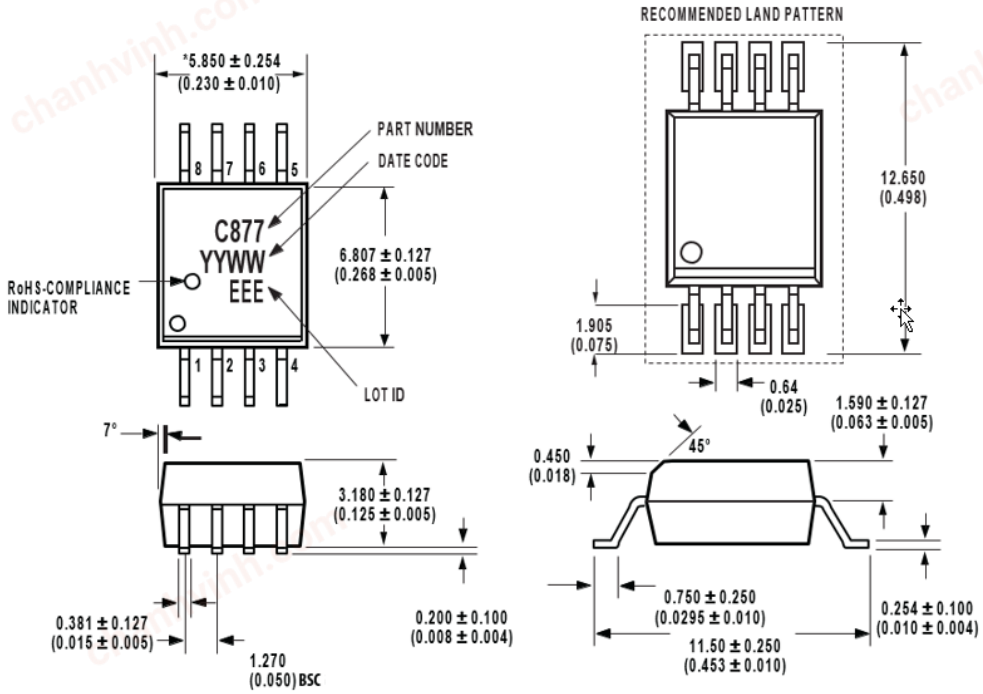
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# Package Outline Drawings

## Stretched SO-8 Package (SSO-8)

**Figure 3: Package Dimensions**




* Total package width (inclusive of mold flash)
6.100 ± 0.250 mm
Dimensions in millimeters and (inches).

Notes:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25 mm (10 mils) max.

# Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Use non-halide flux.

# Regulatory Information

The ACPL-C877 is approved by the following organizations.

| | |
|---|---|
| IEC/EN 60747-5-5 | Maximum working insulation voltage $V_{IORM}$ = 1414 $V_{PEAK}$. |
| UL | Approval under UL 1577, component recognition program up to $V_{ISO}$ = 5000 $V_{rms}$. File E55361. |
| CSA | Approval under CAN/CSA-C22.2 No. 62368-1. |

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# IEC/EN 60747-5-5 Insulation Characteristics

**Table 2: IEC/EN 60747-5-5 Insulation Characteristics[a]**

| Description | Symbol | Value | Units |
|---|---|---|---|
| Installation Classification per DIN VDE 0110/1.89, Table 1 | | | |
| For Rated Mains Voltage ≤ 150 $V_{rms}$ | | I-IV | |
| For Rated Mains Voltage ≤ 300 $V_{rms}$ | | I-IV | |
| For Rated Mains Voltage ≤ 450 $V_{rms}$ | | I-IV | |
| For Rated Mains Voltage ≤ 600 $V_{rms}$ | | I-IV | |
| For Rated Mains Voltage ≤ 1000 $V_{rms}$ | | I-III | |
| Climatic Classification | — | 55/110/21 | — |
| Pollution Degree (DIN VDE 0110/1.89) | — | 2 | — |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 1414 | $V_{peak}$ |
| Input to Output Test Voltage, Method b<br>$V_{IORM}$ × 1.875 = $V_{PR}$, 100% Production Test with $t_m$ = 1s, Partial Discharge < 5 pC | $V_{PR}$ | 2652 | $V_{peak}$ |
| Input to Output Test Voltage, Method a<br>$V_{IORM}$ × 1.6 = $V_{PR}$, Type and Sample Test, $t_m$ = 10s, Partial Discharge < 5 pC | $V_{PR}$ | 2262 | $V_{peak}$ |
| Highest Allowable Overvoltage (Transient Overvoltage, tini = 60 seconds) | $V_{IOTM}$ | 8000 | $V_{peak}$ |
| Safety-Limiting Values (Maximum values allowed in the event of a failure.) | | | |
| Case Temperature | $T_S$ | 175 | °C |
| Input Current[b] | $I_{S,INPUT}$ | 230 | mA |
| Output Power[b] | $P_{S,OUTPUT}$ | 600 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500V | $R_S$ | ≥$10^9$ | Ω |

a. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.

b. Safety-limiting parameters are dependent on ambient temperature. The Input Current, $I_{S,INPUT}$, derates linearly above 25°C free-air temperature at a rate of 2.53 mA/°C; the Output Power, $P_{S,OUTPUT}$, derates linearly above 25°C free-air temperature at a rate of 4 mW/°C.

# Insulation and Safety Related Specifications

| Parameter | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (External Clearance) | L(101) | 8.0 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L(102) | 8.0 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | — | 0.5 | mm | Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity. |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN EN 112/VDE 0303 Part 1. |
| Isolation Group | — | IIIa | — | Material Group (DIN VDE 0110, 1/89, Table 1). |

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# UL 1577 Specification Sheet

| Model | Package Type | Current, mA | | Power, mW | | Isolation Voltage 1 min, $V_{rms}$ | Maximum Operating Temperature °C | Maximum Junction Temperature °C | Maximum Storage Temperature °C |
|---|---|---|---|---|---|---|---|---|---|
| | | Emitter | Sensor | Emitter | Sensor | | | | |
| ACPL-C877 | 3 | 13 | 10 | 71.5 | 55 | 5000 | 110 | 125 | 125 |

# Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Storage Temperature | $T_S$ | –55 | +125 | °C |
| Ambient Operating Temperature | $T_A$ | –40 | +110 | °C |
| Supply Voltage | $V_{DD1}$, $V_{DD2}$ | –0.5 | 6.0 | V |
| Steady-State Input Voltage[a, b] | $V_{IN+}$, $V_{IN–}$ | –2 | $V_{DD1}$ + 0.5 | V |
| Two-Second Transient Input Voltage[c] | $V_{IN+}$, $V_{IN–}$ | –6 | $V_{DD1}$ + 0.5 | V |
| Digital Output Voltages | MCLK, MDAT | –0.5 | $V_{DD2}$ + 0.5 | V |
| Lead Solder Temperature | 260°C for 10 seconds, 1.6 mm below seating plane | | | |

a. DC voltage of up to –2V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.

b. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

c. Transient voltage of 2 seconds up to –6V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.

# Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | –40 | +110 | °C |
| $V_{DD1}$ Supply Voltage | $V_{DD1}$ | 4.5 | 5.5 | V |
| $V_{DD2}$ Supply Voltage | $V_{DD2}$ | 3 | 5.5 | V |
| Analog Input Voltage[a] | $V_{IN+}$, $V_{IN–}$ | 0 | 2 | V |

a. Full scale signal input range 3.2 V.

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# Electrical Specifications

Unless otherwise noted, $T_A$ = –40°C to +110°C, $V_{DD1}$ = 4.5V to 5.5V, $V_{DD2}$ = 3V to 5.5V, $V_{IN+}$ = 0V to 2V, and $V_{IN–}$ = 0V (single-ended connection); tested with $Sinc^3$ filter, 256 decimation ratio.

| Parameter | Symbol | Min. | Typ.[a] | Max. | Units | Test Conditions | Figure |
|---|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | | |
| Resolution | | 16 | — | — | Bits | Decimation filter output set to 16 bits. | |
| Integral Nonlinearity | INL | –32 | — | 32 | LSB | $T_A$ = –40°C to +110°C; see Definitions. | |
| Differential Nonlinearity | DNL | –0.9 | — | 0.9 | LSB | No missing codes, guaranteed by design; see Definitions. | |
| Offset Error | $V_{OS}$ | –10 | 0 | 10 | mV | $T_A$ = 25°C; $R_{sense}$ (R2) = 0Ω; see Definitions. | 6 |
| Offset Drift vs. Temperature | $TCV_{OS}$ | — | 8 | 20 | µV/°C | $R_{sense}$ (R2) = 0Ω. | |
| Offset Drift vs. $V_{DD1}$ | | — | 500 | — | µV/V | | |
| Internal Reference Voltage | $V_{REF}$ | | 3.2 | — | V | | |
| Gain Error | $G_E$ | –1 | — | 1 | % | $T_A$ = 25°C, $V_{IN+}$ = 0V to 2V; see Definitions. | |
| | | –2 | — | 2 | % | $T_A$ = –40°C to +110°C, $V_{IN+}$ = 0V to 2V. | 7 |
| Gain Error Drift vs. Temperature | $TCG_E$ | — | 40 | — | ppm/°C | | |
| Gain Error Drift vs. $V_{DD1}$ | | — | 0.16 | — | %/V | See note[b]. | |
| **Analog Inputs** | | | | | | | |
| Linear-Scale Input Differential Voltage Range | LSR | 0 | — | 2 | V | $V_{IN} = V_{IN+} – V_{IN–}$; recommended input voltage range for specified performance. | |
| Full-Scale Input Differential Voltage Range | FSR | –0.1 | — | 3.2 | V | $V_{IN} = V_{IN+} – V_{IN–}$; see note[c]. | |
| Input Bias Current | $I_{INA}$ | –20 | ±2 | 20 | nA | $V_{IN+}$ = 0V, $V_{IN–}$ = 0V. | |
| Input Resistance | $R_{IN}$ | 0.1 | 1 | — | GΩ | $V_{IN+}$ = 2V, $V_{IN–}$ = 0V. | |
| Input Capacitance | $C_{INA}$ | — | 8 | — | pF | Across $V_{IN+}$, $V_{IN–}$ = 0V. | |
| **Dynamic Characteristics** | | | | | | $V_{IN+}$ = 400 mVpp, 1-kHz sine wave. | |
| Signal-to-Noise Ratio | SNR | 62 | 76 | — | dB | $T_A$ = –40°C to +110°C; $V_{IN+}$ = 0V to 2V, 1 kHz sine wave; see Definitions. | 8 |
| Signal-to-(Noise + Distortion) Ratio | SNDR | 60 | 66 | — | dB | $T_A$ = –40°C to +110°C; $V_{IN+}$ = 0V to 2V, 1 kHz sine wave; see Definitions. | 9 |
| Effective Number of Bits | ENOB | — | 10 | — | Bits | See Definitions. | |
| Isolation Transient Immunity | CMTI | — | 25 | — | kV/µs | $V_{CM}$ = 1 kV; $T_A$ = 25°C; see Definitions. | |
| **Digital Outputs** | | | | | | | |
| Output High Voltage | $V_{OH}$ | $V_{DD2}$ – 0.4 | $V_{DD2}$ – 0.2 | — | V | $I_{OUT}$ = –4 mA. | |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OUT}$ = +4 mA. | |

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| Parameter | Symbol | Min. | Typ.[a] | Max. | Units | Test Conditions | Figure |
|---|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1}$ | — | 8 | 13 | mA | $V_{IN+}$ = 0V to 2V. | 10 |
| $V_{DD2}$ Supply Current | $I_{DD2}$ | — | 6.8 | 10 | mA | | 11 |
| | | — | 6.0 | 8.5 | mA | $V_{DD2}$ = 3.3V supply. | 12 |

a. All Typical values are at $T_A$ = 25°C, $V_{DD1}$ = 5V, $V_{DD2}$ = 5V.

b. Gain Error Drift vs. $V_{DD1}$ is expressed as 5 mV/V with reference to $V_{REF}$.

c. Beyond the full-scale input range, the data output is either all zeros or all ones.

# Timing Specifications

Unless otherwise noted, $T_A$ = –40°C to +110°C, $V_{DD1}$ = 4.5V to 5.5V, $V_{DD2}$ = 3V to 5.5V.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Notes | Figure |
|---|---|---|---|---|---|---|---|---|
| Modulator Clock Output Frequency | $f_{MCLK}$ | 9 | 10 | 11 | MHz | $C_L$ = 15 pF | a | 13 |
| Modulator Clock Rising Time | $t_r$ | — | 5 | — | ns | $C_L$ = 15 pF | | |
| Modulator Clock Falling Time | $t_f$ | — | 5 | — | ns | $C_L$ = 15 pF | | |
| Data Setup Time after MCLK Rising Edge | $t_S$ | 50 | — | — | ns | $C_L$ = 15 pF | | 4 |
| Data Hold Time after MCLK Rising Edge | $t_H$ | 10 | — | — | ns | $C_L$ = 15 pF | | 4 |
| Clock and Data Startup Time | $t_{START}$ | — | 0.5 | — | ms | $V_{DD1}$ step to 4.5V, $V_{DD2}$ >3.0V. | | 5 |

a. $f_{MCLK}$ specification is based on average value which is equal to SDM CLK.

**Figure 4: Data Timing**

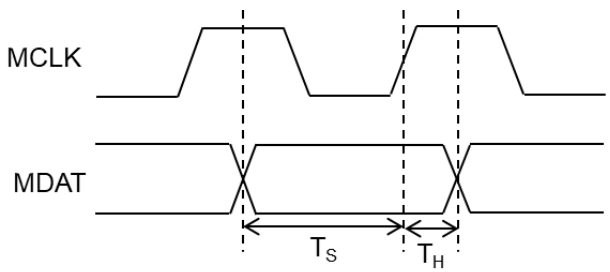
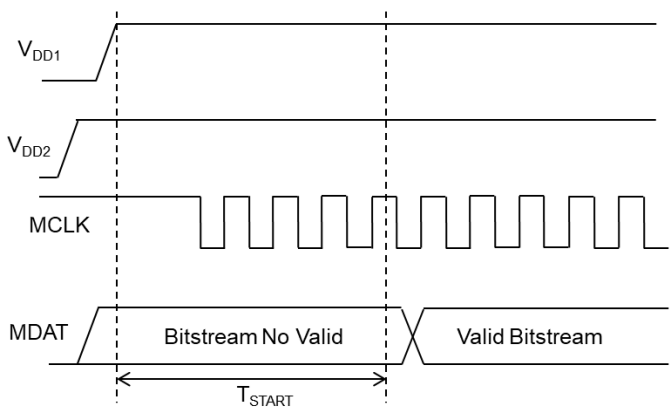



**Figure 5: Clock and Data Startup Time**



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# Package Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions/Notes | Note |
|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage | $V_{ISO}$ | 5000 | — | — | $V_{rms}$ | RH ≤ 50%, t = 1 min; $T_A$ = 25°C | a, b |
| Input-Output Resistance | $R_{I-O}$ | — | $>10^{12}$ | — | Ω | $V_{I-O}$ = 500 Vdc | c |
| Input-Output Capacitance | $C_{I-O}$ | — | 0.5 | — | pF | f = 1 MHz | c |

a. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 $V_{rms}$ for 1 second (leakage detection current limit, $I_{I-O}$ ≤ 5 μA). This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN 60747-5-5 Insulation Characteristics table.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN 60747-5-5 Insulation Characteristics table and your equipment level safety specification.

c. This is a two-terminal measurement: pins 1 to 4 are shorted together and pins 5 to 8 are shorted together.

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# Typical Performance Plots

Unless otherwise noted, $T_A$ = 25°C, $V_{DD1}$ = 5V, $V_{DD2}$ = 5V, $V_{IN+}$ = 0V to 2V, and $V_{IN-}$ = 0V, with Sinc$^3$ filter, 256 decimation ratio.

**Figure 6: Offset Change vs. Temperature**

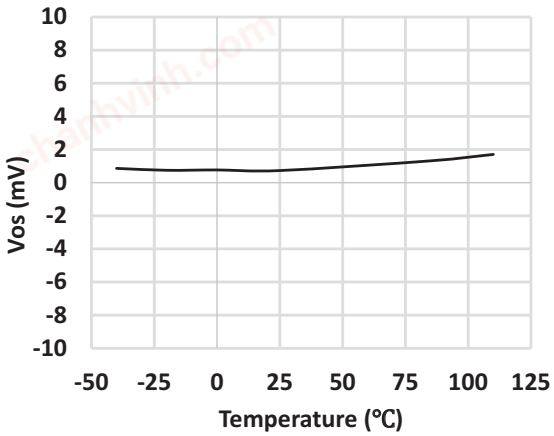



**Figure 7: Gain Error Change vs. Temperature**

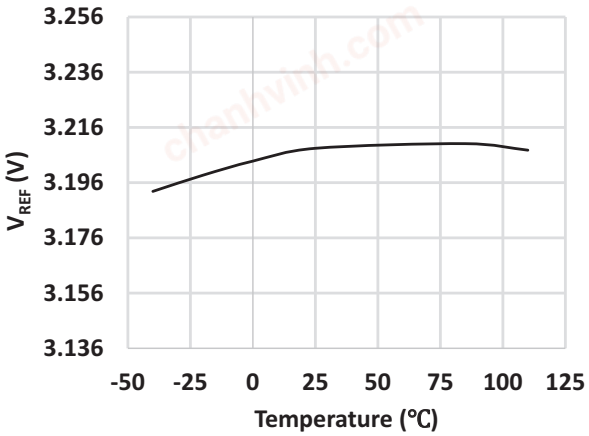



**Figure 8: SNR vs. Temperature**

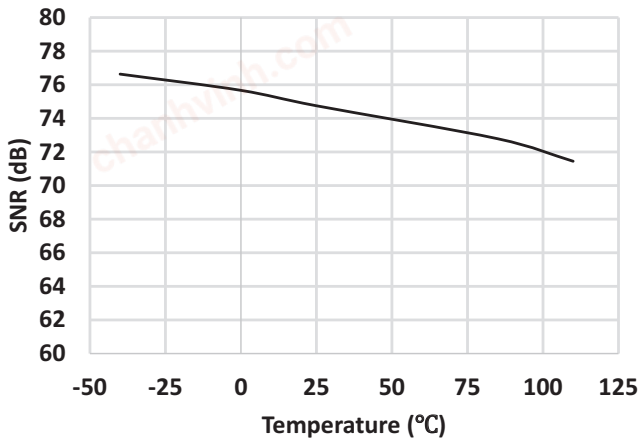



**Figure 9: SNDR vs. Temperature**

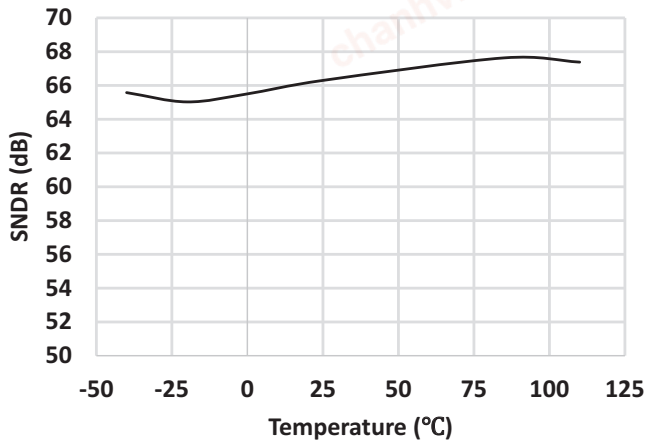



**Figure 10: $I_{DD1}$ vs. $V_{IN}$ DC Input at Various Temperatures**

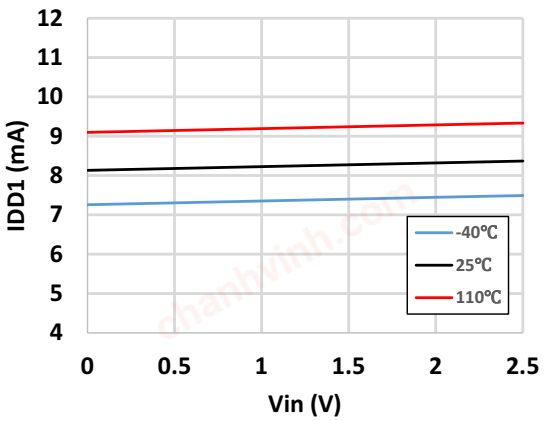
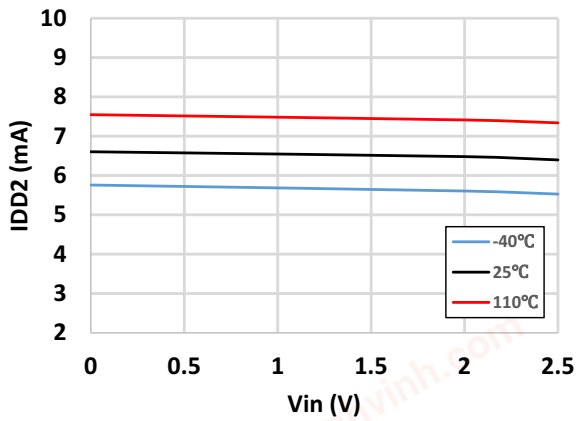



**Figure 11: $I_{DD2}$ ($V_{DD2}$ = 5V) vs. $V_{IN}$ DC Input at Various Temperatures**



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**Figure 12: $I_{DD2}$ ($V_{DD2}$ = 3.3V) vs. $V_{IN}$ DC Input at Various Temperatures**

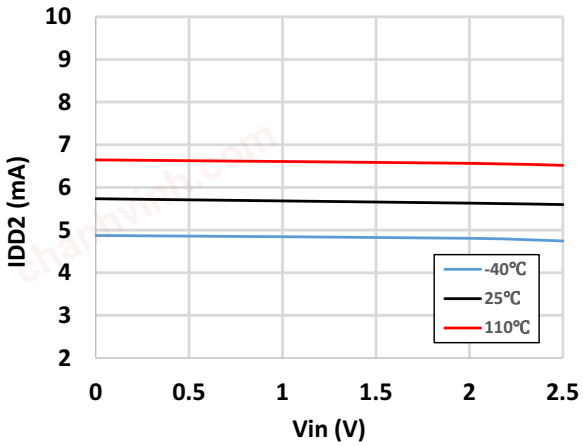
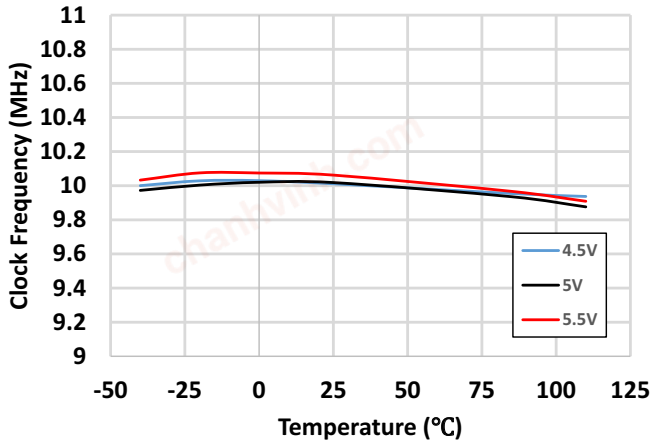



**Figure 13: Clock Frequency vs. Temperature for Various $V_{DD1}$**



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# Definitions

## Integral Nonlinearity (INL)

INL is the maximum deviation of a transfer curve from a straight line passing through the endpoints of the ADC transfer function, with offset and gain errors adjusted out.

## Differential Nonlinearity (DNL)

DNL is the deviation of an actual code width from the ideal value of 1 LSB between any two adjacent codes in the ADC transfer curve. DNL is a critical specification in closed-loop applications. A DNL error of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

## Offset Error

Offset error is the deviation of the actual input voltage corresponding to the mid-scale code (32,768 for a 16-bit system with an unsigned decimation filter) from 0V. Offset error can be corrected by software or hardware.

## Gain Error

Gain error is deviation of actual $V_{REF}$ from ideal $V_{REF}$. The actual $V_{REF}$ is derived from full-scale positive differential input voltage multiplies by the best fit-line gain. The best fit-line gain is the linear gain covering the entire linear-scale differential input range from 0V to 2V. Gain error can be corrected by software or hardware.

*Actual $V_{REF}$ = Full-Scale Positive Differential Input x Best Fit-Line Gain*

*Gain Error (%) = [Actual $V_{REF}$/Ideal $V_{REF}$] – 1 (%)*

## Signal-to-Noise Ratio (SNR)

The SNR is the measured ratio of AC signal power to noise power below half of the sampling frequency. The noise power excludes harmonic signals and DC.

## Signal-to-(Noise + Distortion) Ratio (SNDR)

The SNDR is the measured ratio of AC signal power to noise plus distortion power at the output of the ADC. The signal power is the rms amplitude of the fundamental input signal. Noise plus distortion power is the rms sum of all non-fundamental signals up to half the sampling frequency (excluding DC).

## Effective Number of Bits (ENOB)

The ENOB determines the effective resolution of an ADC, expressed in bits, defined by ENOB = (SNDR – 1.76) / 6.02.

## Isolation Transient Immunity (CMR)

The isolation transient immunity specifies the minimum rate-of-rise/fall of a common-mode signal applied across the isolation boundary beyond which the modulator clock or data is corrupted.

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# Product Overview

## Description

The ACPL-C877 isolated digital voltage sensor converts an analog input signal into a high-speed (10 MHz typical) single-bit data stream by means of a sigma-delta over-sampling modulator. The time average of the modulator data is directly proportional to the input signal voltage. The modulator uses internal clock of 10 MHz. The modulator data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information is represented by the density of ones in the data output.

The other main function of the modulator (optocoupler) is to provide galvanic isolation between the analog signal input and the digital data output. It provides high noise margins and excellent immunity against isolation-mode transients that allows direct measurement of low-level signals in highly noisy environments, for example measurement of motor bus voltage in power inverters.

With 0.5-mm minimum DTI, the ACPL-C877 provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive- or magnetic-coupling with DTI in micro-meter range. Offered in an SSO-8 package, the isolated ADC delivers the reliability, small size, superior isolation and over-temperature performance motor drive designers need to accurately measure voltage.

## Analog Input

The ACPL-C877 front-end contains a fully-differential amplifier followed by a sigma-delta modulator. The fully-differential analog inputs accept signals of 0V to 2V (full scale from -0.1V to 3.2V), which is ideal for direct connection to resistive divider network for voltage sensing or other high-level signal sources applications such as motor drive DC-link bus voltage sensing and insulation resistance voltage measurement usually used together with Broadcom® ASSR-601J high voltage photo-mosfet relay. Users are able to use higher input range from 2V to 3.2V, as long as within full-scale range (3.2V), for the purpose of over-voltage or overload detection.

## Latch-up Consideration

Latch-up risk of CMOS devices needs careful consideration, especially in applications with direct connection to signal source that is subject to frequent transient noise. The analog input structure of the ACPL-C877 is designed to be resilient to transients and surges, which are often encountered in highly noisy application environments such as motor drive and other power inverter systems. Other situations could cause transient voltages to the inputs include short circuit and overload conditions. The ACPL-C877 is tested with DC voltage of up to –2V and 2-second transient voltage of up to –6V to the analog inputs with no latch-up or damage to the device.

## Modulator Data Output

Input signal information is contained in the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 14. A differential input signal of 0V ideally produces a data stream of ones and zeros in equal densities. A differential input of 2V corresponds to 81.25% density of ones. A differential input of 3.2V or higher results in ideally all ones in the data stream, while input less than -0.1V is not defined. Table 3 shows this relationship.

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**Figure 14: Modulator Output vs. Analog Input**

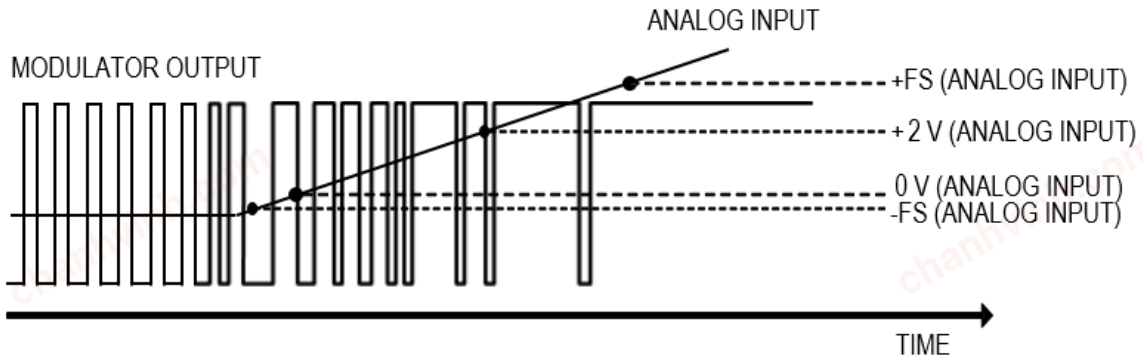



**Table 3: Input Voltage with Ideal Corresponding Density of 1s at Modulator Data Output, and ADC Code**

| Analog Input | Voltage Input | Density of 1s | ADC Code (16-bit Unsigned Decimation) |
|---|---|---|---|
| +Full-Scale | +3.2 V | 100% | 65,535 |
| +Recommended Input Range | +2 V | 81.25% | 53,248 |
| Zero | 0 V | 50% | 32,768 |
| –Full-Scale | –0.1 V | 48.438% | 31,744 |

**NOTE:**

1. With bipolar offset binary coding scheme, the digital code begins with digital 31,744 at -0.1V input and increases proportionally to the analog input until the full-scale code is reached at the +FS input. Input voltage < -0.1V, the output saturates close to –FS.
2. Ideal density of 1s at modulator data output can be calculated with $V_{IN}$/6.4 V + 50%; similarly, the ADC code can be calculated with ($V_{IN}$/6.4 V) × 65,536 + 32,768, assuming a 16-bit unsigned decimation filter.

## Digital Filter

A digital filter converts the single-bit data stream from the modulator into a multi-bit output word similar to the digital output of a conventional A/D converter. With this conversion, the data rate of the word output is also reduced (decimation). A $Sinc^3$ filter is recommended to work together with the ACPL-C877. With 256 decimation ratio and 16-bit word settings, the output data rate is 39 kHz (= 10 MHz/256). This filter can be implemented in an ASIC, an FPGA or a DSP. Some of the ADC codes with corresponding input voltages are shown in Table 3.

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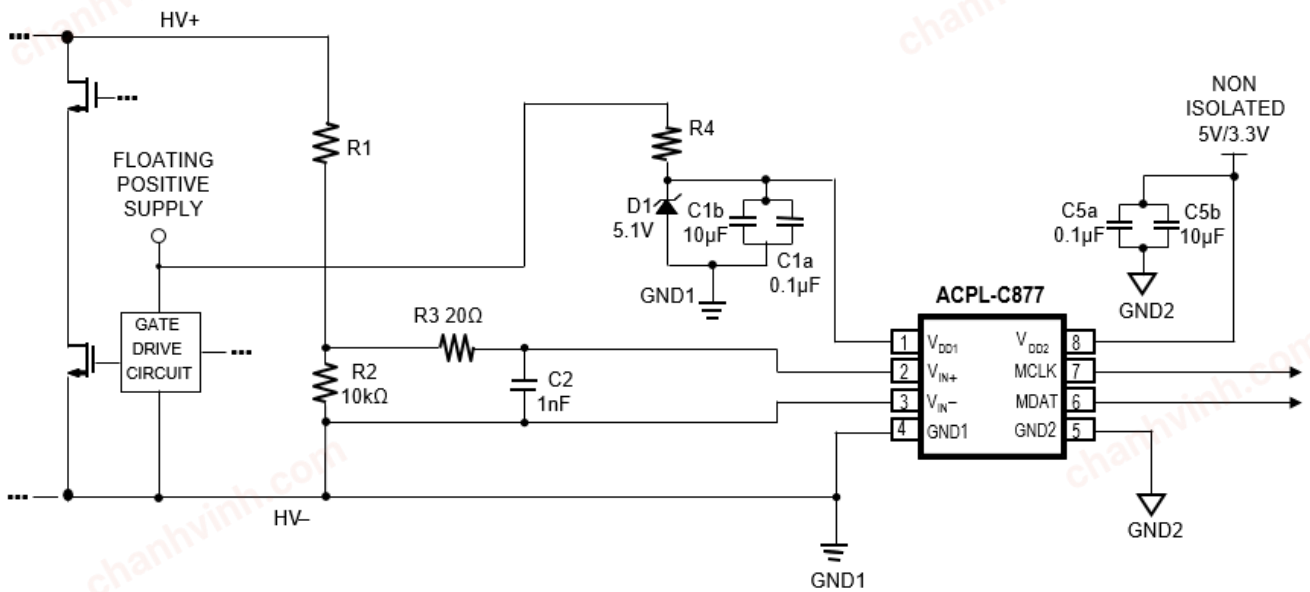


# Application Information

## Typical Application Circuit

Figure 15 shows a typical application circuit for motor control bus voltage sensing. By choosing the appropriate voltage divider network, a wide range of voltage can be monitored.

**Figure 15: Typical Application Circuit in Motor Bus Voltage Setting**




## Measurement Accuracy and Power Dissipation of the Resistive Voltage Divider

The effective input resistance, $R_{eff}$ of the typical application circuit in Figure 15, is made up of sense resistor, $R_2$ and the input resistance of the ACPL-C877, $R_{in}$. That creates a current divider that will result in an additional measurement error factor, $\varepsilon_{rin}$ on top of the device gain error.

$$R_{eff} = R_2 // R_{in} = \frac{R_2 \times R_{in}}{R_2 + R_{in}}$$

$$\varepsilon_{rin} = 1 - \frac{R_{eff}}{R_2}$$

With $R_{in}$ of 1 GΩ for ACPL-C877, this additional measurement error is negligible for $R_2$ up to 1 MΩ, where the error is approximately 0.1%. This error can be further reduced to 0.01% if $R_2$ is selected to be 100 kΩ or 0.001% for a 10 kΩ sense resistor. However, the drawback of using a lower value sense resistor is higher power dissipation in the voltage divider resistor network.

For example, for a 600Vdc bus, $R_1$ is selected to be 2.99 MΩ if $R_2$ is 10 kΩ. Likewise, $R_1$ will be 29.9 MΩ if $R_2$ is 100 kΩ. Without considering $R_{in}$ of ACPL-C877, the power dissipation of the voltage divider resistor network is 120 mW for $R_1$ + $R_2$ combination of 2.99 MΩ + 10 kΩ.

$$2V = \left(\frac{R_2}{R_1 + R_2}\right) 600V$$

$$R_1 = 299 \times R_2$$

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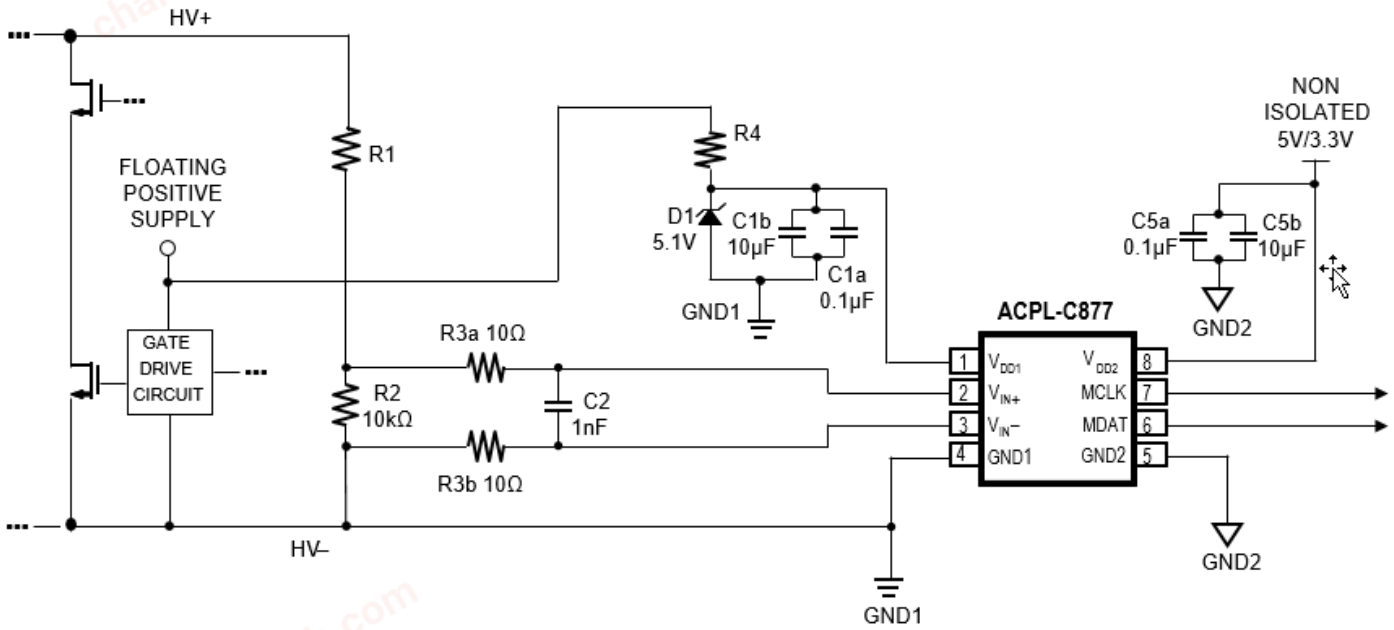
## Voltage Divider Resistor Connections

The recommended method for connecting the isolated modulator to the shunt resistor is shown in Figure 15. $V_{IN+}$ of the ACPL-C877 is connected to the positive terminal of the sense resistor, R2, while $V_{IN-}$ is shorted to GND1, with the power-supply return path functioning as the sense line to the negative terminal of the sense resistor. This allows a single pair of wires or PC board traces to connect the isolated modulator circuit to the sense resistor. By referencing the input circuit to the negative side of the resistor, any load current induced noise transients on the resistor are seen as a common-mode signal and will not interfere with the voltage sense signal.

If the same power supply is used both for the gate drive circuit and for the voltage sensing circuit, it is very important that the connection from GND1 of the isolated modulator to the sense resistor be the only return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolated modulator circuit and the gate drive circuit should be the positive power supply line.

In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting $V_{IN+}$ and $V_{IN-}$ directly across the sense resistor with two conductors, and connecting GND1 to the shunt resistor with a third conductor for the power-supply return path, as shown in Figure 16. The input currents induced by the common-mode of the fully differential amplifier on both of the pins are balanced on the filter resistors, R3a and R3b, and cancelled out each other. Any noise induced on one pin will be coupled to the other pin by the capacitor C2 and creates only common mode noise which is rejected by the device. When connected this way, both input pins should be bypassed. To minimize electromagnetic interference of the sense signal, all of the conductors (whether two or three are used) connecting the isolated modulator to the sense resistor should be either twisted pair wire or closely spaced traces on a PC board.

**Figure 16: Schematic for Three Conductor Shunt Connection**



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The shunt resistor, R2 together with R3 in Figure 15 or R3a and R3b in Figure 16, which are in series with the input leads form a low pass anti-aliasing filter with the input bypass capacitor C2. These resistors perform another important function as well; to dampen any ringing, which might be present in the circuit formed by the shunt, the input bypass capacitor, and the inductance of wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

With a relatively large shunt resistor, R2 value of 10 kΩ, the low pass filter that forms at the input of ACPL-C877 can be assumed to comprise only the R2 and C2 of both recommended application circuits in Figure 15 and Figure 16. The bandwidth can be estimated as

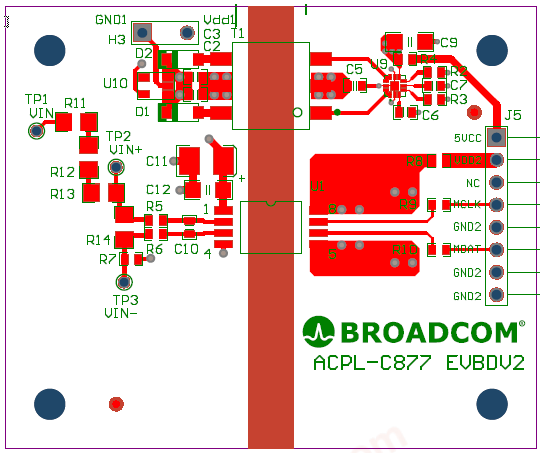
$$f3dB = \frac{1}{2\pi R2C2}$$

For DC voltage sensing, C2 can remain at 1nF, which will result in bandwidth of 16 kHz. For AC voltage sensing and also to capture transient voltages, the R2 and C2 capacitor values needs to be adjusted such that the bandwidth of the low pass filter is at least 20 times wider than the intended voltage sensing frequency so that the input signal into ACPL-C877 is not distorted.

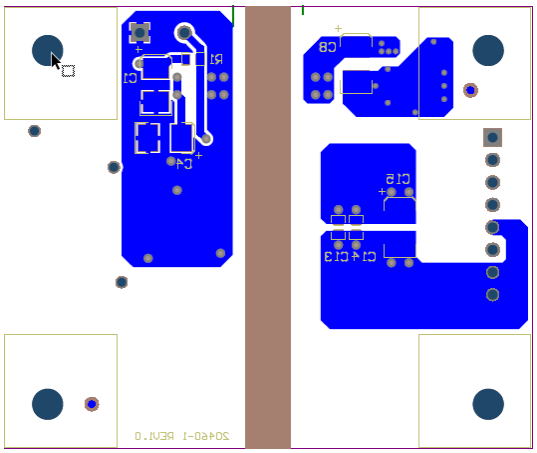
## PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, and so on. In addition, the layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

**Figure 17: An Example of Good PCB Layout for ACPL-C87**




Top Layer



Bottom Layer

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