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BROADCOM®

Data Sheet

ACPL-C87AT/ACPL-C87BT

Automotive High Precision DC Voltage Isolation Sensor

Description

The Broadcom® ACPL-C87AT/C87BT isolation sensors utilize superior optical coupling technology, with sigma-delta (Σ-Δ) analog-to-digital converter, chopper stabilized amplifiers, and a fully differential circuit topology to provide unequaled isolation-mode noise rejection, low offset, high gain accuracy and stability.

ACPL-C87AT (±1% gain tolerance) and ACPL-C87BT (±0.5% gain tolerance) are designed for high precision DC voltage sensing in electronic motor drives, DC/DC and AC/DC converter and battery monitoring system. The ACPL-C87AT/C87BT features high input impedance and operate with full span of analog input voltage up to 2.46V. The shutdown feature provides power saving and can be controlled from external source, such as microprocessor.

The high common-mode transient immunity (15 kV/µs) of the ACPL-C87AT/C87BT maintains the precision and stability needed to accurately monitor DC rail voltage in high noise motor control environments. This galvanic safe isolation solution is delivered in a compact, surface mount stretched SO-8 (SSO-8) package that meets worldwide regulatory safety standards.

Broadcom R^2Coupler® isolation products provide the reinforced insulation and reliability needed for critical automotive and high temperature industrial applications.

Features

- Unity gain
- ± 0.5% (ACPL-C87BT) and ± 1% (ACPL-C87AT) gain tolerance @ 25°C
- –0.3 mV Input offset voltage
- 0.05% non linearity
- 25 ppm/°C gain drift vs. temperature
- 100 kHz bandwidth
- 0 to 2V nominal input range
- Qualified to AEC-Q100 Grade 1 test guidelines
- Operating temperature: –40°C to +125°C
- Shutdown feature (active high)
- 15 kV/µs common-mode rejection at V_{CM} = 1 kV
- Working voltage, V_{IORM} = 1414 V_{peak}
- Compact, surface mount stretched SO8 package
- Worldwide safety approval:
  - UL 1577 (5000 V_{RMS}/1 minute)
  - CSA
  - IEC/EN/DIN EN 60747-5-5

Applications

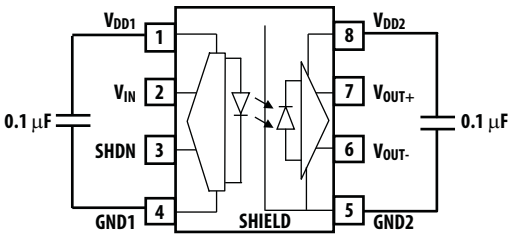
- Automotive BMS battery pack voltage sensing
- Automotive DC/DC converter voltage sensing
- Automotive motor inverter DC bus voltage sensing
- Automotive AC/DC (charger) DC output voltage sensing
- Isolation interface for temperature sensing
- General-purpose voltage sensing and monitoring

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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Functional Diagram

Figure 1: Functional Diagram



A 0.1-µF bypass capacitor must be connected between pin 1 and pin 4, and pin 5 and pin 8 as shown.

Figure 2: Functional Diagram 2

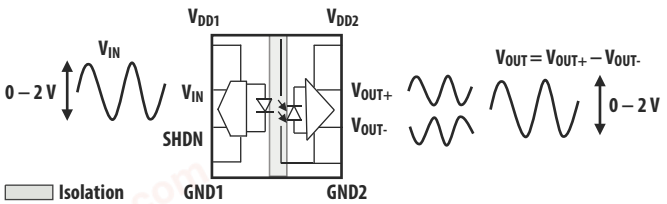
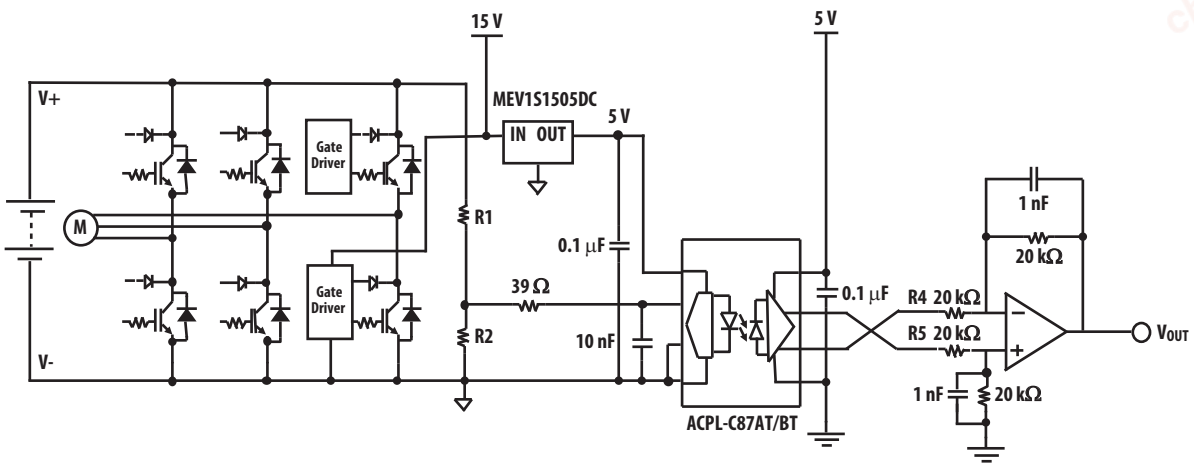
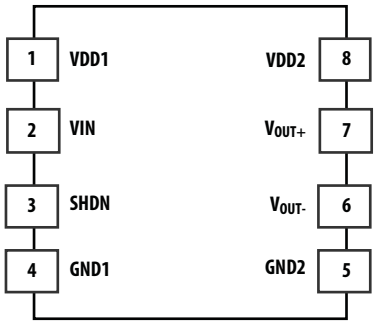


Figure 3: Typical Voltage Sensing Circuit



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Figure 4: Package Pinout



Pin Description

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	V_{DD1}	Input power supply When V_{DD1} = 0, then V_{OUT+} = 0V, V_{OUT-} = 2.6V	8	V_{DD2}	Output power supply
2	V_{IN}	Voltage input, full scale range = 2.46V	7	V_{OUT+}	Positive output voltage
3	SHDN	Shutdown (active high) When active, then V_{OUT+} = 0V, V_{OUT-} = 2.6V	6	V_{OUT-}	Negative output voltage
4	GND1	Input side ground	5	GND2	Output side ground

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	UL 5000 V_{rms} / 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-C87AT	-000E	Stretched SO-8	X		X	X	80 per tube
ACPL-C87BT	-500E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

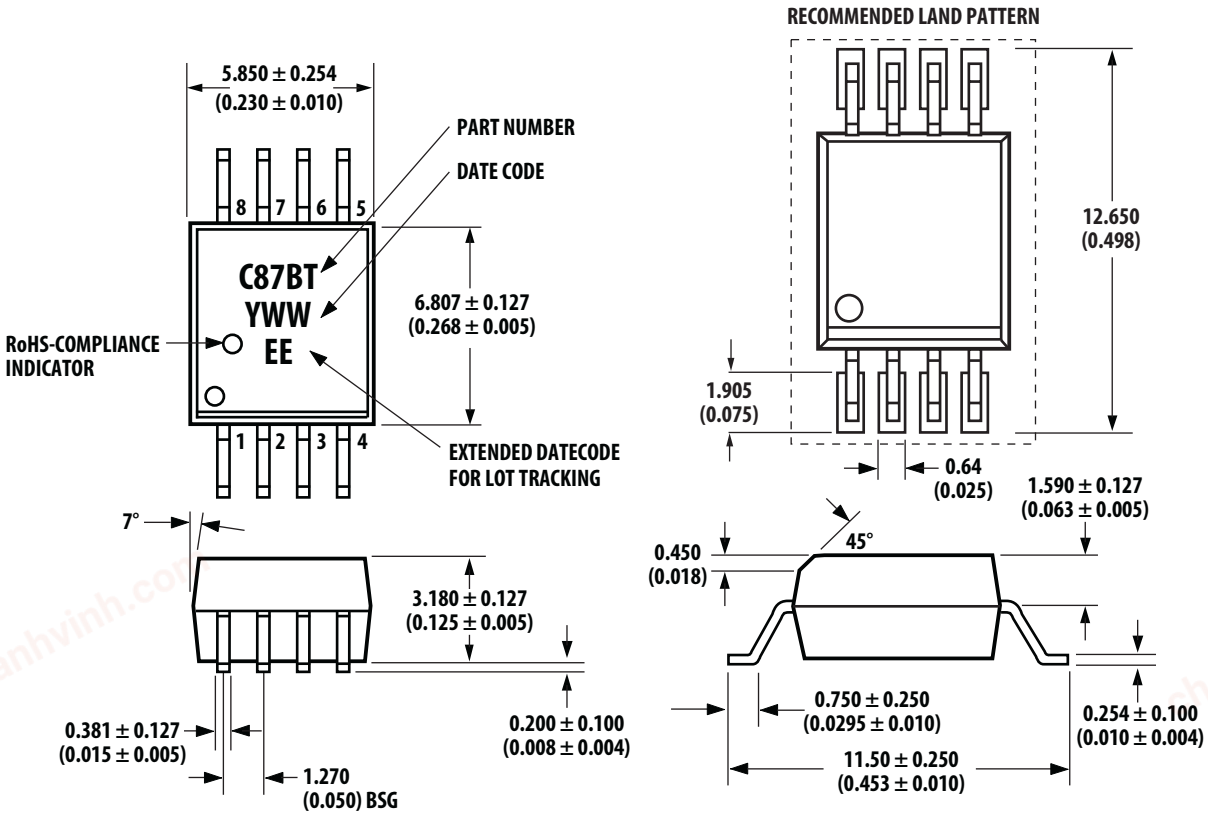
Example:

ACPL-C87AT-500E to order product of SSO-8 Surface Mount package in Tape and Reel packaging with RoHS compliant. Contact your Broadcom sales representative or authorized distributor for information.

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Package Outline Drawing (Stretched SO8)

Figure 5: Package Outline Drawing



Dimensions in millimeters and (inches).

Note:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25mm (10mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Use non-halide flux.

Regulatory Information

The ACPL-C87AT and ACPL-C87BT are approved by the following organizations.

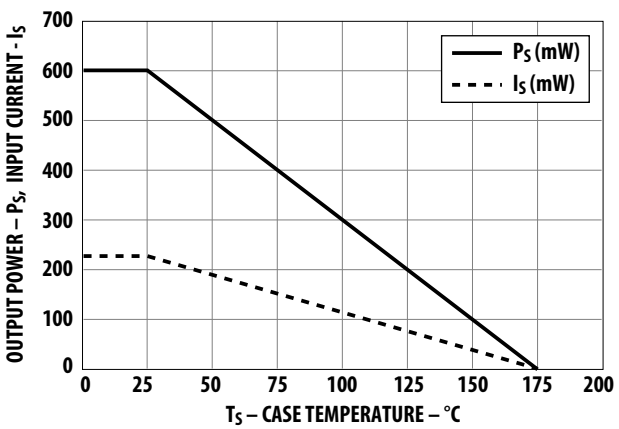
UL	CSA	IEC/EN/DIN EN 60747-5-5
UL 1577, component recognition program up to V_{ISO} = 5kV_{RMS}	Approved under CSA Component Acceptance Notice #5.	IEC 60747-5-5 EN 60747-5-5 DIN EN 60747-5-5

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IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol		Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	
for rated mains voltage ≤ 450 V_{rms}		I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – IV	
for rated mains voltage ≤ 1000 V_{rms}		I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2651	V_{peak}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test with t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure, also see Figure 6.			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	> 10^9	Ω

Figure 6: Dependence of Safety-Limiting Values on Temperature



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Insulation and Safety-Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN BDE0109)		IIIa		Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	150	°C	
Ambient Operating Temperature	T_A	–40	125	°C	
Supply Voltages	V_{DD1}, V_{DD2}	–0.5	6.0	Volts	
Input Voltage	V_{IN}	–2.0	V_{DD1} + 0.5	Volts	
Shutdown Voltage	V_{SD}	–0.5	V_{DD1} + 0.5	Volts	
Output Voltages	V_{OUT+}, V_{OUT-}	–0.5	V_{DD2} + 0.5	Volts	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Ambient Operating Temperature	T_A	-40	125	°C	
Input Supply Voltage	V_{DD1}	4.5	5.5	Volts	
Output Supply Voltage	V_{DD2}	3.0	5.5	Volts	
Input Voltage	V_{IN}	0	2.0	Volts	
Shutdown Voltage	V_{SD}	V_{DD1} – 0.5	V_{DD1}	Volts	

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Electrical Specifications

Unless otherwise noted, all typical values at T_A = 25°C, V_{DD1} = V_{DD2} = 5V, V_{IN} = 0 to 2V, V_{SD} = 0V; all Minimum/Maximum specifications are at recommended voltage supply conditions: 4.5V ≤ V_{DD1} ≤ 5.5V, 4.5V ≤ V_{DD2} ≤ 5.5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Power Supplies								
Input Supply Current	I_{DD1}	—	10.5	15	mA	V_{SD} = 0V	18, 19	
Input Supply Current (Shutdown Mode)	$I_{DD1(SD)}$	—	20	—	µA	V_{SD} = 5V		
Output Supply Current	I_{DD2}	—	6.5	12	mA		18, 20	
DC Characteristics								
Gain (ACPL-C87BT, ± 0.5%)	G0	0.995	1	1.005	V/V	T_A = 25°C, V_{IN} = 0 to 2 V, V_{DD1} = V_{DD2} = 5.0V	8	a
Gain (ACPL-C87AT, ± 1%)	G1	0.99	1	1.01	V/V	T_A = 25°C, V_{IN} = 0 to 2 V, V_{DD1} = V_{DD2} = 5.0V	8, 11	a
Magnitude of Gain Change vs. Temperature	$\lvert dG/dT_A \rvert$	—	25	—	ppm/°C	T_A = -40°C to +125°C	11	
Magnitude of Gain Change vs. V_{DD1}	$\lvert dG/dV_{DD1} \rvert$	—	0.05	—	%/V	T_A = 25°C	12	
Magnitude of Gain Change vs. V_{DD2}	$\lvert dG/dV_{DD2} \rvert$	—	0.02	—	%/V	T_A = 25 °C	12, 13	
Nonlinearity	NL	—	0.05	0.12	%	V_{IN} = 0 to 2V, T_A = –40°C to +125°C	15, 16	
Input Offset Voltage	V_{OS}	–10	-0.3	10	mV	V_{IN} is shorted to GND1, T_A = 25°C	7, 9, 10	
Magnitude of Input Offset Change vs. Temperature	$\lvert dV_{OS}/dT_A \rvert$	—	21	—	µV/°C	V_{IN} is shorted to GND1, T_A = –40°C to +125°C	7, 9	
Inputs and Outputs								
Full-Scale Differential Voltage Input Range	FSR	—	2.46	—	V	Referenced to GND1		
Input Bias Current	I_{IN}	–0.1	-0.001	0.1	µA	V_{IN} = 0V	22	
Equivalent Input Impedance	R_{IN}	—	1000	—	MΩ		22	
Output Common-Mode Voltage	V_{OCM}	—	1.23	—	V	V_{IN} = 0V, V_{SD} = 0V		
VOUT+ Range	V_{OUT+}	—	V_{OCM}+1.23	—	V	V_{IN} = 2.5V		
VOUT - Range	V_{OUT-}	—	V_{OCM} – 1.23	—	V	V_{IN} = 2.5V		
Output Short-Circuit Current	$\lvert I_{OSC} \rvert$	—	30	—	mA	V_{OUT+} or V_{OUT-}, shorted to GND2 or V_{DD2}		
Output Resistance	R_{OUT}	—	36	—	Ω	V_{IN} = 0V		

a. Gain is defined as the slope of the best-fit line of differential output voltage (V_{OUT+} – V_{OUT-}) versus input voltage over the nominal range, with offset error adjusted. A 0.5% gain tolerance for ACPL-C87BT, and a 1% tolerance for ACPL-C87AT.

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Electrical Specifications (Continued)

Unless otherwise noted, all typical values at T_A = 25°C, V_{DD1} = V_{DD2} = 5V, V_{IN} = 0 to 2V, V_{SD} = 0V; all Minimum/Maximum specifications are at recommended voltage supply conditions: 4.5V ≤ V_{DD1} ≤ 5.5V, 4.5V ≤ V_{DD2} ≤ 5.5V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
AC Characteristics								
Small-Signal Bandwidth (–3 dB)	$f_{-3\ dB}$	—	100	—	kHz			
V_{OUT} Noise	N_{OUT}	—	1.3	—	mV_{RMS}	V_{IN} = 2V; BW = 1 kHz	23	a
Input to Output Propagation Delay (10% to 10%)	t_{PD10}	—	2.2	3.5	µs	V_{IN} = 0 to 2V Step	21, 26	
Input to Output Propagation Delay (50% to 50%)	t_{PD50}	—	3.7	6.0	µs	V_{IN} = 0 to 2V Step	21, 26	
Input to Output Propagation Delay (90% to 90%)	t_{PD90}	—	5.3	7.0	µs	V_{IN} = 0 to 2V Step	21, 26	
Output Rise/Fall Time (10% to 90%)	$t_{R/F}$	—	2.7	4.0	µs	Step Input		
Shutdown Time	t_{SD}	—	25	—	µs		25	
Shutdown Recovery Time	t_{ON}	—	150	—	µs		25	
Power Supply Rejection	PSR	—	–78	—	dB	1 Vp-p, 1 kHz sine wave ripple on V_{DD1}, differential output		
Common Mode Transient Immunity	CMTI	10	15	—	kV/µs	V_{CM} = 1 kV, T_A = 25°C	24	b

a. Noise is measured at the output of the differential to single ended post amplifier.

b. Common mode transient immunity (CMTI) is tested by applying a fast rising/falling voltage pulse across GND1 (pin 4) and GND2 (pin 5). The output glitch observed is less than 0.2V from the average output voltage for less than 1 µs.

Package Characteristics

Unless otherwise noted, all typical values are at T_A = 25°C; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	5000	—	—	V_{RMS}	RH < 50%, t = 1 minute, T_A = 25°C		b, c
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 V_{DC}		b
Input-Output Capacitance	C_{I-O}	—	0.5	—	pF	f =1 MHz		b

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.

b. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.

c. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.

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Typical Characteristic Plots and Test Conditions

All ±3σ plots are based on characterization test result at the point of product release. For guaranteed specification, refer to the respective Electrical Specifications section.

Figure 7: Input Offset Voltage Test Circuit

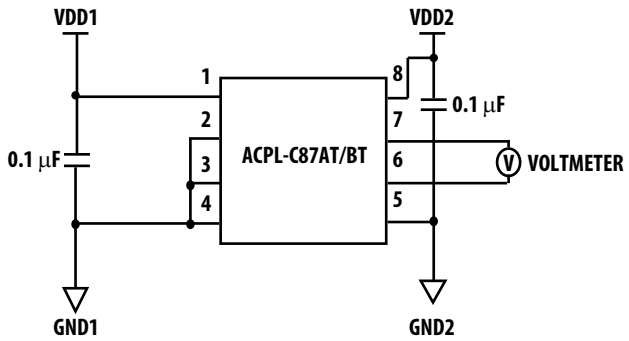


Figure 8: Gain and Nonlinearity Test Circuit

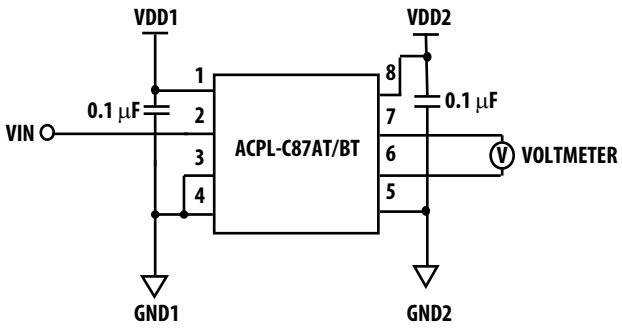


Figure 9: Input Offset Voltage vs. Temperature

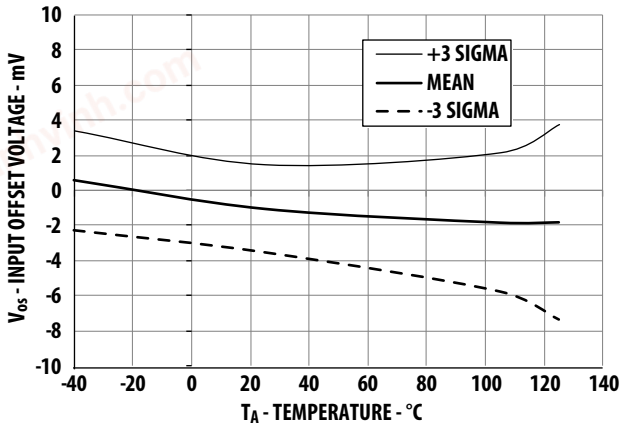


Figure 10: Input Offset vs. Supply Voltage

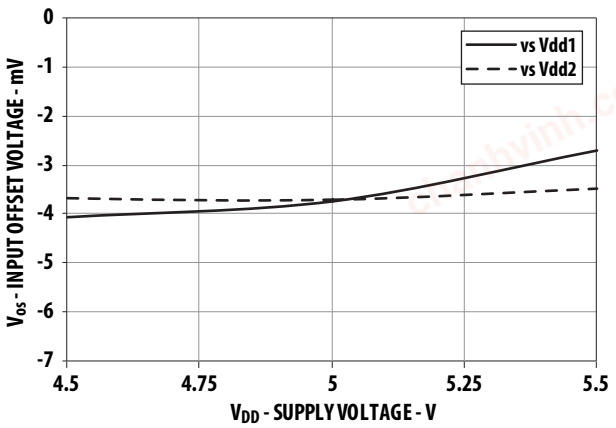


Figure 11: Gain vs. Temperature

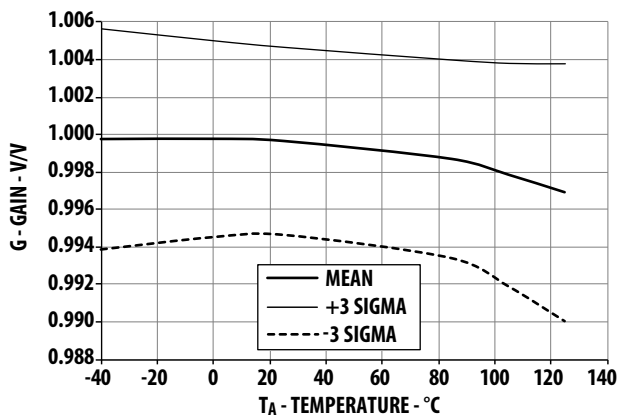
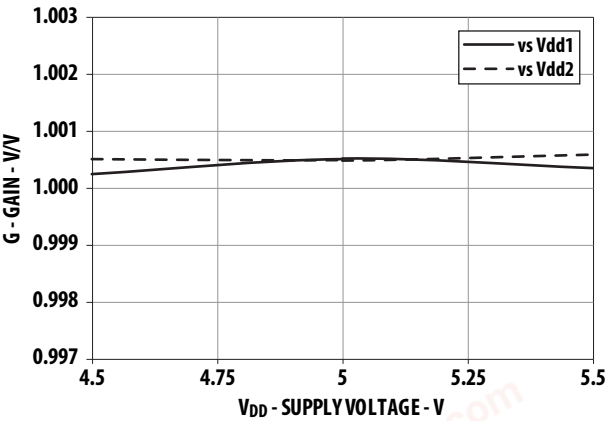


Figure 12: Gain vs. Supply Voltage



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Figure 13: Gain vs Temperature at Different V_{DD2}

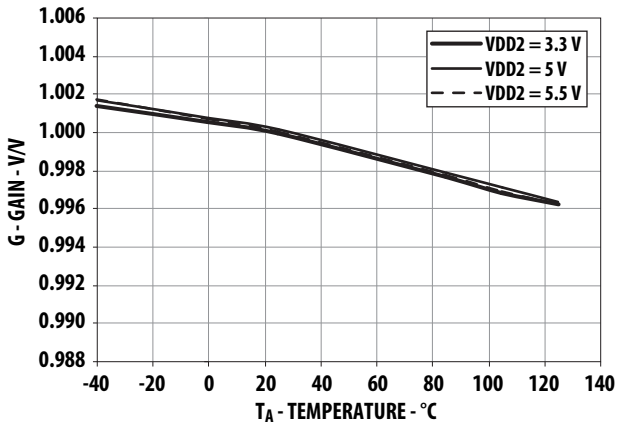


Figure 14: Nonlinearity vs. Supply Voltage

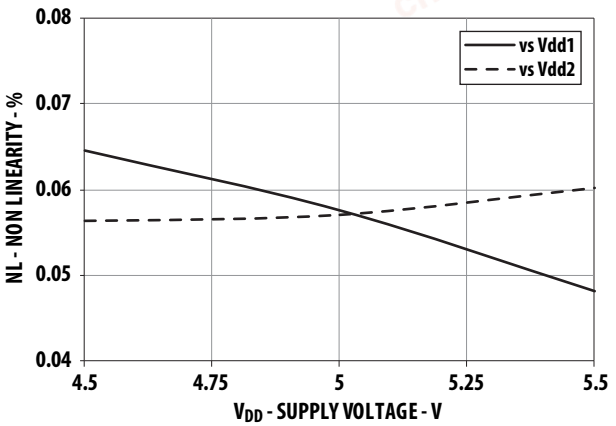


Figure 15: Nonlinearity vs. Temperature

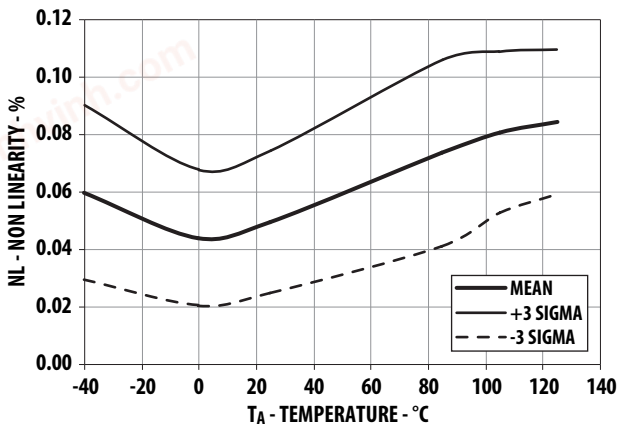


Figure 16: Nonlinearity vs. Temperature at Different V_{DD2}

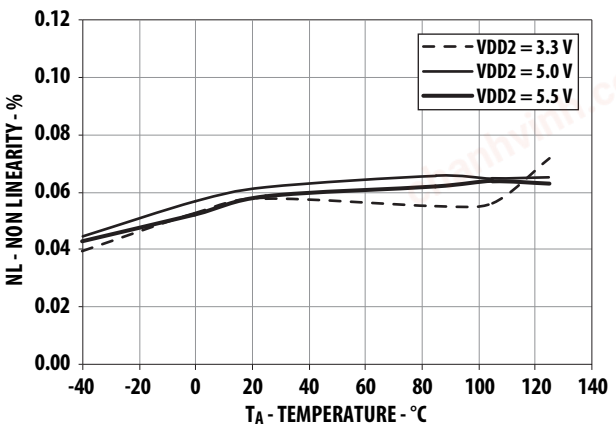


Figure 17: Output Voltage vs. Input Voltage

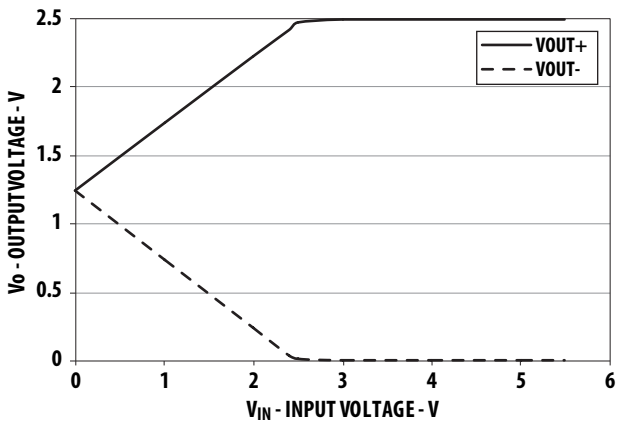
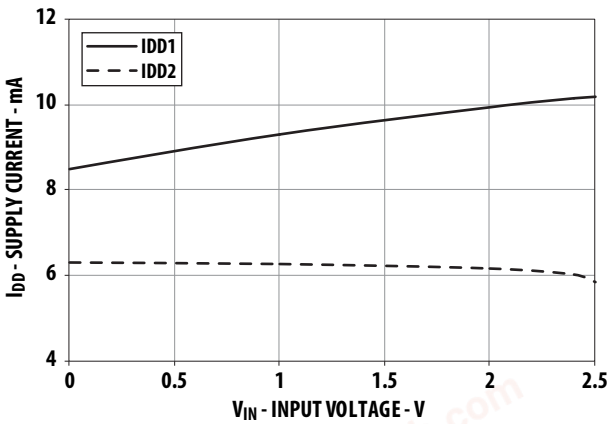


Figure 18: Typical Supply Current vs. Input Voltage



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Figure 19: Typical Input Supply Current vs. Temperature at Different V_{DD1}

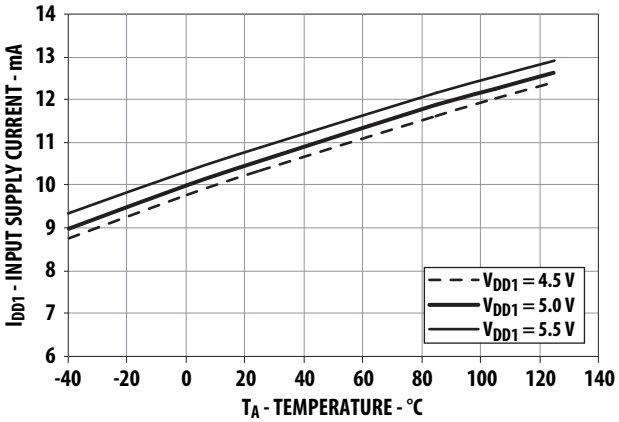


Figure 20: Typical Output Supply Current vs. Temperature at Different V_{DD2}

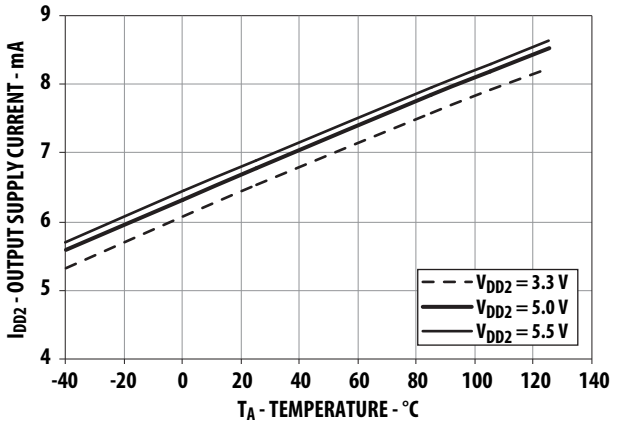


Figure 21: Typical Propagation Delay vs. Temperature

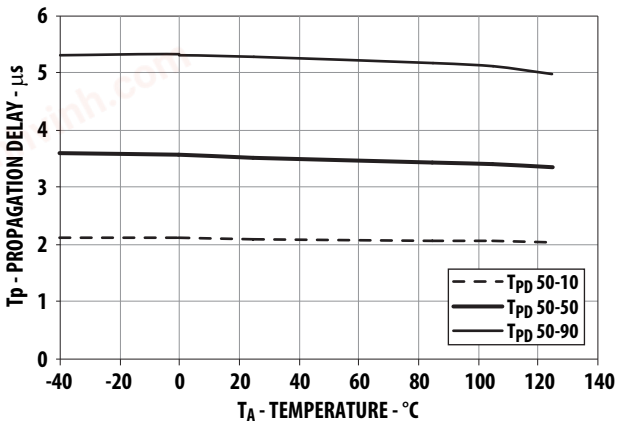


Figure 22: Input Current vs. Input Voltage

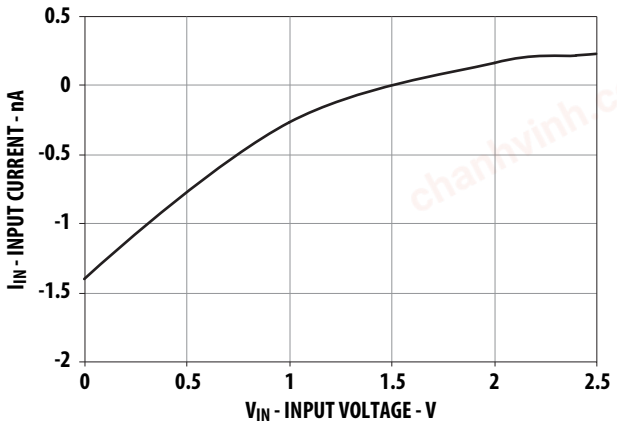


Figure 23: AC Noise vs. Filter Bandwidth

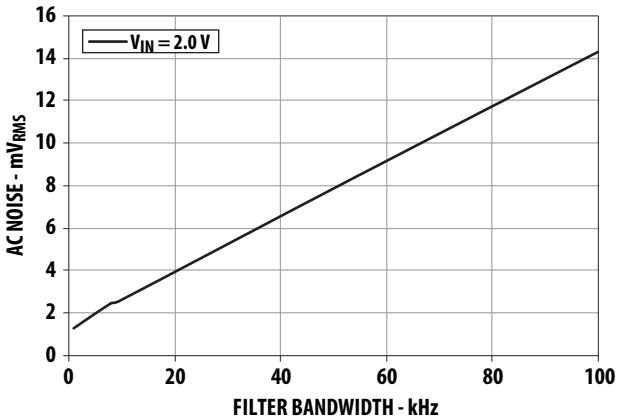
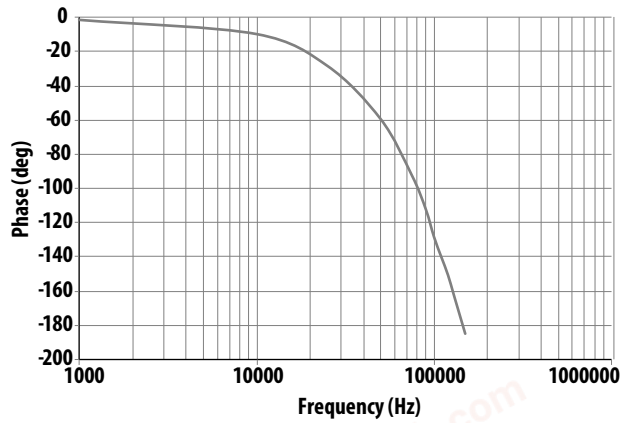


Figure 24: Phase vs. Frequency



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Figure 25: Common Mode Transient Immunity Test Circuit

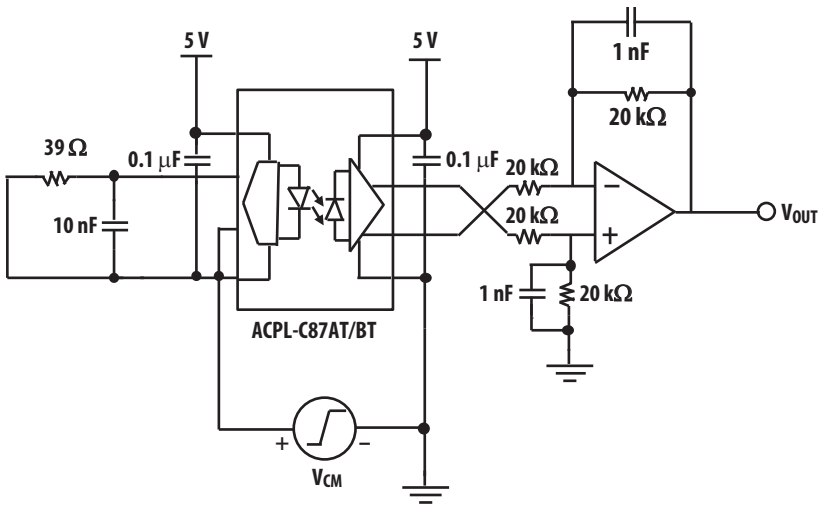


Figure 26: Shutdown Timing Diagram

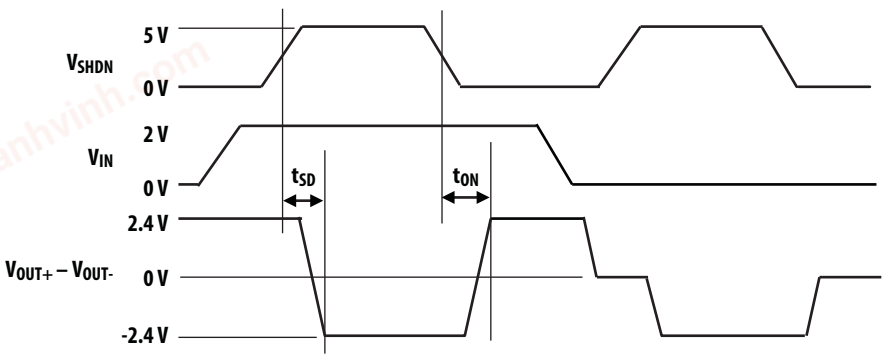
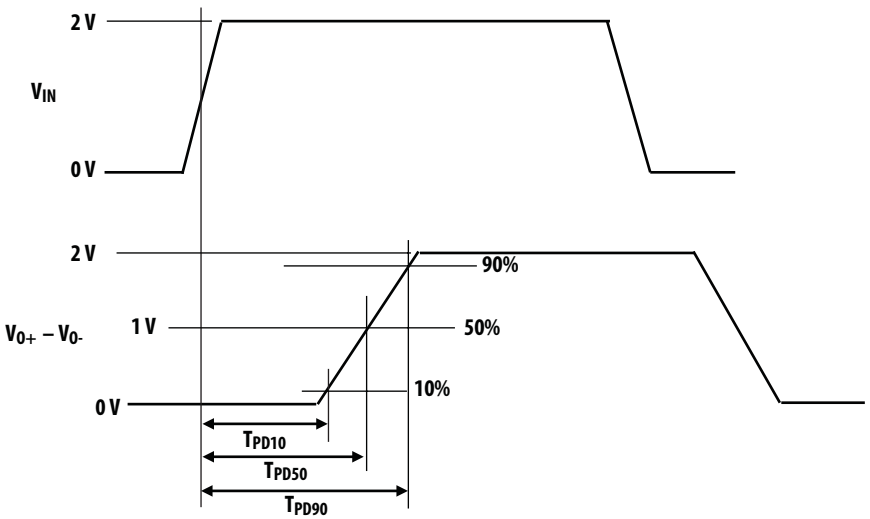


Figure 27: Propagation Delay Diagram



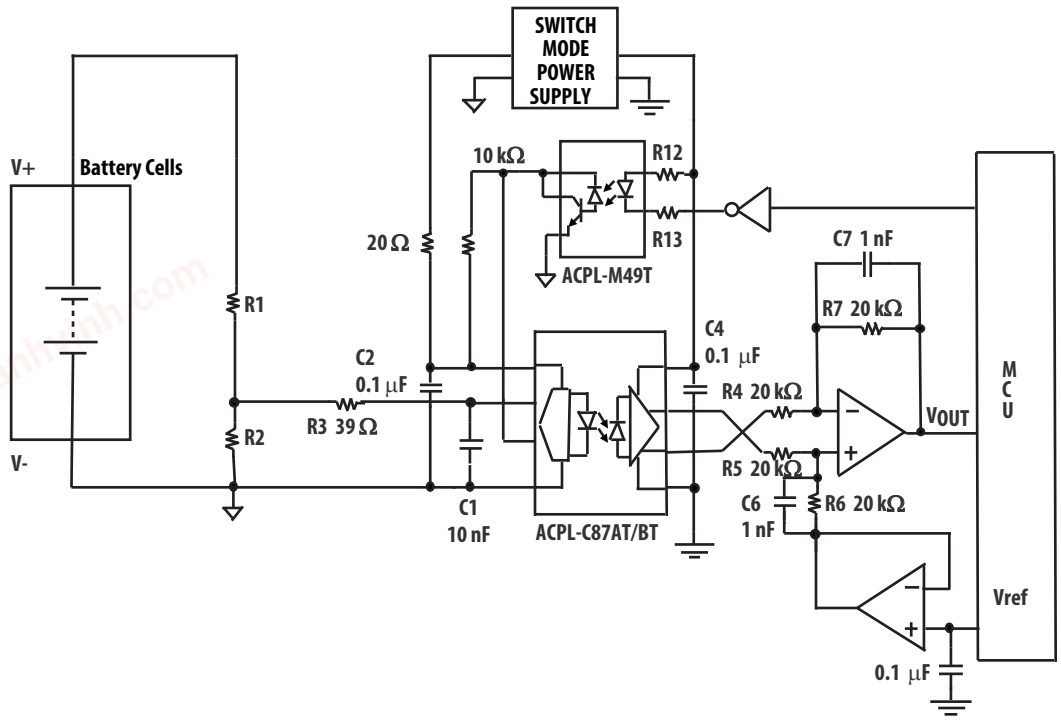
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Application Information

The circuit shown in the Figure 28 is a high voltage sensing application using ACPL-C87AT/BT (isolation amplifier) and ACPL-M49T (optocoupler). The high voltage input is sensed by the precision voltage divider resistors R1 and sensing resistor R2. The ratio of the voltage divider is determined by the allowable input range of the isolation amplifier (0 to 2 V). This small analog input goes through a 39Ω and 10 nF anti aliasing filter (ACPL-C87AT/BT use Σ-Δ modulation).

Inside the isolation amplifier: the analog input signal is digitized and optically transmitted to the output side of the amplifier. The detector will then decode the signal and converted back to analog signal. The output differential signals of ACPL-C87AT/BT go through an op-amp to convert the differential signals to a single ended output.

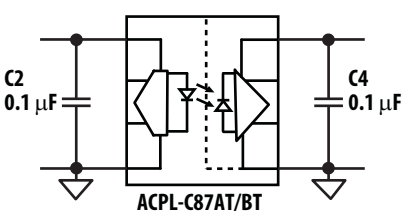
Figure 28: Typical Application Circuit for Battery Voltage Sensing



Bypass Capacitor

A 0.1-µF bypass capacitor must be connected as near as possible between V_{DD1} to GND1 and V_{DD2} to GND2 (Figure 29).

Figure 29: Bypass Capacitors C2, C4



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Anti-aliasing Filter

A 39Ω resistor and a 10-nF capacitor are recommended to be connected to the input (V_{IN}) as anti-aliasing filter because ACPL-C87AT/BT uses sigma data modulation (Figure 30). The value of the capacitor must be greater than 1 nF and bandwidth must be less than 410 kHz.

Figure 30: Anti-aliasing Filter C1, R3

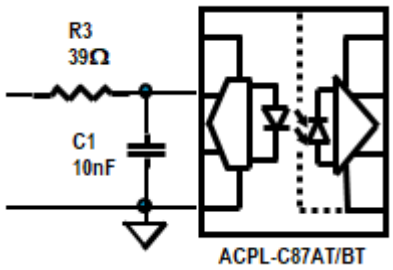
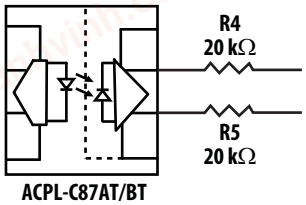


Figure 31: Loading Resistors R4, F5



Designing the Input Resistor Divider

1. Choose the sensing current (Isense) for bus voltage; for example, 1 mA.
2. Determine R2,

$$R_2 = \frac{\text{Voltage input range}}{I_{SENSE}} = \frac{2\ V}{1\ mA} = 2\ k\Omega$$

3. Determine R1 using voltage divider formula:

$$(V+ - V-) \bullet \frac{R_2}{R_1 + R_2} = \text{Voltage input range, or}$$

$$R_1 = \frac{(V+ - V-) \bullet R_2}{\text{Voltage input range}} - R_2$$

where (V+ – V-) is the high voltage input; for example, 0 to 600V,

$$R_1 = \frac{(600\ V - 0\ V) \bullet 2\ k\Omega}{2\ V} - 2\ k\Omega = 598\ k\Omega$$

To reduce the voltage stress of a sole resistor, R1 can be a series of several resistors.

Post Amplifier Circuit

The output of ACPL-C87AT/BT is a differential output (V_{OUT+} and V_{OUT-} pins). A post amplifier circuit is needed to convert the differential output to single ended output with a reference ground. The post amplifier circuit can also be configured to establish a desired gain if needed. It also functions as filter to high frequency chopper noise. The bandwidth can be adjusted by changing the feedback resistor and capacitor (R7 and C7). Adjusting this bandwidth to a minimum level helps minimize the output noise.

Post op-amp resistive loading (R4, R5) should be equal or greater than 20 kΩ (Figure 31). Resistor values lower than this can affect the overall system error due to output impedance of isolation amplifier.

The application circuit in Figure 28 features two op-amps to improve the linearity at voltage near 0V caused by the limited headroom of the amplifier. The second op-amp can set the reference voltage to above 0V.

Shutdown Function

ACPL-C87AT/BT has a shutdown function to disable the device and make the output ($V_{OUT+} - V_{OUT-}$) low. A voltage of 5V on SHDN pin will shutdown the device producing an output ($V_{OUT+} - V_{OUT-}$) of –2.6V. To be able to control the SHDN function (example, from microprocessor), an optocoupler (ACPL-M49T) is used.

Total System Error

Total system error is the sum of the resistor divider error, isolation amplifier error and post amplifier error. The resistor divider error is due to the accuracy of the resistors used. It is recommended to use high accuracy resistor of 0.1%. Post amplifier error is due to the resistor matching and the voltage offset characteristic which can be found on the supplier data sheet.

Isolation Amplifier Error is shown in the following table.

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Isolation Amplifier Error Calculation

			3σ Distribution or Specification[a]			
		Typical	ACPL-C87AT	ACPL-C87BT		Figure
A	Error due to offset voltage (25°C)	0.015%	0.5%	0.5%	Offset Voltage /Recommended input voltage range (2.0V)	specs
B	Error due to offset voltage drift (across temperature)	0.1%	0.4%	0.4%	Offset Voltage /Recommended input voltage range (2.0V)	
C	Error due to gain tolerance (25°C)	0%	1%	0.5%		specs
D	Error due to gain drift (across temperature)	0.25%	0.8%	0.8%		
E	Error due to Nonlinearity (across temperature)	0.05%	0.12%	0.12%		
F	**Total uncalibrated error (A+B+C+D+E)**	0.415%	2.82%	2.32%		specs
G	**Total offset calibrated error (F – A)**	0.4%	2.32%	1.82%		
H	**Total gain and offset calibrated error (G – C)**	0.4%	1.32%	1.32%		

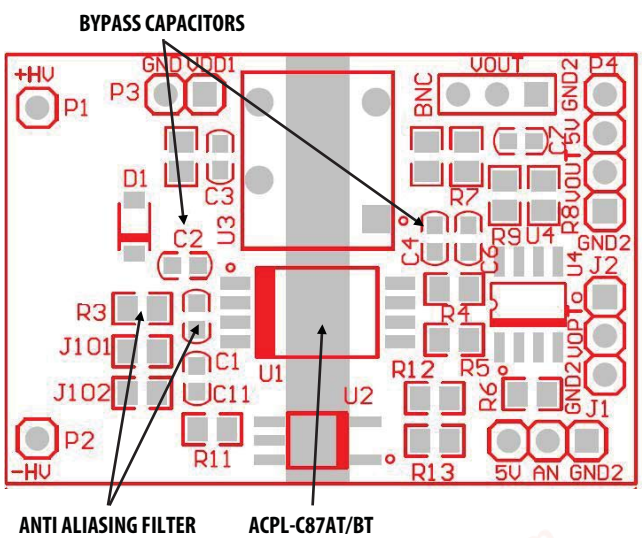
a. 3σ distribution is based on corner wafers.

PCB Layout Recommendations

Bypass capacitor C2 and C4 must be located close to ACPL-C87xT Pins 1 and Pin 8 respectively. Grounded pins of C4 and C5 can be connected by vias through the respective ground layers. If the design has multiple layers, a dedicated layer for ground is recommended for flexibility in component placement.

Anti aliasing filters R3 and C1 also need to be connected as close as possible to Pin 2 of ACPL-C87AT/BT. See Figure 32 for actual component placement of the anti-aliasing filter and bypass capacitors.

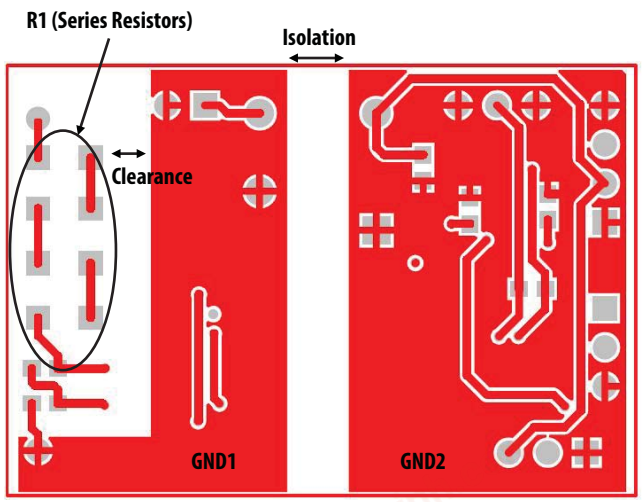
Figure 32: Component Placement Recommendation



GND1 and GND2 must be totally isolated in the PCB layout (Figure 33). Distance of separation depends on the high voltage level of the equipment. The higher the voltage level, the larger the distance of separation needed. Designers can refer to specific IEC standard of their equipment for the creepage/clearance requirements.

R1, which is directly connected to the high voltage input, must have sufficient clearance with the low voltage components. Clearance depends on the high voltage level of the input. Designers can refer to specific IEC standards of their equipment for the clearance requirements.

Figure 33: Bottom Layer Layout Recommendation



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