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Data Sheet

# ACPL-C799U

## ±50 mV Optically Isolated Sigma-Delta Modulator With Wide Operating Temperature

## Description

The Broadcom® ACPL-C799U is a 1-bit, second-order sigma-delta (Σ–Δ) modulator that converts an analog input signal into a high-speed data stream with galvanic isolation based on optical coupling technology. The ACPL-C799U operates from a 5V power supply with dynamic range of 77 dB with an appropriate digital filter. The differential inputs of ±50 mV (full scale ±80 mV) are ideal for direct connection to shunt resistors or other low-level signal sources in applications such as motor phase current measurement.

The analog input is continuously sampled by a means of sigma-delta oversampling using an in-built clock. The signal information is contained in the modulator data, as a density of ones with data rate of 10 MHz, and the data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter. The serial interface for the data and clock has a wide supply range of 3V to 5.5V.

Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With 0.5 mm minimum distance through insulation (DTI), the ACPL-C799U provides reliable reinforced insulation and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive- or magnetic-coupling with DTI in micrometer range. Offered in a Stretched SO-8 (SSO-8) package, the isolated ADC delivers the reliability, small size, superior isolation, and overtemperature performance motor drive designers need to accurately measure current at much lower price compared to traditional current transducers.

## Features

- 1-bit, second-order sigma-delta modulator
- 10-MHz internal clock
- 16-bit resolution no missing codes (12 bits ENOB)
- Signal-to-Noise Ratio: 77 dB Typ.
- Compact, surface-mount SSO-8 package
- Superior optical isolation and insulation
- Common-mode transient immunity: 25 kV/µs
- Safety and regulatory approval:
  - IEC/EN/DIN EN 60747-5-5: 1414 $V_{PEAK}$ working insulation voltage
  - UL 1577: 5000 $V_{RMS}$/1 minute isolation voltage
  - CAN/CSA-C22.2 No. 62368-1

## Specifications

- Wide operating temperature range: –40°C to +125°C
- Gain error: ±1%
- Offset drift: ±1.3 µV/°C maximum
- ±50 mV linear range with single 5V supply (±80 mV full-scale)
- Wide supply range for digital interface: 3V to 5.5V

## Applications

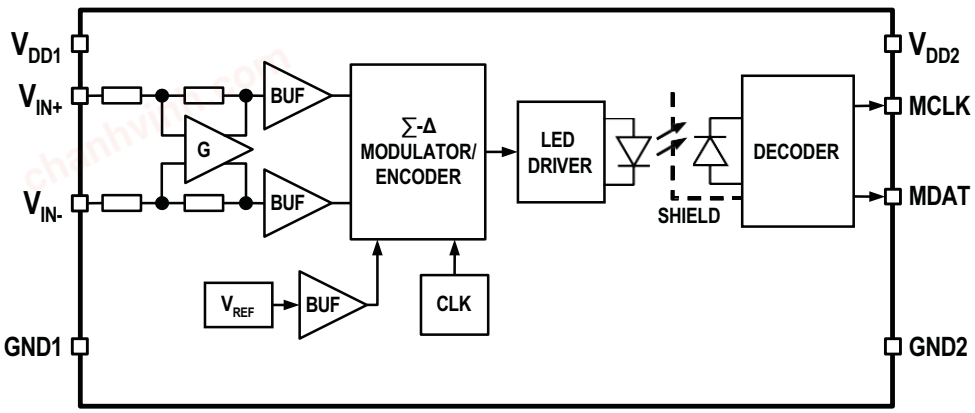
- Motor phase and rail current sensing
- Power inverter current sensing
- Industrial process control
- Data acquisition systems
- General purpose current sensing
- Traditional current transducer replacements

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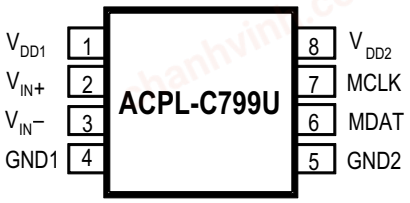
# Schematic Diagram

**Figure 1: Schematic Diagram**




# Pin Configuration and Descriptions

**Figure 2: Pin Configuration**




# Pin Descriptions

**Table 1: Pin Descriptions**

| Pin Number | Symbol | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply voltage for signal input side (analog side), relative to GND1 |
| 2 | $V_{IN+}$ | Positive analog input, recommended input range ± 50 mV |
| 3 | $V_{IN–}$ | Negative analog input, recommended input range ± 50 mV |
| 4 | GND1 | Supply ground for signal input side |
| 5 | GND2 | Supply ground for data/clock output side (digital side) |
| 6 | MDAT | Modulator data output |
| 7 | MCLK | Modulator clock output |
| 8 | $V_{DD2}$ | Supply voltage for data output side, relative to GND2 |

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# Ordering Information

**Table 2: Ordering Information**

| Part Number | Option (RoHS Compliant) | Package | Surface Mount | Tape and Reel | UL 5000 VRMS / 1 Minute Rating | IEC/EN/DIN EN 60747-5-5 | Quantity |
|---|---|---|---|---|---|---|---|
| ACPL-C799U | -000E | Stretched SO-8 | X | — | X | X | 80 per tube |
| | -500E | | X | X | X | X | 1000 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example:

ACPL-C799U-500E to order product of Surface Mount package in Tape and Reel packaging with RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

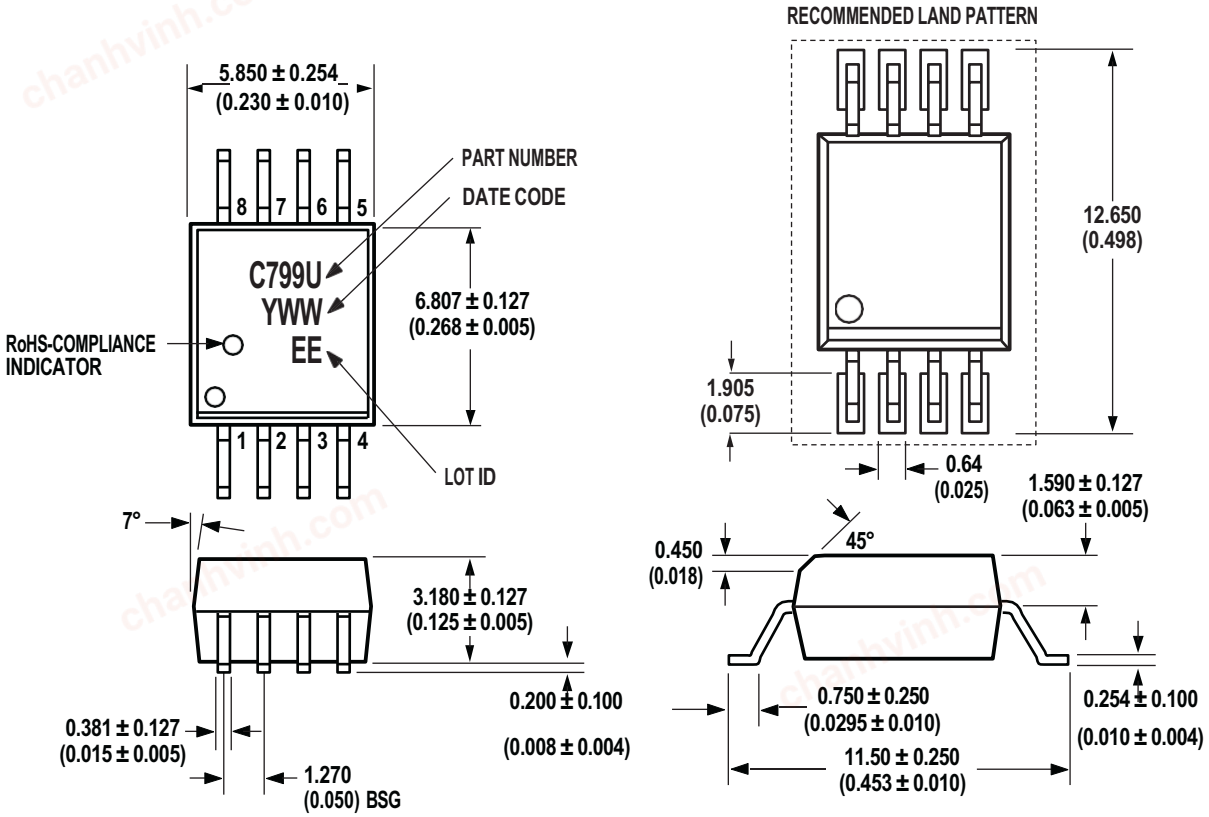
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# Package Outline Drawings

## Stretched SO-8 Package (SSO-8)

**Figure 3: Package Outline Drawing**




Dimensions in millimeters and (inches).

Notes:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25 mm (10 mils) max.

# Recommended PB-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

# Regulatory Information

The ACPL-C799U is approved by the following organizations.

**Table 3: Regulatory Information**

| | |
|---|---|
| IEC/EN/DIN EN 60747-5-5 | Approval with Maximum Working Insulation Voltage $V_{IORM}$ = 1414 $V_{PEAK}$. |
| UL | Approval under UL 1577, component recognition program up to $V_{ISO}$ = 5000 $V_{RMS}$/1 minute. File E55361. |
| CSA | Approval under CAN/CSA-C22.2 No. 62368-1. |

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# IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

**Table 4: IEC/EN/DIN EN 60747-5-5 Insulation Characteristics**

| Description | Symbol | Value | Units |
|---|---|---|---|
| Installation Classification per DIN VDE 0110/1.89, Table 1 | | | |
| For rates mains voltage ≤ 600 $V_{RMS}$ | — | I-IV | — |
| For rated mains voltage ≤ 1000 $V_{RMS}$ | — | I-III | — |
| Climatic Classification | — | 40/125/21 | — |
| Pollution Degree (DIN VDE 0110/1.89) | — | 2 | — |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 1414 | $V_{PEAK}$ |
| Input to Output Test Voltage, Method b<br>$V_{IORM}$ × 1.875 = $V_{PR}$, 100% Production Test with $t_m$ = 1 second, Partial Discharge < 5 pC | $V_{PR}$ | 2652 | $V_{PEAK}$ |
| Input to Output Test Voltage, Method a<br>$V_{IORM}$ × 1.6 = $V_{PR}$, Type and Sample Test, $t_m$ = 10 seconds, Partial Discharge < 5 pC | $V_{PR}$ | 2262 | $V_{PEAK}$ |
| Highest Allowable Overvoltage (Transient Overvoltage, $t_{ini}$ = 60 seconds) | $V_{IOTM}$ | 8000 | $V_{PEAK}$ |
| Safety-Limiting Values (Maximum values allowed in the event of a failure) | | | |
| Case Temperature | $T_S$ | 175 | °C |
| Input Current[a] | $I_{S,INPUT}$ | 230 | mA |
| Output Power[a] | $P_{S,OUTPUT}$ | 600 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500V | $R_S$ | $\geq 10^9$ | Ω |

a. Transient voltage of 2 seconds up to –6V on the inputs does not cause latch-up or damage to the device.

# Insulation and Safety-Related Specifications

**Table 5: Insulation and Safety-Related Specifications**

| Parameter | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (External Clearance) | L(101) | 8.0 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L(102) | 8.0 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | — | 0.5 | mm | Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity. |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | — | IIIa | — | Material Group (DIN VDE 0110, 1/89, Table 1) |

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# Absolute Maximum Ratings

**Table 6: Absolute Maximum Ratings**

| Parameter | Symbol | Min. | Max. | Units | Note |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | –55 | +150 | °C | — |
| Ambient Operating Temperature | $T_A$ | –40 | +125 | °C | — |
| Supply Voltage | $V_{DD1}$, $V_{DD2}$ | –0.5 | 6.0 | V | — |
| Steady-State Input Voltage | $V_{IN+}$, $V_{IN–}$ | –2 | $V_{DD1}$ + 0.5 | V | a |
| Two-Second Transient Input Voltage | $V_{IN+}$, $V_{IN–}$ | –6 | $V_{DD1}$ + 0.5 | V | b |
| Digital Output Voltages | MCLK, MDAT | –0.5 | $V_{DD2}$ + 0.5 | V | — |
| Lead Solder Temperature | 260°C for 10 seconds, 1.6 mm below seating plane | | | | — |

a. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

b. Transient voltage of 2 seconds up to –6V on the inputs does not cause latch-up or damage to the device.

# Recommended Operating Conditions

**Table 7: Recommended Operating Conditions**

| Parameter | Symbol | Min. | Max. | Units | Note |
|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | –40 | +125 | °C | — |
| $V_{DD1}$ Supply Voltage | $V_{DD1}$ | 4.5 | 5.5 | V | — |
| $V_{DD2}$ Supply Voltage | $V_{DD2}$ | 3 | 5.5 | V | — |
| Analog Input Voltage | $V_{IN+}$, $V_{IN–}$ | –50 | +50 | mV | a |

a. Full scale signal input range ±80 mV.

# Electrical Specifications

All minimum and maximum values are at recommended conditions, unless otherwise noted. All typical values are at $T_A$ = 25°C, $V_{DD1}$ = 5V, $V_{DD2}$ = 5V, tested with a Sinc3 filter and 256 decimation ratio.

**Table 8: Electrical Specifications**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions/Notes | | Figure | Note |
|---|---|---|---|---|---|---|---|---|---|
| Static Characteristics | | | | | | | | | |
| Resolution | — | 16 | — | — | Bits | Decimation filter output set to 16 bits. | | — | — |
| Integral Nonlinearity | INL | –16 | ±8 | 16 | LSB | See Definitions. | | — | — |
| Differential Nonlinearity | DNL | –0.9 | — | 0.9 | LSB | No missing codes, guaranteed by design. See Definitions. | | — | — |
| Offset Error | $V_{OS}$ | –1.0 | 0.1 | 1.0 | mV | $T_A$ = 25°C, $V_{DD1}$ = 5V. Short before anti-aliasing filter. See Definitions. | | 5 | — |
| Offset Error Drift vs. Temperature | $dV_{OS}/dT_A$ | –1.3 | ±0.1 | 1.3 | µV/°C | $V_{DD1}$ = 5V | Short before anti-aliasing filter. See Definitions. | — | a |
| Offset Drift vs. $V_{DD1}$ | $dV_{OS}/dV_{DD1}$ | — | 0.1 | — | mV/V | — | | — | — |

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**Table 8: Electrical Specifications (Continued)**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions/Notes | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| Internal Reference Voltage | $V_{REF}$ | — | 80 | — | mV | — | — | — |
| Reference Voltage Tolerance (Gain Error) | — | –1 | — | 1 | % | $T_A$ = 25°C. See Definitions. | — | — |
| | | –2 | — | 2 | % | $T_A$ = –40°C to +125°C. See Definitions. | 6 | — |
| $V_{REF}$ Drift vs. Temperature | $dV_{REF}/dT_A$ | — | 50 | — | ppm/°C | — | — | — |
| $V_{REF}$ Drift vs. $V_{DD1}$ | $dV_{REF}/dV_{DD1}$ | — | 50 | — | µV/V | — | — | — |
| Analog Inputs | | | | | | | | |
| Full-Scale Differential Voltage Input Range | FSR | — | $V_{REF}$ | — | mV | $V_{IN} = V_{IN+} – V_{IN–}$ | — | b |
| Input Bias Current | $I_{INA}$ | — | –0.2 | — | mA | $V_{DD1}$ = 5V, $V_{DD2}$ = 5V, $V_{IN+} = V_{IN–}$ = 0V | 7 | c |
| Input Resistance | $R_{IN}$ | — | 1.9 | — | kΩ | Across $V_{IN+}$ or $V_{IN–}$ to GND1 | — | c |
| Input Capacitance | $C_{INA}$ | — | 8 | — | pF | Across $V_{IN+}$ or $V_{IN–}$ to GND1, Vp-p = 80 mV, 1 MHz sine wave. | — | — |
| Dynamic Characteristics | | | | | | VS = –50 mVp to 50 mVp, 1 kHz sine wave | | |
| Signal-to-Noise Ratio | SNR | 70 | 77 | — | dB | See Definitions. | 8 | — |
| Signal-to-(Noise + Distortion) Ratio | SNDR | 64 | 76 | — | dB | See Definitions. | 9 | — |
| Effective Number of Bits | ENOB | — | 12 | — | Bits | See Definitions. | — | — |
| Isolation Transient Immunity | CMR | 25 | — | — | kV/µs | $V_{CM}$ = 1 kV. See Definitions. | — | — |
| Digital Outputs | | | | | | | | |
| Output High Voltage | $V_{OH}$ | $V_{DD2}$ – 0.4 | $V_{DD2}$ – 0.2 | — | V | $I_{OUT}$ = –4 mA | — | — |
| Output Low Voltage | $V_{OL}$ | — | 0.2 | 0.4 | V | $I_{OUT}$ = 4 mA | — | — |
| Power Supply | | | | | | | | |
| $V_{DD1}$ Supply Current | $I_{DD1}$ | — | 11.3 | 17.5 | mA | — | 10 | — |
| $V_{DD2}$ Supply Current | $I_{DD2}$ | — | 5 | 6.5 | mA | — | 11, 12 | — |

a. The maximum offset error Vos_max and minimum offset error Vos_min is determined within the full operating temperature range. Offset Error Drift vs. Temperature is calculated by using the box method: $dV_{OS}/dT_A = ±(Vos_max – Vos_min) / AmbientTempRange$.

b. Beyond the positive full-scale input range the data output is all ones. Beyond the negative full-scale input range the data output is all zeroes.

c. Time averaged values are shown. $R_{IN} = \Delta V_{IN} / \Delta I_{IN}$.

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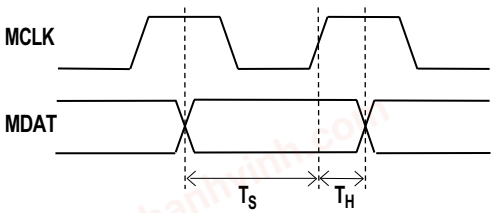
# Timing Specifications

All minimum and maximum values are at recommended conditions, unless otherwise noted. All typical values are at $T_A$ = 25°C, $V_{DD1}$ = 5V, $V_{DD2}$ = 5V.

**Table 9: Timing Specifications**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure |
|---|---|---|---|---|---|---|---|
| Modulator Clock Output Frequency | $f_{MCLK}$ | 9 | 10 | 11 | MHz | $C_L$ = 15 pF | 13 |
| Modulator Clock Duty Cycle | DC | 40 | 50 | 70 | % | $C_L$ = 15 pF | — |
| Modulator Clock Rising Time | $t_R$ | — | 5 | — | ns | $C_L$ = 15 pF | — |
| Modulator Clock Falling Time | $t_F$ | — | 5 | — | ns | $C_L$ = 15 pF | — |
| Data Setup Time Before MCLK Rising Edge | $t_S$ | 50 | 70 | — | ns | $C_L$ = 15 pF | — |
| Data Hold Time After MCLK Rising Edge | $t_H$ | 10 | 20 | — | ns | $C_L$ = 15 pF | — |

**Figure 4: MCLK and MDAT Data Timing**




# Package Characteristics

**Table 10: Package Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage | $V_{ISO}$ | 5000 | — | — | $V_{RMS}$ | RH ≤ 50%, t = 1 minute, $T_A$ = 25°C | a, b |
| Input-Output Resistance | $R_{I-O}$ | — | $>10^{14}$ | — | Ω | $V_{I-O}$ = 500 $V_{DC}$ | c |
| Input-Output Capacitance | $C_{I-O}$ | — | 0.5 | — | pF | f = 1 MHz | c |

a. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 $V_{RMS}$ for 1 second (leakage detection current limit, $I_{I-O}$ ≤ 5 μA). This test is performed before the 100% production test for partial discharge (method b) shown in Table 4, IEC/EN/DIN EN 60747-5-5 Insulation Characteristics.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to Table 4, IEC/EN/DIN EN 60747-5-5 Insulation Characteristics and your equipment-level safety specification.

c. This is a two-terminal measurement: pins 1 through 4 are shorted together and pins 5 through 8 are shorted together.

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# Typical Performance Plots

**Figure 5: Offset Voltage Change vs. Temperature**

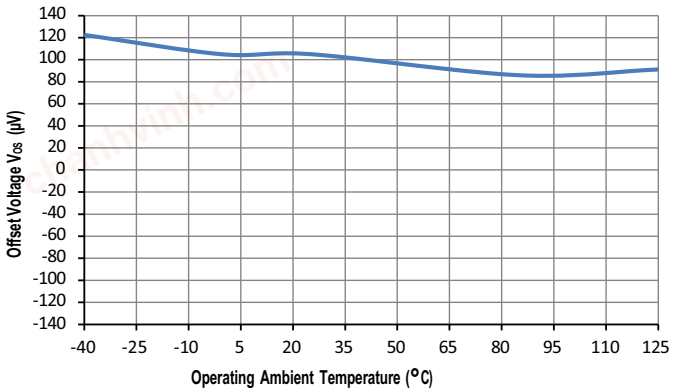



**Figure 6: Reference Voltage $V_{REF}$ Change vs. Temperature**

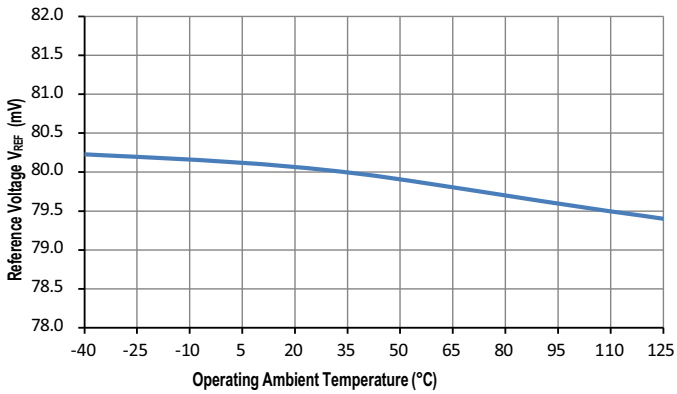



**Figure 7: Input Current vs. Input Voltage**

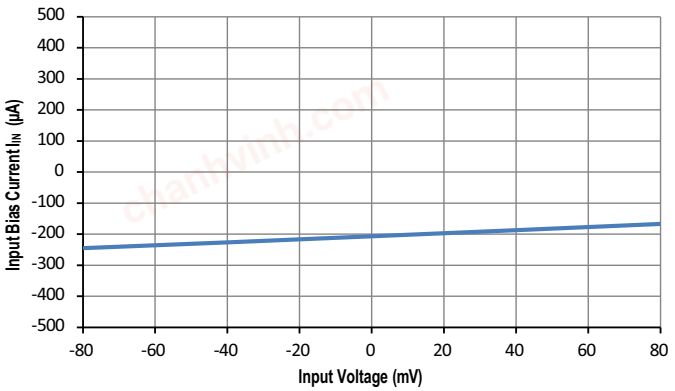



**Figure 8: SNR vs. Temperature**

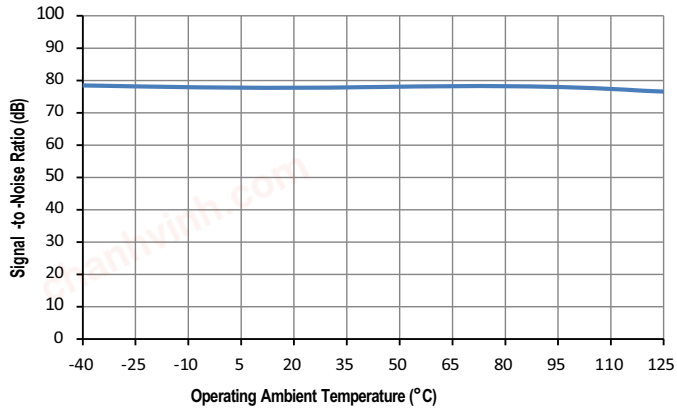



**Figure 9: SNDR vs. Temperature**

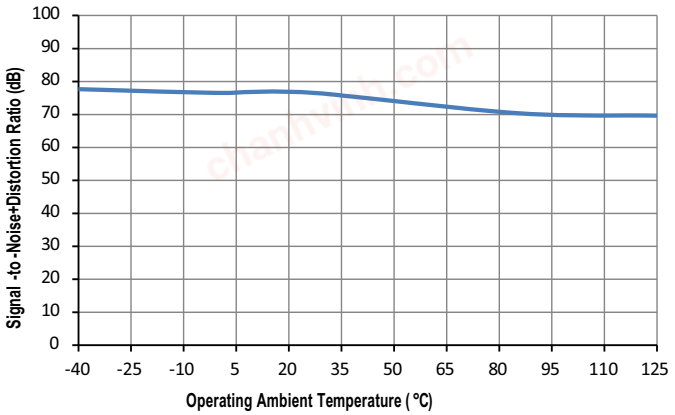
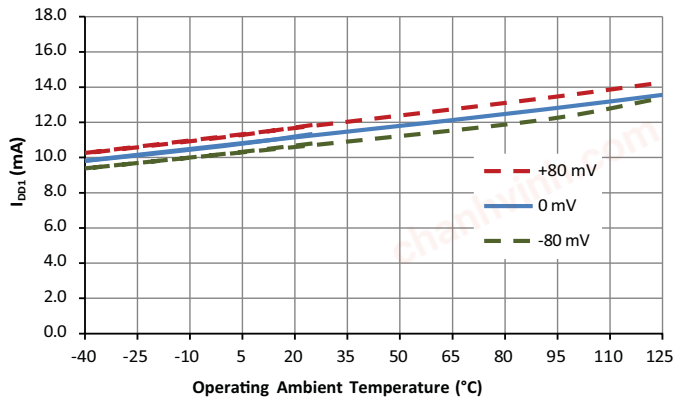



**Figure 10: $I_{DD1}$ ($V_{DD1}$ = 5V) vs. Temperature at Various $V_{IN}$ DC Inputs**



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**Figure 11: $I_{DD2}$ ($V_{DD2}$ = 5V) vs. Temperature at Various $V_{IN}$ DC Inputs**

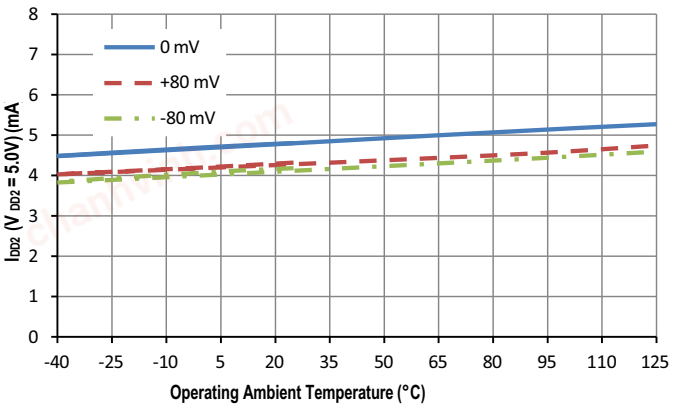



**Figure 12: $I_{DD2}$ ($V_{DD2}$ = 3.3V) vs. Temperature at Various $V_{IN}$ DC Inputs**

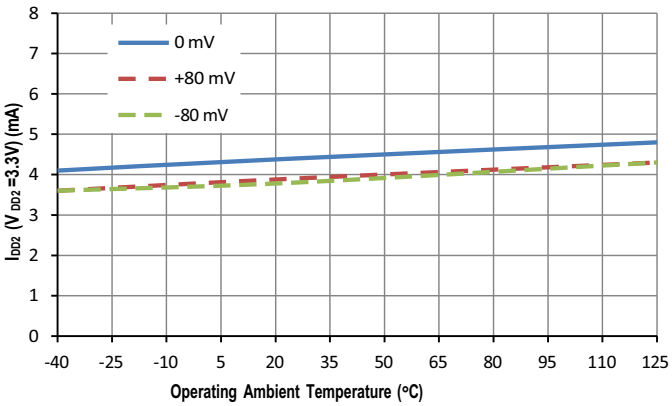
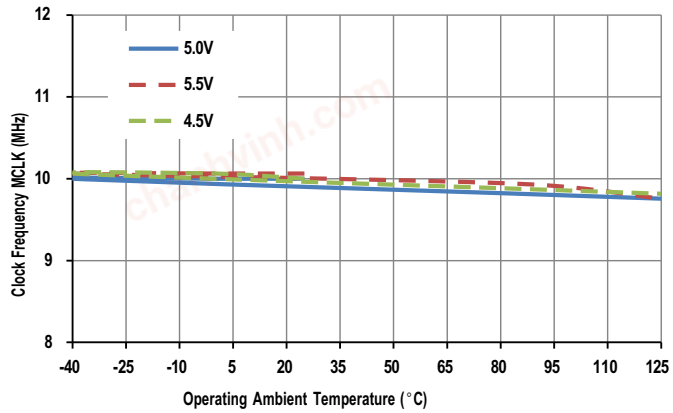



**Figure 13: Clock Frequency vs. Temperature at Various $V_{DD1}$**



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# Definitions

## Integral Nonlinearity (INL)

INL is the maximum deviation of a transfer curve from a straight line passing through the endpoints of the ADC transfer function, with offset and gain errors adjusted out.

## Differential Nonlinearity (DNL)

DNL is the deviation of an actual code width from the ideal value of 1 LSB between any two adjacent codes in the ADC transfer curve. DNL is a critical specification in closed-loop applications. A DNL error of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

## Offset Error

Offset error is the deviation of the actual input voltage corresponding to the mid-scale code (32,768 for a 16-bit system with an unsigned decimation filter) from 0V. Offset error can be corrected by software or hardware.

## Gain Error (Full-Scale Error)

Gain error includes positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the actual input voltage corresponding to positive full-scale code (65,535 for a 16-bit system) from the ideal differential input voltage ($V_{IN+} – V_{IN–}$ = +80 mV), with offset error adjusted out. Negative full-scale gain error is the deviation of the actual input voltage corresponding to negative full-scale code (0 for a 16-bit system) from the ideal differential input voltage ($V_{IN+} – V_{IN–}$ = –80 mV), with offset error adjusted out. Gain error includes reference error. Gain error can be corrected by software or hardware.

## Signal-to-Noise Ratio (SNR)

The SNR is the measured ratio of AC signal power to noise power below half of the sampling frequency. The noise power excludes harmonic signals and DC.

## Signal-to-(Noise + Distortion) Ratio (SNDR)

The SNDR is the measured ratio of AC signal power to noise plus distortion power at the output of the ADC. The signal power is the RMS amplitude of the fundamental input signal. Noise plus distortion power is the RMS sum of all non-fundamental signals up to half the sampling frequency (excluding DC).

## Effective Number of Bits (ENOB)

The ENOB determines the effective resolution of an ADC for sinusoidal inputs, expressed in bits, defined by:

ENOB = (SNDR – 1.76) / 6.02

## Isolation Transient Immunity (CMR)

The isolation transient immunity (also known as Common-Mode Rejection or CMR) specifies the minimum rate-of-rise/fall of a common-mode signal applied across the isolation boundary beyond which the modulator clock or data is corrupted. Data and clock output are measured within specifications after 1 µs of common-mode transient occurs.

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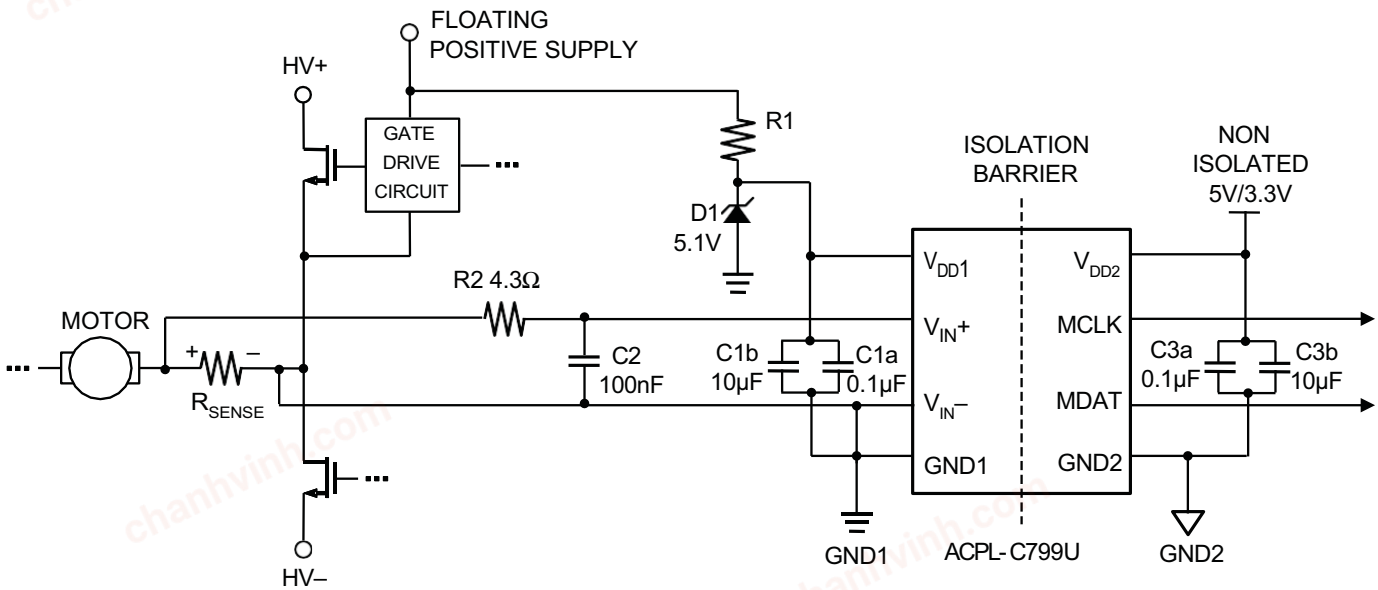


# Application Information

## Typical Application Circuit

Figure 14 shows a typical application circuit for motor control phase current sensing. By choosing the appropriate shunt resistance, a wide range of current can be monitored, from less than 1A to more than 100A.

**Figure 14: Typical Application Circuit in Motor Phase Current Sensing**



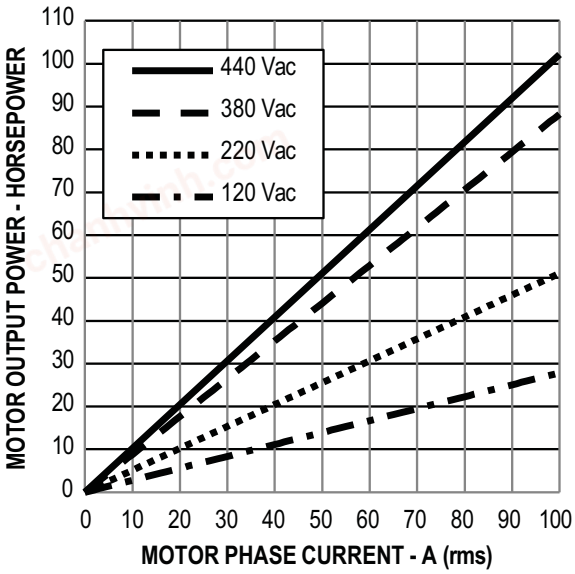

### Shunt Resistors

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, while larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolated modulator.

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**Figure 15: Motor Output Horsepower vs. Motor Phase Current and Supply**




The first step in selecting a shunt is determining how much current the shunt will be sensing. The graph in Figure 15 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolated modulator. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the shunt should see during normal operation. For example, if a motor will have a maximum RMS current of 70 $A_{rms}$ and can experience up to 50% overloads during normal operation, then the peak current is 150A (= 70 x 1.414 x 1.5). Assuming a maximum input voltage of 50 mV without overload condition, the maximum value of shunt resistance in this case would be about 0.5 mΩ. Under overload conditions, the maximum input voltage will then be 75 mV (150A x 0.5 mΩ), well within the ±80 mV FSR.

The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 2.45W in the previous example.

If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum value to decrease power dissipation. The minimum value of the shunt is limited by precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. The effect increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal resistance of the shunt or by using a shunt with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the shunt on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal shunt, as the value of shunt resistance decreases, the resistance of the leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the lead during assembly (these issues will be discussed in more detail). Secondly, the leads are typically made from a material such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall. Both of these effects are eliminated

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when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

Several two-terminal and four-terminal surface-mount-type shunt resistors from various suppliers suitable for sensing currents in motor drives up to 70 $A_{rms}$ (71 hp or 53 kW) are shown as examples in Table 11.

**Table 11: Example of Two-Terminal and Four Terminal Shunt Resistors for Motor Drives up to 70 $A_{rms}$**

| Manufacturer/Shunt Resistor Part Number | Shunt Resistor Type | Shunt Resistance | Maximum RMS Current | Motor Power Range 120Vac to 440Vac | |
|---|---|---|---|---|---|
| | | mΩ | A | hp | kW |
| KOA/CSR Series | Four-terminal | 5 | 7 | 1.8 to 6.7 | 1.4 to 5 |
| Isabellenhütte/BVS Series | Two-terminal | | | | |
| Vishay/WSL4026 Series | Four-terminal | 2 | 17 | 4 to 17 | 3 to 13 |
| Isabellenhütte/BVE Series | Two-terminal | | | | |
| KOA/PSG4 Series | Four-terminal | 1 | 35 | 9 to 36 | 7 to 27 |
| KOA/PSB Series | Two-terminal | | | | |
| Isabellenhütte/BVR Series | Four-terminal | 0.5 | 70 | 19 to 72 | 14 to 54 |
| KOA/PSJ2 Series | Two-terminal | | | | |

When laying out a PC board for the shunts, a couple of points should be kept in mind. The Kelvin connections to the shunt should be brought together under the body of the shunt and then run very close to each other to the input of the isolated modulator; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the shunt is not located on the same PC board as the isolated modulator circuit, a tightly twisted pair of wires can accomplish the same thing.

Multiple layers of the PC board can also be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the shunt to help distribute the current between the layers of the PC board. The PC board should use 2-oz. or 4-oz. copper for the layers, resulting in a current carrying capacity in excess of 20A. Making the current carrying traces on the PC board fairly large can also improve the shunt's power dissipation capability by acting as a heat sink. Use of vias where the load current enters and exits the PC board is also recommended.

## Shunt Connections

The recommended method for connecting the isolated modulator to the shunt resistor is shown in Figure 14. $V_{IN+}$ of the ACPL-C799U is connected to the positive terminal of the shunt resistor, while $V_{IN-}$ is shorted to GND1, with the power supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board trace to connect the isolated modulator circuit to the shunt resistor. By referencing the input circuit to the negative side of the sense resistor, any load current-induced noise transients on the shunt are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current shunt.

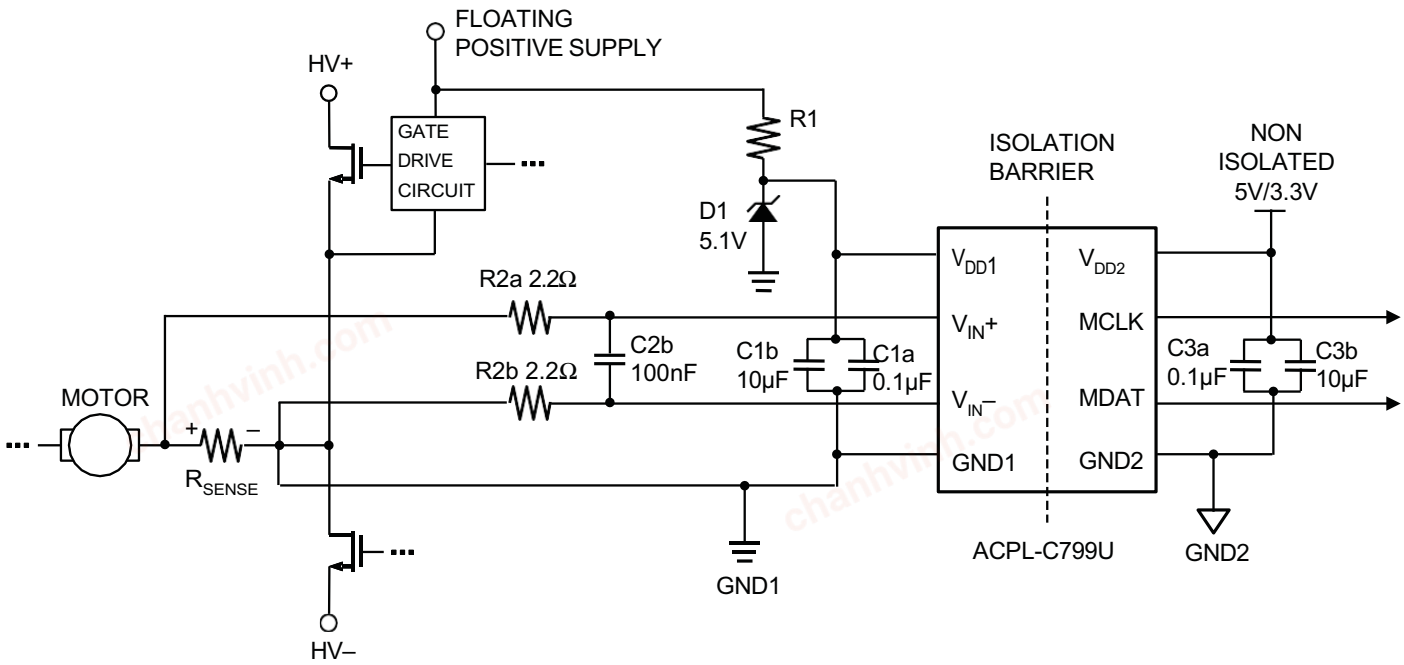
If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the isolated modulator to the sense resistor be the only return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolated modulator circuit and the gate drive circuit should be the positive power supply line.

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In some applications, however, supply currents flowing through the power supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting $V_{IN+}$ and $V_{IN-}$ directly across the shunt resistor with two conductors, and connecting GND1 to the shunt resistor with a third conductor for the power supply return path, as shown in Figure 16. The input currents induced by the common-mode of the fully differential amplifier on both of the pins are balanced on the filter resistors, R2a and R2b, and cancel out each other. Any noise induced on one pin will be coupled to the other pin by the capacitor C2 and creates only common-mode noise which is rejected by the device. When connected this way, both input pins should be bypassed. To minimize electromagnetic interference of the sense signal, all of the conductors (whether two or three are used) connecting the isolated modulator to the sense resistor should be either twisted-pair wire or closely spaced traces on a PC board.

**Figure 16: Schematic for Three-Conductor Shunt Connection**




The resistors R2 in Figure 14 or R2a and R2b in Figure 16, which are in series with the input leads, form a low-pass anti-aliasing filter with the input bypass capacitor C2. These resistors perform another important function as well; to dampen any ringing which might present in the circuit formed by the shunt, the input bypass capacitor, and the inductance of wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

## Analog Input

The ACPL-C799U front-end contains a fully-differential amplifier followed by a sigma-delta modulator. The fully-differential analog inputs accept signals of ±50 mV (full scale ±80 mV), which is ideal for direct connection to shunt-based current sensing or other low-level signal sources applications such as motor phase current measurements. Users are able to use higher input range, for example ±75 mV, as long as within full-scale range (±80 mV), for purpose of overcurrent or overload detection.

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## Latch-up Consideration

Latch-up risk of CMOS devices needs careful consideration, especially in applications with direct connection to signal source that is subject to frequent transient noise. The analog input structure of the ACPL-C799U is designed to be resilient to transients and surges, which are often encountered in highly noisy application environments such as motor drives and other power inverter systems.

Other situations that could cause transient voltages to the inputs include short circuit and overload conditions. The ACPL-C799U is tested with DC voltage of up to –2V and 2-second transient voltage of up to –6V to the analog inputs with no latch-up or damage to the device.

## Modulator Data Output and Digital Filter

Input signal information is contained in the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 17. A differential input signal of 0V ideally produces a data stream of ones and zeros in equal densities. A differential input of –50 mV corresponds to 18.75% density of ones, and a differential input of +50 mV is represented by 81.25% density of ones in the data stream. A differential input of +80 mV or higher ideally results in all ones in the data stream, while an input of –80 mV or lower ideally results in all zeros. Table 12 shows this relationship.

**Figure 17: Modulator Output vs. Analog Input**

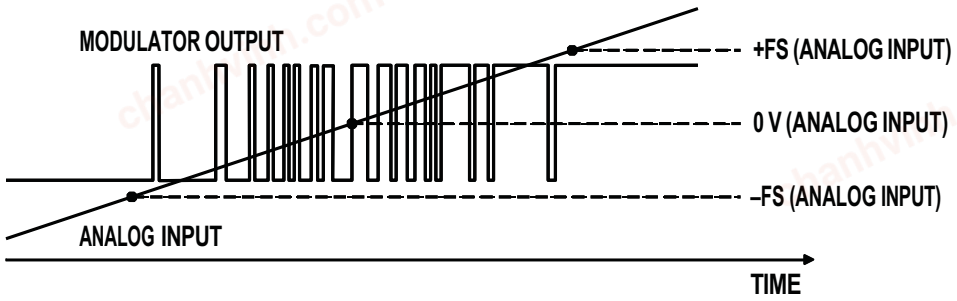



**Table 12: Input Voltage with Ideal Corresponding Density of 1s at Modulator Data Output and ADC Code**

| Analog Input | Voltage Input | Density of 1s | ADC Code (16-bit unsigned decimation) |
|---|---|---|---|
| +Full-Scale | +80 mV | 100% | 65,535 |
| +Recommended Input Range | +50 mV | 81.25% | 53,248 |
| Zero | 0 mV | 50% | 32,768 |
| –Recommended Input Range | –50 mV | 18.75% | 12,288 |
| –Full-Scale | –80 mV | 0% | 0 |

**NOTE:**

1. With a bipolar offset binary coding scheme, the digital code begins with digital 0 at –FS input and increases proportionally to the analog input until the full-scale code is reached at the +FS input. The zero crossing occurs at the mid-scale input.
2. The ideal density of 1s at modulator data output can be calculated with $V_{IN}$/160 mV + 50%; similarly, the ADC code can be calculated with ($V_{IN}$/160 mV) × 65,536 + 32,768, assuming a 16-bit unsigned decimation filter.

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A digital filter converts the single-bit data stream from the modulator into a multi-bit output word similar to the digital output of a conventional A/D converter. With this conversion, the data rate of the word output is also reduced (decimation). A Sinc3 filter is recommended to work together with the ACPL-C799U. With a 256 decimation ratio and 16-bit word settings, the output data rate is 39 kHz (= 10 MHz/256). This filter can be implemented in an ASIC, an FPGA, or a DSP. Some of the ADC codes with corresponding input voltages are shown in Table 12.

## Power Supplies and Bypassing

As shown in Figure 14, a floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5V using a simple zener diode (D1); the value of resistor R1 should be chosen to ensure sufficient current can be supplied from the existing floating supply. The voltage from the current sensing resistor or shunt ($R_{SENSE}$) is applied to the input of the ACPL-C799U through an RC anti-aliasing filter (R2 and C2). Finally, the clock and data output from the ACPL-C799U are connected to the digital filter. Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

The power supply for the isolated modulator is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line-powered transformer or a high-frequency DC-DC converter.

A three-terminal regulator can also be used to reduce the floating supply voltage to 5V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 14, the bypass capacitors (C1a, C1b, and C3a) should be located as close as possible to the input and output power supply pins of the isolated modulator. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolated modulator. For better filtering, additional 1 µF to 10 µF capacitors (C3b) can be used.

As for the input bypass capacitor C2, it also forms part of the anti-aliasing filter, and is recommended to prevent high frequency noise from aliasing down to lower frequencies and interfering with the input signal.

## PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, and so on. In addition, the layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

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