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ACPL-C797T

Automotive Optically Isolated Sigma-Delta Modulator

AVAGO TECHNOLOGIES

Data Sheet

Description

The ACPL-C797T is a 1-bit, second-order sigma-delta (Σ-Δ) modulator that converts an analog input signal into a high-speed data stream with galvanic isolation based on optical coupling technology. The ACPL-C797T operates from a 5 V power supply with dynamic range of 79 dB with an appropriate digital filter. The differential inputs of ±200 mV (full scale ±320 mV) are ideal for direct connection to shunt resistors or other low-level signal sources in applications such as motor phase current measurement.

The ACPL-C797T isolated modulator converts a low-bandwidth analog input into a high-speed one-bit data stream by means of a Sigma-Delta (Σ-Δ) over-sampling modulator. The modulator data and on-chip sampling clock are encoded and transmitted across the isolation boundary where they are recovered and decoded into separate high-speed clock and data channels. Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients.

Offered in a a compact SSO-8 package, the isolated ADC delivers the reliability, small size, superior isolation and over-temperature performance that motor drive designers need to accurately measure current. Avago R^2Coupler™ isolation products provide the reinforced insulation and reliability needed for critical automotive and high-temperature industrial applications.

Functional Block Diagram

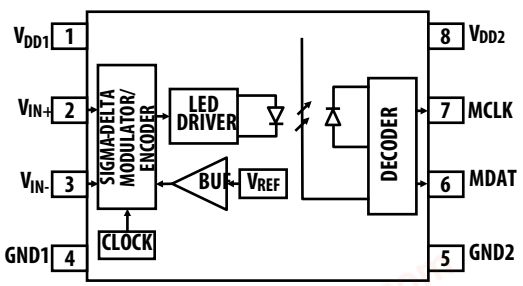

Figure 1.

Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40 °C to +125 °C
- 1-bit, second-order sigma-delta modulator
- 10 MHz internal clock
- 16-bit resolution no missing codes (12 bits ENOB)
- Signal-to-Noise Ratio: 79 dB Typ.
- Gain error: ±1%
- ±200 mV linear range with single 5 V supply (±320 mV full scale)
- Wide supply range for digital interface: 3 V to 5.5 V
- Compact, surface mount SSO-8 package
- Superior optical isolation and insulation
- Common-mode transient immunity: 25 kV/µs
- Safety and regulatory approval:
  - IEC/EN/DIN EN 60747-5-5: 1414 V_{PEAK} working insulation voltage
  - UL 1577: 5000 V_{RMS}/1 minute isolation voltage
  - CSA: Component Acceptance Notice #5

Applications

- Automotive electric motor phase and rail current sensing
- Automotive inverter DC bus current sensing
- Automotive battery current sensing
- Automotive DC-DC converter current sensing
- Automotive AC-DC Charger current sensing
- General-purpose current and voltage sensing

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

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Pin Configuration and Description

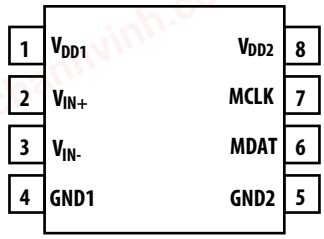

Figure 2. Pin configuration

Pin description

Pin No.	Symbol	Description
1	V_{DD1}	Supply voltage for signal input side (analog side), relative to GND1
2	V_{IN+}	Positive analog input, recommended input range ±200 mV
3	V_{IN-}	Negative analog input, recommended input range ±200 mV (normally connected to GND1)
4	GND1	Supply ground for signal input side
5	GND2	Supply ground for data/clock output side (digital side)
6	MDAT	Modulator data output
7	MCLK	Modulator clock output
8	V_{DD2}	Supply voltage for data output side, relative to GND2

Ordering Information

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 V_{RMS}/1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-C797T	-000E	Stretched SO-8	X		X	X	80 per tube
	-500E		X	X	X	X	1000 per reel

To order, choose a part number from the Part Number column and combine with the desired option from the Option column to form an order entry.

Example:

ACPL-C797T-500E to order product of Surface Mount package in Tape and Reel packaging with RoHS compliance.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

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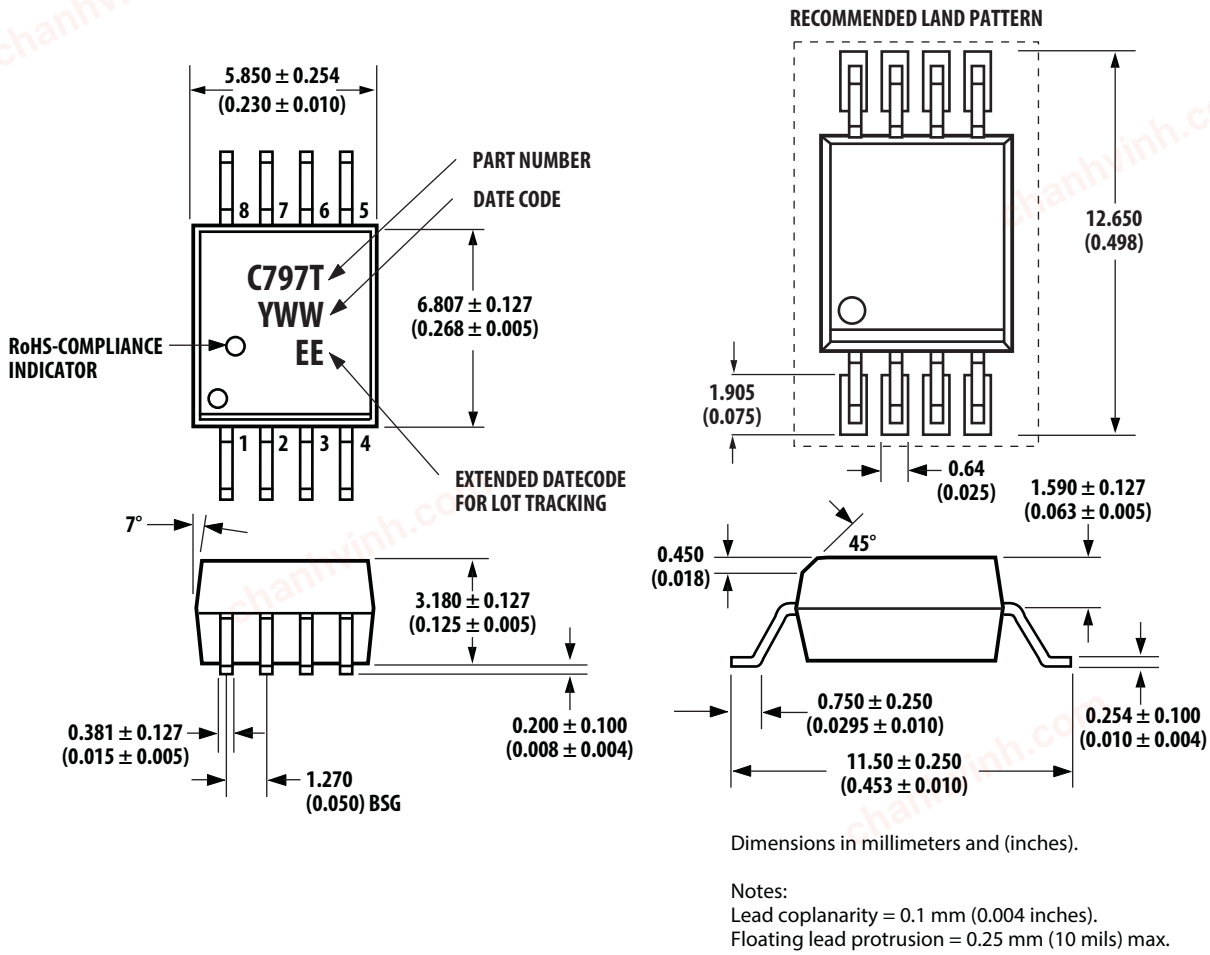
Package Outline Drawings

Stretched SO-8 Package (SSO-8)



Dimensions in millimeters and (inches).

Notes:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25 mm (10 mils) max.

Figure 3. Package Outline Drawing

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-C797T is approved by the following organizations:

IEC/EN/DIN EN 60747-5-5

Approved with Maximum Working Insulation Voltage V_{IORM} = 1414 V_{PEAK}.

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}/1min. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

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IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Value	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I – IV I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
Input-to-Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	2651	V_{PEAK}
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	2262	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values (Maximum values allowed in the event of a failure) Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-55	+150	°C	
Ambient Operating Temperature	T_A	-40	+125	°C	
Supply Voltage	V_{DD1}, V_{DD2}	-0.5	6.0	V	
Steady-State Input Voltage[1,3]	V_{IN}+, V_{IN}–	-2	V_{DD1} + 0.5	V	1
Two-Second Transient Input Voltage[2]	V_{IN}+, V_{IN}–	-6	V_{DD1} + 0.5	V	2
Digital Output Voltages	MCLK, MDAT	-0.5	V_{DD2} +0.5	V	
Lead Solder Temperature	260 °C for 10 sec., 1.6 mm below seating plane				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	+125	°C
V_{DD1} Supply Voltage	V_{DD1}	4.5	5.5	V
V_{DD2} Supply Voltage	V_{DD2}	3	5.5	V
Analog Input Voltage[3]	V_{IN}+, V_{IN}–	-200	+200	mV

Notes:
1. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.
2. Transient voltage of 2 seconds down to -6 V on the inputs does not cause latch-up or damage to the device.
3. Full scale signal input range ±320 mV.

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Electrical Specifications

All minimum and maximum values are at recommended operating conditions unless otherwise stated. All typical values are at T_A = 25 °C, V_{DD1} = 5 V, V_{DD2} = 5 V, tested with Sinc^3 filter, 256 decimation ratio.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
STATIC CHARACTERISTICS								
Resolution		16			Bits	Decimation filter output set to 16 bits		
Integral Nonlinearity	INL	-32	3	32	LSB	See Definitions section		
Differential Nonlinearity	DNL	–0.9		0.9	LSB	No missing codes, guaranteed by design. See Definitions section		
Offset Error	V_{OS}	-0.3	0.7	1.7	mV	Short V_{IN}+ and V_{IN}- to GND1. See Definitions section	5	
Offset Drift vs. V_{DD1}			100		µV/V	Short V_{IN}+ and V_{IN}- to GND1.		
Internal Reference Voltage	V_{REF}		320		mV			
Reference Voltage Tolerance (Gain error)		–1		1	%	T_A = 25 °C. See Definitions section		
		-2		2	%	T_A = –40 °C to +125 °C. See Definitions section	6	
V_{REF} Drift vs. Temperature	dV_{REF}/dT_A		60		ppm/°C			
V_{REF} Drift vs. V_{DD1}	dV_{REF}/dV_{DD1}		-1.3		mV/V			
ANALOG INPUTS								
Full-Scale Differential Voltage Input Range	FSR		±320		mV	$V_{IN} = V_{IN}+ - V_{IN}–$		4
Average Input Bias Current	I_{INA}		30		nA	V_{DD1} = 5 V, $V_{IN}+ = V_{IN}– = 0$ V	7	5
Average Input Resistance	R_{IN}		26		kΩ	Across V_{IN}+ or V_{IN}– to GND1		5
Input Capacitance	C_{INA}		8		pF	Across V_{IN}+ or V_{IN}– to GND1		
DYNAMIC CHARACTERISTICS						$V_{IN}+$ = 400 mV_{pp}, 1 kHz sine wave		
Signal-to-Noise Ratio	SNR	70	79		dB	See Definitions section	8	
Signal-to-(Noise + Distortion) Ratio	SNDR	60	78		dB	See Definitions section	9	
Effective Number of Bits	ENOB		12		bits	See Definitions section		
Isolation Transient Immunity	CMR	25			kV/µs	V_{CM} = 1 kV; See Definitions section		
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}	V_{DD2} – 0.5	V_{DD2} – 0.2		V	I_{OUT} = –4 mA		
Output Low Voltage	V_{OL}		0.2	0.6	V	I_{OUT} = 4 mA		
POWER SUPPLY								
V_{DD1} Supply Current	I_{DD1}		10.4	17	mA	$V_{IN}+$ = –320 mV to +320 mV	10	
V_{DD2} Supply Current	I_{DD2}		6	9	mA		11,12	

Notes:
4. Beyond the full-scale input range the data output is either all zeroes (negative full scale) or all ones (positive full scale).
5. Due to the switched-capacitor nature of the isolated modulator, time averaged values are shown. $R_{IN} = \Delta V_{IN} / \Delta I_{IN}$.

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Timing Specifications

All minimum and maximum values are at recommended operating conditions, unless otherwise stated. All typical values are at T_A = 25 °C, V_{DD1} = 5 V, V_{DD2} = 5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Modulator Clock Output Frequency	f_{MCLK}	9	10	11	MHz	C_L = 15 pF, V_{DD2} = 4.5 V to 5.5 V	13	
		8		12		C_L = 15 pF		
Duty Cycle	D	40	54	70	%	C_L = 15 pF		
10% to 90% Rise Time	t_R		5		ns	C_L = 15 pF		
90% to 10% Fall Time	t_F		5		ns	C_L = 15 pF		
Data Setup Time Before MCLK Rising Edge	t_S	55	77		ns	C_L = 15 pF	4	
Data Hold Time After MCLK Rising Edge	t_H	10			ns	C_L = 15 pF	4	

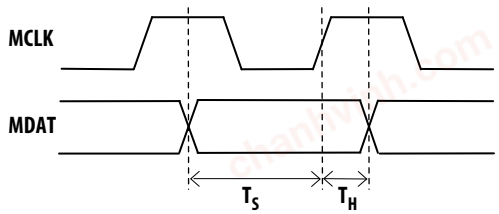

Figure 4. Data timing

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{RMS}	RH ≤ 50%, t = 1 min, T_A = 25 °C	6, 7
Input-Output Resistance	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 V_{DC}	8
Input-Output Capacitance	C_{I-O}		0.5		pF	f =1 MHz	8

Notes:

6. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
7. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table and your equipment level safety specification.
8. This is a two-terminal measurement: pins 1-4 are shorted together and pins 5-8 are shorted together.

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Typical Performance Plots

Unless otherwise noted, T_A = 25 °C, V_{DD1} = 5 V, V_{DD2} = 5 V, V_{IN}+ = –200 mV to +200 mV, and V_{IN}– = 0 V, with Sinc^3 filter, 256 decimation ratio.

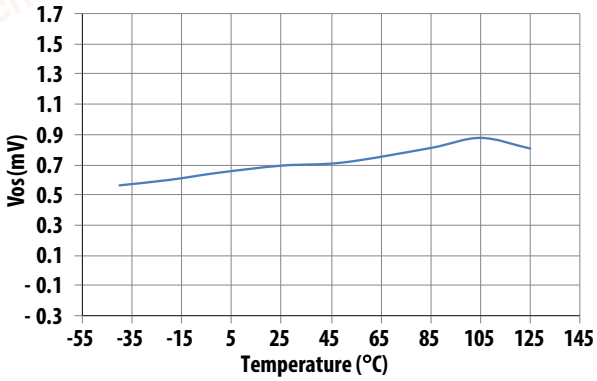

Figure 5. Offset change vs. temperature

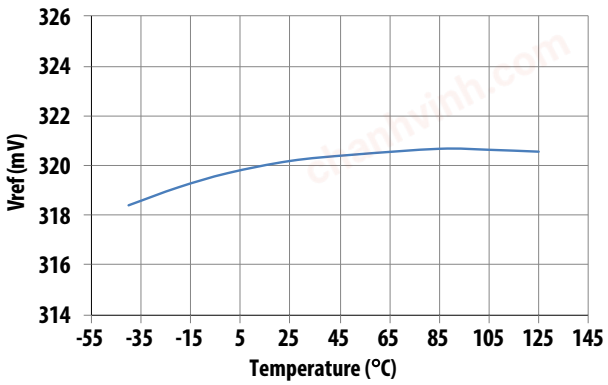

Figure 6. Reference voltage vs. temperature

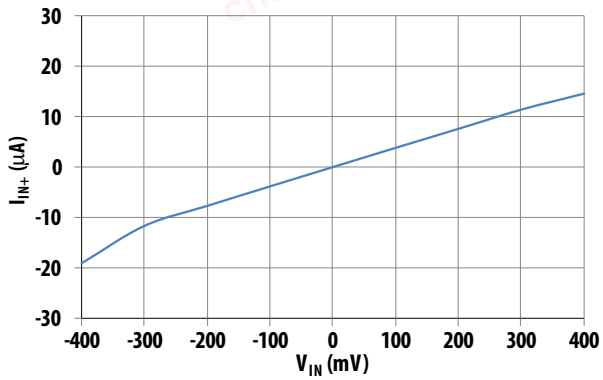

Figure 7. Input bias current vs. input voltage

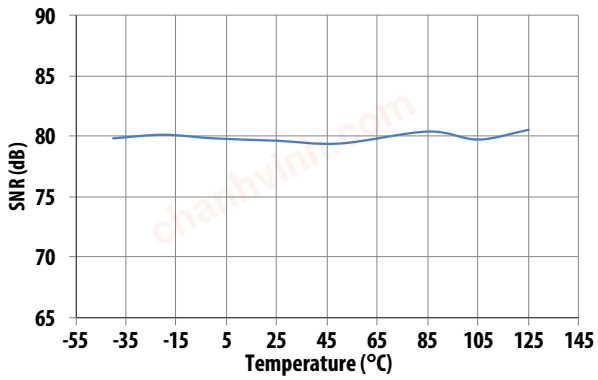

Figure 8. SNR vs. temperature

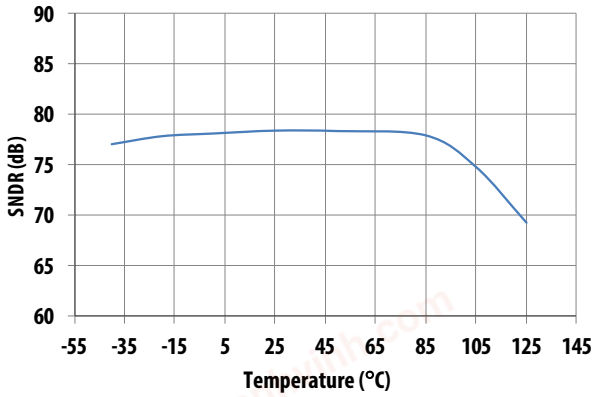

Figure 9. SNDR vs. temperature

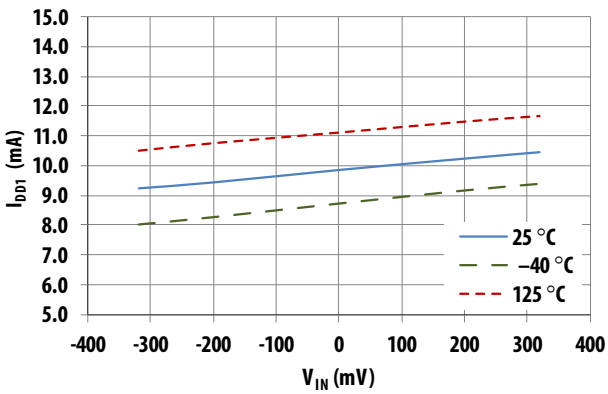

Figure 10. I_{DD1} vs. V_{IN} DC input

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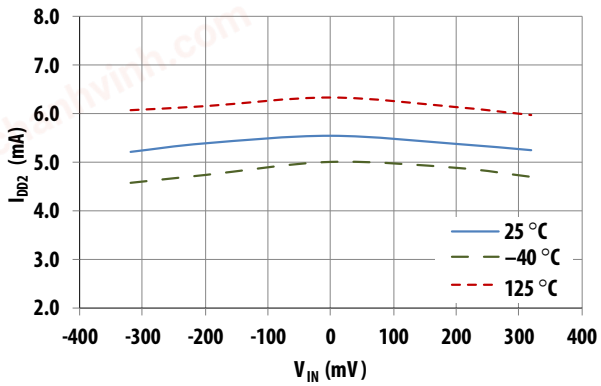

Figure 11. I_{DD2} (V_{DD2} = 5 V) vs. V_{IN} DC input

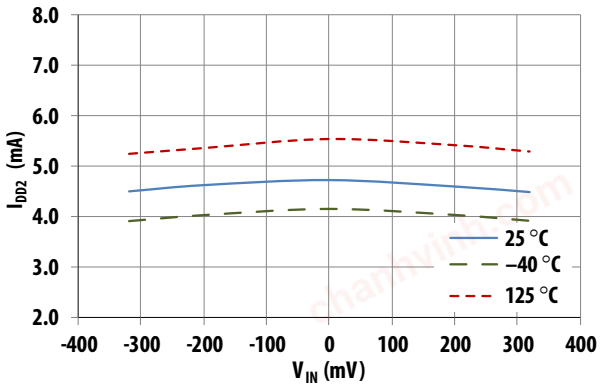

Figure 12. I_{DD2} (V_{DD2} = 3.3 V) vs. V_{IN} DC input

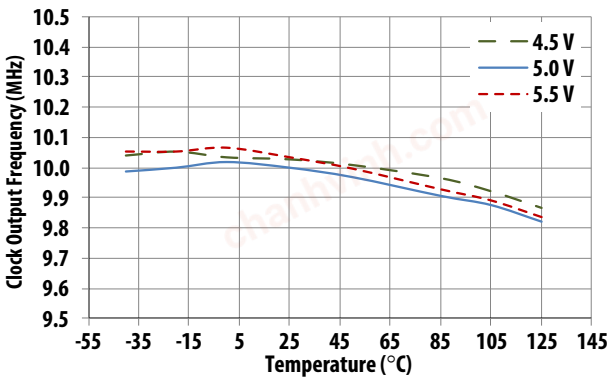

Figure 13.Clock frequency vs. temperature for various V_{DD1}

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Definitions

Integral Nonlinearity (INL)

INL is the maximum deviation of a transfer curve from a straight line passing through the endpoints of the ADC transfer function, with offset and gain errors adjusted out.

Differential Nonlinearity (DNL)

DNL is the deviation of an actual code width from the ideal value of 1 LSB between any two adjacent codes in the ADC transfer curve. DNL is a critical specification in closed-loop applications. A DNL error of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Offset error is the deviation of the actual input voltage corresponding to the mid-scale code (32,768 for a 16-bit system with an unsigned decimation filter) from 0 V. Offset error can be corrected by software or hardware.

Gain Error (Reference Voltage Tolerance, Full-Scale Error)

Gain error includes positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the actual input voltage corresponding to positive full-scale code (65,535 for a 16-bit system) from the ideal differential input voltage ($V_{IN}+ - V_{IN}- =$ +320 mV), with offset error adjusted out. Negative full-scale gain error is the deviation of the actual input voltage corresponding to negative full-scale code (0 for a 16-bit system) from the ideal differential input voltage ($V_{IN}+ - V_{IN}- = -320$ mV), with offset error adjusted out. Gain error includes reference error. Gain error can be corrected by software or hardware.

Signal-to-Noise Ratio (SNR)

The SNR is the measured ratio of AC signal power to noise power below half of the sampling frequency. The noise power excludes harmonic signals and DC.

Signal-to-(Noise + Distortion) Ratio (SNDR)

The SNDR is the measured ratio of AC signal power to noise plus distortion power at the output of the ADC. The signal power is the RMS amplitude of the fundamental input signal. Noise plus distortion power is the RMS sum of all non-fundamental signals up to half the sampling frequency (excluding DC).

Effective Number of Bits (ENOB)

The ENOB determines the effective resolution of an ADC, expressed in bits, defined by ENOB = (SNDR – 1.76)/6.02

Isolation Transient Immunity (CMR)

The isolation transient immunity (also known as Common-Mode Rejection or CMR) specifies the minimum rate-of-rise/fall of a common-mode signal applied across the isolation boundary beyond which the modulator clock or data is corrupted. Data and clock output are measured within specifications after 1 µs of common mode transient occurs.

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Application Information

Typical Application Circuit

A typical motor phase current sensing circuit is shown in Figure 14. A shunt resistor is selected according to the sensing current range and ACPL-C797T input voltage range. Two or three sets of shunt and ACPL-C797T combination are applied in a three-phase motor driving.

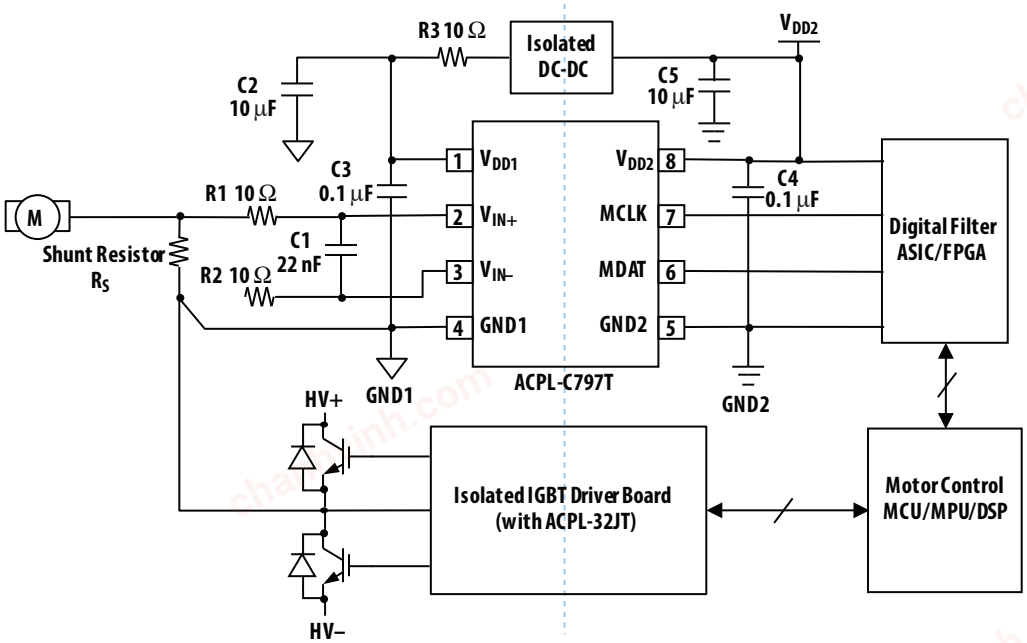

Figure 14. Typical ACPL-C797T application circuit in motor phase current sensing

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Shunt Resistor

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize dI/dt induced voltage spikes, which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, while larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolated Sigma-Delta modulator.

The first step in selecting a shunt is determining how much current the shunt will be sensing. The RMS current in each phase of a three-phase motor is a function of average motor output power and motor drive supply voltage. The maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolated modulator. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the shunt should see during normal operation. For example, if a sinusoids phase current motor has a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (= 10 × 1.414 × 1.5). Assuming a maximum input voltage of 200 mV, the maximum value of shunt resistance in this case would be about 10 mΩ (≈ 200 mV/21.1 A).

The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 1 W in the previous example.

If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum value to decrease power dissipation. The minimum value of the shunt is limited by precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents are large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal-dependent temperature rise of the shunt. The effect increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal resistance of the shunt, or by using a shunt with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the shunt on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal shunt, as the value of shunt resistance decreases, the resistance of the leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt depends on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far the solder wicks up the lead during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall. Both of these effects are eliminated when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

When laying out a PC board for the shunts, keep these points in mind. Make sure the Kelvin connections to the shunt are brought together under the body of the shunt and then run very close to each other to the input pins 2 and 3 of the isolated Sigma-Delta modulator; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the shunt is not located on the same PC board as the isolated Sigma-Delta modulator circuit, then a tightly twisted pair of wires can accomplish the same thing.

Also, multiple layers of the PC board can be used to increase the current-carrying capacity. To help distribute the current between the layers of the PC board, surround each non-Kelvin terminal of the shunt with numerous plated-through vias. Use 2 or 4 oz. per square feet of copper for the layers of the PC board; this will result in a current-carrying capacity in excess of 20 A. Making the current-carrying traces on the PC board fairly large can also improve the shunt's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

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Analog Input

The differential analog inputs of the ACPL-C797T are implemented with a fully-differential, switched-capacitor circuit. The ACPL-C797T accepts a signal of ±200 mV (full scale ±320 mV), which is ideal for direct connection to shunt-based current sensing or other low-level signal source applications such as motor phase current measurement. An internal voltage reference determines the full-scale analog input range of the modulator (±320 mV); an input range of ±200 mV is recommended to achieve optimal performance. Users are able to use a higher input range, for example ±250 mV, as long as within a full-scale range, for the purpose of overcurrent or overload detection. Figure 15 shows the simplified equivalent circuit of the analog input.

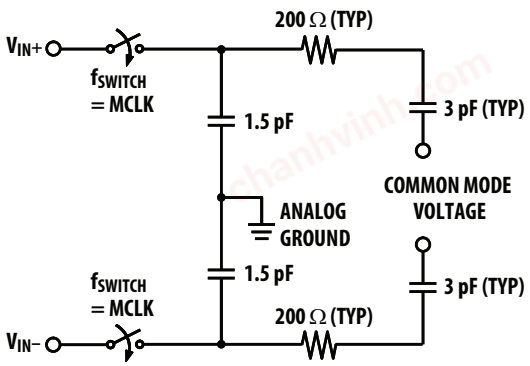

Figure 15. Analog input equivalent circuit

In the typical application circuit (Figure 14), the ACPL-C797T is connected in single-ended input mode. The voltage from the shunt resistor is applied to the input of the ACPL-C797T through an RC anti-aliasing filter (R1/R2 and C1). The input currents created by the switching actions on both of the pins are balanced on the filter resistors and cancelled out each other. Any noise induced on one pin will be coupled to the other pin by the capacitor C1 and creates only common mode noise which is rejected by the device. The filter prevents high frequency noise from aliasing down to lower frequencies and interfering with the input signal. Typical values for R1 (= R2) and C1 are 10 Ω and 22 nF, respectively. The bypass capacitor (C1) is also recommended at the input due to the switched-capacitor nature of the input circuit. Place the input anti-aliasing filter as close as possible to the input pins.

Latch-up Consideration

Carefully consider the latch-up risk of CMOS devices, especially in applications with direct connection to a signal source that is subject to frequent transient noise. The analog input structure of the ACPL-C797T is designed to be resilient to transients and surges, which are often encountered in highly noisy application environments such as motor drive and other power inverter systems. Other situations could cause transient voltages to the inputs include short circuit and overload conditions. The ACPL-C797T is tested with DC voltage of up to –2 V and 2-second transient voltage of up to –6 V to the analog inputs with no latch-up or damage to the device.

Power Supply

The output side power supply V_{DD2} is same as microcontroller or microprocessor's power supply. The input side power supply V_{DD1} must be isolated to output side circuit. The V_{DD1} can be derived from an isolated DC-DC converter from vehicle's $12V_{DC}$ battery input, or from an isolated DC-DC converter from MCU/MPU's power supply as shown in the application circuit.

As shown in Figure 14, bypass capacitors (C2, C4) should be located as close as possible to the input and output power-supply pins of the isolated modulator. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolated modulator.

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Modulator Data Output and Digital Filter

Input voltage signal is converted into the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 16. A differential input signal of 0 V ideally produces a data stream of ones and zeros in equal densities. A differential input of –200 mV corresponds to 18.75% density of ones, and a differential input of +200 mV is represented by 81.25% density of ones in the data stream. A differential input of +320 mV or higher results in ideally all ones in the data stream, while input of –320 mV or lower will result in all zeros ideally.

A digital filter is required to convert the single-bit data stream from the modulator into a multi-bit output word similar to the digital output of a conventional A/D converter. With this conversion, the data rate of the word output is also reduced (decimation). A $Sinc^3$ filter is recommended to work together with the ACPL-C797T. With 256 decimation ratio and 16-bit word settings, the output data rate is 39 kHz (= 10 MHz/256). The $Sinc^3$ filter can be implemented in an MCU/MPU/DSP/ASIC. Some of the ADC codes with corresponding input voltages are shown in the following table.

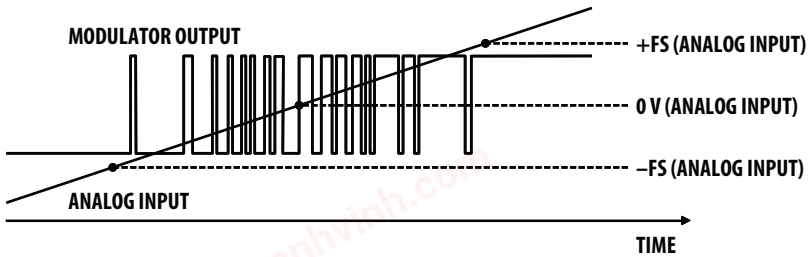

Figure 16. Modulator output vs. analog input

Input voltage with ideal corresponding density of 1s at modulator data output, and ADC code

Analog Input	Voltage Input	Density of 1s	ADC Code (16-bit unsigned decimation)
Full-Scale Range	640 mV		
+Full-Scale	+320 mV	100%	65,535
+Recommended Input Range	+200 mV	81.25%	53,248
Zero	0 mV	50%	32,768
–Recommended Input Range	–200 mV	18.75%	12,288
–Full-Scale	–320 mV	0%	0

Notes:
1. With bipolar offset binary coding scheme, the digital code begins with digital 0 at –FS input and increases proportionally to the analog input until the full-scale code is reached at the +FS input. The zero crossing occurs at the mid-scale input.
2. Ideal density of 1s at modulator data output can be calculated with $V_{IN}/640\ mV + 50\%$; similarly, the ADC code can be calculated with $(V_{IN}/640\ mV) \times 65{,}536 + 32{,}768$, assuming a 16-bit unipolar decimation filter.

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PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices: keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, and so on. In addition, the layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

Voltage Sensing

The ACPL-C797T can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (26 kΩ) and input bias current (30 nA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth. To obtain higher bandwidth, the input bypass capacitor (C2) can be reduced, but it should not be reduced much below 1000 pF to maintain adequate input bypassing of the isolated modulator.

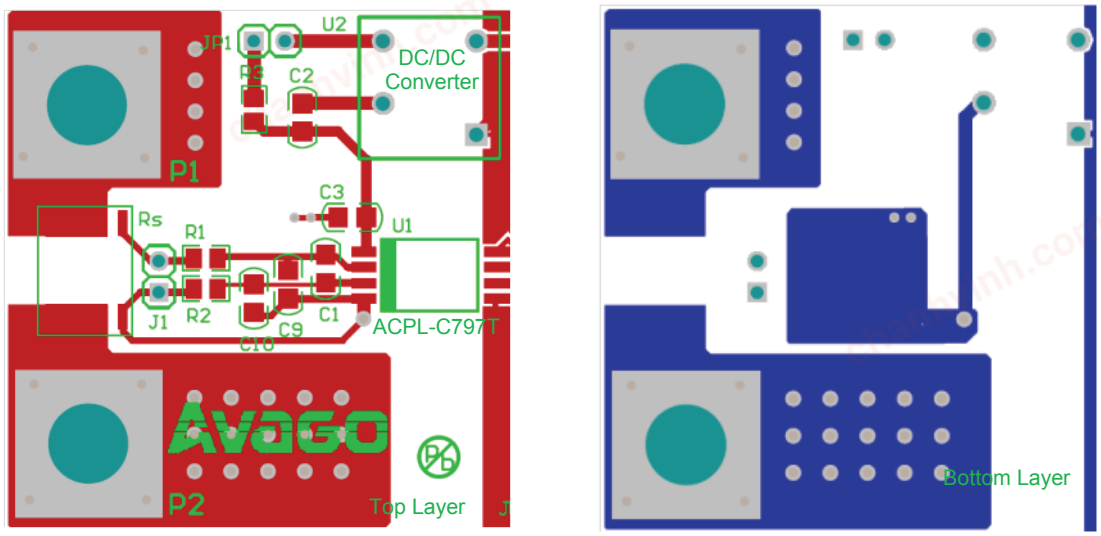

Figure 17. Recommended PCB layout for input circuit of ACPL-C797T

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