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ACPL-782T

Automotive Isolation Amplifier with R²Coupler™ Isolation

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product



Description

The ACPL-782T isolation amplifier was designed for voltage and current sensing in electronic motor drives and battery system monitoring. In a typical implementation, and motor currents flow through an external resistor and the resulting analog voltage drop is sensed by the ACPL-782T. A differential output voltage is created on the other side of the ACPL-782T optical isolation barrier. This differential output voltage is proportional to the motor current and can be converted to a single-ended signal by using an op-amp as shown in the recommended application circuit. Since common-mode voltage swings of several hundred volts in tens of nanoseconds are common in modern switching inverter motor drives, the ACPL-782T was designed to ignore very high common-mode transient slew rates (of at least 10 kV/µs).

The high CMR capability of the ACPL-782T isolation amplifier provides the precision and stability needed to accurately monitor motor current and DC rail voltage in high noise motor control environments, providing for smoother control (less "torque ripple") in various types of motor control applications.

The product can also be used for general analog signal isolation applications requiring high accuracy, stability, and linearity under similarly severe noise conditions. The ACPL-782T utilizes sigma delta (Σ–Δ) analog-to-digital converter technology, chopper stabilized amplifiers, and a fully differential circuit topology.

Together, these features deliver unequaled isolation-mode noise rejection, as well as excellent offset and gain accuracy and stability over time and temperature. This performance is delivered in a compact, auto-insertable, industry standard 8-pin DIP package that meets worldwide regulatory safety standards. (A gull-wing surface mount option -300E is also available).

Avago R²Coupler isolation products provide the reinforced insulation and reliability needed for critical in automotive and high temperature industrial applications.

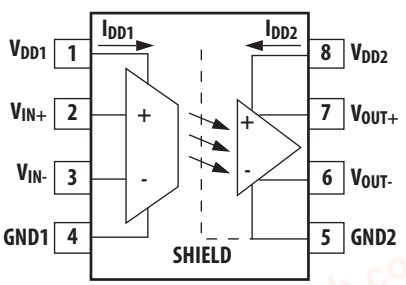
Features

- ±2% Gain Tolerance @ 25°C
- 15 kV/µs Common-Mode Rejection at V_{CM} = 1000V
- 30ppm/°C Gain Drift vs. Temperature
- 0.3 mV Input Offset Voltage
- 100 kHz Bandwidth
- 0.004% Nonlinearity
- Compact, Auto-Insertable Standard 8-pin DIP Package
- Worldwide Safety Approval:
  - UL 1577 (3750 V_{RMS}/1 min.) and
  - CSA
  - IEC 60747-5-5, DIN EN 60747-5-2(VDE 0884 Teil 2)
- Qualified to AEC-Q100 Test Guidelines
- Automotive Operating Temperature -40 to 125°C
- Advanced Sigma-Delta (Σ–Δ) A/D Converter Technology
- Fully Differential Circuit Topology

Applications

- Automotive Motor Inverter Current/Voltage Sensing
- Automotive AC/DC and DC/DC converter Current/Voltage sensing
- Automotive Battery ECU
- Automotive Motor Phase Current Sensing
- Isolation Interface for Temperature Sensing
- General Purpose Current Sensing and Monitoring

Functional Diagram



The connection of a 0.1 µF bypass capacitor between pins 1 and 4, pins 5 and 8 is recommended.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

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Part Number	Option (RoHS Compliant)	Package	Surface Mount	Gullwing	Tape & Reel
ACPL-782T	-000E	300mil DIP-8			
	-300E		X	X	
	-500E		X	X	X

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

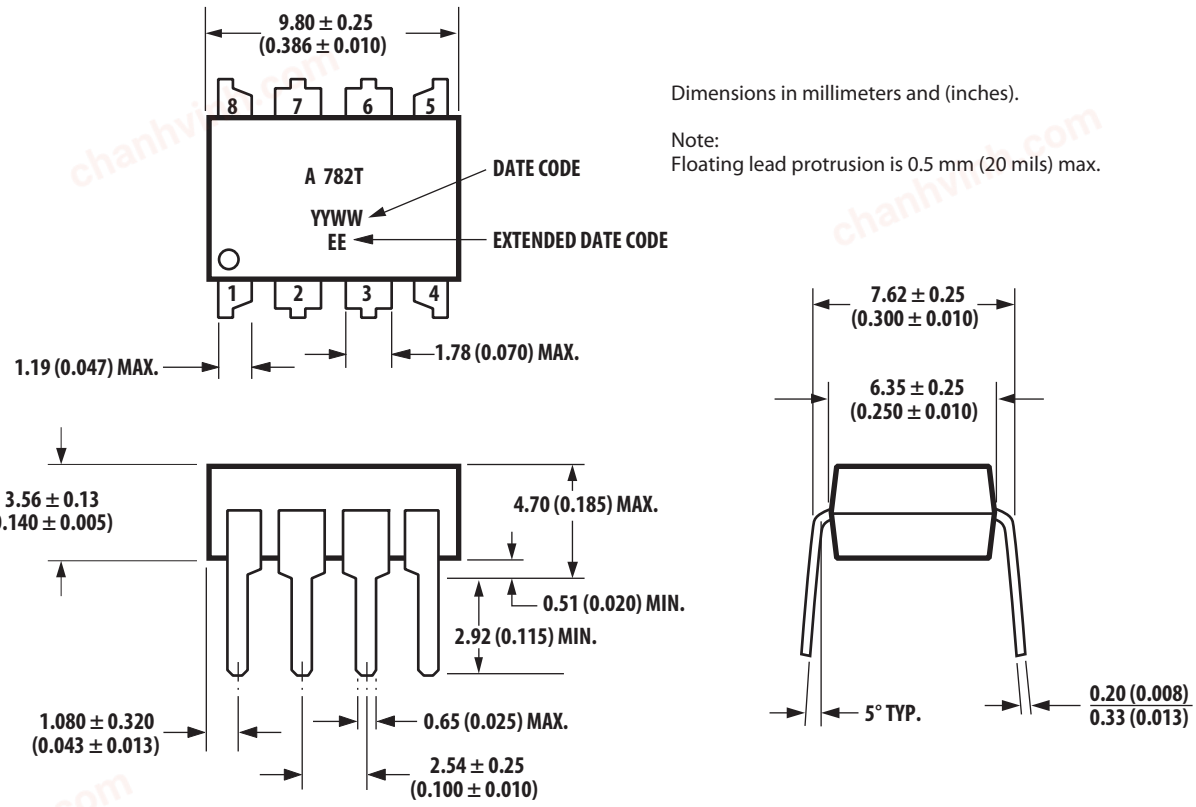
Example:

ACPL-782T-500E to order product of gullwing SMT DIP-8 package in Tape and Reel packaging with RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-782T-000E Standard DIP Package



Dimensions in millimeters and (inches).

Note:
Floating lead protrusion is 0.5 mm (20 mils) max.

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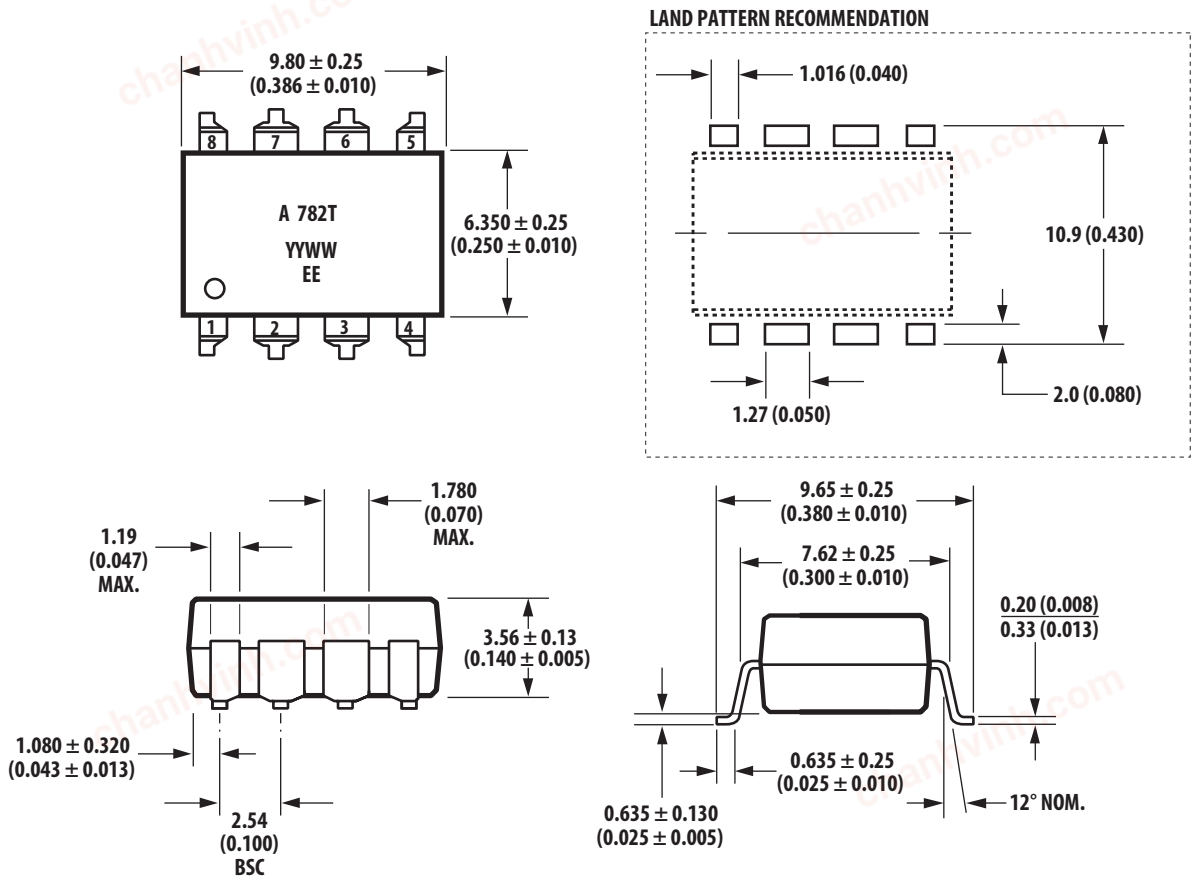
Gull Wing Surface Mount Option 300E and 500E



Dimensions in millimeters (inches).
Tolerances (unless otherwise specified): xx.xx = 0.01
xx.xxx = 0.005

Note: Floating lead protrusion is 0.5 mm (20 mils) max.

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-782T-000E is approved by the following organizations:

UL

UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS}

CSA

Approved under CSA Component AcceptanceNotice #5, File CA 88324.

IEC/DIN

IEC 60747-5-5

DIN EN 60747-5-2(VDE 0884 Teil 2)

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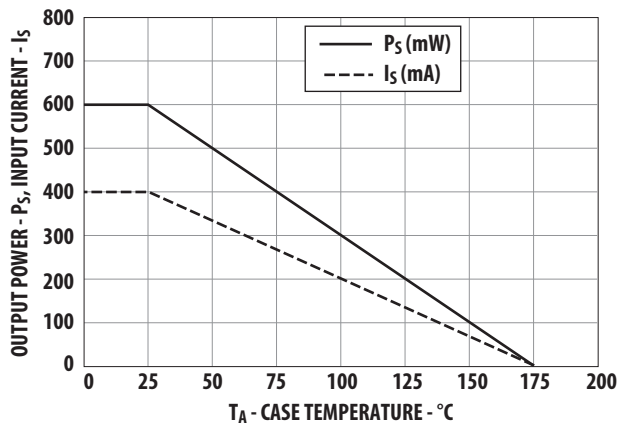
IEC 60747-5-5, DIN EN 60747-5-2(VDE 0884 Teil 2) Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage 300 Vrms		I-IV	
for rated mains voltage 450 Vrms		I-III	
for rated mains voltage 600 Vrms		I-II	
Climatic Classification		55/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	891	V_{PEAK}
Input to Output Test Voltage, Method b[2] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1670	V_{PEAK}
Input to Output Test Voltage, Method a[2] V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial discharge < 5 pC	V_{PR}	1426	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	V_{PEAK}
Safety-limiting values—maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current[3]	$I_{S,INPUT}$	400	mA
Output Power[3]	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S , V_{IO} = 500 V	R_S	$>10^9$	Ω

Notes:
1. Insulation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits within the application. Surface Mount Classification is Class A in accordance with CECC00802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC 60747-5-5/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.
3. Refer to the following figure for dependence of PS and IS on ambient temperature.



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Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	130	°C
Operating Temperature	T_A	-40	125	°C
Supply Voltage	V_{DD1}, V_{DD2}	0	5.5	Volts
Steady-state Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} + 0.5	Volts
2 second Transient Input Voltage		-6.0		Volts
Output Voltage	V_{OUT}	-0.5	V_{DD2} + 0.5	Volts
Solder Reflow Temperature Profile		See Package Outline Drawings Section		

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Ambient Operating Temperature	T_A	-40	125	°C	
Power Supply Voltage	V_{DD1}, V_{DD2}	4.5	5.5	Volts	
Input Voltage (Accurate & Linear)	V_{IN+}, V_{IN-}	-200	200	mV	1
Input Voltage (Functional)	V_{IN+}, V_{IN-}	-2	2	V	

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DC Electrical Specifications

Unless otherwise noted, all typical and figures are at the nominal operating conditions of $V_{IN+} = 0$, $V_{IN-} = 0$ V, $V_{DD1} = V_{DD2} = 5$ V and $T_A = 25°C$; all Min. /Max. Specifications are within the Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-2.0	0.3	2.0	mV	T_A=25°C	1,2	
		-4.0		4.0	mV	-40°C < T_A < +125°C, -4.5V < (V_{DD1}, V_{DD2}) < 5.5V		
Magnitude of Input Offset Change vs. Temperature	$\lvert\Delta V_{OS}/\Delta T_A\rvert$		3.0	10.0	µV/°C		3	2
Gain	G	7.84	8.00	8.16	V/V	-200 mV < V_{IN+} < 200 mV, T_A = 25°C,	4,5,6	3
Magnitude of V_{OUT} Gain Change vs. Temperature	$\lvert\Delta G/G/\Delta T_A\rvert$		30		PPM/°C			4
V_{OUT} 200 mV Nonlinearity	NL_{200}		0.0037	0.35	%	-200 mV < V_{IN+} < 200 mV	7,8	5
Magnitude of V_{OUT} 200mV Nonlinearity Change vs. Temperature	$\lvert\Delta NL_{200}/\Delta T\rvert$		0.0002		%/°C			
V_{OUT} 100 mV Nonlinearity	NL_{100}		0.0027	0.2	%	-100 mV < V_{IN+} < 100mV		6
Maximum Input Voltage before V_{OUT} Clipping	$\lvert V_{IN+}\rvert$MAX		308.0		mV		9	
Input Supply Current	I_{DD1}		10.86	16.0	mA	V_{IN+} = 400 mV	10	7
Output Supply Current	I_{DD2}		11.56	20.0	mA	V_{IN+} = -400 mV		8
Input Current	I_{IN+}	-5	-0.5		µA		11	9
Magnitude of Input Bias Current vs. Temperature coefficient	$\lvert\Delta I_{IN}/\Delta T\rvert$		0.45		nA/°C			
Output Low Voltage	V_{OL}		1.29		V			10
Output High Voltage	V_{OH}		3.80		V			
Output Common-Mode Voltage	V_{OCM}	2.2	2.545	2.8	V			
Output Short-Circuit Current	$\lvert I_{OSC}\rvert$		18.6		mA			11
Equivalent Input Impedance	R_{IN}		500		kΩ			
V_{OUT} Output Resistance	R_{OUT}		15		Ω			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		76		dB			12

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AC Electrical Specifications

Unless otherwise noted, all typicals and figures are at the nominal operating conditions of V_{IN+} = 0, V_{IN-} = 0 V, V_{DD1} = V_{DD2} = 5 V and T_A = 25°C; all Min./Max. specifications are within the Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
V_{OUT} Bandwidth (-3 dB) sine wave.	BW	50	100		kHz	V_{IN+} = 200mVpk-pk	12,13	
V_{OUT} Noise	N_{OUT}		6		mV_{RMS}	V_{IN+} = 0.0 V		13
V_{IN} to V_{OUT} Signal Delay (50 – 10%)	t_{PD10}		2.03	3.3	µs	Measured at output of MC34081on Figure 15.	4,15	
V_{IN} to V_{OUT} Signal Delay (50 – 50%)	t_{PD50}		3.47	5.6	µs	V_{IN+} = 0 mV to 150mV step.		
V_{IN} to V_{OUT} Signal Delay (50 – 90%)	t_{PD90}		4.99	9.9	µs			
V_{OUT} Rise/ Fall Time (10 – 90%)	$t_{R/F}$		2.96	6.6	µs			
Common Mode Transient Immunity	CMTI	10.0	15.0		kV/µs	V_{CM} = 1 kV, T_A = 25°C	16	14
Power Supply Rejection	PSR		170		mV_{RMS}	With recommended application circuit.		15

Package Characteristics

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			V_{RMS}	RH < 50%, t = 1 min. T_A = 25°C		16,17
Resistance (Input-Output)	R_{I-O}		$>10^9$		Ω	V_{I-O} = 500 V_{DC}		18
Capacitance (Input-Output)	C_{I-O}		1.2		pF	f = 1 MHz		18

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Notes:
General Note: Typical values represent the mean value of all characterization units at the nominal operating conditions. Typical drift specifications are determined by calculating the rate of change of the specified parameter versus the drift parameter (at nominal operating conditions) for each characterization unit, and then averaging the individual unit rates. The corresponding drift figures are normalized to the nominal operating conditions and show how much drift occurs as the par-ticular drift parameter is varied from its nominal value, with all other parameters held at their nominal operating values. Note that the typical drift specifications in the tables below may differ from the slopes of the mean curves shown in the corresponding figures.

1. Avago Technologies recommends operation with V_{IN-} = 0 V (tied to GND1). Limiting V_{IN+} to 100 mV will improve DC nonlinearity and nonlinearity drift. If V_{IN-} is brought above V_{DD1} – 2 V, an internal test mode may be activated. This test mode is for testing LED coupling and is not intended for customer use.
2. This is the Absolute Value of Input Offset Change vs. Temperature.
3. Gain is defined as the slope of the best-fit line of differential output voltage (V_{OUT+}–V_{OUT-}) vs. differential input voltage (V_{IN+}–V_{IN-}) over the specified input range.
4. This is the Absolute Value of Gain Change vs. Temperature in PPM level.
5. Nonlinearity is defined as half of the peak-to-peak output deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.
6. NL100 is the nonlinearity specified over an input voltage range of ±100 mV.
7. The input supply current decreases as the differential input voltage (V_{IN+}–V_{IN-}) decreases.
8. The maximum specified output supply current occurs when the differential input voltage (V_{IN+}–V_{IN-}) = -200 mV, the maximum recommended operating input voltage. However, the output supply current will continue to rise for differential input voltages up to approximately -300 mV, beyond which the output supply current remains constant.
9. Because of the switched-capacitor nature of the input sigma-delta converter, time-averaged values are shown.
10. When the differential input signal exceeds approximately 308 mV, the outputs will limit at the typical values shown.
11. Short circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground.
12. CMRR is defined as the ratio of the differential signal gain (signal applied differentially between pins 2 and 3) to the common-mode gain (input pins tied together and the signal applied to both inputs at the same time), expressed in dB.
13. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 400 kHz at room temperature), and is not attenuated by the internal output filter. A filter circuit can be easily added to the external post-amplifier to reduce the total RMS output noise. The internal output filter does eliminate most, but not all, of the sigma-delta quantization noise. The magnitude of the output quantization noise is very small at lower frequencies (below 10kHz) and increases with increasing frequency.
14. CMTI (Common Mode Transient Immunity or CMR, Common Mode Rejection) is tested by applying an exponentially rising/falling voltage step on pin 4 (GND1) with respect to pin 5 (GND2). The rise time of the test waveform is set to approximately 50 ns. The amplitude of the step is adjusted until the differential output (V_{OUT+}–V_{OUT-}) exhibits more than a 200 mV deviation from the average output voltage for more than 1µs. The ACPL-782T will continue to function if more than 10 kV/µs common mode slopes are applied, as long as the breakdown voltage limitations are observed.
15. Datasheet value is the differential amplitude of the transient at the output of the ACPL-782T when a 1 V_{pk-pk}, 1 MHz square wave with 40 ns rise and fall times is applied to both V_{DD1} and V_{DD2}.
16. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V_{RMS} for 1 second (leakage detection current limit, II-O ≤ 5 µA). This test is performed before the 100% production test for partial discharge (method b) shown in IEC 60747-5-5/DIN EN 60747-5-2 Insulation Characteristic Table.
17. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refers to the IEC 60747-5-5/DIN EN 60747-5-2 insulation characteristics table and your equipment level safety specification.
18. This is a two-terminal measurement: pins 1–4 are shorted together and pins 5–8 are shorted together.

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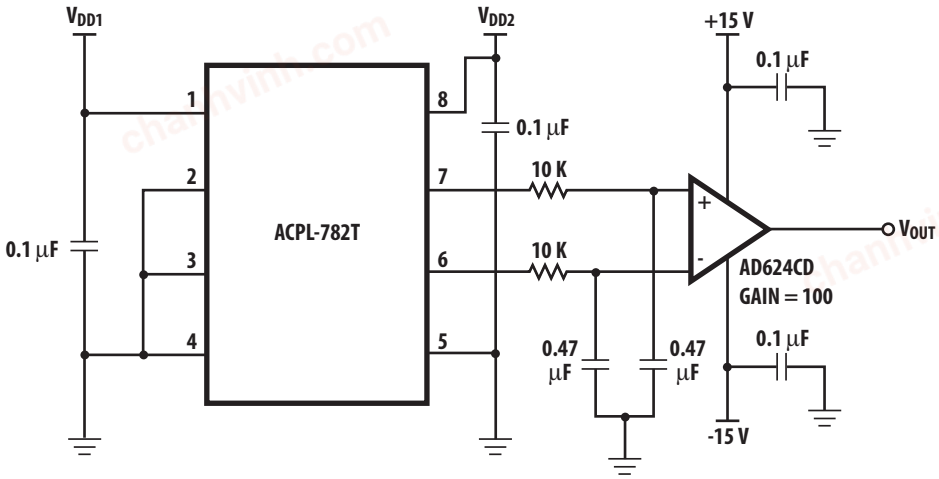

Figure 1. Input Offset Voltage Test Circuit.

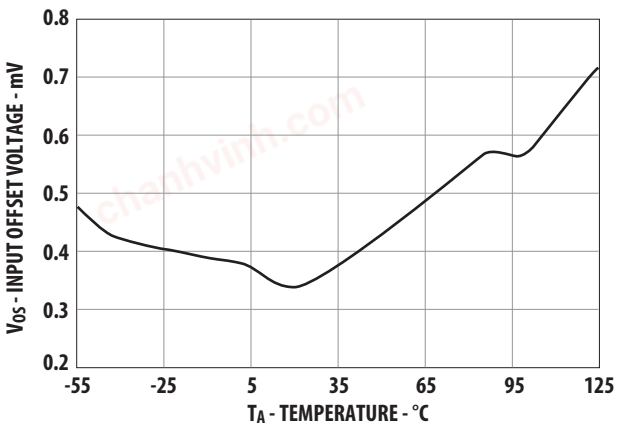

Figure 2. Input Offset Voltage vs. Temperature.

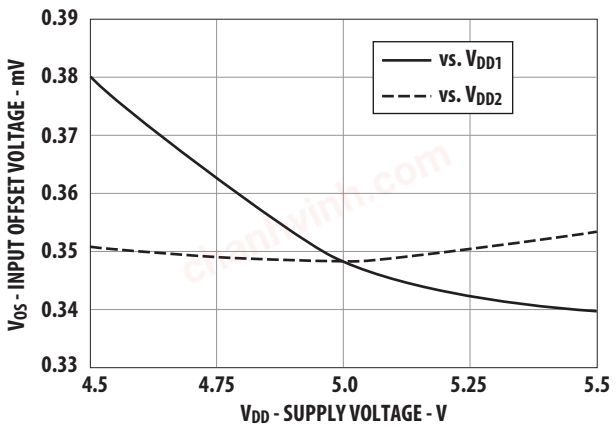

Figure 3. Input Offset Voltage vs. Supply.

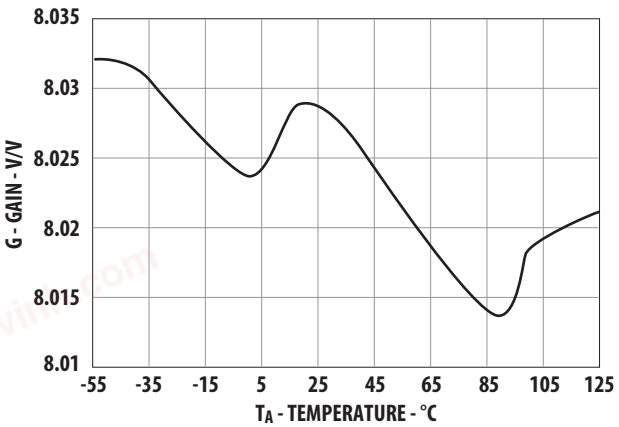

Figure 4. Gain vs. Temperature.

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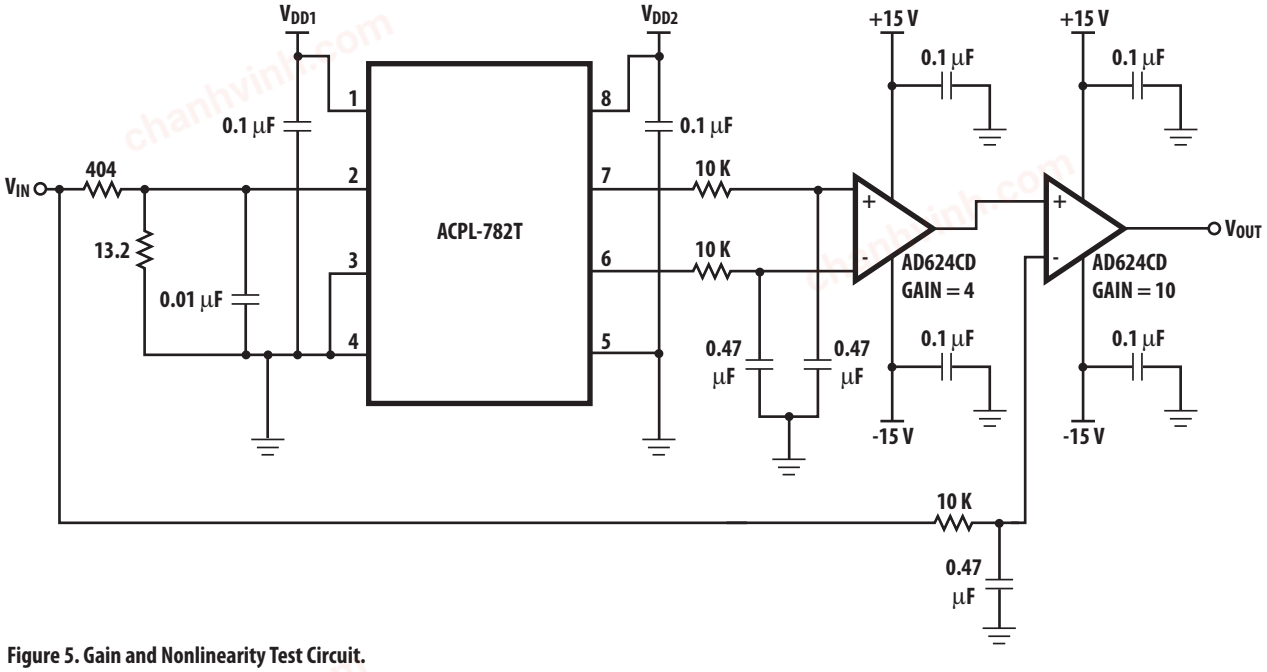

Figure 5. Gain and Nonlinearity Test Circuit.

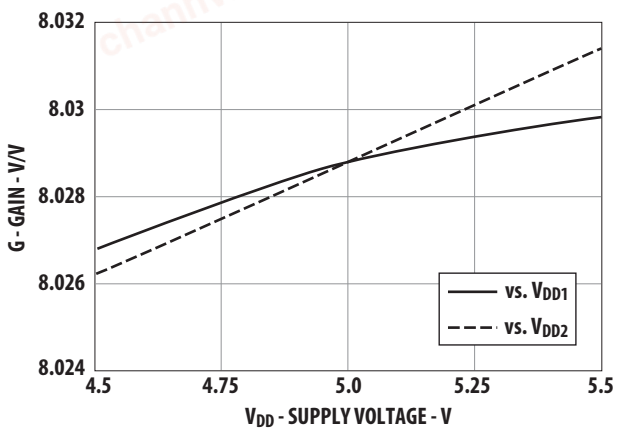

Figure 6. Gain vs. Supply.

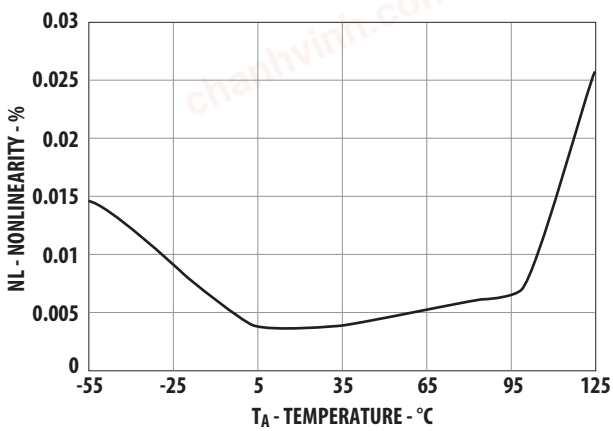

Figure 7. Nonlinearity vs. Temperature.

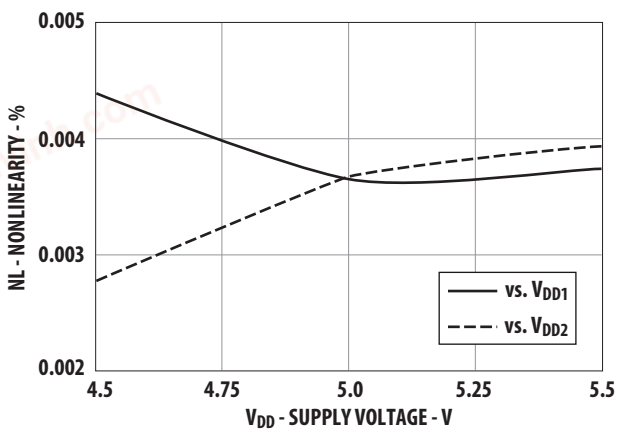

Figure 8. Nonlinearity vs. Supply.

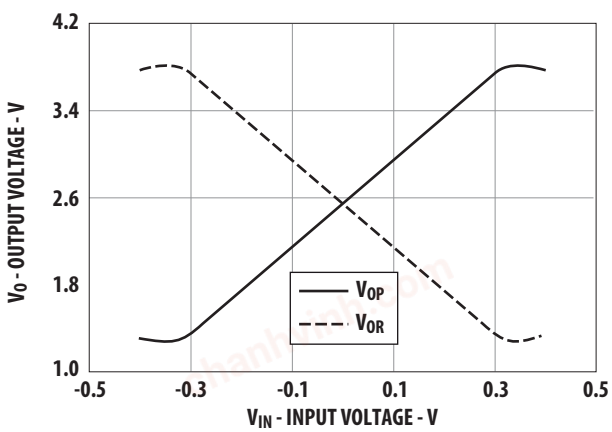

Figure 9. Output Voltage vs. Input Voltage.

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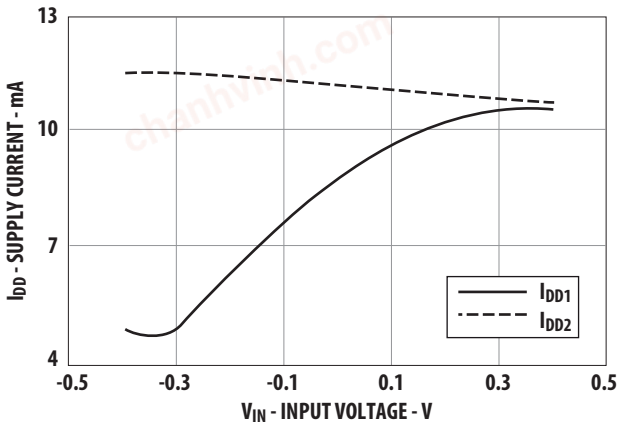

Figure 10. Supply Current vs. Input Voltage.

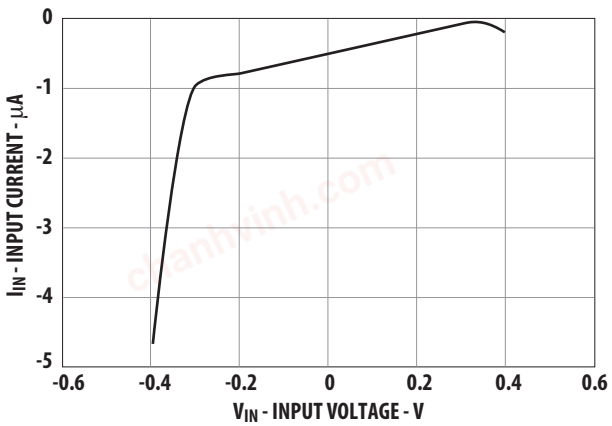

Figure 11. Input Current vs. Input Voltage.

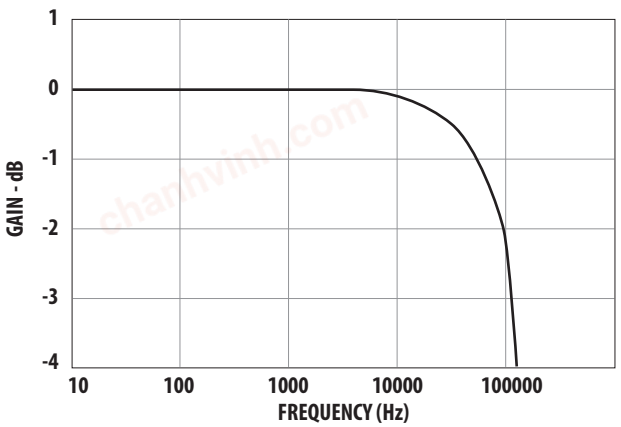

Figure 12. Gain vs. Frequency.

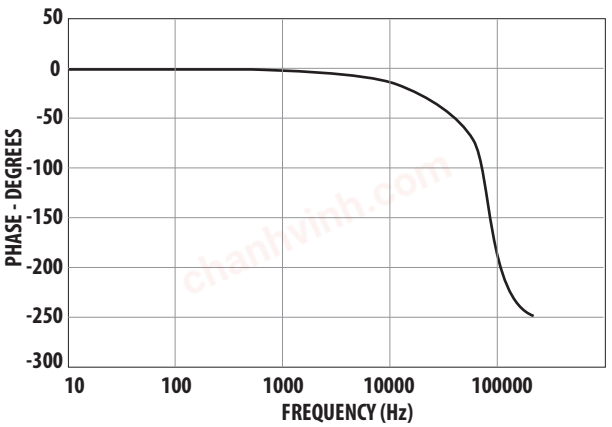

Figure 13. Phase vs. Frequency.

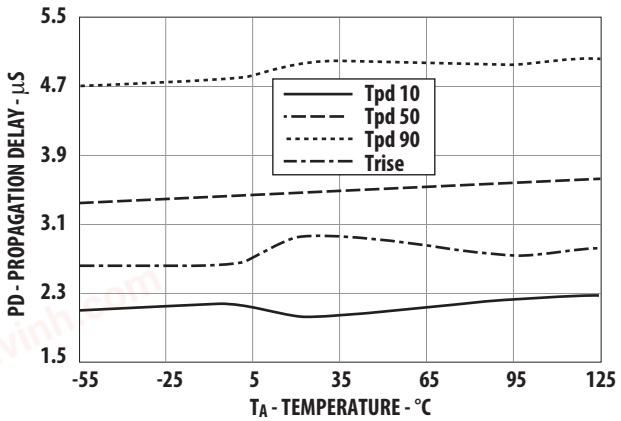

Figure 14. Propagation Delay vs. Temperature.

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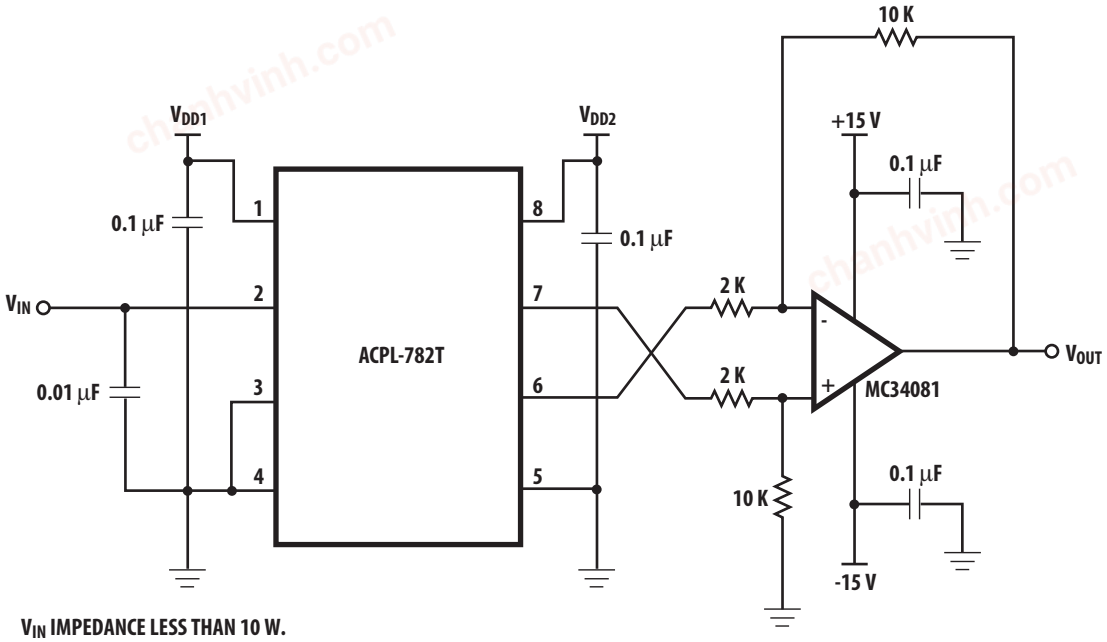

V_{IN} IMPEDANCE LESS THAN 10 W.

Figure 15. Propagation Delay Test Circuits.

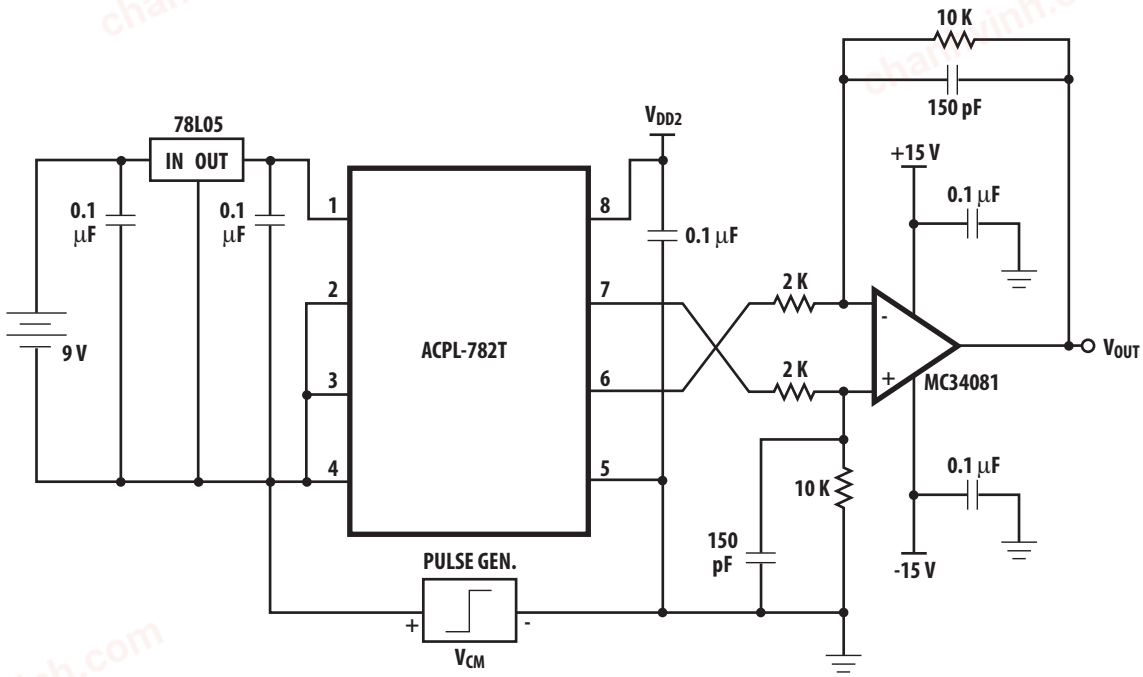

Figure 16. CMTI Test Circuits.

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Application Information

Power Supplies and Bypassing

The recommended supply connections are shown in Figure 17. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple zener diode (D1); the value of resistor R4 should be chosen to supply sufficient current from the existing floating supply. The voltage from the current sensing resistor (Rsense) is applied to the input of the ACPL-782T through an RC anti-aliasing filter (R2 and C2). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

The power supply for the ACPL-782T is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

An inexpensive 78L05 three-terminal regulator can also be used to reduce the floating supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 18, 0.1 µF bypass capacitors (C1, C2) should be located as close as possible to the pins of the ACPL-782T. The bypass capacitors are required because of the high-speed digital nature of the signals inside the ACPL-782T. A 0.01µF bypass capacitor (C2) is also recommended at the input due to the switched-capacitor nature of the input circuit. The input bypass capacitor also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal. The input filter also performs an important reliability function—it reduces transient spikes from ESD events flowing through the current sensing resistor.

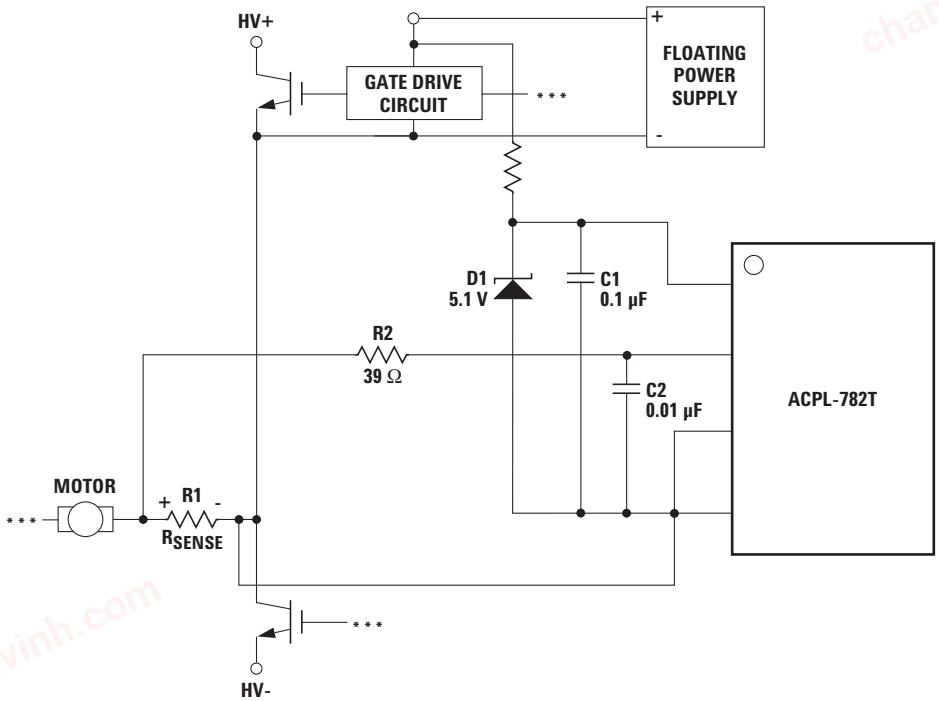

Figure 17. Recommended Supply and Sense Resistor Connections.

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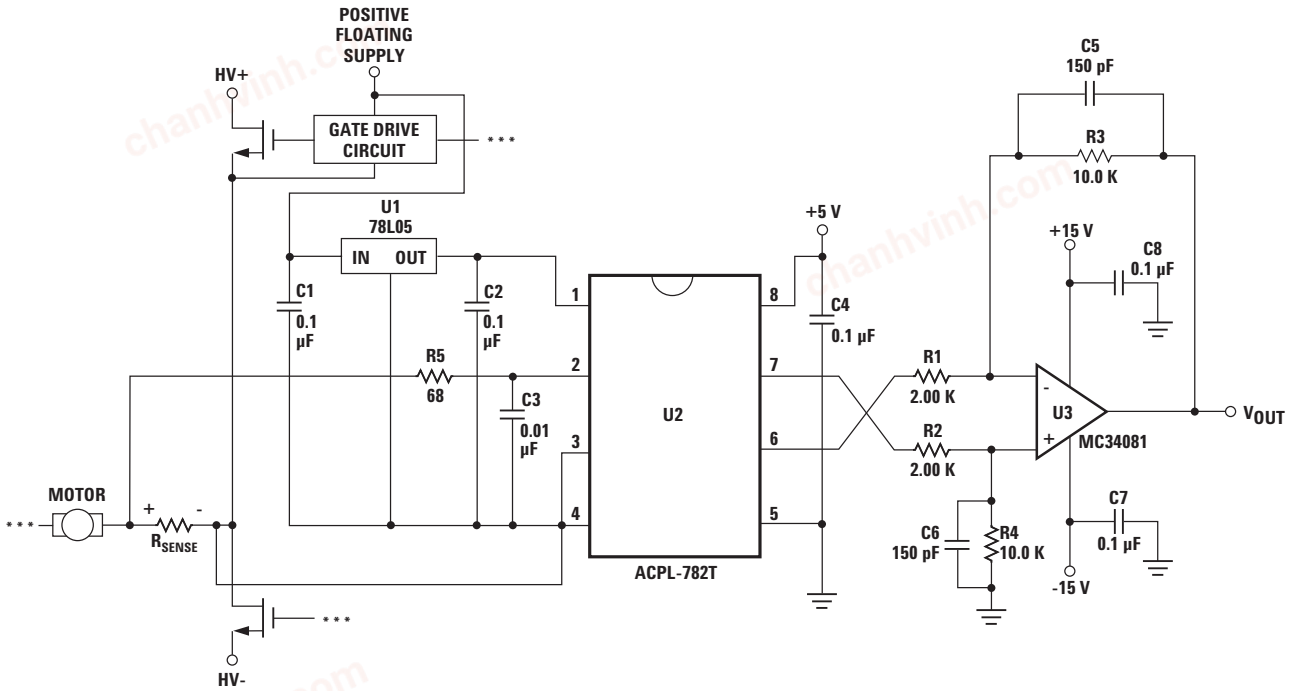

Figure 18. Recommended Application Circuit.

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. In addition, the layout of the PCB can also affect the isolation transient immunity (CMTI) of the ACPL-782T, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMTI performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the ACPL-782T.

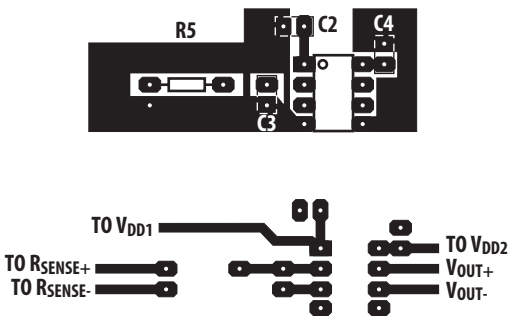

Figure 19. Example Printed Circuit Board Layout.

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Current Sensing Resistors

The current sensing resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistance decreases power dissipation, while larger sense resistance can improve circuit accuracy by utilizing the full input range of the ACPL -782T.

The first step in selecting a sense resistor is determining how much current the resistor will be sensing. The graph in Figure 20 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the sense resistor is determined by the current being measured and the maximum recommended input voltage of the isolation amplifier. The maximum sense resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the sense resistor should see during normal operation. For example, if a motor will have a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (=10 x 1.414 x 1.5). Assuming a maximum input voltage of 200 mV, the maximum value of sense resistance in this case would be about 10 mΩ.

The maximum average power dissipation in the sense resistor can also be easily calculated by multiplying the sense resistance times the square of the maximum RMS current, which is about 1 W in the previous example. If the power dissipation in the sense resistor is too high, the resistance can be decreased below the maximum value to decrease power dissipation. The minimum value of the sense resistor is limited by precision and accuracy requirements of the design. As the resistance value is reduced, the output voltage across the resistor is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the sense resistor will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

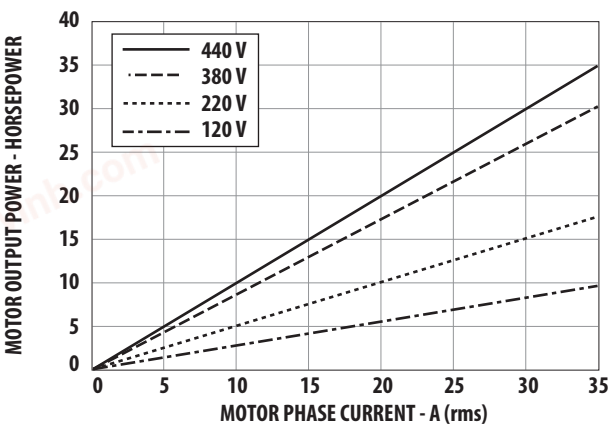

Figure 20. Motor Output Horsepower vs. Motor Phase Current and Supply Voltage.

When sensing currents large enough to cause significant heating of the sense resistor, the temperature coefficient (tempco) of the resistor can introduce nonlinearity due to the signal dependent temperature rise of the resistor. The effect increases as the resistor-to-ambient thermal resistance increases. This effect can be minimized by reducing the thermal resistance of the current sensing resistor or by using a resistor with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the current sensing resistor on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal current sensing resistor, as the value of resistance decreases, the resistance of the leads become a significant percentage of the total resistance. This has two primary effects on resistor accuracy. First, the effective resistance of the sense resistor can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the leads during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material, such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco overall.

Both of these effects are eliminated when a four-terminal current sensing resistor is used. A four- terminal resistor has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

When laying out a PC board for the current sensing resistors, a couple of points should be kept in mind. The Kelvin connections to the resistor should be brought together under the body of the resistor and then run very close to each other to the input of the ACPL-782T; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the sense resistor is not located on the same PC board as the ACPL-782T circuit, a tightly twisted pair of wires can accomplish the same thing.

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Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the sense resistor to help distribute the current between the layers of the PC board. The PC board should use 2 or 4 oz. copper for the layers, resulting in a current carrying capacity in excess of 20 A.

Note: Please refer to Avago Technologies Application Note 1078 for additional information on using Isolation Amplifiers.

Sense Resistor Connections

The recommended method for connecting the ACPL-782T to the current sensing resistor is shown in Figure 18. V_{IN+} (pin 2 of the APCL-782T) is connected to the positive terminal of the sense resistor, while VIN- (pin 3) is shorted to GND1 (pin 4), with the power-supply return path functioning as the sense line to the negative terminal of the current sense resistor. This allows a single pair of wires or PC board traces to connect the ACPL-782T circuit to the sense resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the resistor are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current sensing resistor.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the ACPL-782T to the sense resistor be the only return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the ACPL-782T circuit and the gate drive circuit should be the positive power supply line.

Output Side

The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier. Many different op-amps could be used in the circuit, including: TL032A, TL052A, and TLC277 (Texas Instruments), LF412A (National Semiconductor).

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

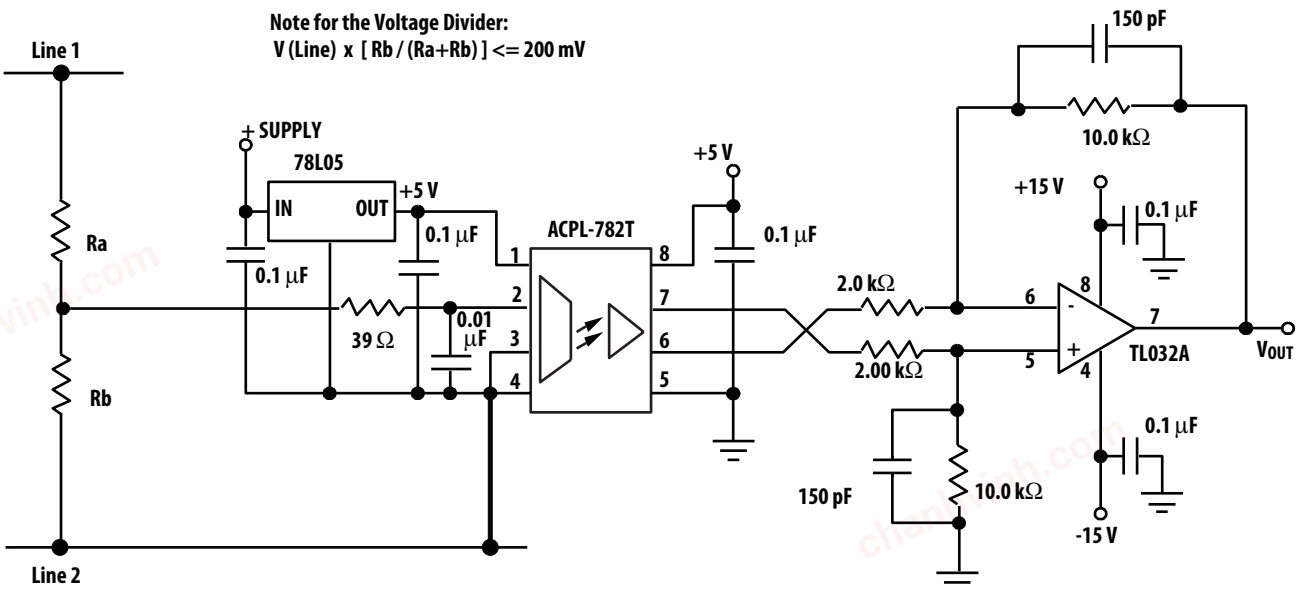

Figure 21. Recommended circuit for voltage sensing application.

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Voltage sensing for DC rail measurement

ACPL-782T is a suitable device to measure the DC rail voltage over different potentials. In a DC rail voltage sensing application, the Line1 and Line2 in Figure 21 are the DC lines to be measured.

Dividing ratio error due to the tolerances of the resistors

From a differential calculation, the error in the voltage divider of Ra and Rb is expressed as

$$\Delta A/A = Ra/(Ra + Rb) * (\Delta Rb/Rb - \Delta Ra/Ra) \quad (1)$$

Where A is the ratio of the resistor divider consisting of Ra and Rb.

Since the errors of the resistors, ΔRb/Rb and ΔRa/Ra are independent to each other, we need to take absolute values in equation (1) to know the maximum possible gain error of the divider and it gives

$$\Delta A/A = Ra/(Ra + Rb) * (|\Delta Rb/Rb| + |\Delta Ra/Ra|) \quad (2)$$

Figure 22 is the plot of the equation (2) when the resistors have 1% tolerance expressing the relationship between the ratio of Ra to (Ra+Rb) and the possible maximum error of the dividing ratio.

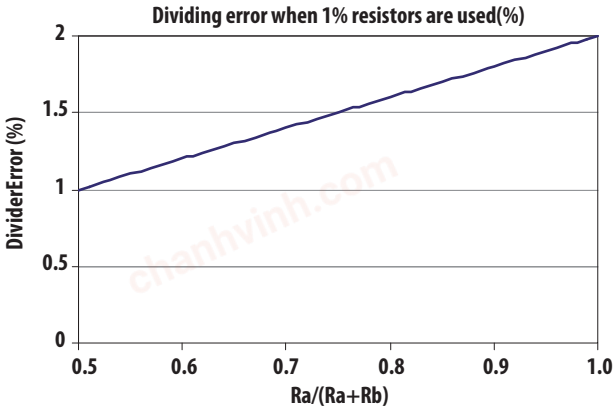
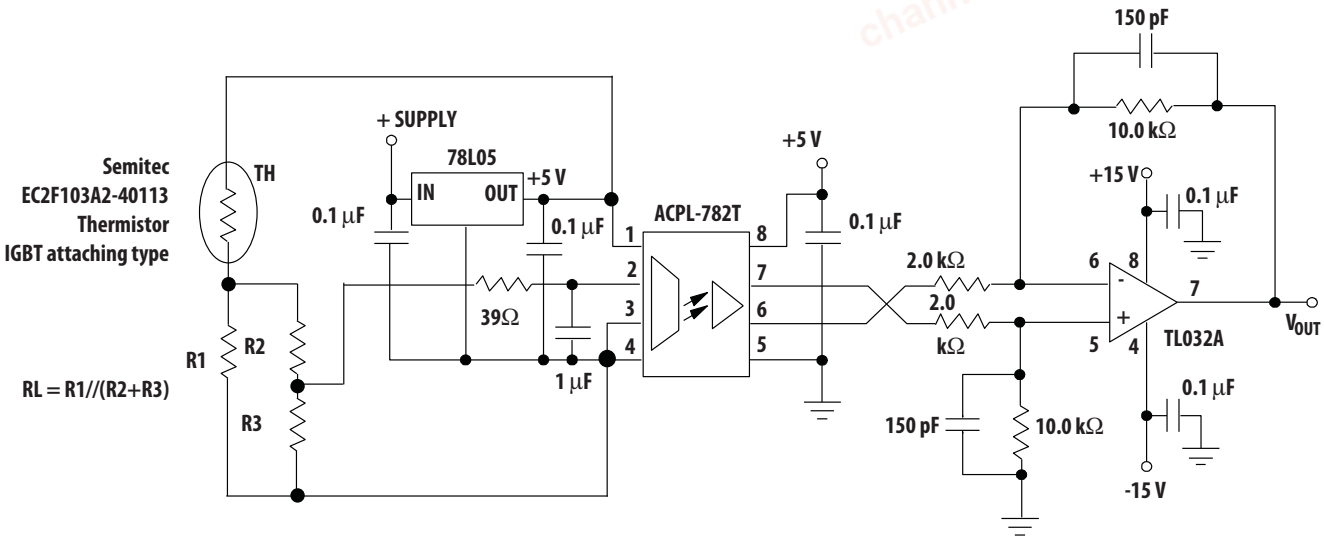


Figure 22: Divider Error % Vs Resistors Divider



Note on the thermistor and the RL:
V_{dd} x [RL/(Rth + RL)] x [R3/(R2 + R3)] <= 200 mV, assuming R2+R3 >> R1
Rth: Resistance of thermistor
RL: Linearizing resistor value = R1//(R2+R3)

Figure 23. Recommended circuit for temperature sensing application.

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Isolated Temperature Sensing using Thermistor

Thermistor is widely used to measure temperatures in most systems application. A galvanic isolation between the potential of the Thermistor and that of the analog-to-digital is often required when they are mounted in locations such as high voltage potential, electrically noisy environments, poorly grounded environments, where lack of isolation causes either safety or EMI issues.

RL = R1//(R2+R3)=R1(R2+R3)/(R1+R2+R3)

R2 and R3 divides the voltage across RL so that the voltage fed into ACPL-782T does not exceed +200 mV. The high impedance characteristic of the input terminals of ACPL-782T helps in determining those resistors value since one can select relatively high resistance of R2 and R3 and R1 can be determined easily.

If R2+R3 >> R1, RL ~ R1
Dividing ratio ~ R3/(R2+R3)

As can be seen from the circuit, one might eliminate R1 and RL~(R2+R3) in this case.

An application example with a Thermistor designed for measuring IGBT's surface temperatures is shown in Figure 23. Where TH is the thermistor and the RL is a resistor for linearization. Suitable RL value is determined from the Thermistor characteristic and the temperature range to measure. Please note that the RL value is the compound value of R1, R2 and R3.

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