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BROADCOM®

Data Sheet

ACPL-352J

5.0 Amp Output Current IGBT and SiC/GaN MOSFET Gate Drive Optocoupler with Integrated Overcurrent Sensing, FAULT, GATE, and UVLO Status Feedback

Description

The Broadcom® ACPL-352J is a 5.0A intelligent gate drive optocoupler. The high peak output current and wide operating voltage range make it ideal for driving IGBT or SiC/GaN MOSFET directly in motor control and inverter applications.

The device features fast propagation delay with excellent timing skew performance. It provides IGBT/MOSFET with overcurrent protection and functional safety reporting. This full-featured and easy-to-implement gate drive optocoupler comes in a compact, surface-mountable SO-16 package. It provides reinforced insulation certified for safety regulatory IEC/EN/DIN, UL and CSA.

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Features

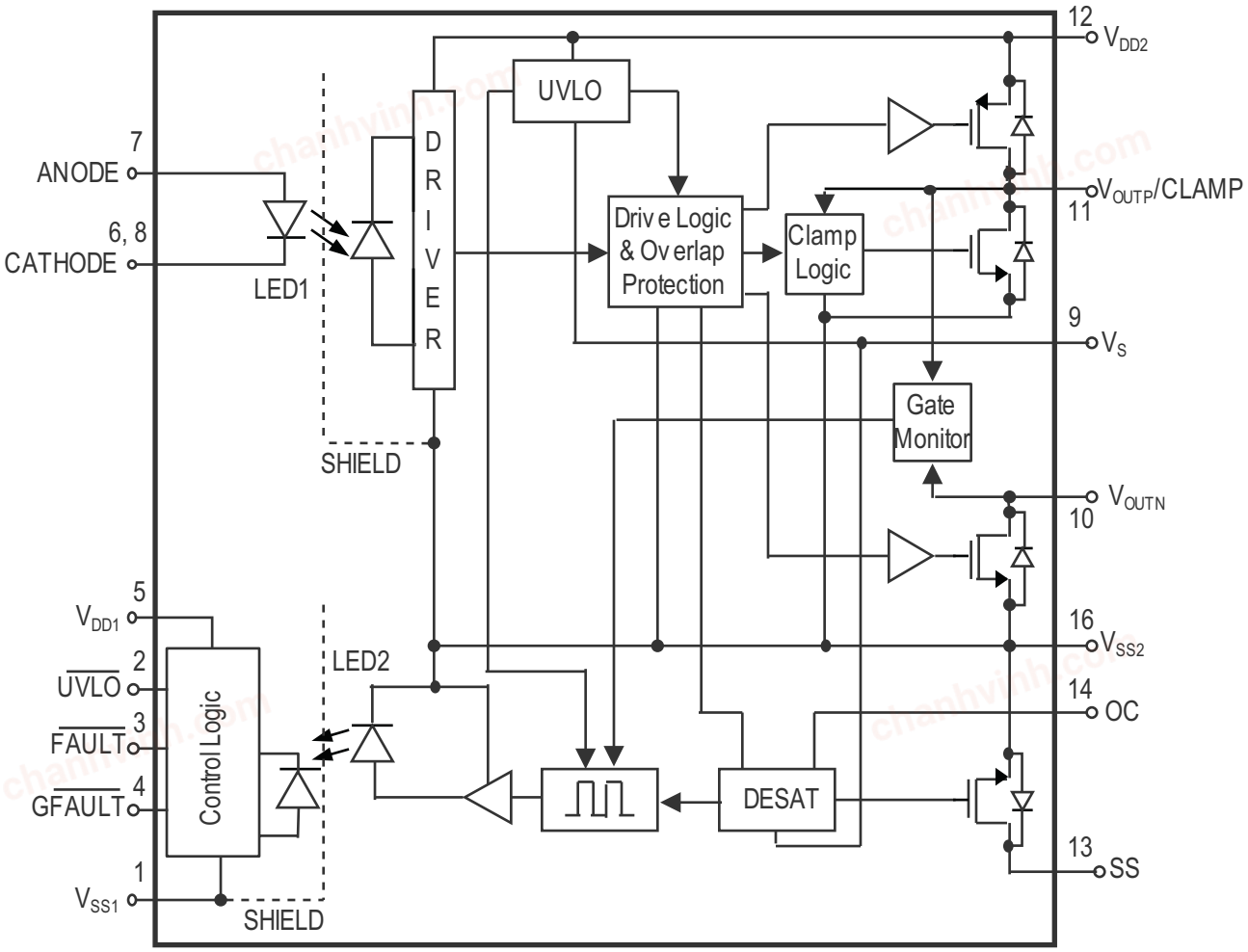
- 5.0A maximum peak output current
- 4.5A minimum peak output current
- 150-ns maximum propagation delay
- Dual output drive to control turning on and off time
- Overcurrent detection with configurable Soft shutdown
- Functional safety reporting:
  - Overcurrent FAULT feedback
  - IGBT/MOSFET GATE status feedback
  - UVLO status feedback
- Under Voltage Lock-Out (UVLO) with hysteresis
- 100-kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500V
- 15V to 30V wide operating V_{DD2} range
- –40°C to 105°C industrial temperature range
- 8.3-mm creepage and clearance
- Safety approval:
  - UL Recognized 5000 V_{RMS} for 1min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1414 V_{PEAK}

Applications

- IGBT and SiC/GaN MOSFET gate drive
- Industrial drives and inverters
- Renewable energy inverters
- Switching power supplies

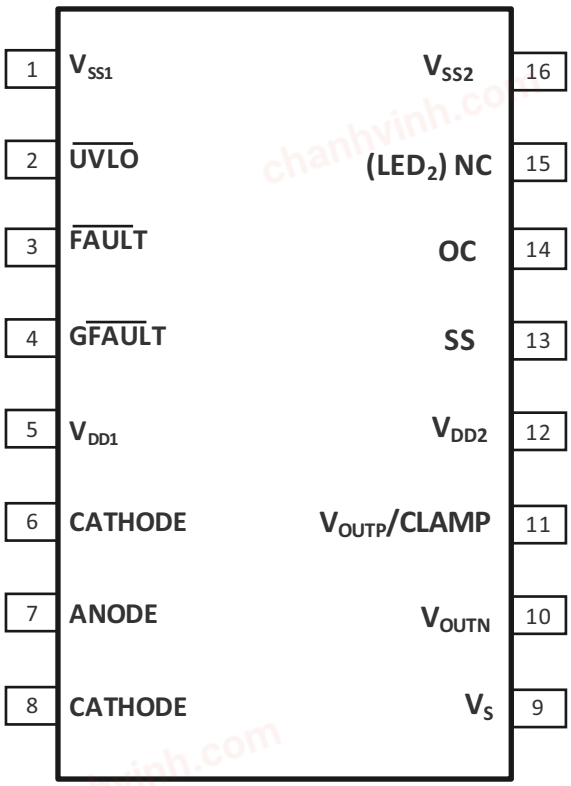
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Functional Diagram



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Pin Description



Pin	Symbol	Description
1	V_{SS1}	Input ground
2	UVLO	V_{DD2} under voltage lock out feedback
3	FAULT	Overcurrent fault feedback
4	GFAULT	IGBT/MOSFET Gate status feedback
5	V_{DD1}	Input power supply
6	CATHODE	Input LED cathode
7	ANODE	Input LED anode
8	CATHODE	Input LED cathode
9	V_S	Common (IGBT emitter or MOSFET source) output supply voltage.
10	V_{OUTN}	Driver output to turn off IGBT or MOSFET Gate
11	V_{OUTP}/CLAMP	Driver output to turn on IGBT or MOSFET Gate/Miller Clamp
12	V_{DD2}	Positive output power supply
13	SS	Soft shutdown
14	OC	Overcurrent input pin. When the voltage on OC pin exceeds an internal reference voltage of 9V while the IGBT/MOSFET is on, FAULT output is changed from logic high to low state.
15	(LED_2)NC	No connection
16	V_{SS2}	Negative output power supply

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Ordering Information

ACPL-352J is UL Recognized with 5000 Vrms for 1 minute per UL1577.

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
ACPL-352J	-000E	SO-16	X		X	45 per tube
	-500E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

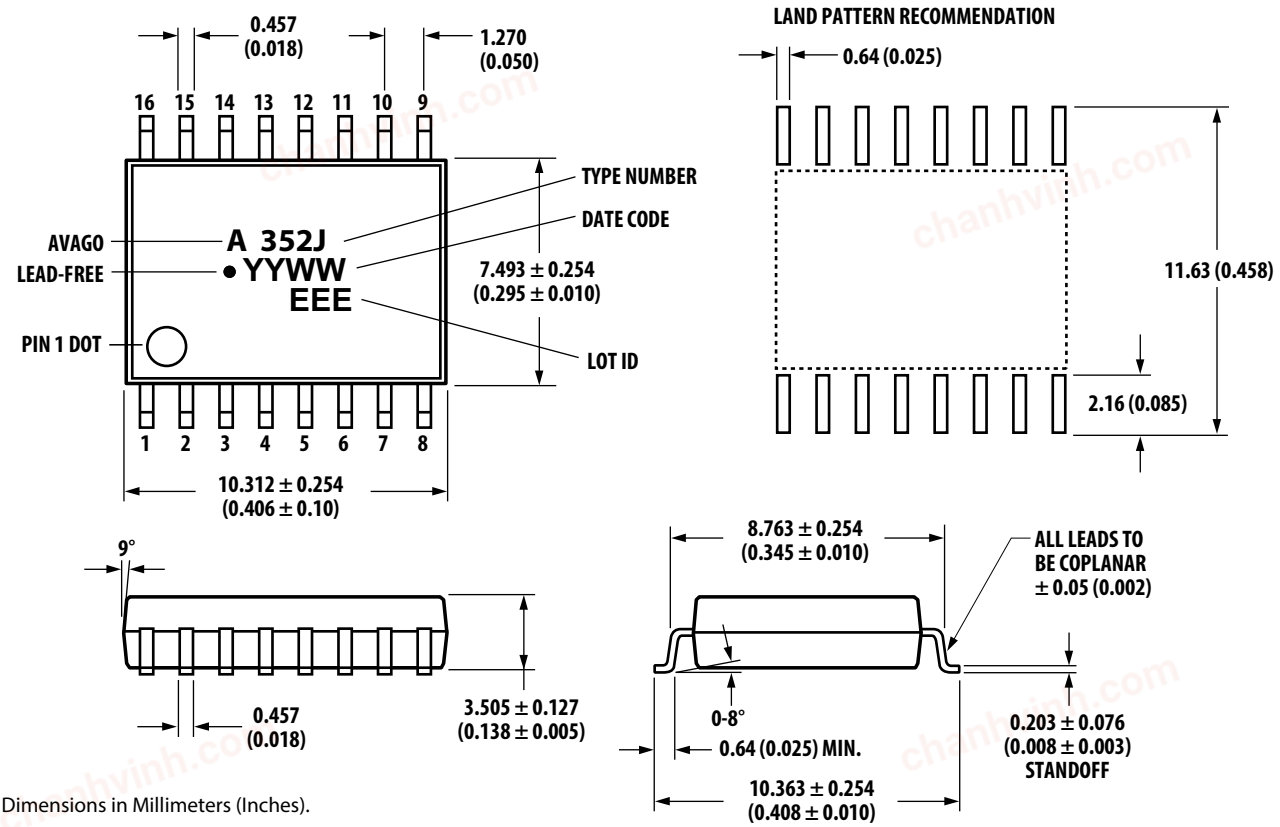
Example:

ACPL-352J-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

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ACPL-352J 16-Lead Surface Mount Package



Dimensions in Millimeters (Inches).

Floating lead protrusion is 0.25 mm (10 mils) Max.

Note: Initial and continued variation in color of the white mold compound is normal and does not affect performance or reliability of the device.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-352J is approved by the following organizations.

IEC/EN/DIN EN 60747-5-5	Maximum working insulation voltage V_{IORM} = 1414V_{PEAK}.
UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 $_{VRMS}$. File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.

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IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

NOTE: Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/39, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I - IV	
for rated mains voltage ≤ 300 V_{rms}		I - IV	
for rated mains voltage ≤ 600 V_{rms}		I - IV	
for rated mains voltage ≤1000 V_{rms}		I - III	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2652	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	2262	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage tini = 60 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values - maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	400	mA
Output Power	$P_{S, OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Avago Regulatory Guide to Isolation Circuits*, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

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Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-352J	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

NOTE: All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances also change depending on factors such as pollution degree and insulation level.

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	–40	105	°C	
Output IC Junction Temperature	T_J	—	125	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1-µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1.0	A	
Reverse Input Voltage	V_R	—	5	V	
High Peak Output Current	$I_{OH(PEAK)}$	—	5	A	b
Low Peak Output Current	$I_{OL(PEAK)}$	—	5	A	b
Positive Input Supply Voltage	V_{DD1}	0	7	V	
FAULT Output Current	I_{FAULT}	—	10	mA	
FAULT Pin Voltage	V_{FAULT}	–0.5	V_{DD1}	V	
Total Output Supply Voltage	$(V_{DD2} – V_{SS2})$	–0.5	35	V	
Negative Output Supply Voltage	$(V_S – V_{SS2})$	–0.5	17	V	
Positive Output Supply Voltage	$(V_{DD2} – V_S)$	–0.5	$35 – (V_S – V_{SS2})$	V	
Input Current (Rise/Fall Time)	$t_{r(IN)}/t_{f(IN)}$	—	500	ns	
High Side Pull Up Voltage	V_{OUTP}	$V_{SS2} – 0.5$	$V_{DD2} + 0.5$	V	
Low Side Pull Down Voltage	V_{OUTN}	$V_{SS2} –0.5$	$V_{DD2} + 0.5$	V	
Overcurrent Pin Voltage	V_{OC}	$V_S – 0.5$	$V_{DD2} + 0.5$	V	
Peak Clamp Sinking Current	I_{CLAMP}	—	3	A	b
Miller Clamp Pin Voltage	V_{CLAMP}	$V_{SS2} – 0.5$	$V_{DD2} + 0.5$	V	
Output IC Power Dissipation	P_O	—	600	mW	c
Input LED Power Dissipation	P_I	—	110	mW	d

a. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 10 µs.The output must be limited to –5.0A/5.0A of peak current by external resistors. See Supply and Ground Planes Layout and Loading Conditions section in the Application Information to prevent output noise at 5A rated current.

c. Derate linearly above 95°C free-air temperature at a rate of 20 mW/°C.

d. Derate linearly above 95°C free-air temperature at a rate of 3.7 mW/°C. The maximum LED junction temperature should not exceed 125°C.

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Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	–40	105	°C	
Positive Input Supply Voltage	V_{DD1}	4.5	5.5	V	
Total Output Supply Voltage	$(V_{DD2} – V_{SS2})$	15	30	V	
Negative Output Supply Voltage	$(V_S – V_{SS2})$	0	15	V	
Positive Output Supply Voltage	$(V_{DD2} – V_S)$	15	$30 – (V_S – V_{SS2})$	V	
Input Current (ON)	$I_{F(ON)}$	8	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	0.8	V	

Electrical Specifications (DC)

All typical values at T_A = 25°C, V_{DD1} = 5V, $V_{DD2} – V_S$ = 15V, $V_S – V_{SS2}$ = 15V; All minimum and maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
V_{OUTP} High Level Peak Output Current	I_{OH}	–4.5	9.0	—	A	$V_{DD2} – V_{OUTP}$ =15V	3	a
V_{OUTN} Low Level Peak Output Current	I_{OL}	4.5	7.0	—	A	$V_{OUTN} – V_{SS2}$ = 15V	4	a
V_{OUTP} Output PMOS $R_{DS(ON)}$	R_{OUTP}	0.4	0.7	1.5	Ω	I_{OP} = –4.5A, I_F = 8 mA	5	a
V_{OUTN} Output NMOS $R_{DS(ON)}$	R_{OUTN}	0.3	0.6	1.2	Ω	I_{ON} = 4.5A, V_F = 0V	6	a
V_{OUTP} Output Voltage	V_{OH}	V_{DD2} – 0.60	V_{DD2} – 0.06	—	V	I_{OP} = –100 mA, I_F = 8 mA	1	b, c
V_{OUTN} Output Voltage	V_{OL}	—	V_{SS2} + 0.04	V_{SS2} + 0.60	V	I_{ON} = 100 mA, V_F = 0V	2	
Clamp Threshold Voltage	V_{TH_CLAMP}	—	2	3	V			
Clamp Low Level Sinking Current	I_{CLAMP}	2	2.5	—	A	V_{CLAMP} = V_{SS2} + 2.5V	7	
Clamp Output Transistor $R_{DS(ON)}$	$R_{DS,CLAMP}$	—	0.9	2	Ω	I_{CLAMP} = 2.5A		
SS Pull Down Current	I_{OSS}	70	140	—	mA	SS – V_{SS2} ≥15V, I_F = 8 mA, OC= Open	8	
SS R_{DSON}	R_{OUTSS}	—	16	40	Ω	I_{SS} = 70 mA, I_F = 8 mA, OC = Open		
High Level Output Supply Current (V_{DD2})	I_{DD2H}	—	5.7	7.5	mA	I_F = 8 mA, No Load	9	
Low Level Output Supply Current (V_{DD2})	I_{DD2L}	—	4.8	6.5	mA	V_F = 0V, No Load	9	
High Level Output Supply Current (V_{SS2})	I_{SS2H}	–2.2	–1.7	—	mA	I_F = 8 mA, No Load	10	
Low Level Output Supply Current (V_{SS2})	I_{SS2L}	–1.2	–0.8	—	mA	V_F = 0V, No Load	10	
Input Threshold Current Low to High	I_{FLH}	0.5	2	6.5	mA		11, 12	

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Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Threshold Voltage High to Low	V_{FHL}	0.8	—	—	V			
Input Forward Voltage	V_F	1.2	1.55	1.95	V	I_F = 8 mA		
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.7	—	mV/°C	I_F = 8 mA		
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 100 µA		
Input Capacitance	C_{IN}	—	70	—	pF	f = 1 MHz, V_F = 0V		
UVLO Threshold, $V_{DD2} – V_S$	V_{UVLO+}	12	12.9	13.5	V	I_F = 8 mA, $V_{OUTP} – V_E$ > 5V		b, c, d
	V_{UVLO-}	11	11.8	12.5	V	I_F = 8 mA, $V_{OUTP} – V_E$ < 5V		b, c, e
UVLO Hysteresis, $V_{DD2} – V_S$	$V_{UVLO+} – V_{UVLO–}$	0.5	1	—	V			
OC Sensing Voltage Threshold	V_{OC}	8.5	9	9.5	V	$V_{DD2} – V_S > V_{UVLO+}$	13	c
Blanking Capacitor Charging Current	I_{CHG}	0.85	1	1.15	mA	V_{OC} = 2V	14	c, f
OC Low Voltage when Blanking Capacitor Discharge	V_{DSCHG}	—	1.1	2	V	I_{DSCHG} = 50 mA		c, f
Input Supply Current (V_{DD1})	I_{DD1}	—	1.6	2.5	mA		15	
FAULT Logic Low Output Current	I_{FAULTL}	4	9.2	—	mA	V_{FAULT} = 0.4V, V_{DD1} = 5V		
FAULT Logic High Output Current	I_{FAULTH}	—	—	20	µA	$V_{FAULT} = V_{DD1}$ = 5V		
UVLO Logic Low Output Current	I_{UVLOL}	4	9.2	—	mA	V_{UVLO} = 0.4V, V_{DD1} = 5V		
UVLO Logic High Output Current	I_{UVLOH}	—	—	20	µA	$V_{UVLO} = V_{DD1}$ = 5V		
V_{OUTN} GFAULT Sense Threshold Voltage	$V_{GFAULTN}$	—	$V_{DD2} – 2$	—	V			
V_{OUTP} GFAULT Sense Threshold Voltage	$V_{GFAULTP}$	—	$V_{SS2} + 2$	—	V			
GFAULT Logic Low Output Current	$I_{GFAULTL}$	4	9.2	—	mA	V_{GFAULT} = 0.4V, V_{DD1} = 5V		
GFAULT Logic High Output Current	$I_{GFAULTH}$	—	—	20	µA	$V_{GFAULT} = V_{DD1}$ = 5V		

a. Output is sourced at –4.5A /4.5A with a maximum pulse width = 10 µs.

b. 15V is the recommended minimum operating positive supply voltage ($V_{DD2} – V_S$) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 13.5V. For High Level Output Voltage testing, V_{OUTP} is measured with a 50-µs pulse load current. When driving capacitive loads, V_{OUTP} approaches V_{DD2} as I_{OUTP} approaches zero units.

c. Once the system is out of UVLO ($V_{DD2} – V_S > V_{UVLO+}$), the OC detection feature of the ACPL-352J is the primary source of IGBT/MOSFET protection. UVLO needs to be unlocked to ensure OC is functional. Once V_{DD2} exceeds V_{UVLO+} threshold, OC remains functional until V_{DD2} is below VUVLO– threshold. The OC detection and UVLO features of the ACPL-352J work in conjunction to ensure constant IGBT/MOSFET protection.

d. This is the *increasing* (that is, turn-on or *positive going* direction) of $V_{DD2} – V_S$.

e. This is the *decreasing* (that is, turn-off or *negative going* direction) of $V_{DD2} – V_S$.

f. See the overcurrent fault detection blanking time section in the applications notes at the end of this data sheet for further details.

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Switching Specifications (AC)

All typical values at T_A = 25°C, V_{DD1} = 5V, $V_{DD2} – V_S$ = 15V, $V_S – V_{SS2}$ = 15V; All minimum and maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High V_{OUTP} Output Level	t_{PLH}	40	100	150	ns	R_{GP} = 5Ω, R_{GN} = 5Ω, C_G = 5nF, f = 20 kHz, Duty Cycle = 50% I_F = 8 mA	16, 17, 22	a
Propagation Delay Time to Low V_{OUTN} Output Level	t_{PHL}	40	90	150	ns			b
Pulse Width Distortion	PWD	–50	10	50	ns			c
Propagation Delay Difference Between Any Two Parts	PDD ($t_{PLH} – t_{PHL}$)	–75	—	75	ns			d
Propagation Delay Skew	t_{PSK}	—	—	60	ns			e
10% to 90% Rise Time on V_{OUTP}	t_R	—	37	—	ns	R_{GP} = 5Ω, R_{GN} = 5Ω, C_G = 2nF, f = 20 kHz, Duty Cycle = 50%, I_F = 8 mA.		
90% to 10% Fall Time on V_{OUTN}	t_F	—	30	—	ns			
OC Blanking Time	$t_{OC(BLANKING)}$	—	0.75	1	µs	R_{GP} = 5Ω, R_{GN} = 5Ω, C_G = 5 nF, f = 100 Hz, Duty Cycle = 50%, I_F = 8 mA, R_{SS}=133Ω, C_F = 330 pF, R_F = 10 kΩ	21	f
OC Detection to 90% V_{GATE} Delay	$t_{OC(90\%)}$	—	0.13	—	µs		21	g
OC Detection to V_{GATE} = 2V Delay	$t_{OC(2V)}$	—	2.5	—	µs		21	h
OC Detection to OC Pull Low Propagation Delay	$t_{OC(LOW)}$	—	0.25	—	µs		21	i
OC Detection to SS Pull Low Propagation Delay	$t_{SS(LOW)}$	—	0.15	0.8	µs		18, 21	j
OC Detection to Low Level FAULT Signal Delay	$t_{OC(FAULT)}$	—	1.7	3	µs		21	k
Output Mute Time due to Overcurrent	$t_{OC(MUTE)}$	2	3	4	ms		19, 21	l
Time Input Kept Low Before Fault Reset to High	$t_{OC(RESET)}$	2	3	4	ms	C_F = 330 pF, R_F = 10 kΩ	19, 21	m
V_{DD2} to UVLO High Delay	t_{PLH_UVLO}	—	15	22	µs	C_U = 330 pF, R_U = 10 kΩ	23	n
V_{DD2} to UVLO Low Delay	t_{PHL_UVLO}	—	13	30	µs	C_U = 330 pF, R_U = 10 kΩ	23	o
V_{DD2} UVLO to V_{OUTP} High Delay	t_{UVLO_ON}	—	3	—	µs		23	p
V_{DD2} UVLO to V_{OUTN} Low Delay	t_{UVLO_OFF}	—	1.5	—	µs		23	q
Delay Time to V_{GATE} Status Check	t_{GFAULT}	7.5	9.5	13	µs		24	r
V_{GATE} Status Check to Low Level GFAULT Signal Delay	$t_{GFAULT(10\%)}$	—	13.5	17	µs	C_{GF} = 330 pF, R_{GF} = 10 kΩ	24	s
Input Logic Change to High Level GFAULT Signal Delay	$t_{GFAULT(90\%)}$	—	16	25	µs	C_{GF} = 330 pF, R_{GF} = 10 kΩ	24	t

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Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	100	—	—	kV/µs	T_A = 25°C, V_{CM} = 1500V, V_{DD1} = 5V, C_F = 330 pF, R_F = 10 kΩ, I_F = 8 mA		u, v
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	100	—	—	kV/µs	T_A = 25°C, V_{CM} = 1500V, V_{DD1} = 5V, C_F = 330 pF, R_F = 10 kΩ, V_F = 0V		v,w

a. t_{PLH} is defined as propagation delay from 50% of LED input I_F, to 50% of V_{OUTP} high level output.

b. t_{PHL} is defined as propagation delay from 50% of LED input I_F, to 50% of V_{OUTN} low level output.

c. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.

d. Propagation Delay Difference (PDD) is the difference between t_{PHL} and t_{PLH} between any two units under the same test condition.

e. Propagation Delay Skew (t_{PSK}) is the difference in t_{PH}L or t_{PLH} between any two units under the same test condition.

f. The internal delay time to respond to an OC fault condition without any external blanking capacitor.

g. The amount of time from when OC threshold is exceeded to 90% of V_{GATE} at mentioned test conditions.

h. The amount of time from when OC threshold is exceeded to V_{GATE} at 2V at mentioned test conditions.

i. The amount of time from when OC threshold is exceeded to 10% of OC low voltage.

j. The amount of time from when OC threshold is exceeded to 10% of SS (Soft Shut) low voltage.

k. The amount of time from when OC threshold is exceeded to FAULT output low.

l. The amount of time when OC threshold is exceeded, output is muted to LED input.

m. The amount of time when OC mute time is expired, LED input must be kept low for FAULT status to return to High.

n. The delay time when V_{DD2} exceeds UVLO+ threshold to UVLO high – 50% of UVLO positive-going edge.

o. The delay time when V_{DD2} exceeds UVLO– threshold to UVLO low – 50% of UVLO negative-going edge

p. The delay time when V_{DD2} exceeds UVLO+ threshold to 50% of V_{OUTP} high level output.

q. The delay time when V_{DD2} exceeds UVLO– threshold to 50% of V_{OUTN} low level output.

r. The delay to allow sufficient time for the gate to charge or discharge to its final level before checking gate voltage corresponds to LED input logic.

s. The delay time when gate voltage does not correspond to LED input logic to GFAULT output low.

t. The delay time when GFAULT returns to high after LED input logic change or gate voltage crosses the intended level threshold.

u. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output remains in the high state (that is, $V_{DD2} - V_{OUTP}$ < 1.0V or FAULT > 2V). V_{DD2} must be higher than V_{UVLO+}.

v. Split resistor network in the ratio 3:1 with 324Ω at the anode and 107Ω at the cathode.

w. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output remains in a low state (that is, $V_{OUTN} - V_{SS2}$ < 1.0V or FAULT > 2V). V_{DD2} must be higher than V_{UVLO+}.

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Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH < 50%, t = 1 min., T_A = 25°C		a, b, c
Input-Output Resistance	R_{I-O}	—	$>10^9$	—	Ω	V_{I-O} = 500V		c
Input-Output Capacitance	C_{I-O}	—	1.3	—	pF	freq = 1 MHz		
Thermal Coefficient Between								d
LED and Input IC	A_{EI}	—	35.4	—	°C/W			
LED and Output IC	A_{EO}	—	33.1	—	°C/W			
Input IC and Output IC	A_{IO}	—	25.6	—	°C/W			
LED and Ambient	A_{EA}	—	176.1	—	°C/W			
Input IC and Ambient	A_{IA}	—	92	—	°C/W			
Output IC and Ambient	A_{OA}	—	76.7	—	°C/W			

a. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table, if applicable.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.

c. Device considered a two-terminal device: Pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.

d. For further details, see the Thermal Calculation section in the Application Information.

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Figure 1: V_{OH} vs. Temperature

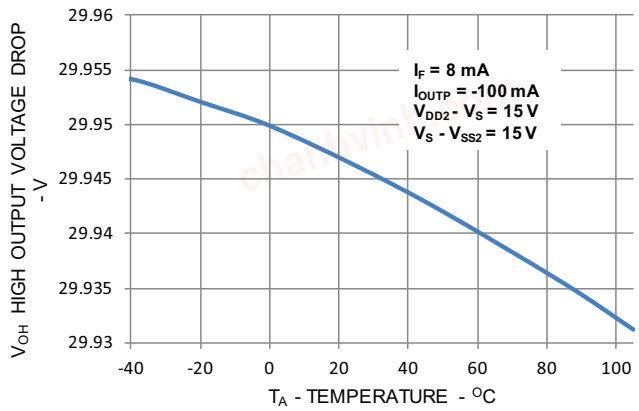


Figure 2: V_{OL} vs. Temperature

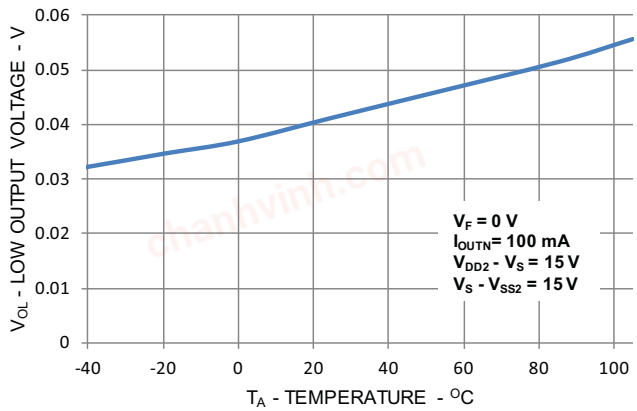


Figure 3: I_{OH} vs. V_{OH}

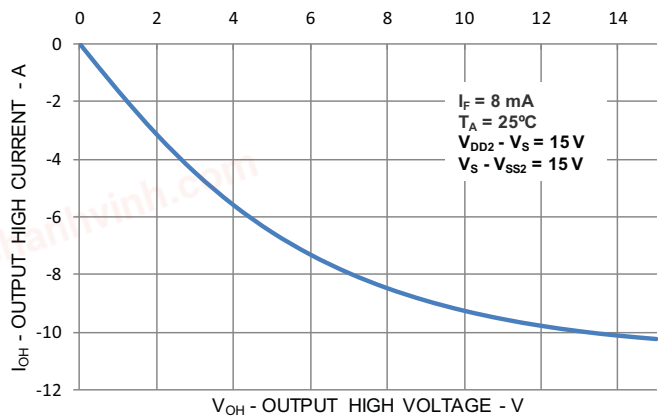


Figure 4: I_{OL} vs. V_{OL}

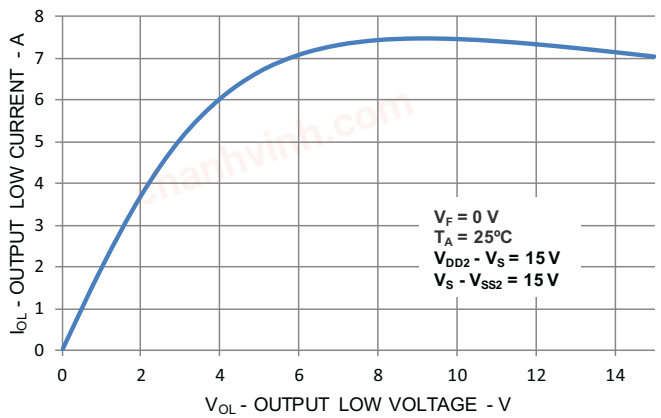


Figure 5: R_{OUTP} vs. Temperature

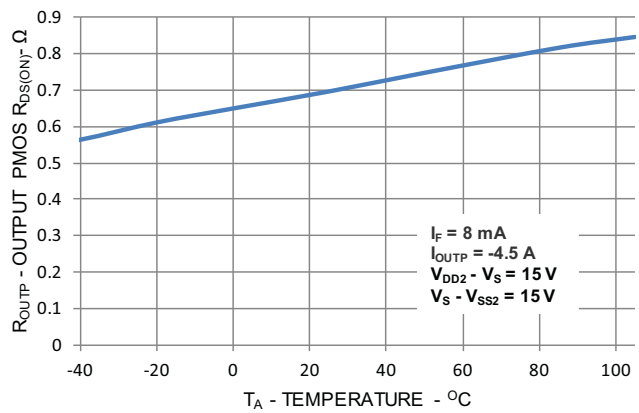
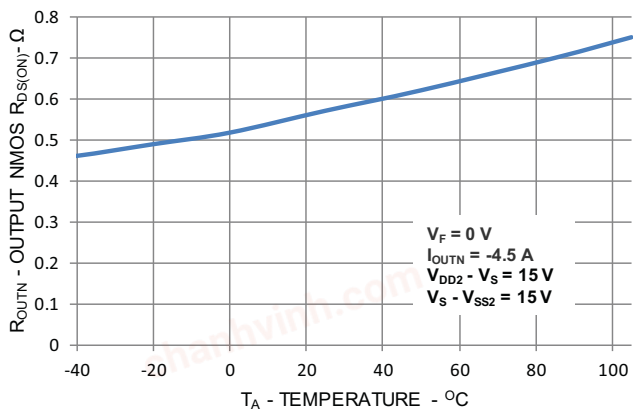


Figure 6: R_{OUTN} vs. Temperature



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Figure 7: I_{CLAMP} vs. Temperature

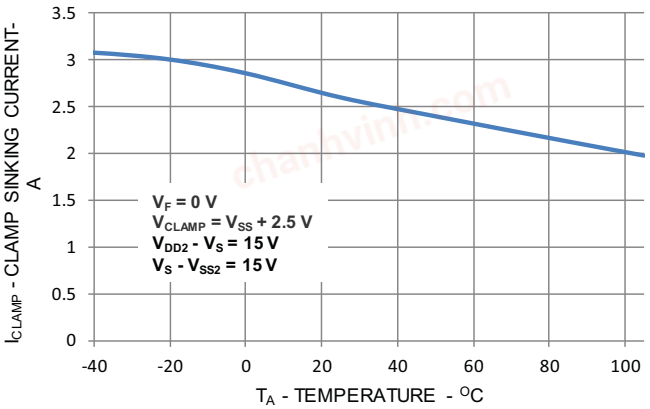


Figure 8: I_{OSS} vs. V_{OSS}

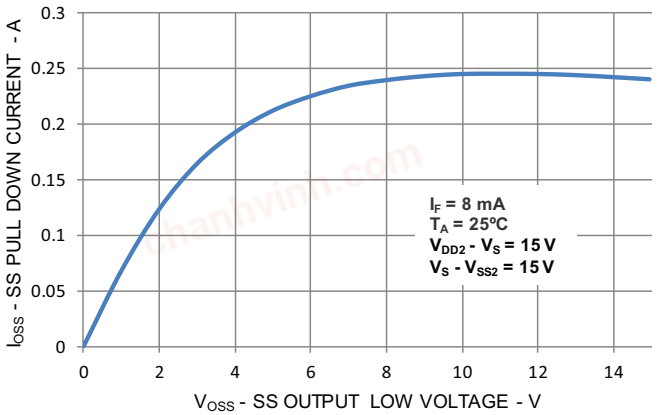


Figure 9: I_{DD2H}/I_{DD2L} vs. Temperature

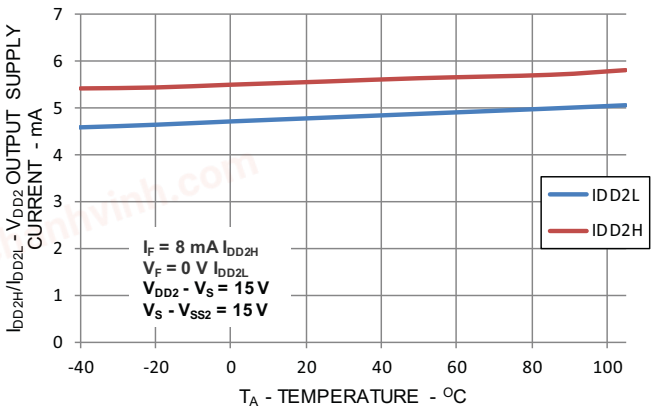


Figure 10: I_{SS2H}/I_{SS2L} vs. Temperature

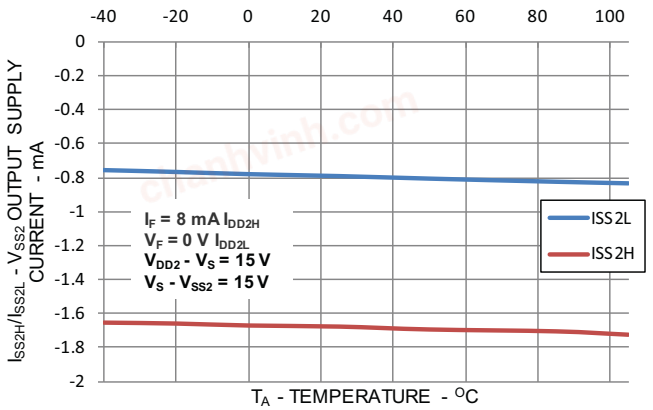


Figure 11: V_{OUTP}/V_{OUTN} vs. I_{FLH}

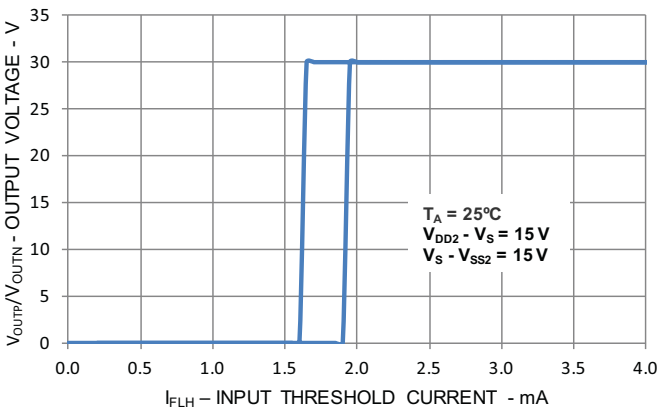
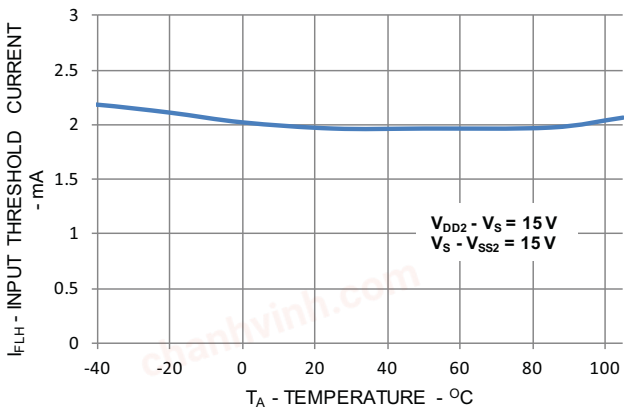


Figure 12: I_{FLH} vs. Temperature



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Figure 13: V_{OC} vs. Temperature

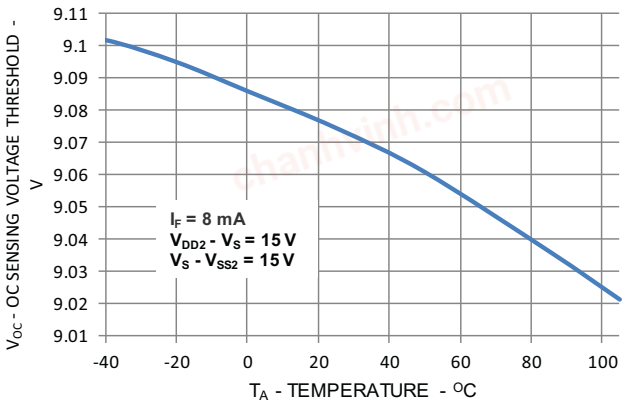


Figure 14: I_{CHG} vs. Temperature

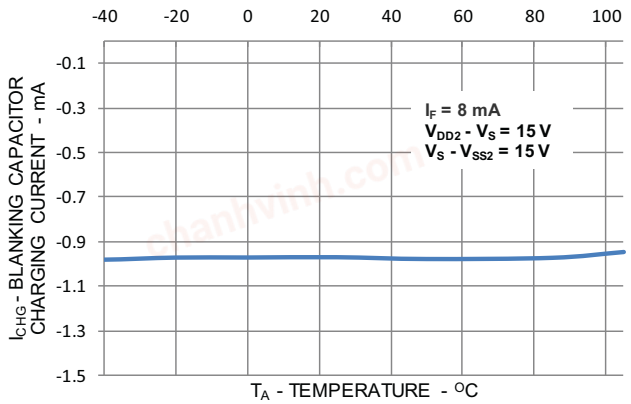


Figure 15: I_{DD1} vs. Temperature

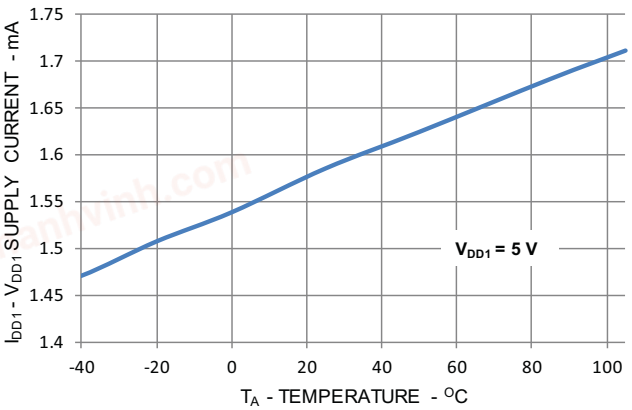


Figure 16: t_{PLH}/t_{PHL} vs. Temperature

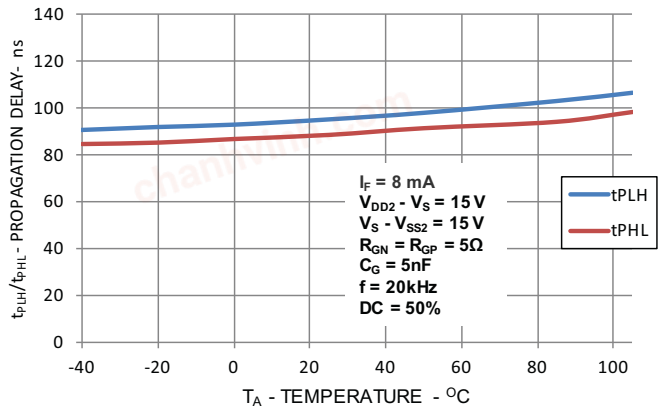


Figure 17: t_{PLH}/t_{PHL} vs. I_F

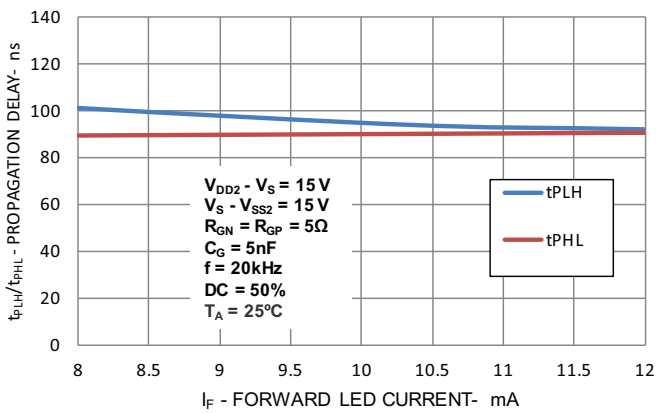
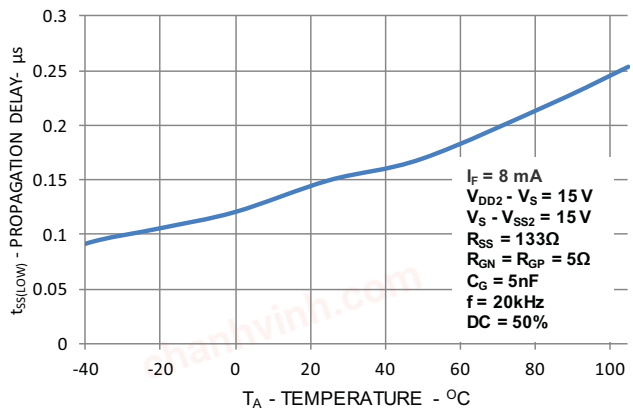
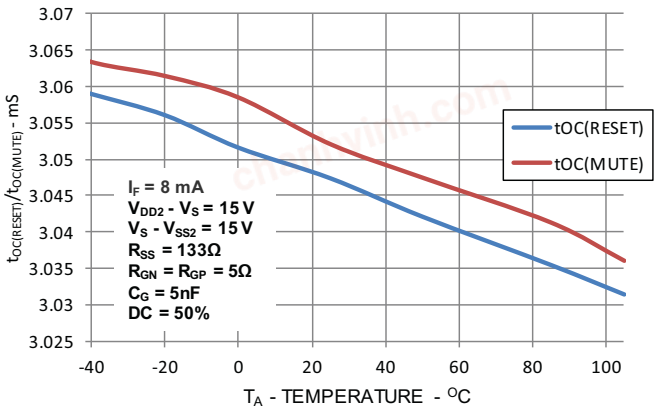


Figure 18: $t_{SS(LOW)}$ vs. Temperature



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Figure 19: $t_{OC(RESET)}/t_{OC(MUTE)}$ vs. Temperature



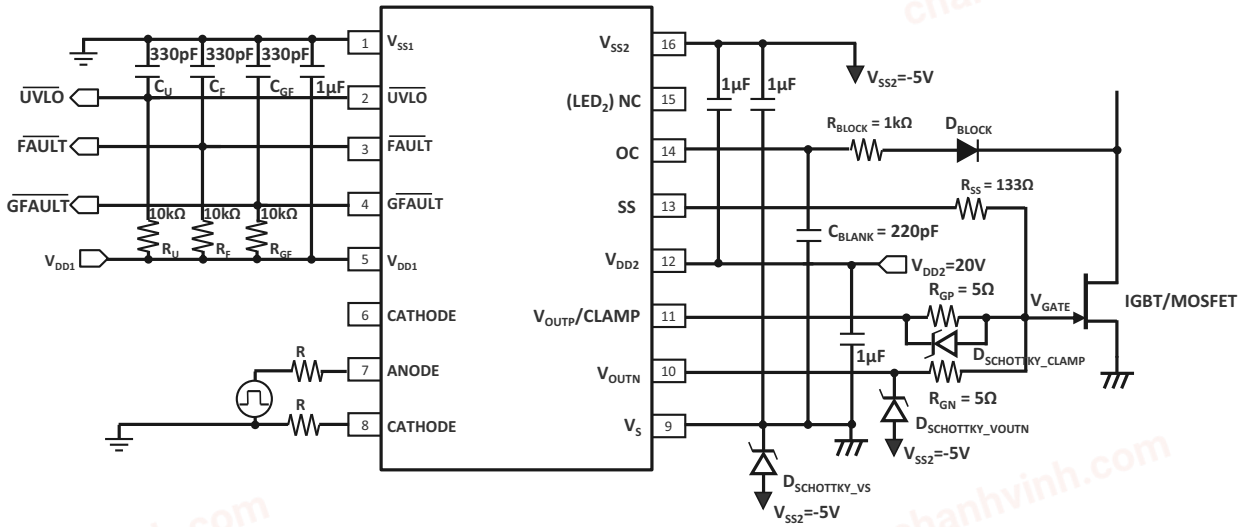
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Application Information

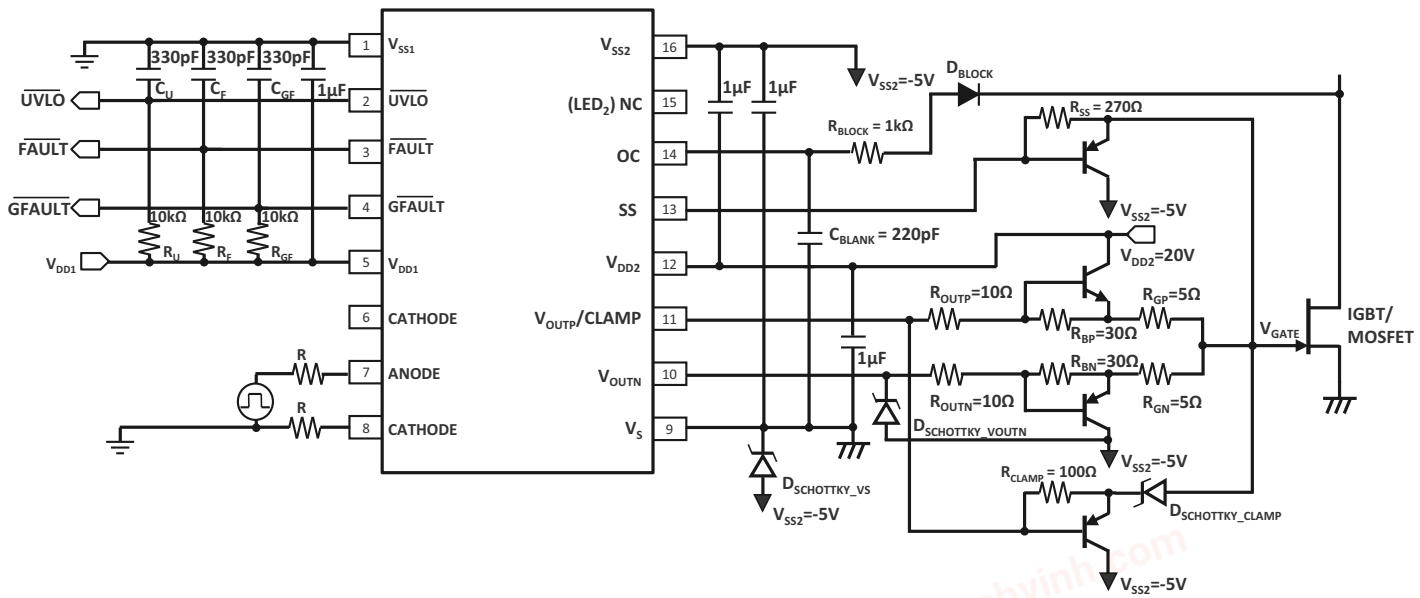
Recommended Application Circuit

Figure 20: Recommended Application Circuits for ACPL-352J

Direct Drive



Buffered Drive



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The ACPL-352J has a LED input control input and three fault reporting mechanisms: namely V_{DD2} under voltage lockout (UVLO), IGBT/MOSFET overcurrent (FAULT) and IGBT/MOSFET gate status (GFAULT). These open drain FAULT, UVLO and GFAULT outputs are connected to 10kΩ pull-up resistors and 330 pF filtering capacitors and are suitable for wired OR applications. UVLO has the highest fault priority and follows by FAULT and GFAULT. The supplies (V_{DD1} and V_{DD2}) are connected to four 1 µF bypass decoupling capacitors to provide the large transient currents necessary during a switching transition.

The two resistors (R) connected to input LED's anode and cathode are recommended to be split ted in the ratio of 3:1. They will help to balance the common mode impedances at the LED's anode and cathode. This helps to equalize the common mode voltage changes at the anode and cathode to give high CMR performance.

The HV blocking diode, D_{BLOCK}, R_{BLOCK} and 220 pF blanking capacitor are used to protect the OC pin and prevent false fault detection. During overcurrent fault condition, the IGBT/MOSFET is soft shut down through the SS pin and the rate of shut down can be adjusted by R_{SS}.

The gate resistor (R_{GP} and R_{GN}) serves to limit gate current and indirectly control the IGBT/MOSFET switching times. $D_{SCHOTTKY_CLAMP}$ is used together with the CLAMP function to shunt parasitic IGBT/MOSFET Miller current during the off cycle.

The status of the IGBT/MOSFET gate voltage is monitored by output pins V_{OUTP} and V_{OUTN}. The GFAULT output goes low when the gate voltage does not correspond to the LED input logic.

For the buffered drive circuit, R_{BP} is used to switch off NPN buffer faster and to prevent shoot through during the PWM "off" cycle. Similarly, R_{BN} is used to switch off PNP buffer faster and to prevent shoot through during the PWM "on" cycle.The Miller current sinking strength can be increased with the PNP buffer and the diode $D_{SCHOTTKY_CLAMP}$. During the PWM "on" cycle, $D_{SCHOTTKY_CLAMP}$ is used to block the forward charging path from V_{OUTP} (20V) to V_{GATE} (–5V). R_{CLAMP} will conduct the 20V from V_{OUTP} to the cathode of the Schottky diode so that the base and the emitter of the PNP buffer will be at the same 20V. This is to prevent V_{BE} stress across the PNP buffer, which has an absolute maximum voltage of 5V to 7V.

Schottky diodes, $D_{SCHOTTKY_VOUTN}$, and $D_{SCHOTTKY_VS}$ are used to prevent V_{OUT} and V_S from going below V_{SS2} due to negative transient caused by parasitic inductance.

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Output Control

The secondary output stage (V_{OUT}, CLAMP, OC, and SS) is controlled by the combination of V_{DD2}, LED current (I_F) and overcurrent (OC) conditions. Please note that V_{DD1} is used to provide power supply to the device's fault reporting mechanisms. The secondary output stage (V_{OUT}, CLAMP, OC, and SS) remains operational when there is no V_{DD1} supply. The following table shows the logic truth table for these outputs. The logic level is defined by the respective threshold of each function pin.

Condition	Inputs			Secondary Outputs			Fault Reporting Outputs		
	V_{DD2}	I_F	OC	V_{OUTN}	V_{OUTP}/CLAMP	SS	UVLO	FAULT	GFAULT
V_{DD2} UVLO	Low	X	Not Active	Low	Low(CLAMP)	High-Z	Low	High	High
Overcurrent	High	Low	Not Active	Low	Low(CLAMP)	High-Z	High	High	High
	High	High	Active(OC)	High-Z	Low(CLAMP)	Low	High	Low	High
Normal Switching	High	Low	Not Active	Low	Low(CLAMP)	High-Z	High	High	High
	High	High	Active(no OC)	High-Z	High(V_{OUTP})	High-Z	High	High	High
Gate Status	High	Low	Not Active	Low	High-Z(V_{OUTP})[a]	High-Z	High	High	Low
	High	High	Active(no OC)	High-Z[b]	High(V_{OUTP})	High-Z	High	High	Low

a. The V_{OUTP}/CLAMP is the GFAULT sense pin and sense higher than V_{SS2} + 2V after time t_{GFAULT}.

b. The V_{OUTN} is the GFAULT sense pin and sense lower than V_{DD2} – 2V after time t_{GFAULT}.

Introduction to Overcurrent (or DESAT) Detection and Protection

The power stage of a typical three phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBT/MOSFET. These failure modes can be grouped into four basic categories: phase and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, overload conditions induced by the load, and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBT/MOSFET can increase rapidly, causing excessive power dissipation and heating. The IGBT/MOSFET becomes damaged when the current load approaches the saturation current of the device, and the collector/drain to emitter/source voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn-off the IGBT/MOSFET during a fault condition.

The ACPL-352J OC pin monitors the drain/source voltages of the MOSFET or the collector/emitter voltages of the IGBT. When the MOSFET goes into overcurrent or IGBT into desaturation and these voltages exceed the predetermined threshold, V_{OC}. The ACPL-352J trigger a local fault shutdown sequence and slowly reduces the high overcurrent to prevent damaging voltage spikes. The fault is reported to controller through the isolated feedback channel of the ACPL-352J.

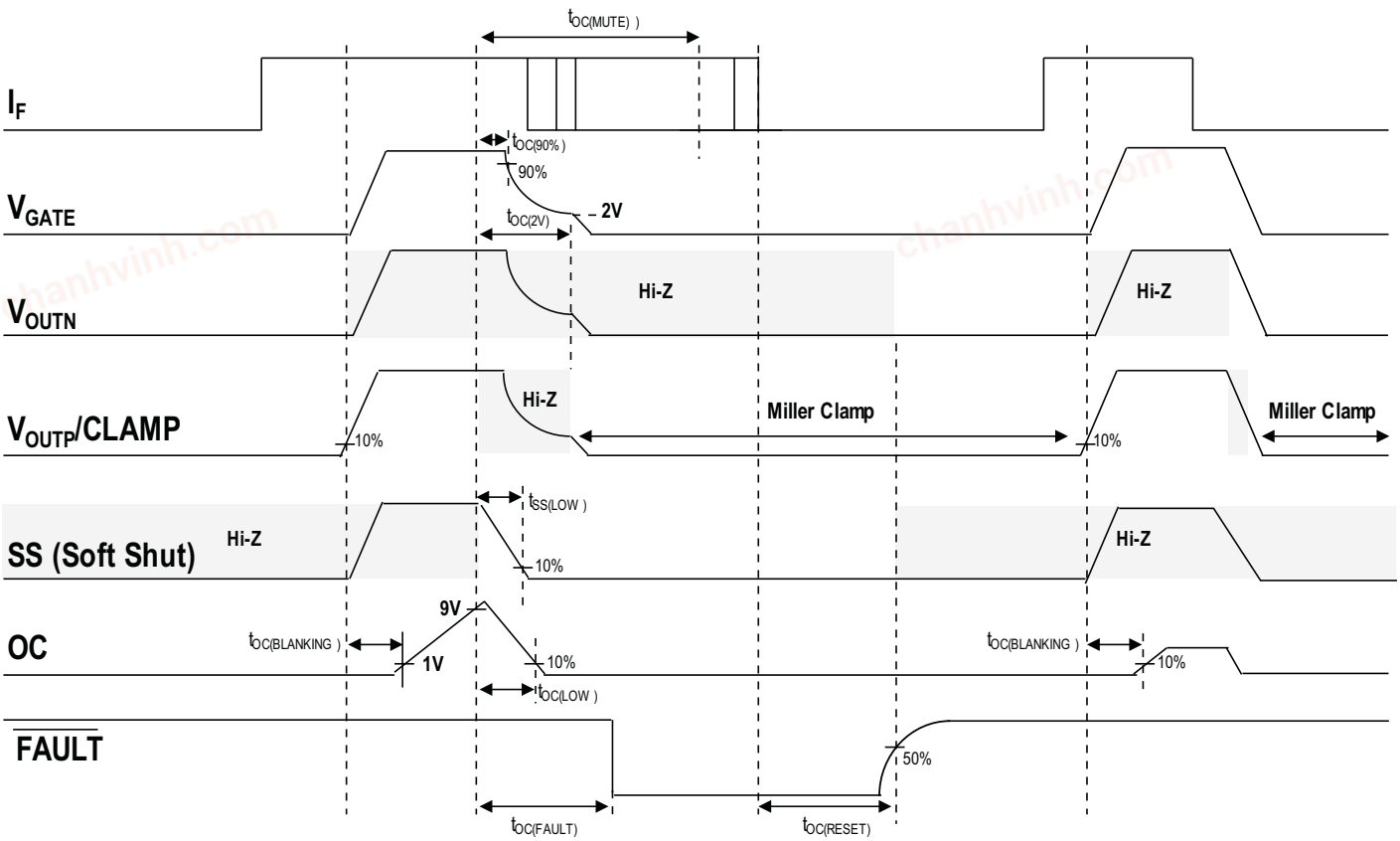
During the off state (no LED input) of the IGBT, the fault detect circuitry is simply disabled to prevent false fault signals.

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Description of Operation during Overcurrent Condition

1. OC terminal monitors IGBTs V_{CE} or MOSFET V_{DS} voltage.
2. When the voltage on the OC terminal exceeds 9V, the output voltages (V_{OUTP} and V_{OUTN}) go to Hi-Z state and the SS pull down the V_{GATE} at a slow rate adjustable via resistor R_{SS}.
3. FAULT output goes low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.
5. When $t_{OC(MUTES)}$ expires, LED input needs to be kept low for $t_{OC(RESET)}$ before fault condition is cleared. FAULT status will return to high and SS output will return to Hi-Z state.
6. In the event LED goes high during $t_{OC(RESET)}$, the $t_{OC(RESET)}$ timing resets and the LED input needs to be kept low for another $t_{OC(RESET)}$ before fault condition is cleared.
7. V_{GATE} starts to respond to LED input after fault condition is cleared.

Figure 21: Circuit Behaviors during Overcurrent Event



OC Fault Detection Blanking Time

The OC fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the OC threshold. This time period, called the total OC blanking time, is controlled by the both internal OC blanking time $t_{OC(BLANKING)}$ (Figure 21) and external blanking time, determined by internal charge current, the OC voltage threshold, and the external blanking capacitor.

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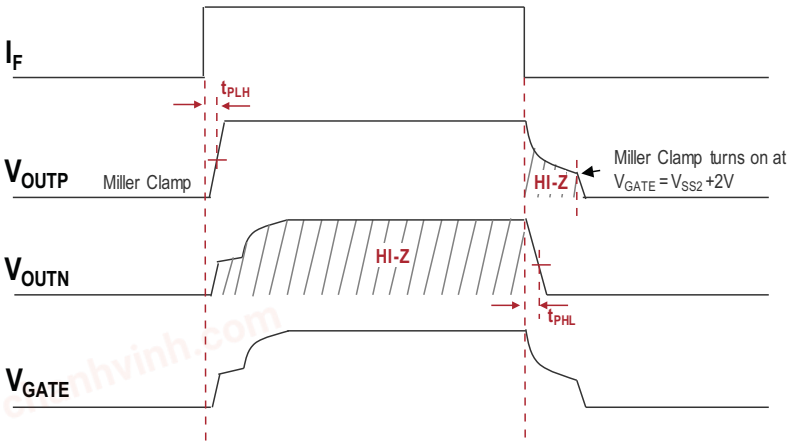
The total blanking time is calculated in terms of internal blanking time ($t_{OC(BLANKING)}$), external capacitance (C_{BLANK}), FAULT threshold voltage (V_{OC}), and blanking capacitor charge current (I_{CHG}) as:

$$t_{BLANK} = t_{OC(BLANKING)} + C_{BLANK} \times V_{OC}/I_{CHG}$$

Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When LED current is driven high the output of ACPL-352J is capable of delivering 5A maximum sourcing current to drive the IGBT's/MOSFET's gate. While LED is switched off the gate driver can provide 5A maximum sinking current to switch the gate off fast. Additional miller clamping pull-down transistor is activated when output voltage reaches about 2V with respect to V_{SS2} to provide low impedance path to miller current as shown in Figure 22.

Figure 22: Gate Drive Signal Behavior

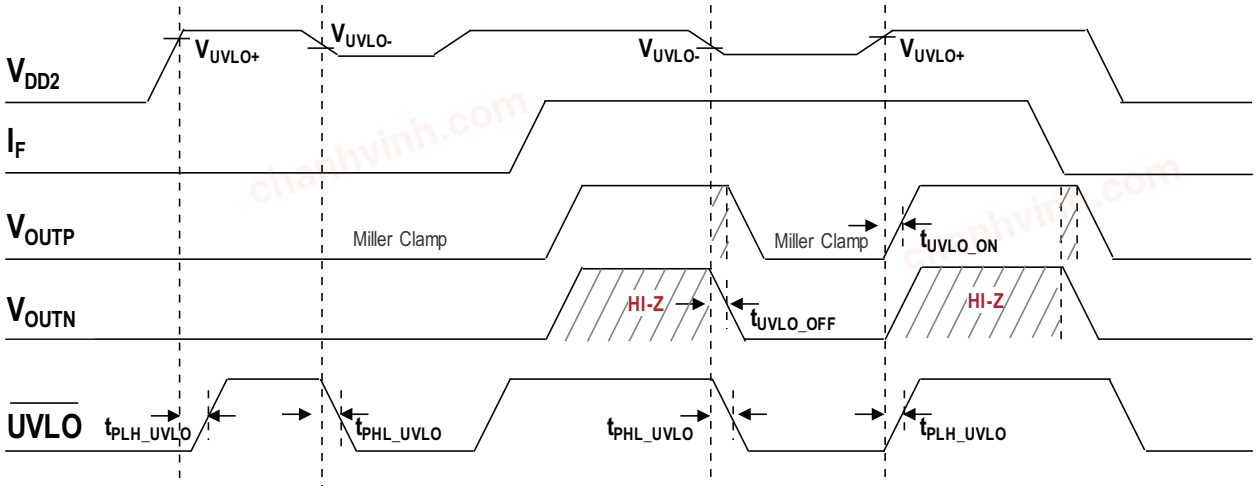


Description of Under Voltage Lock Out

Insufficient gate voltage to IGBT/MOSFET can increase turn on resistance of IGBT/MOSFET, resulting a large power loss and IGBT/MOSFET damage due to high heat dissipation. ACPL-352J monitors the output power supply, V_{DD2} constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output shuts off to protect IGBT/MOSFET from low voltage bias. During power up, the UVLO feature locks the gate driver output low to prevent unwanted turn on at lower supply voltage.

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Figure 23: Circuit Behaviors at Power Up and Power Down



Description of Gate Status Monitoring

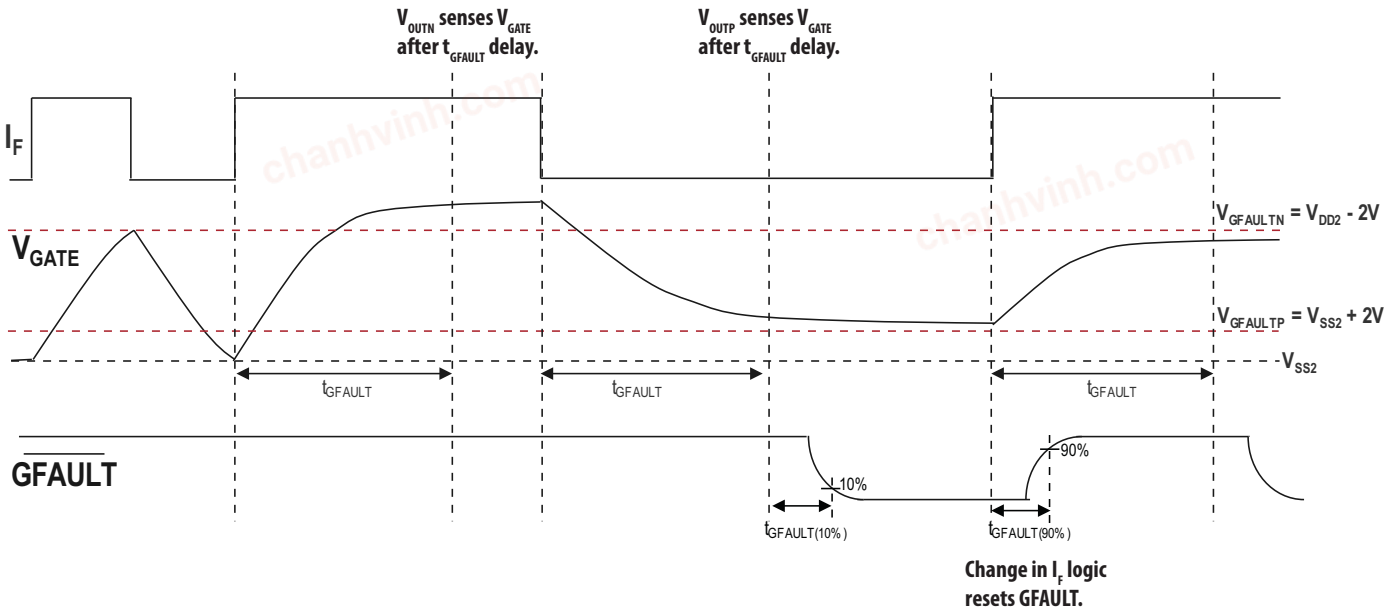
The status of the IGBT/MOSFET gate voltage is monitored by output pins V_{OUTP} and V_{OUTN}. The GFAULT output goes low when the gate voltage does not correspond to the LED input logic. The status of the gate is checked after a minimum delay time t_{GFAULT} to allow sufficient time for the gate to charge or discharge to its final level. There is no check for short input pulses to prevent false GFAULT reporting since the gate is not be able to reach its intended level.

When the LED input logic is high, V_{OUTN} is sensed to check if the gate voltage is higher than $V_{DD2} – 2V$ after t_{GFAULT} delay. GFAULT output goes low if gate voltage is lower than $V_{DD2} – 2V$. Likewise, when the LED input logic is low, V_{OUTP} is sensed to check if the gate voltage is lower than $V_{SS2} + 2V$. GFAULT output returns to high upon input logic change or if the gate voltage manages to cross the threshold of $V_{DD2} – 2V$ or $V_{SS2} + 2V$.

As V_{OUTP} and CLAMP functions share the same pin, the gate voltage is continuously monitored by the V_{OUTP} whether it is in Hi-Z or CLAMP state when the LED input logic is low.

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Figure 24: Circuit Behaviors during Gate Status Monitoring



Selecting the Gate Resistor (Rg)

Step 1: Calculate R_G minimum from the $I_{O(PEAK)}$ specification. The IGBT/MOSFET and R_G in Figure 20 can be analyzed as a simple RC circuit with a voltage supplied by ACPL-352J.

$$R_G \geq \frac{V_{DD2}-V_{SS2}}{I_{OPEAK}} - R_{OUTP(MIN)}$$
$$= \frac{20-(-5)V}{5A} - 0.4\Omega$$
$$= 4.6\Omega$$

or

$$R_G \geq \frac{V_{DD2}-V_{SS2}}{I_{OPEAK}} - R_{OUTN(MIN)}$$
$$= \frac{20-(-5)V}{5A} - 0.3\Omega$$
$$= 4.7\Omega$$

The external gate resistor, R_G and internal minimum turn-on resistance, R_{DSON} ensure the output current does not exceed the device absolute maximum rating of 5A. In this case, we use worst case $R_G \geq 4.8\Omega$.

Step 2: Check the ACPL-352J power dissipation and increase R_G if necessary. The ACPL-352J total power dissipation (P_T) is equal to the sum of the LED power (P_E), input IC power (P_I) and the output IC power (P_O).

$P_T = P_E + P_I + P_O$

Assuming operation conditions of I_F = 8 mA, R_G = 4.8Ω, Max Duty Cycle = 80%, Q_G = 0.5 µC, f = 150 kHz and T_A = 80°C.

Calculation of LED Power Dissipation

$P_E = I_F \times V_F \times$ Duty Cycle
= 8 mA × 1.95V × 0.8 = 12.5 mW

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Calculation of Input IC Power Dissipation

$P_I = I_{DD1}$ (Max) × V_{DD1} (Recommended Max)
= 2.5 mA × 5.5V = 13.75 mW

Calculation of Input IC Power Dissipation

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$
$= I_{DD2} \times (V_{DD2} - V_{SS2}) + P_{HS} + P_{LS}$

$P_{HS} = (V_{DD2} \times Q_G \times f) \times R_{OUTP(MAX)} / (R_{OUTP(MAX)} + R_G) / 2$

$P_{LS} = (V_{DD2} \times Q_G \times f) \times R_{OUTN(MAX)} / (R_{OUTN(MAX)} + R_G) / 2$

P_{HS} = (25V × 0.5 µC × 150 kHz) × 1.5Ω / (1.5Ω + 4.8Ω) / 2 = 192.64 mW

P_{LS} = (25V × 0.5 µC × 150 kHz) × 1.2Ω / (1.2Ω + 4.8Ω) / 2 = 160.71 mW

P_O = 7.5 mA × 25V + 192.64 mW + 160.71 mW
= 540.9 mW < 600 mW ($P_{O(MAX)}$ at 95°C)

The value of 7.5 mA for I_{DD2} in the previous equation is the maximum I_{CC2} over the entire operating temperature range.

Since P_O is less than $P_{O(MAX)}$, Rg = 4.8Ω is alright for the power dissipation.

Thermal Calculation

Application and environmental design for ACPL-352J needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 125°C. The equations provided below are for the purposes of calculating the maximum power dissipation effect on junction temperatures.

LED Junction Temperature, T_E = $(A_{EA} \times P_E) + (A_{EI} \times P_I) + (A_{EO} \times P_O) + T_A$
= (176.1°C/W × 12.5 mW) + (35.4°C/W × 13.75 mW) + (33.1°C/W × 540.9 mW) + 80°C
= 100.6°C

Input IC Junction Temperature, T_I = $(A_{EI} \times P_E) + (A_{IA} \times P_I) + (A_{IO} \times P_O) + T_A$
= (35.4 °C/W × 12.5 mW) + (92 °C/W × 13.75 mW) + (25.6 °C/W × 540.9 mW) + 80°C
= 95.6°C

Output IC Junction Temperature, T_O = $(A_{EO} \times P_E) + (A_{IO} \times P_I) + (A_{OA} \times P_O) + T_A$
= (33.1 °C/W × 12.5 mW) + (25.6 °C/W × 13.75 mW) + (76.7 × 540.9 mW) + 80°C
= 122.2°C

OC (Overcurrent) Blocking Diodes and Threshold

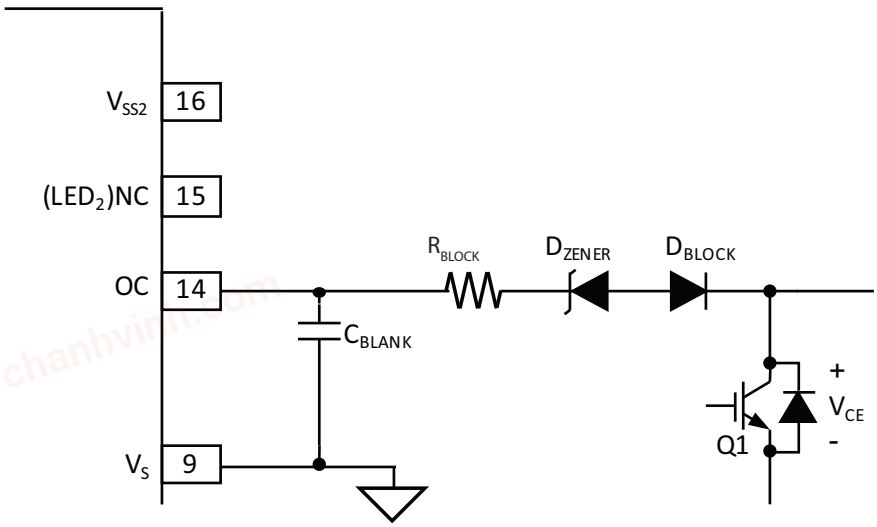
The D_{BLOCK} diode's function is to conduct forward current, allowing sensing of the IGBT's V_{CE} or MOSFET's V_{DS} when it is *on* and to block high voltages when it is *off*.

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During IGBT/MOSFET switching off and towards the end of the forward conduction of the D_{BLOCK} diode, a reverse current flow for short time. This reverse recovery effect causes the diode not able to achieve its blocking capability until the mobile charge in the junction is depleted. During this time, there is commonly a very high dV/dt voltage ramp rate across the IGBT/MOSFET. This results in $I_{CHARGE} = C_{D\text{-}BLOCK} \times dV/dt$ charging current, which charges the blanking capacitor, C_{BLANK}. In order to minimize this charging current and avoid false overcurrent triggering, it is best to use fast response diodes.

In the recommended application circuit shown in Figure 25, the voltage on pin 14 (OC) is $V_{OC} = (I_{CHG} \times R_{BLOCK}) + V_F + V_{CE}$, (where V_F is the forward ON voltage of D_{BLOCK} and V_{CE} is for example, the IGBT collector-to-emitter voltage). The value of $V_{OC,FAULT(TH)}$ that triggers OC to signal a FAULT condition is nominally $9V - (I_{CHG} \times R_{BLOCK}) - V_F$. If desired, this threshold voltage can be decreased by using multiple D_{BLOCK} diodes or low voltage zener diode in series. If n is the number of D_{BLOCK} diodes, the nominal threshold value becomes $V_{OC,FAULT(TH)} = 9V - (I_{CHG} \times R_{BLOCK}) - (n \times V_F)$. If a Zener diode is used, the nominal threshold value becomes $V_{OC,FAULT(TH)} = 9V - (I_{CHG} \times R_{BLOCK}) - V_F - V_Z$. In the case of using two diodes instead of one, diodes with half of the total required maximum reverse-voltage rating may be chosen.

Figure 25: OC (Overcurrent) Blocking Diodes and Threshold



OC Pin Protection Resistor

The freewheeling of flyback diodes connected across the IGBT/MOSFET can have large instantaneous forward voltage transients which greatly exceed the nominal forward voltage of the diode. This can result in a large negative voltage spike on the OC pin which draws substantial current out of the driver if protection is not used. To limit this current to levels that do not damage the driver IC, a 1-kΩ resistor should be inserted in series with the D_{BLOCK} diode.

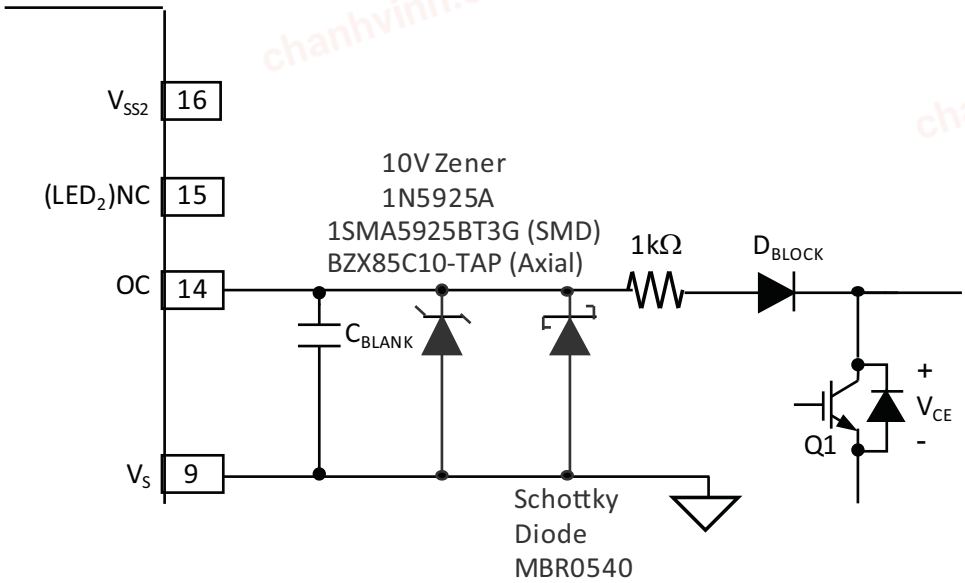
False Fault Prevention Diodes

One of the situations that can cause the driver to generate a false fault signal is if the substrate diode of the driver becomes forward biased. This can happen if the reverse recovery spikes coming from the IGBT/MOSFET freewheeling diodes bring the OC pin below ground. Hence, the OC pin voltage is *brought* above the threshold voltage. This negative going voltage spike is typically generated by inductive loads or reverse recovery spikes of the IGBT/MOSFETs free-wheeling diodes. In order to prevent a false fault signal, it is highly recommended to connect a Zener diode and Schottky diode across the OC pin and V_S pin.

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This circuit solution is shown in Figure 26. The Schottky diode prevents the substrate diode of the gate driver optocoupler from being forward biased while the Zener diode (value around 10V) is used to prevent any positive high transient voltage to affect the OC pin.

Figure 26: False Fault Prevention Diodes

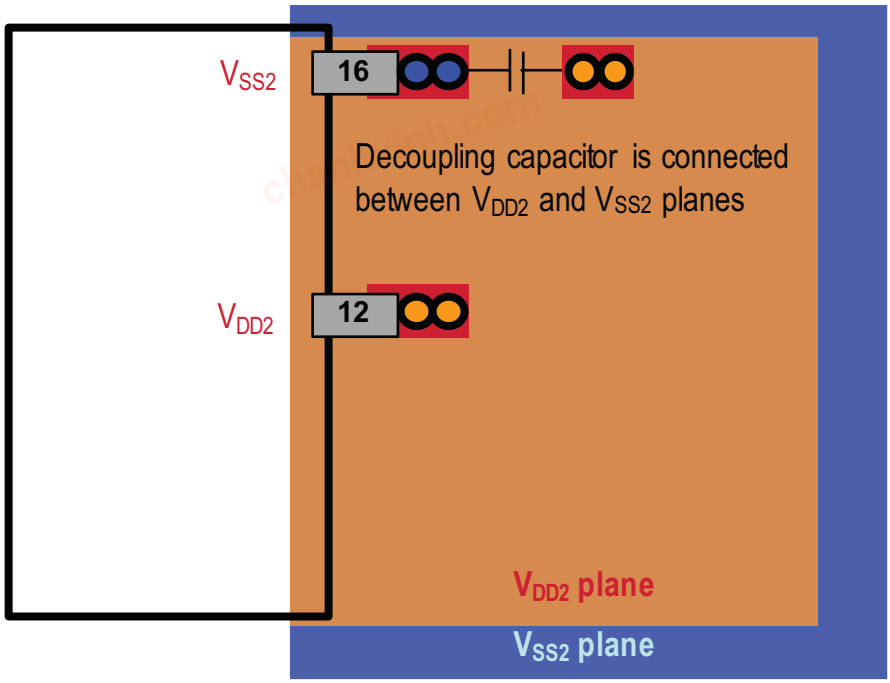


Supply and Ground Planes Layout and Loading Conditions

At 5A rated high current switching, decoupling capacitor must be close to V_{DD} and V_{SS} pins. And due to the fast switching, large V_{DD} and V_{SS} planes are recommended to prevent noise by lowering the parasitic inductance. Without the V_{DD} and V_{SS} planes, it is recommended to connect total load bigger than 2-nF during all applications or board testing to prevent output noise.

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Figure 27: Recommended V_{DD2} and V_{SS2}, Supply and Ground Planes Layout



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